Smartcoder (AU6802N1)

Specifications

Note: *Smartcoder, Smartsyn* and *Singlsyn* are TRADEMARKS of Tamagawa Seiki Co., Ltd .

REVISIONS

No.	DATE	PAGES	DESCRIPTION	APP'D

ED'N No. . .

DS'D	DATE	MODEL No.	TITLE
A. Suganuma	'03.04.04	AU6802N1	Smartcoder (AU6802N1) Specifications
CH'D			
APP'D H. Kushihara			

DWG No.	3	4	5	6	7	8	9	10	11	12	Sheet
80110147	1	1	0	1	4	1	1	I	4	E	1/37

TAMAGAWA SEIKI CO., LTD. JAPAN

参考出図

Table of Contents

参考出図

Specification,
Smartcoder (AU6802N1)

1. Scope

This specification applies to *Smartcoder (AU6802N1),* R/D (Resolver to Digital) converter IC, designed for automotive, transit and other vehicle related applications.

2. References

(1) 168025000F47 : Outline drawing of Smartcoder (AU6802N1)

(2) 168025002D37 : Block diagram of Smartcoder (AU6802N1)

3. Requirements

3.1 General

Smartcoder (AU6802N1) defined in this specification is an electronic device that has been developed for vehicle applications. Features that were considered in the design of this analog/digital hybrid semi-conductor integrated circuit technology include size, low cost and mass production.

参考出図

3.2 Functions and Performances

3.2.1 Description of Functions

Smartcoder (AU6802N1) is an R/D (Resolver to Digital) conversion IC used with a brushless Resolver (BRX*) such as *Singlsyn, Smartsyn,* etc. It converts the electrical information (analog signal) corresponding to a mechanical rotational angle of the Resolver to the corresponding digital data and transmits it.

It was developed for the main purpose of being simple, low cost, and having high quality enough to be mounted on vehicles, while maintaining high reliability that the Resolver (Synchro) system has conventionally had. It provides you with a wide range of applications in angle detection.

BRX*: One-phase excitation and two-phase output (Amplitude modulation type) brushless Resolver

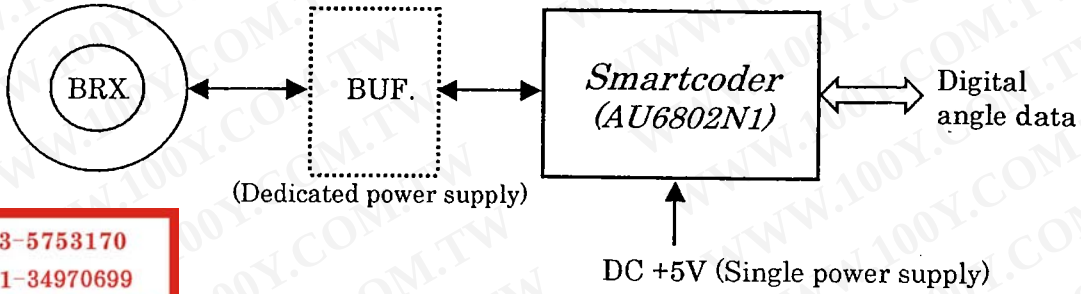


Figure 1. Example of system

The *Smartcoder (AU6802N1)* realizes a high reliable absolute angle detection system when combined with the brushless Resolver (BRX) and it has the following special features.

(1) Vehicle-mount quality:
- Quality level: Transportation equipment involved with safety
- Operating temperature range: -40 to +125 °C
  (Power dissipation should be considered.)
- Storage temperature range: -65 to +150 °C

(2) Simple to use:
- Real time output (High tracking rate): 240,000 rpm for 10-bit resolution
  60,000 rpm for 12-bit resolution
- Single power supply of DC 5 V
  (Integrated oscillator for exciting Resolver: 10/20 kHz)
- Small size and light weight
  (10 × 10 mm; Pin interval: 0.65 mm; 52-pin TQFP)
- Resolution of 10/12 bits (Selectable)
- Output redundancy: Pulse/Parallel/Bus (Selectable) + Serial output
- Built-in test (Internal error detection) function
- Available monitor output of Resolver signals capable of detecting layer short-circuit (SINMNT and COSMNT output)
- Capable of setting the number of poles for UVW output signal
  (Selectable from the multiplication of ×1, ×2, ×3 or ×4)
- Clock input (20 MHz):
  External CLK input/Crystal resonator/Ceramic resonator (Selectable)

3.2.2 Functional Structure

The internal structure of *Smartcoder (AU6802N1)* is according to the block diagram (168025002D37).

3.2.3 Main Functions

(1) R/D conversion

This is the major function that converts the Resolver signal (analog) to the corresponding digital data with the resolution of 10/12 bits by means of the digital tracking method.

(2) Built-in test (abnormality detection)

This function detects any abnormal signal of the sensor (Resolver) and any abnormal state of the R/D converter by a built-in test. This function is independent from R/D conversion function and does not restrict the output by its result (i.e. any detection of abnormal state). The contents of detection are shown below.

- Abnormal sensor signal: Breaking of exciting source lines (R1 & R2) including defective contact, or lack of exciting voltage such as breaking-down of exciting output circuit or short circuit of lines. Breaking of Resolver signal lines (S1, S2, S3 & S4) including defective contact, or short circuit between the signal lines of S1-S3 and S2-S4.during the limited rotation.
- Abnormal R/D conversion: Excessive residuals (ε) of control signal in the tracking control loop (i.e. Negative feedback control loop).

(3) Resolution selection

The resolution in the electric angle of 360 degrees can be selected from 10 bits (i.e. division of 1,024) and 12 bits (i.e. division of 4,096) by setting the resolution selection terminal (MDSEL).

(4) Exciting source/frequency selection

The exciting source (in sine wave) for the Resolver is integrated and an exciting frequency of 10/20 kHz can be selected by setting the frequency selection terminals (FSEL1 & 2).

(5) Internal switching of control mode in R/D conversion

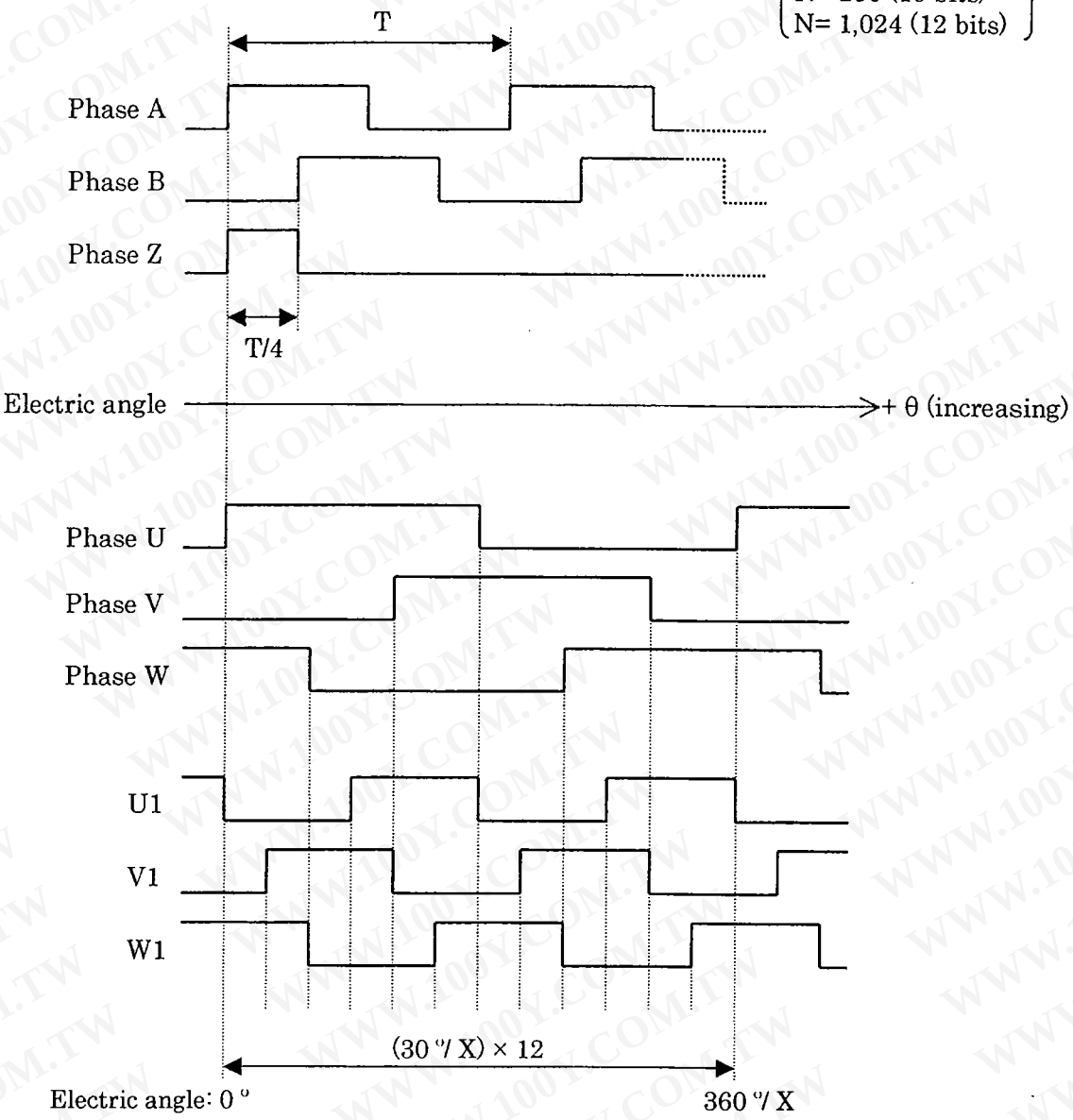
The ON/OFF of acceleration mode control that assumes unexpected high angular acceleration response by any sudden angular velocity change or mechanical load disturbance (e.g. shock) to the shaft of the Resolver, etc. can be set by setting the acceleration mode control terminal (ACMD). Refer to Paragraph 6.5 for details.

(6) Pulse output equivalent to an encoder

- Output phases: Phases A, B, Z, U, V & W and U1, V1 & W1
- Number of pulses (A, B): 256 P/T (Electric angle) for the resolution of 10 bits
  1,024 P/T (Electric angle) for the resolution of 12 bits
- Selectable number of poles for UVW: 1X, 2X, 3X and 4X
  (Corresponding to the electric angle of 360, 180, 120 and 90 degrees respectively)

The operating waveform of pulse signals equivalent to an encoder is shown in Figure 2.

T= 360 °/ N
N= 256 (10 bits)
N= 1,024 (12 bits)



Selection of number of poles: X = 1, 2, 3 or 4

Figure 2. Operating pulse waveform equivalent to an encoder

Note: The pulses equivalent to an encoder may chatter at the edge of switching. It should be noted that the phase relation between A and B pulses and the pulse width, etc. may be disarranged. In case of using A and B pulses, they should be reversibly counted in the signal processing side to prevent the angle error accumulation due to chattering or noise, etc.

	DWG No.	3	4	5	6	7	8	9	10	11	12	Sheet
	8 0	1	1	0	1	4	1	1	I	4	E	6/

参考出図

(7) Output signal selection

The output terminal (D0~ D11) can be switched to the parallel output mode or pulse output mode equivalent to an encoder by setting the output selection terminal (OUTMD).

The output signal format is shown in Table 1.

Table 1. Output signal format

	D11	D10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Pulse mode OUTMD="L"	Pulse output equivalent to an encoder									ERR output	ERR HLD output	PRTY output
	Phase A	Phase B	Phase Z	Phase U	Phase V	Phase W	U1	V1	W1			
Parallel mode OUTMD="H"	MSB Φ1	Φ2	Φ3	Φ4	Φ5	Φ6	Φ7	Φ8	Φ9	10bit-LSB Φ10	Φ11	12bit-LSB Φ12

Three types of output mode can be selected as follows by combining with bus interface control signals (CSB & RDB).

(i) Pulse (+ Serial data) interface mode
(ii) Parallel I/O interface mode (Stand-alone)
(iii) Parallel bus interface mode

(8) Serial signal output

The absolute angle output can be transmitted in serial format corresponding to the external clock signal (SCK). The angle data at the falling-edge of SCSB signal is transmitted in DATA of the serial format to synchronize with the external clock signal. The operational waveform of serial signal output is shown in Figure 3.

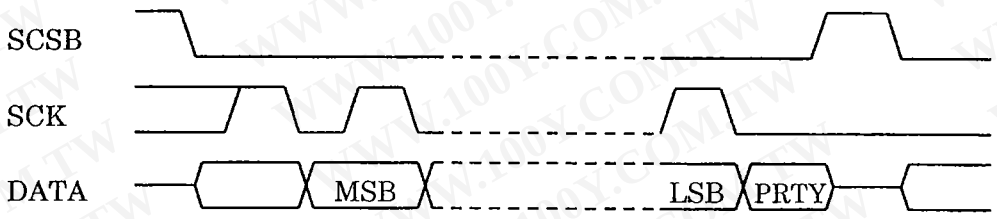


Figure 3. Operational waveform of serial signal output

(9) Error detection of output data

One bit of vertical parity for the angle data (Φ1~ Φ10 or Φ1~ Φ12) is transmitted as even parity (PRTY).

参考出図

3.2.4 Performance of R/D Conversion

The performance of R/D conversion is shown in Table 2.

Table 2. Performance of R/D conversion

No.	Items	Specifications		Remarks
1	Conversion type	Tracking type (Negative feedback control loop)		
2	Resolution	1,024 (= 2^{10})	4,096 (= 2^{12})	Division for 1 revolution of electric angle
3	Conversion accuracy	±2 LSB	±4 LSB	Static absolute accuracy in electric angle
4	Settling time (AMCD="H")	1 ms typ.	2.5 ms typ.	For step input of 180 ° in electric angle
	Settling time (AMCD="L")	15 ms typ.	60 ms typ.	
5	Max.tracking rate	240,000 rpm	60,000 rpm	Range of traceable angular velocity in electric angle
6	Max. angular acceleration	256,000 rad/s²	64,000 rad/s²	Range of traceable angular acceleration in electric angle
7	Response	±0.2 ° max. /10,000 rpm	±0.4 ° max. /10,000 rpm	Output response delay in electric angle for constant angular velocity

Note: The phase shift of the exciting component of the Resolver output signals (i.e. COSMNT & SINMNT) relative to the external input signal for exciting the Resolver (i.e. R1E-R2E) should be within ±10 degrees.

参考出図

3.2.5 Input/Output Signals

The list of input/output signals is shown in Table 3.

Table 3. List of input/output signals

No.	Symbol	Class	Remarks	No.	Symbol	Class	Remarks
1	R1E	A/I	External excit. (Diff.) input	27	D0	D/O (BUS)	PRTY / Φ12
2	R2E	A/I		28	D1	D/O (BUS)	ERRHLD/ Φ11
3	VCC	----	Analog PS	29	D2	D/O (BUS)	ERR / Φ10
4	SINMNT	A/O	SIN monitor	30	D3	D/O (BUS)	W1 / Φ9
5	S4	A/I	SIN input (Differential)	31	D4	D/O (BUS)	V1 / Φ8
6	S2	A/I		32	D5	D/O (BUS)	U1 / Φ7
7	AGND	----	Analog GND	33	DGND	----	Digital GND
8	S1	A/I	COS input (Differential)	34	D6	D/O (BUS)	Phase W / Φ6
9	S3	A/I		35	D7	D/O (BUS)	Phase V / Φ5
10	COSMNT	A/O	COS monitor	36	D8	D/O (BUS)	Phase U / Φ4
11	VCC	----	Analog PS	37	D9	D/O (BUS)	Phase Z / Φ3
12	RSO	A/O	Exciting source	38	D10	D/O (BUS)	Phase B / Φ2
13	COM	A/O	Com. (VCC/2)	39	D11	D/O (BUS)	Phase A / Φ1
14	AGND	----	Analog GND	40	DGND	----	Digital GND
15	MDSEL	D/I	Resolution select	41	CSB	D/I	Chip select
16	ACMD	D/I	Acc, mode control	42	RDB	D/I	Read
17	XSEL1	D/I	UVW No. of poles	43	INHB (RD)	D/I	Inhibit
18	XSEL2	D/I	UVW No. of poles	44	PRTY	D/O (BUS)	Parity
19	OUTMD	D/I	Output mode sel.	45	ERRHLD	D/O	Error (Hold)
20	SCSB	D/I	Serial CSB	46	ERRSTB	D/I	Error reset
21	DATA	D/O (BUS)	Serial data	47	FSEL1	D/I	Frequency sel.
22	SCK	D/I	Serial clock	48	FSEL2	D/I	Frequency sel.
23	VDD	----	Digital PS	49	VDD	----	Digital PS
24	XTAL	----	To osc. element	50	TEST1	D/I	(Test mode setting)
25	CLKIN	D/I	Ext. CLK input	51	TEST2	D/I	(Test mode setting)
26	DGND	----	Digital GND	52	AGND	----	Analog GND

Note: 1. "No." is corresponding to the pin number of terminal.

2. "Class" means as follows:
   * A/I : Analog input
   * A/O: Analog output
   * D/I : Digital input
   * D/O: Digital output

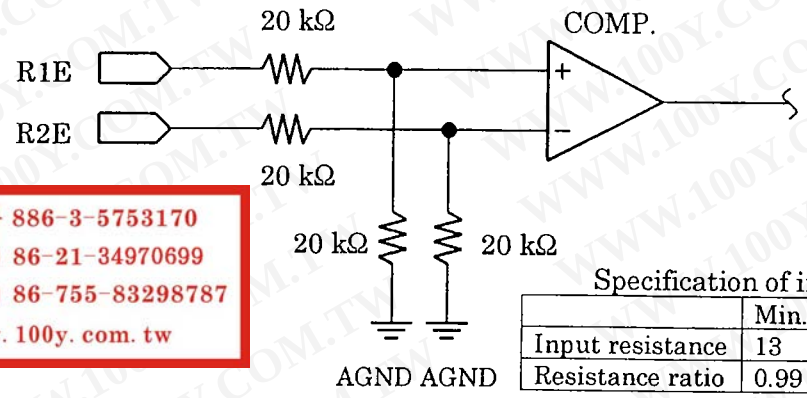
3. TEST1 signal in No. 50 and TEST2 signal in No. 51 do not affect the operation directly, and these terminals should usually be connected to the digital PS (VDD).

参考出図

3.2.6 Input/Output Circuits (Excluding any protection circuits)

(1) External input circuit for exciting the Resolver <R1E, R2E>

The equivalent input circuit for exciting the Resolver externally (R1E, R2E) is shown in Figure 4.



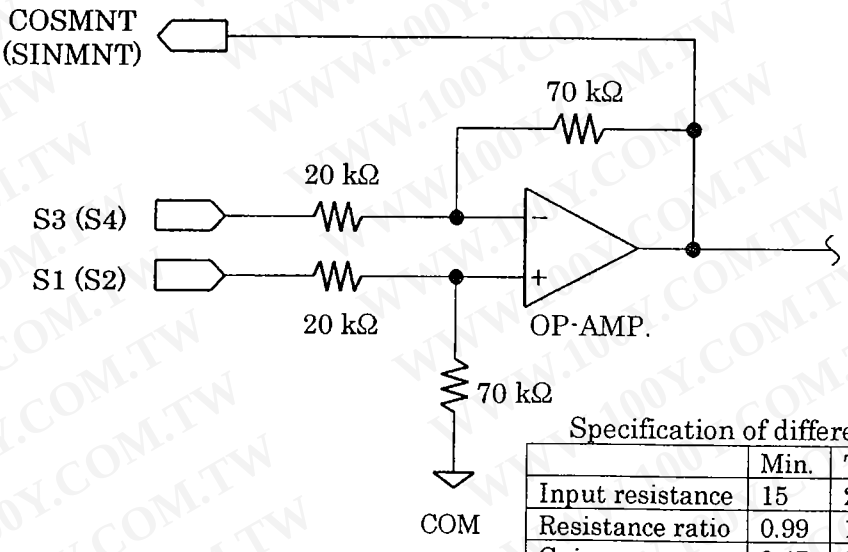
Specification of input resistance

	Min.	Typ.	Max	Unit
Input resistance	13	20	35	kΩ
Resistance ratio	0.99	1	1.01	---

Figure 4. Equivalent input circuit for exciting the Resolver externally

(2) Input (differential) circuit for Resolver signals <S1-S3, S2-S4> and monitor output

The equivalent circuits for the Resolver signal inputs (differential) (S1-S3 & S2-S4) and monitor output (COSMNT & SINMNT) are shown in Figure 5.



Specification of differential amplifier

	Min.	Typ.	Max	Unit
Input resistance	15	20	25	kΩ
Resistance ratio	0.99	1	1.01	---
Gain	3.47	3.5	3.53	---

Figure 5. Equivalent input circuit for Resolver signals (differential)

参考出図

(3) Analog output circuit <RSO, COM>

The equivalent output circuit for exciting the Resolver (RSO) and common (COM) is shown in Figure 6.

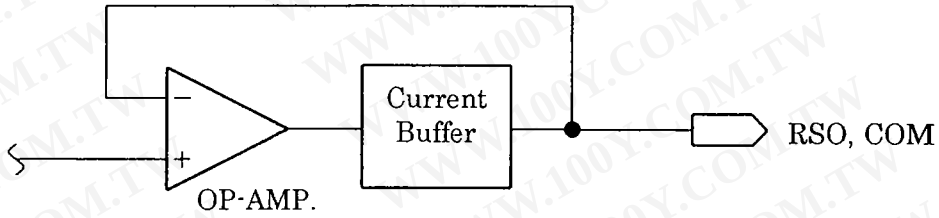


Figure 6. Equivalent circuit for analog output

(4) Digital input circuit

The equivalent circuit for digital inputs is shown in Figure 7.

[Applicable signals: MDSEL, ACMD, XSEL1, XSEL2, OUTMD, SCSB, SCK, CSB, RDB, INHB (RD), ERRSTB, FSEL1, FSEL2]

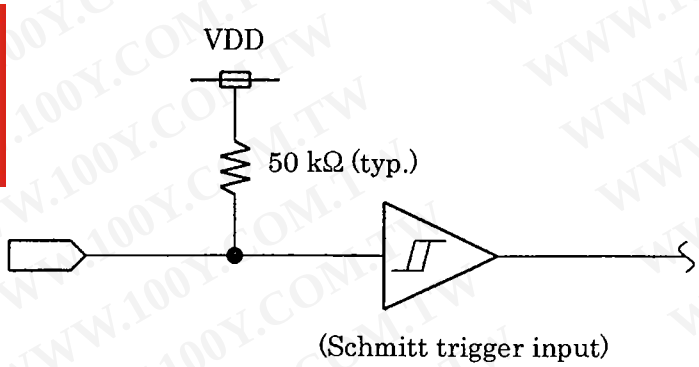


Figure 7. Equivalent circuit for digital inputs

(5) Digital output circuit <ERRHLD>

The equivalent circuit for digital output (ERRHLD signal) is shown in Figure 8.

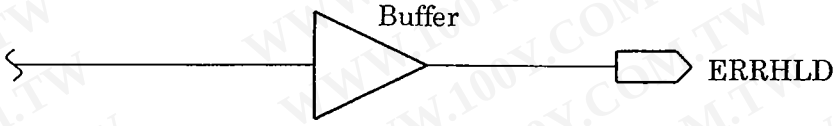


Figure 8. Equivalent circuit for digital output

参考出図

(6) Parallel output circuit structure

The multiplex circuit structure of parallel output (D0~ D11) is shown in Figure 9.

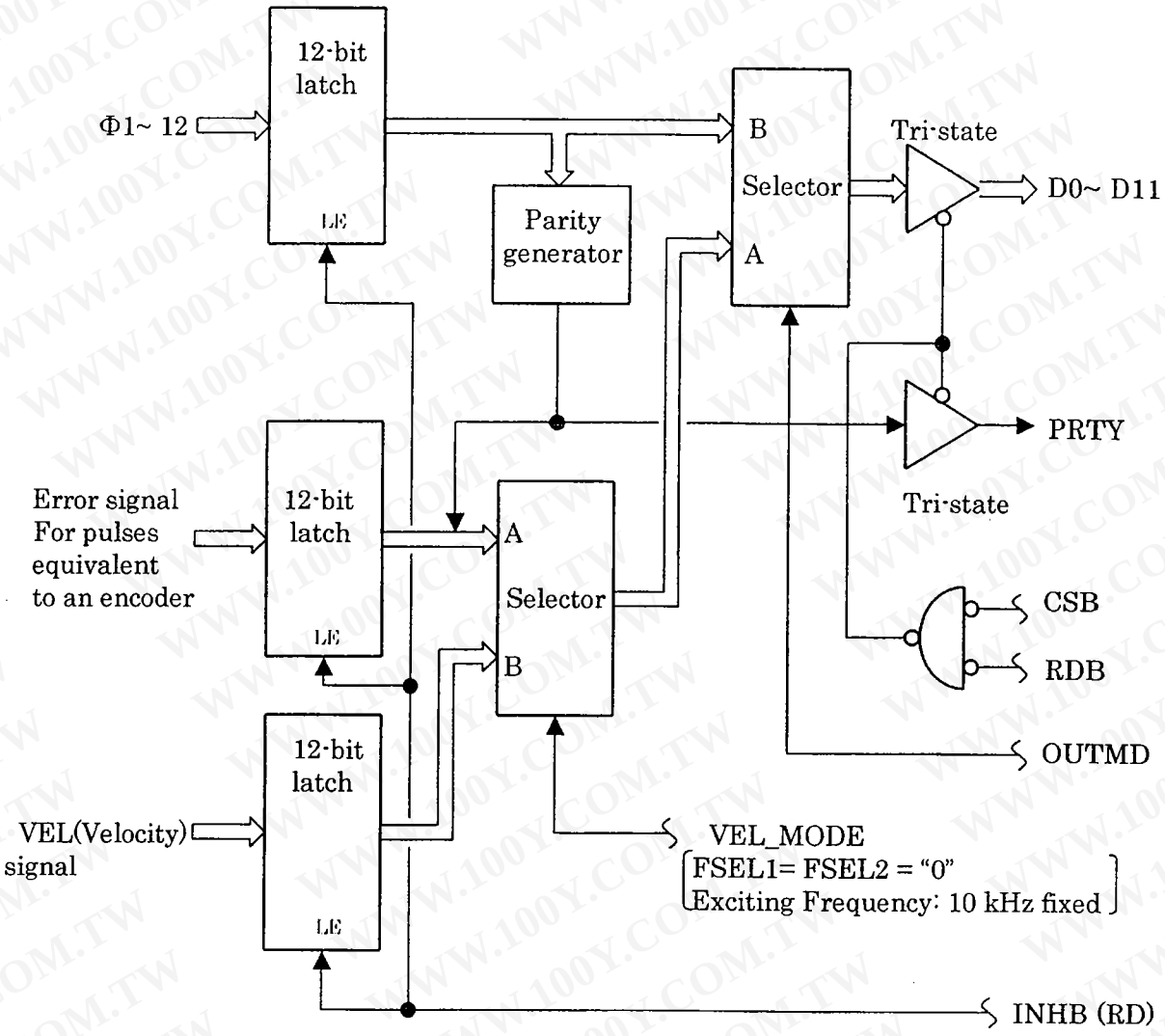


Figure 9. Multiplex circuit structure for parallel output

参考出図

(7) BUS interface circuit

The equivalent circuit for BUS interface is shown in Figure 10.

< Applicable signals: D0~ D11, PRTY >

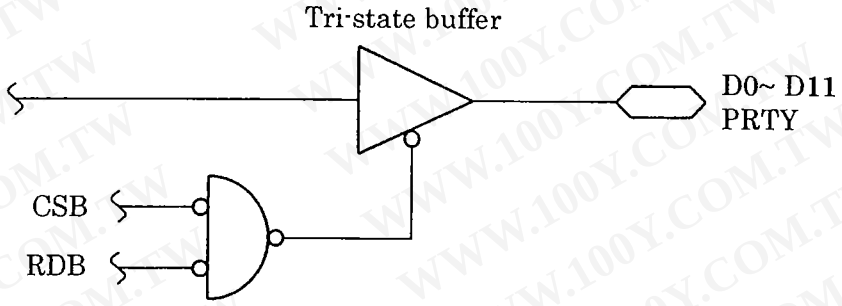


Figure 10. Equivalent circuit for bus interface

(8) Serial DATA signal output circuit

The equivalent circuit for serial data output is shown in Figure 11.

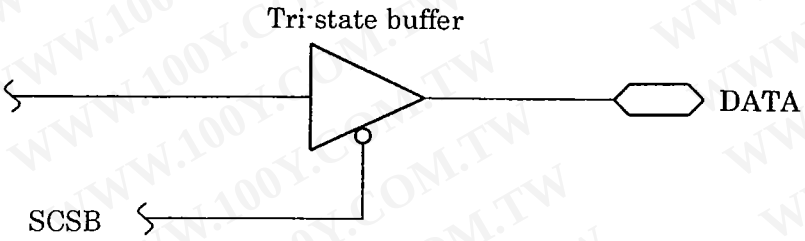


Figure 11. Equivalent circuit for serial data output

参考出図

3.2.7 Electrical Characteristics

(1) Signal source output for exciting Resolver (RSO)

- Output waveform : Sine wave (31-level interpolation D/A output)
- Frequency : 10/20 kHz (Selectable)
- Output voltage : 2 Vp-p ±10% (Balanced potential to COM; VCC = 5 V)
- Load impedance : 1 kΩ min.

(2) External signal input for exciting Resolver (R1E, R2E)

- Frequency : 8~ 20.4 kHz
- Input voltage range : 0~ VCC
- Input impedance : According to Paragraph 3.2.6 (1)

(3) Resolver signal input (S1-S3, S2-S4)

- Frequency : 8~ 20.4 kHz
- Input voltage : 1.1 Vp-p max. (Differential input:)
- Input impedance : According to Paragraph 3.2.6 (2)

(4) Resolver signal monitor output (COSMNT,SINMNT)

- Frequency : 8~ 20.4 kHz (Same as input frequency)
- Output voltage range : 3.5 Vp-p min. (Balanced potential to COM; VCC = 5 V)
- Load impedance : 10 kΩ min.

(5) Common output (COM)

- Output voltage : 0.5 × VCC ±5 %
- Load impedance : 1 kΩ min.

(6) Internal threshold set value for built-in test (Internal error detection)

The internal threshold set value for the built-in test (Internal error detection) is shown in Table 4. The circuit structure for the built-in test is shown in Attached figure 1. For internal error detection of sensor signal, the internal threshold setting value is equivalent to the "reference value" that is directly compared to the Resolver signal monitor output (COSMNT, SINMNT), also, it is equivalent to the "reference value" that is directly compared to the control residuals (ε) for internal error detection of R/D conversion.

Table 4. Internal threshold set value for built-in test (Internal error detection)

Contents of built-in test (Internal error detection)			Set threshold	Time delay
Abnormal signal of sensor	Breaking/down circuit of exciting lines (Short circuit of signal lines during the limited rotation)	High end	0.55 × VCC	0.2 ms max.
		Low end	0.45 × VCC	
	Breaking of signal lines		0.15 × VCC	0.1 ms max.
Abnormal conversion of R/D	Excessive residual (ε) of control loop	High end	0.55 × VCC	See the Note below.
		Low end	0.45 × VCC	

Note: It is judged as an internal error when the probability of excessive control residuals exceeds 50 % in the average value for the period of approximate 5 ms during the acceleration mode "ON" or for the period of approximate 120 ms during the acceleration mode "OFF".

(7) Input/output of digital signals

■ Absolute maximum rating

Absolute maximum rating of digital signals is shown in Table 5.

Table 5. Absolute maximum rating of digital signals (VDD = 5V ±5%, Ta = -40~ +125 °C)

Items	Symbol	Applicable terminal	Absolute maximum rating	Unit
Input voltage	V_I	All digital input	-0.3~ VDD+ 0.3	V
Output current	Io	All digital output	±10	mA

■ Recommended operating range

The recommended operating range of digital signals is shown in Table 6.

Table 6. Recommended operating range of digital signals (VDD = 5V ±5%, Ta = -40~ +125 °C)

Items	Symbol	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	2.0		VDD	V
Low level input voltage	V_{IL}	0		0.8	V
Input rising-up time	tri	0		1.0	ms
Input falling-down time	tfi	0		1.0	ms
Hysteresis voltage	V_H		0.2		V
External CLK input frequency	F_{CLK}	18	20	20.4	MHz
Serial clock (SCK) input frequency	F_{SCK}			2	MHz

■ DC characteristics

DC characteristics of digital signals are shown in Table 7.

Table 7. DC characteristics (VDD = 5V ±5%, Ta = -40~ +125 °C)

Items	Sym.	Condition	Min.	Typ.	Max.	Unit
Input pull-up resistor	R_{PU}		30	50	100	kΩ
Input leak current	I_{IL}	V_I = DGND			-250	μA
High level output voltage	V_{OH}	I_{OH} = 0 mA	VDD-0.1			V
Low level output voltage	V_{OL}	I_{OL} = 0 mA			0.1	V
High level output current	I_{OH}	V_{OH} = VDD-0.4V	-8			mA
Low level output current	I_{OL}	V_{OL} = 0.4 V	8			mA

■ AC characteristics

AC characteristics of digital signals are shown in Table 8.

Table 8. AC characteristics (VDD= 5V ±5%, Ta= -40~ +125 °C)

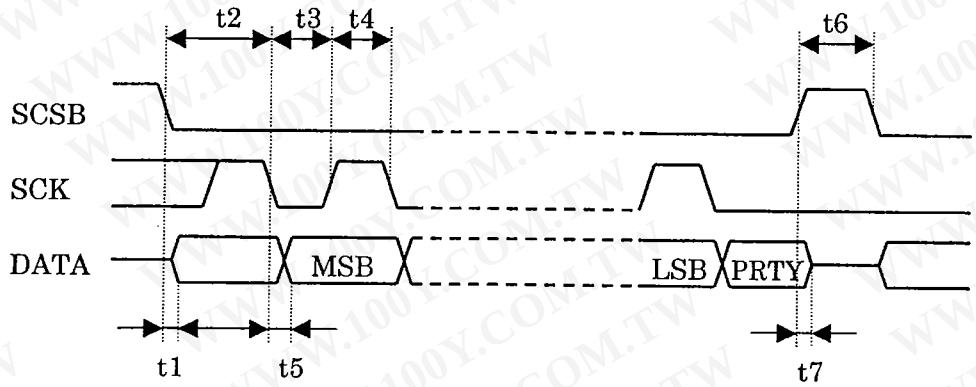
Items	Symbols	Condition	Min.	Typ.	Max.	Unit
Output rising-up time	tr	C_L= 15 pF		1.2	2.2	ns
Output falling-down time	tf	C_L= 15 pF		1.2	2.2	ns
Propagation delay time (Input buffer)	tpd				7.6	ns
Propagation delay time (Output buffer)	tpd	C_L= 15 pF			8.9	ns

Note: Rising-up/falling-down time of output means the time required to pass through the voltage between 0.3 V and 2.7 V.

■ Timing chart

(a) Serial signal interface

The timing chart of serial signals (SCSB, SCK, DATA) is shown in Figure 12.



Parameters	Min.	Typ.	Max.	Unit	Remarks
t1			50	ns	SCSB ↓ → DATA Enable
t2	300			ns	SCSB ↓ → 1st SCK ↓
t3	250			ns	SCK Low Pulse
t4	250			ns	SCK High Pulse
t5			50	ns	SCK ↓ → DATA Valid
t6	300			ns	SCSB High Pulsewidth
t7			50	ns	SCSB ↑ → DATA High-Z

(VDD = 5V ±5%, DGND = 0V, Ta = -40~ +125 °C, CL = 15 pF)

Note: While SCSB input is successively "L", DATA output repeats the same data at every 16 clocks of SCK input, and DATA output comes to "0" after the PRTY bit.

Figure 12. Timing chart of serial signals

(b) Timing of bus control

The timing of bus control is shown in Figure 13.

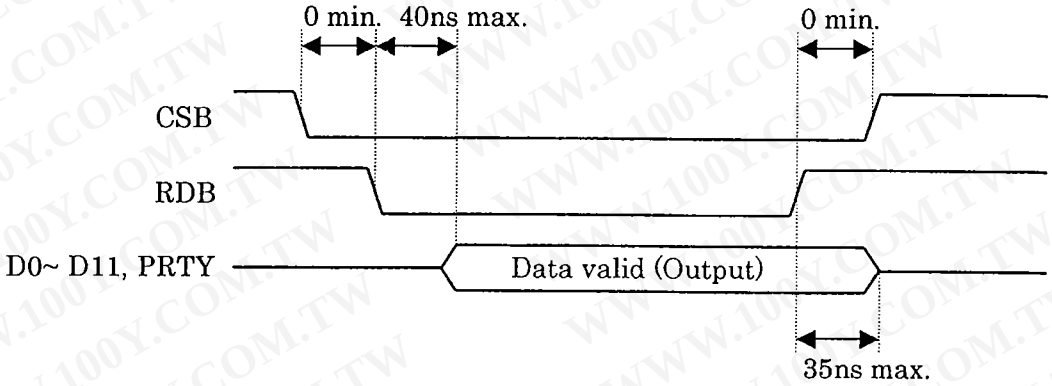


Figure 13. Timing of bus control

(c) Timing of INHB (RD) signal

The timing of INHB (RD) signal is shown in Figure 14.

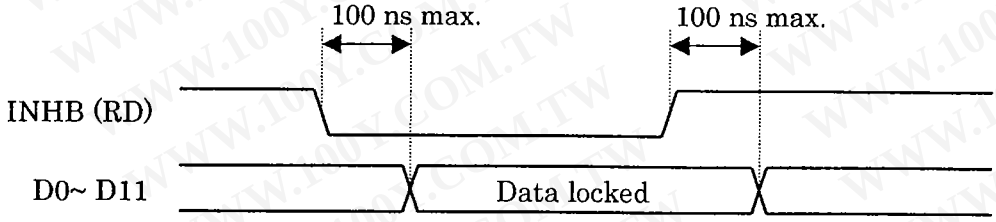


Figure 14. Timing of INHB (RD) signal

(d) Timing of OUTMD signal

The timing of OUTMD signal is shown in Figure 15.

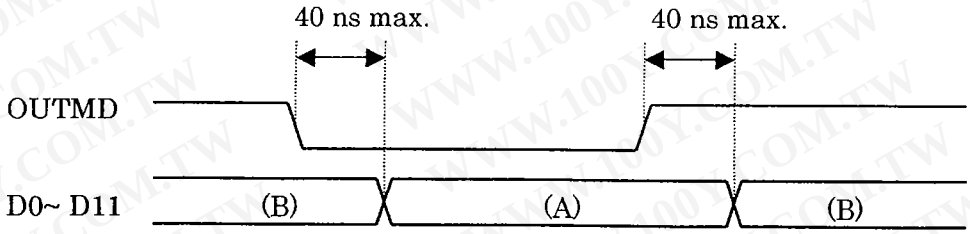


Figure 15. Timing of OUTMD signal

(e) Timing of PRTY signal

The timing of PRTY signal is shown in Figure 16.

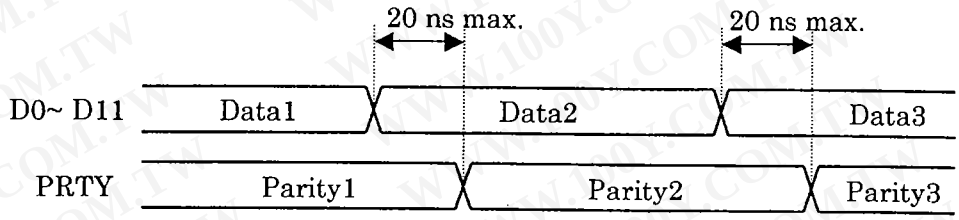
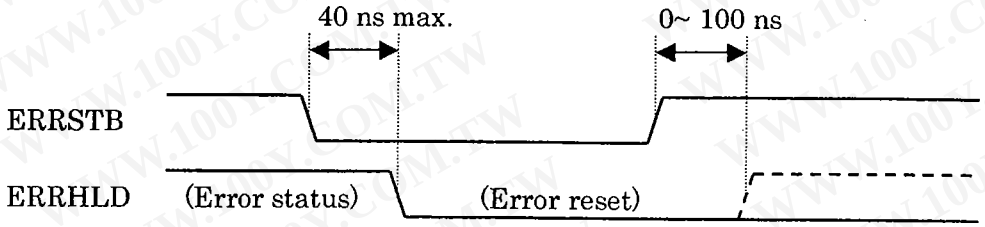


Figure 16. Timing of PRTY signal

(f) Timing of error reset

The timing of error reset is shown in Figure 17.



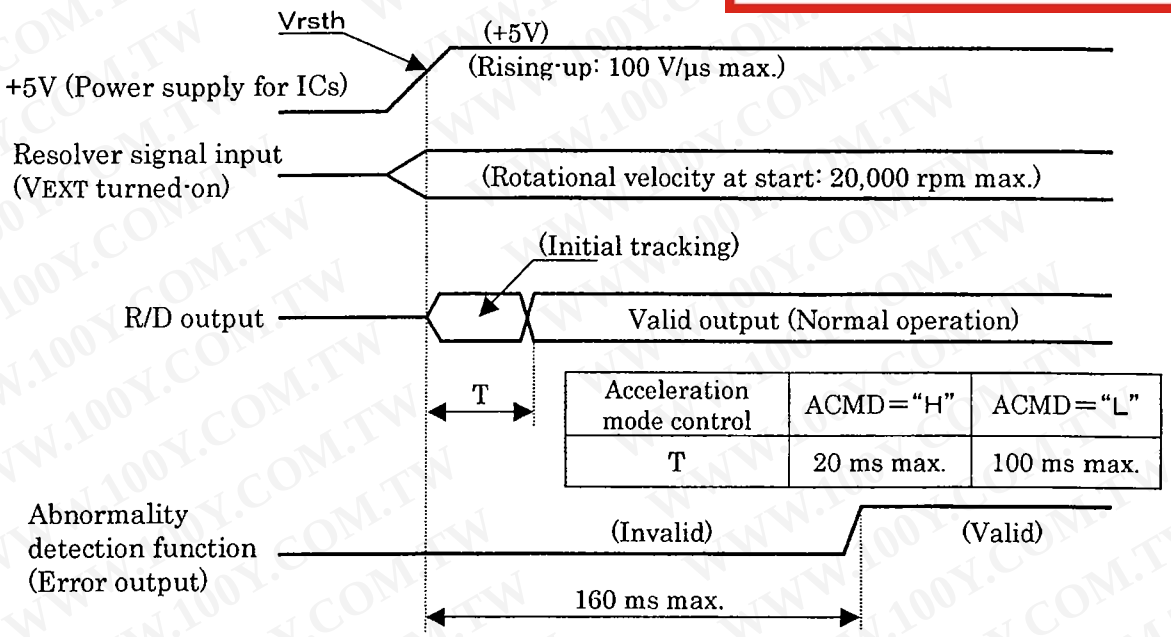
Note: ERRHLD output may transmit when power is turned on (including momentary power outage), when changing the setting condition such as a change of resolution, or when excessive acceleration is continuously applied such that some step inputs are repeated. Therefore, make error reset surely before using. If ERRHLD output does not return to the reset status by error reset, isolate the true cause of the error and remove it.

Figure 17. Timing of error reset

(g) Timing of power on/off

The timing of power-on is shown in Figures 18-1 to 18-4, and the timing of power-off is shown in Figure 19. In actual operation the power should be turned on or started up by any one of the following methods of (i) to (iii).

(i) +5V (Power supply for ICs: VCC & VDD) and the power supply for exciting amplifier of Resolver (V_{EXT}) should be turned on at the same time. Or +5V should be turned on later.
The detailed timing of power-on is shown in Figure 18-1 and the timing of power-off is shown in Figure 19.



Acceleration mode control	ACMD="H"	ACMD="L"
T	20 ms max.	100 ms max.

Figure 18-1. Timing of power-on

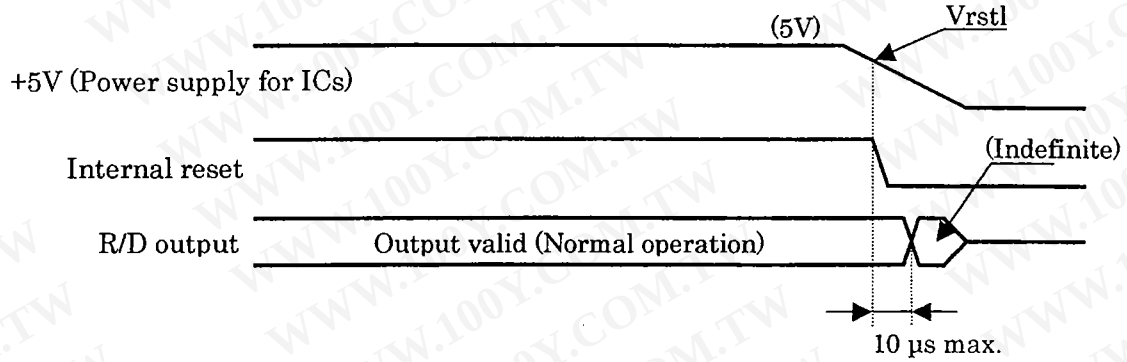


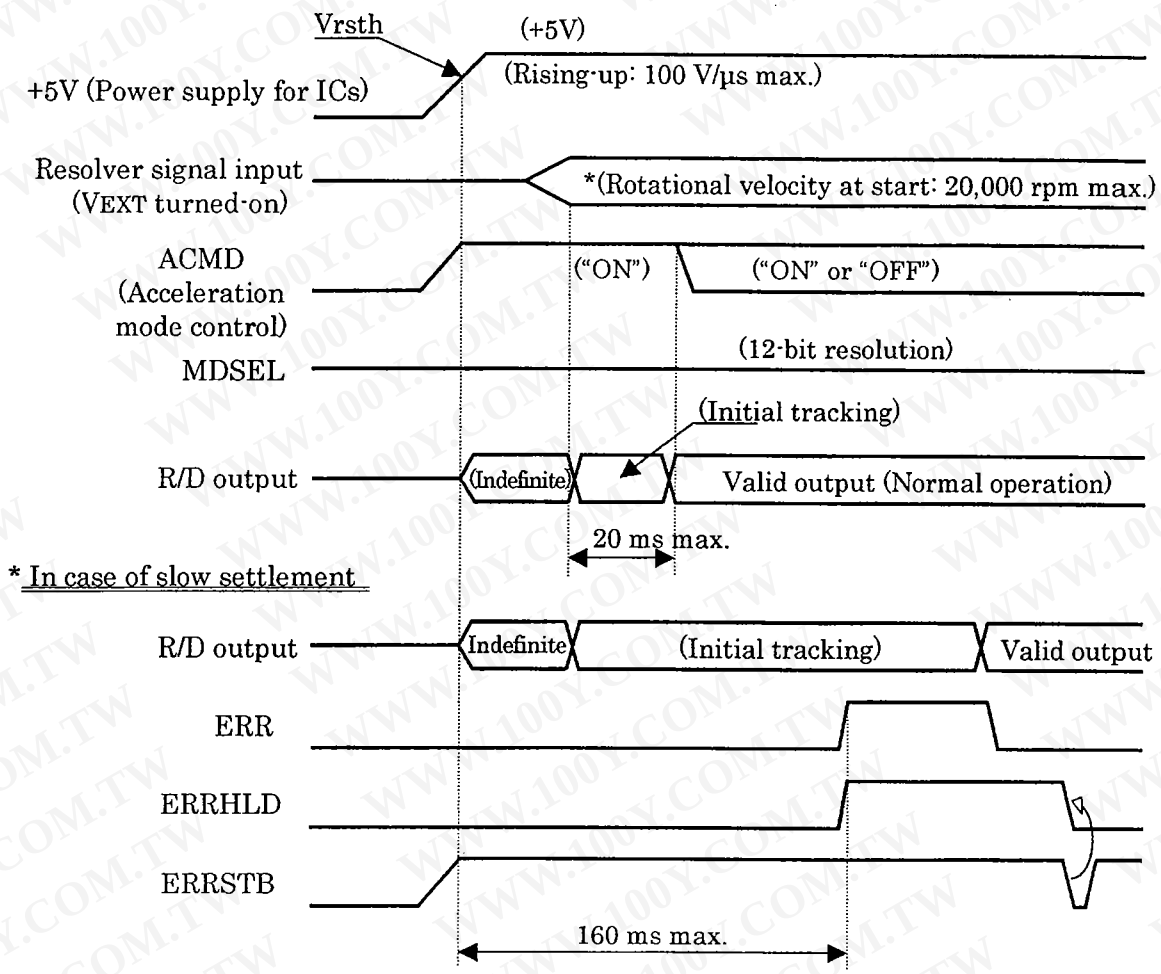
Figure 19. Timing of power-off

■ Specifications of reset voltage

Symbols	Specifications (V)			Remarks
	Min.	Typ.	Max.	
Vrsth	3.9		4.4	Voltage rising-up side
Vrstl	3.7		4.2	Voltage falling-down side
Vrhys		0.2		Hysterisis width

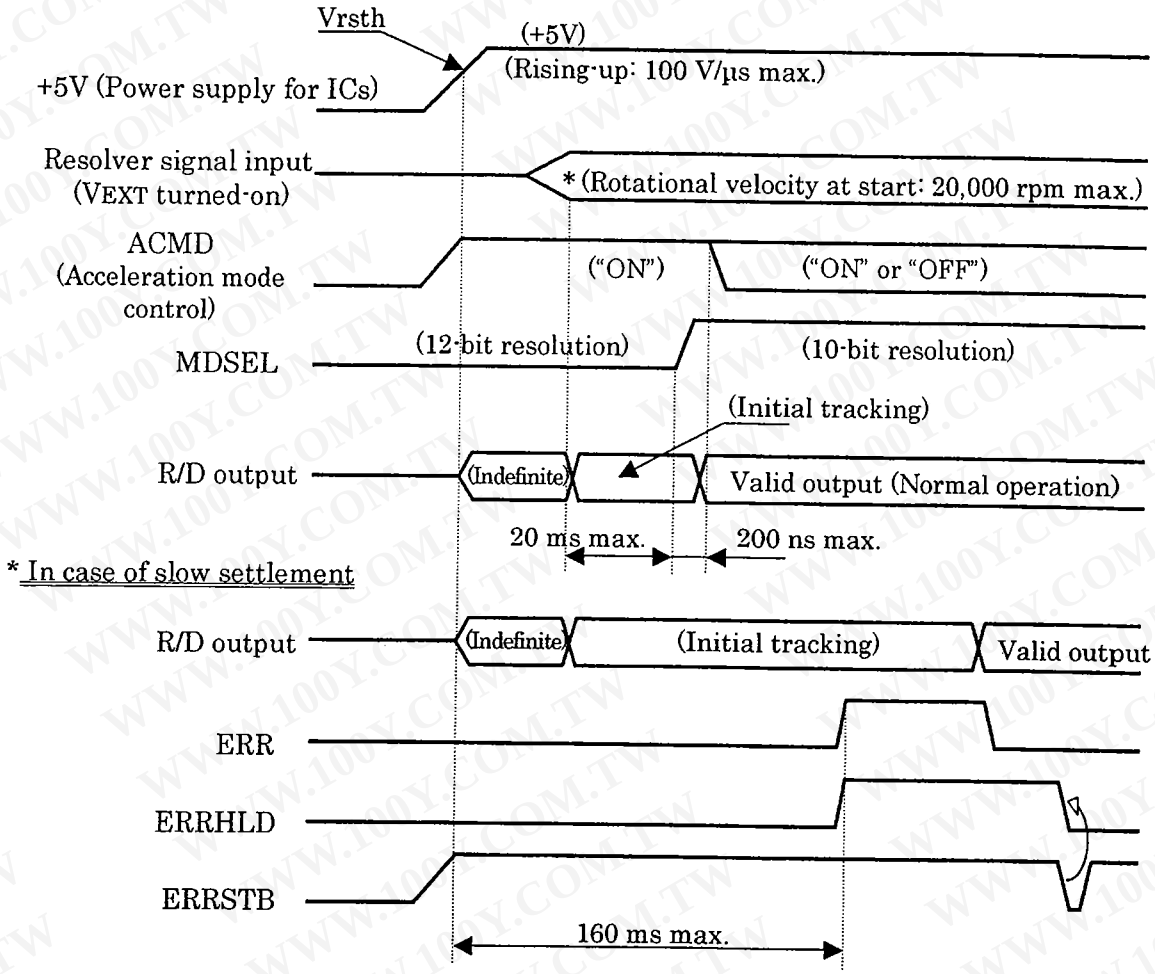
(ii) When +5V (Power supply for ICs: VCC & VDD) has been turned on before the power supply for the Resolver excitation amplifier (V_{EXT}) is turned on, or when only the power supply for the Resolver excitation amplifier (V_{EXT}) has been off instantaneously, it should be started up according to the timing chart (Start-up sequence) shown in Figures 18-2 to 18-4.

Note: In case where some distinguishable time is required to settle the R/D output, an error (Abnormal R/D conversion) may occur until the output is valid. Therefore use it under the condition of system interlock with the error signal in the system operation.



Note *: When the rotational velocity at start exceeds over 20,000 rpm, R/D output may not be rapidly settled. The error (Abnormal R/D conversion) occurs in this case.

Figure 18-2 Timing of power-on
[Start-up sequence for 12-bit resolution in Paragraph (ii)]



Note *: When the rotational velocity at start exceeds over 20,000 rpm, R/D output may not be rapidly settled. The error (Abnormal R/D conversion) occurs in this case.

Figure 18-3 Timing of power-on
[Start-up sequence for 10-bit resolution in Paragraph (ii)]

In case when only the power supply for the Resolver excitation amplifier (VEXT) is instantaneously broken to result any instantaneous breaking on the Resolver signal input, the rapid settlement (i.e. recovering) is performed basically in the same sequence as power-on shown in Figures 18-2 and 18-3 depending on the off-time.

Figure 18-4 shows the recovering sequence of instantaneous power-off for the 10-bit resolution.

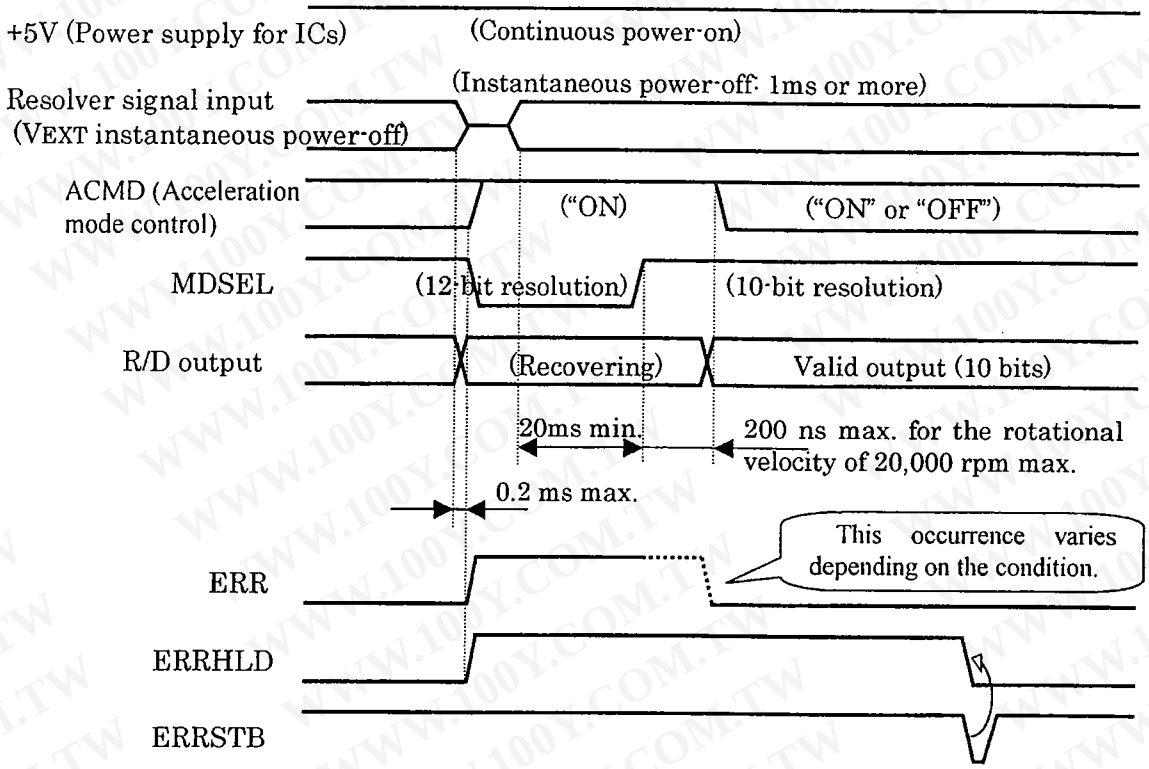


Figure 18-4 Timing of instantaneous VEXT power-off
[Recovering sequence for 10-bit resolution in Paragraph (ii)]

(iii) In case of Paragraph (ii) above, the Resolver excitation power supply can equivalently be supplied at the same time with +5V power supply for ICs (VCC & VDD) by making the circuit structure such as the power supply for Resolver excitation amplifier (VEXT) and +5V power supply for ICs (VCC & VDD) are applied in parallel to the power supply for the Resolver excitation amplifier circuit and then the rapid settlement as Paragraph (i) can be expected. This is the same for the case of instantaneous power-off.

But in case of forming OR circuit by using diodes, it should be noted that +5V power supply for ICs (VCC & VDD) and the power supply for the Resolver excitation amplifier (VEXT) are shortcircuited if any diode might be broken in short-circuit mode.

3.2.8 Power Source

(1) Supply voltage: DC +5 V ±5 % (VCC & VDD),

where the rising rate of power supply should be 100 V/μs max.

(2) Current consumption: 45 mA max. (30 mA typ.),

which means internal current consumption at no load.

3.3 Physical Characteristics

(1) Outline dimensions: 10 × 10 × 1.0 (thickness) mm, TQFP
(Refer to Attached Figure 2.)

(2) Pin assignment: 0.65 mm pitch, 52 pins

(3) Mass: 1 gram max.

3.4 Environmental Conditions

(1) Operating temperature: -40~ +125 °C within the extent shown in Figure 20.
(Ambient temperature)

(2) Storage temperature : -65~ +150 °C

(3) Humidity: 90 % RH max. without condensation

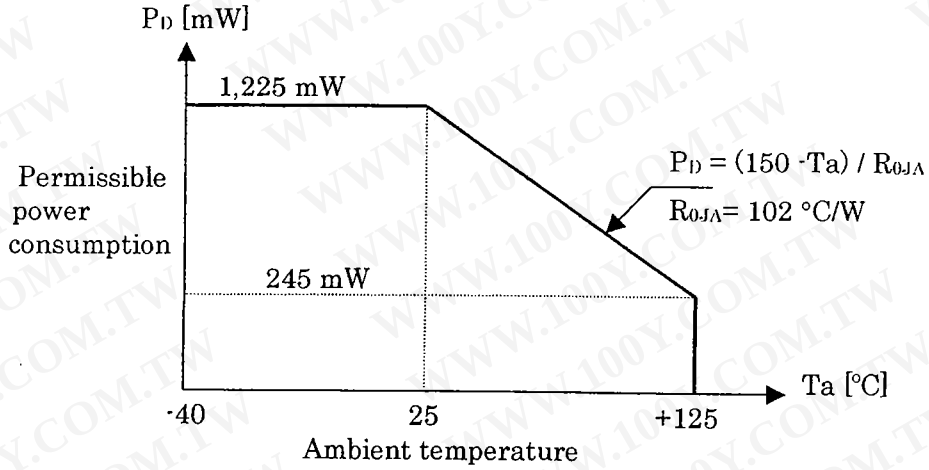


Figure 20. Power derating characteristics

4. Quality Assurance

4.1 Guarantee of Products

Guaranteed term of *Smartcoder (AU6802N1)* is one year after shipping, except in case of conditions caused by disassembling, changing, re-assembling, misusing, or other intention or fault by the customer. Failed products, due to workmanship, within this one-year term will be replaced at no charge.

Smartcoder (AU6802N1) is a semi-conductor integrated circuit (i.e. electronic device) with high-grade quality level for use in automobiles, trains, etc. and is designed for units involving direct control and safety of transportation equipment.

The predicted Mean Time Between Failure (MTBF) is considerably long, but the failure rate is not zero. Therefore, the customer is to assume this responsibility, considering the possibility of failure, and to design multiple back-up measures within the equipment or system to avoid a serious system failure.

4.2 Reliability Test

The following reliability tests are performed to establish the quality of products for the initial manufacturing of the products as shown in Table 9.

Table 9. Contents of Reliability Test

Test items	Condition	Number of samples	Test time	Remarks
High temperature operating life test	Ta= 125 °C (5.25 V)	116	2,000 hr	
High temp. & humidity continuous operation test	85 °C/ 85 % RH (5.25 V)	77	2,000 hr	
Pressure cooker test	121 °C/ 100 % RH 2 atm-pressure	77	500 hr	
Temperature cycle test	-65 / +150 °C 15 minutes for holding 5 minutes for transition	77	2,000 Cyc.	
Latch-up test	Current injection of 250 mA	5	---	

ESD Test

Test items	Description of test	Condition	Number of samples	Remarks
Machine model	All pins to GND/ Power supply pins (R =0 Ω, C =200 pF)	Starting voltage: ±50 V Step voltage: ±50 V~ ±200 V	48	
Human body model	All pins to GND/ Power supply pins (R=1.5 kΩ, C=100 pF)	Starting voltage: ±0.5 kV Step voltage: ±0.5 kV~ ±2 kV	48	

5. Ordering Information

■ AU6802N1 ··· ··· Burn-in* applied products

Note *: Burn-in conditions: Active burn-in (+125 °C, 5.25 V, 8 hrs)

6. Application Note

Examples of practical circuits for application are shown as follows. These examples show only the basic concepts, therefore the decision of constants for practical resistors and the function of protection for input/output circuits, etc. should be designed for each application.

6. 1 Resolver Interface Circuit

(1) Exciting voltage booster amplifier circuit (for single power source)

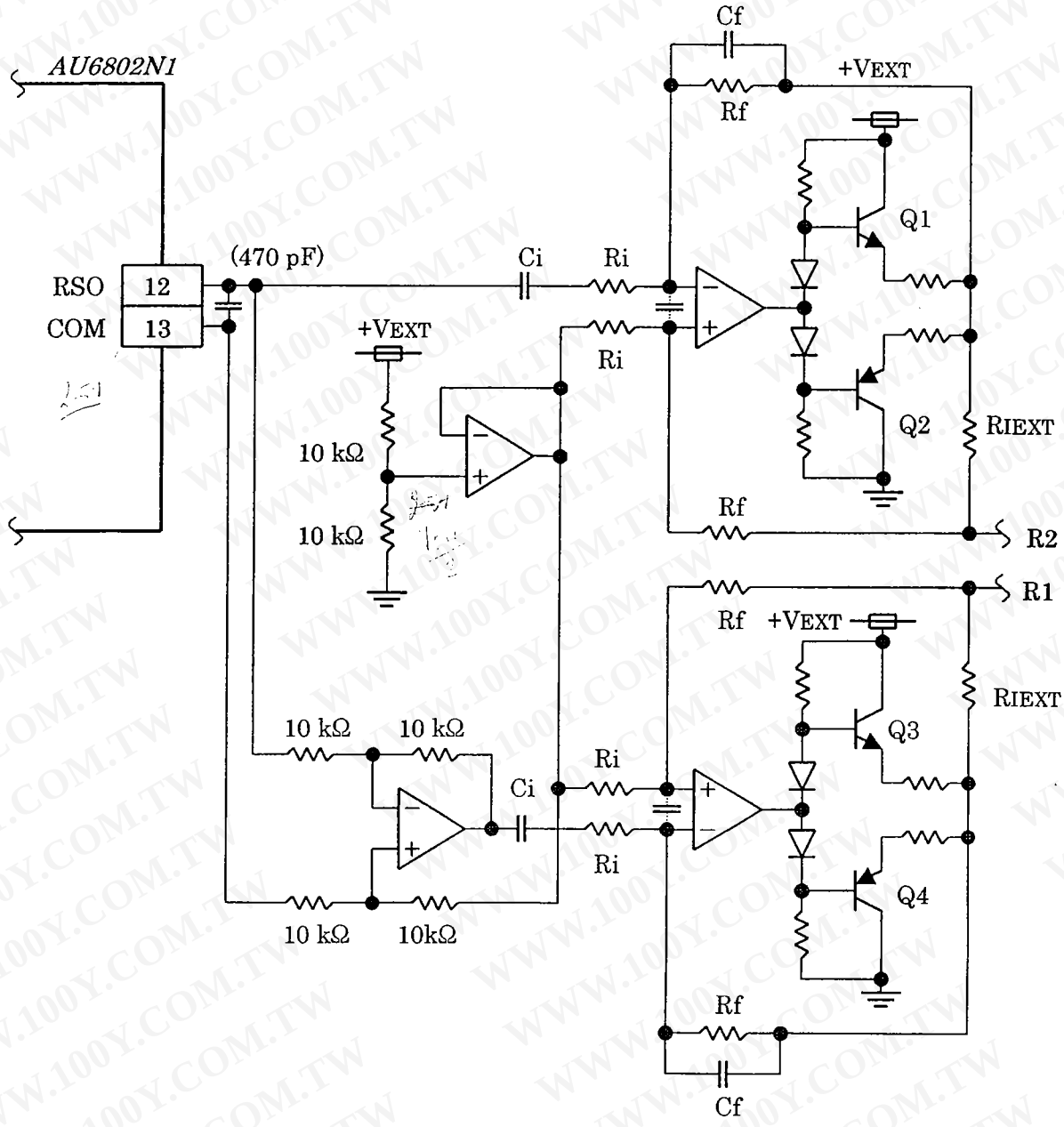


Figure 21-1 Example of exciting voltage booster amplifier circuit (for single power source)

(2) Exciting voltage booster amplifier circuit (for dual power sources)

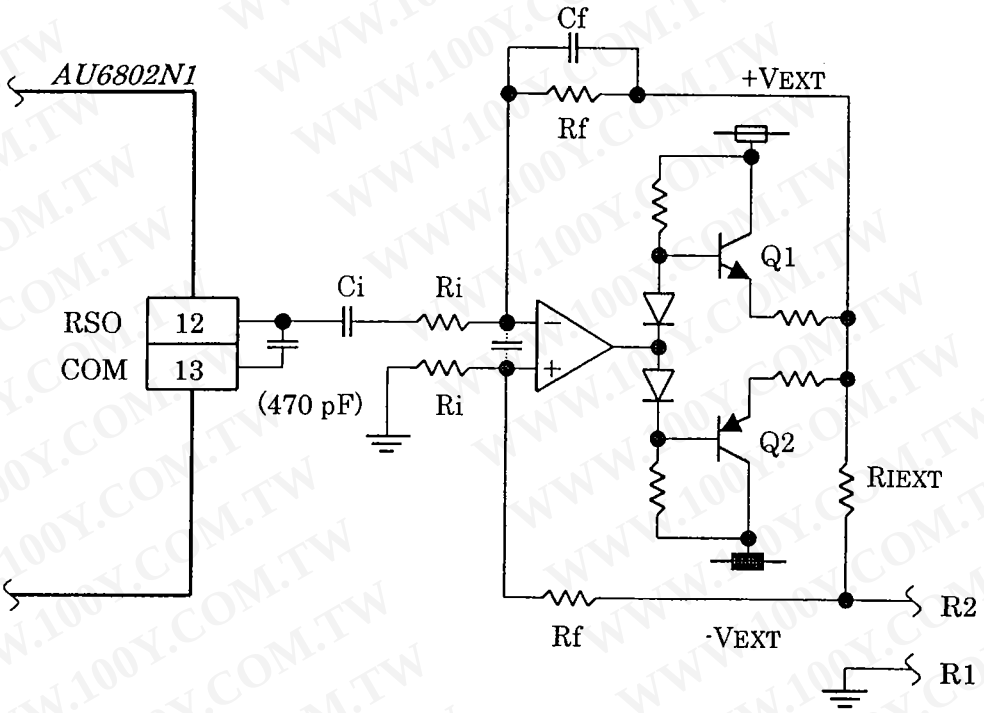


Figure 21-2 Example of exciting voltage booster amplifier circuit (for dual power sources)

(3) Method for setting constants of exciting voltage booster amplifier circuits

The exciting voltage booster amplifier circuits shown as reference are both current control type, and are effective in avoiding the secondary failure caused by a short circuit of exciting lines and can improve the S/N ratio of Resolver signals by means of voltage boosting.

<Description of symbols>

+VEXT, -VEXT: External power supply (For exciting voltage booster amplifier circuit)
IREF: Exciting current of Resolver
RIEXT: Resistor for setting exciting current of Resolver
VREF: Exciting voltage of Resolver
ZRO: Input impedance of Resolver (Specified value)
VRSO: Output voltage of RSO terminal (AU6802N1) (= 2 VP-P)

Step 1: Calculate the exciting current by setting the exciting voltage based on the voltage of external power supply.

$$V_{REF} = I_{REF} \times Z_{RO}$$

Step 2: Calculate the circuit constants based on the exciting current.

$$I_{REF} = (V_{RSO} \times Rf) / (R_{IEXT} \times Ri)$$

<Setting condition>

- $R_{IEXT} \leq (Z_{RO}/10)$ [Ω]
- $Rf \geq 50$ kΩ, $Ci \times Ri \geq 5 \times 10^{(-4)}$ [s], $Cf \times Rf \leq 5 \times 10^{(-6)}$ [s]
- The power supply for an operational amplifier should be the same as that for the transistor buffer.

(4) Input circuit for Resolver signals

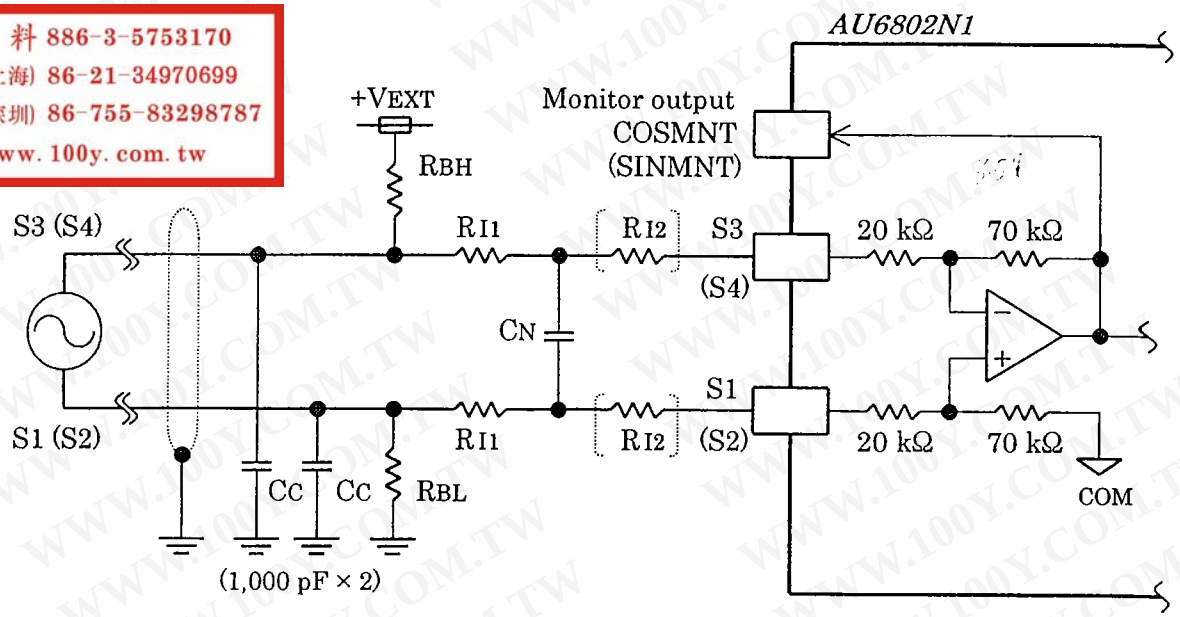


Figure 22. Input circuit for Resolver signals

(5) Method for setting constants of input circuit for Resolver signals

According to the voltage level of Resolver signals (S1-S3, S2-S4), the input gain should be adjusted for the monitor output voltage (COSMNT, SINMNT: Internal signal processing voltage) to be approximately 2 to 3 $V_{P\text{-}P}$. [Note that if this voltage is set out of the range of 0.5 to 3.5 $V_{P\text{-}P}$, abnormal sensor signal will occur!] Also, the value of capacitor (C_N) for normal mode filter is determined corresponding to its noise environment.

Step 1: Set the input gain

$G = 70\ k\Omega / (R_I + 20\ k\Omega)$,

where $R_I = R_{I1} + R_{I2}$, and the tolerance of resistances should basically be ±1 % max., but it should be ±0.25 % max. for high precision applications in the resolution of 12 bits.

Step 2: Set the normal mode filter

Time constant of filter: $T = 2 \times R_{I1} \times C_N$ [s]

Step 3: Set the resistance (R_{BH}, R_{BL}) for applying DC bias

DC bias is applied for the purpose of detecting any breaking of Resolver signal lines (S1~ S4), but it may cause an error in R/D conversion accuracy at the same time. Therefore, it is necessary to consider that the resistor for applying DC bias should be as large as possible in the range negligible to the output impedance (Z_{SS}) of the Resolver, and simultaneously the output value of the Resolver signal monitor should be less than the threshold value of 0.15 × VCC when any breaking of line occurs. In case where DC bias is not set (i.e. RBH and RBL is not attached), the detection of breaking lines is impossible.

(6) Examples of Resolver interface

The constants and parameters of Resolver interface are shown in Table 10 for reference.

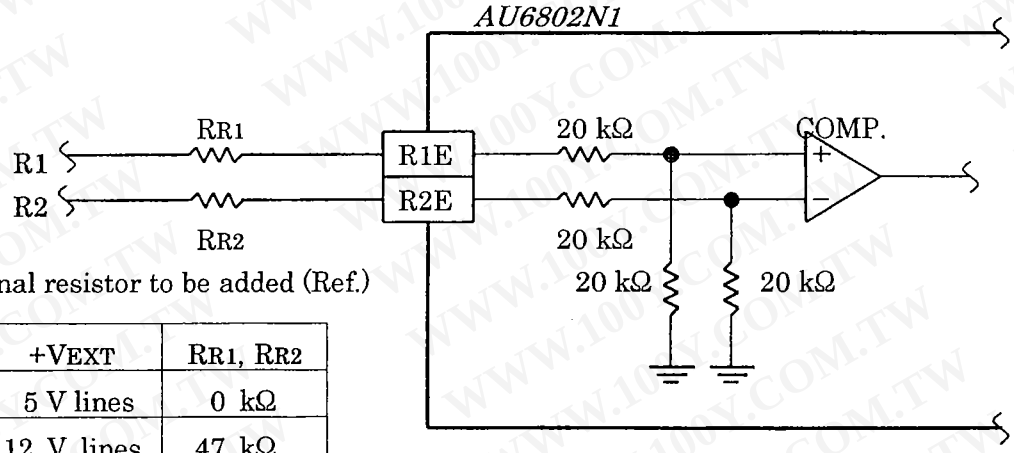
Table 10. Examples of Resolver interface

Power supply for exciting and +VEXT (In case of single power source)	Exciting voltage (VREF) [VP-P]	Resistance for bias [kΩ]		Resolver characteristics		G (Gain)	R1 [kΩ]	Monitor output voltage [VP-P]
		RBH	RBL	Transformation ratio (K)	Signal voltage [VP-P]			
+5 V (Reg.)	4	20	20	0.286	1.144	× 2.33	10	2.67
				0.5	2.0	× 1.32	33	2.64
+12 V (Bat.)	8	50	20	0.286	2.288	× 1.11	43	2.54
				0.5	4.0	× 0.63	91	2.52
+12 V (Reg.)	16	50	20	0.286	4.576	× 0.58	100	2.67
				0.5	8.0	× 0.32	200	2.55
+24 V (Bat.) or +24 V (Reg.)	20 (7 Vrms)	100	20	0.286	5.72	× 0.47	130	2.67
				0.5	10.0	× 0.27	240	2.69
	24 (8.5 Vrms)	100	20	0.286	6.864	× 0.39	160	2.67
				0.5	12.0	× 0.22	300	2.63

Note: In the above column of power supply, (Reg.) means regulated power supply and (Bat.) means power supply by battery.
+12 V (Bat.): +8~ 16 V; +24 V (Bat.): +16~ 32 V

(7) Method of external signal input for exciting Resolver

The equivalent circuit of external signal input for exciting Resolver (R1E, R2E) is shown in Figure 4, but the input voltage of R1 and R2 at the point of the terminals R1E and R2E should not exceed VCC (Power supply voltage) by means of adding the external resistor (RR1, RR2) to divide the voltage.

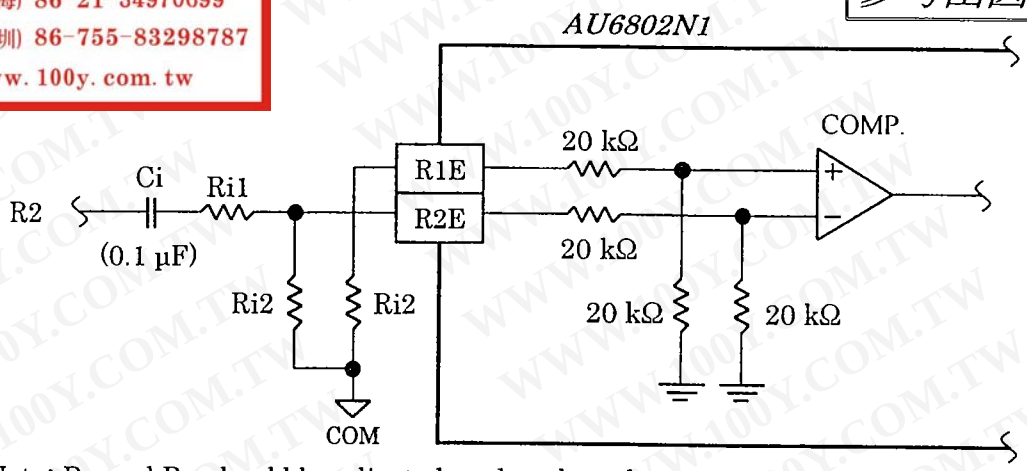


External resistor to be added (Ref.)

+VEXT	RR1, RR2
5 V lines	0 kΩ
12 V lines	47 kΩ
24 V lines	120 kΩ

Figure 23-1. External signal input circuit for exciting Resolver
(In case of single power source for exciting circuit)

参考出図



Note: R_{i1} and R_{i2} should be adjusted so that the voltage at R2E terminal is within 5 V.

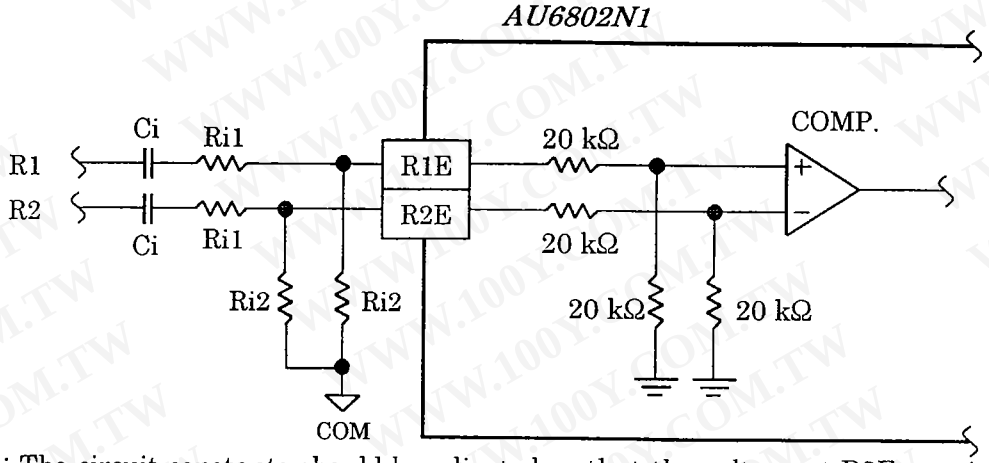
Figure 23-2. External signal input circuit for exciting Resolver
(In case of dual power source for exciting circuit)

(8) Method for adjusting the phase of external input signal for exciting Resolver

When any phase difference exists between the exciting component of Resolver signals (S1– S3 & S2– S4) and the external input signal for exciting Resolver (R1E/R2E), the loop gain of R/D conversion loop is equivalently decreased, which may affect the performance of R/D conversion.

For adjusting the phase, the phase difference between the exciting component of Resolver signal monitor terminals (COSMNT & SINMNT) and the external input signal for exciting Resolver (R1E/R2E) is monitored and a phase adjustment circuit should be inserted into R1E/R2E line so that the phase difference is 10 degrees or less.

(i) Adjustment method for leading phase



Note: The circuit constants should be adjusted so that the voltage at R2E terminal is within 5 V.

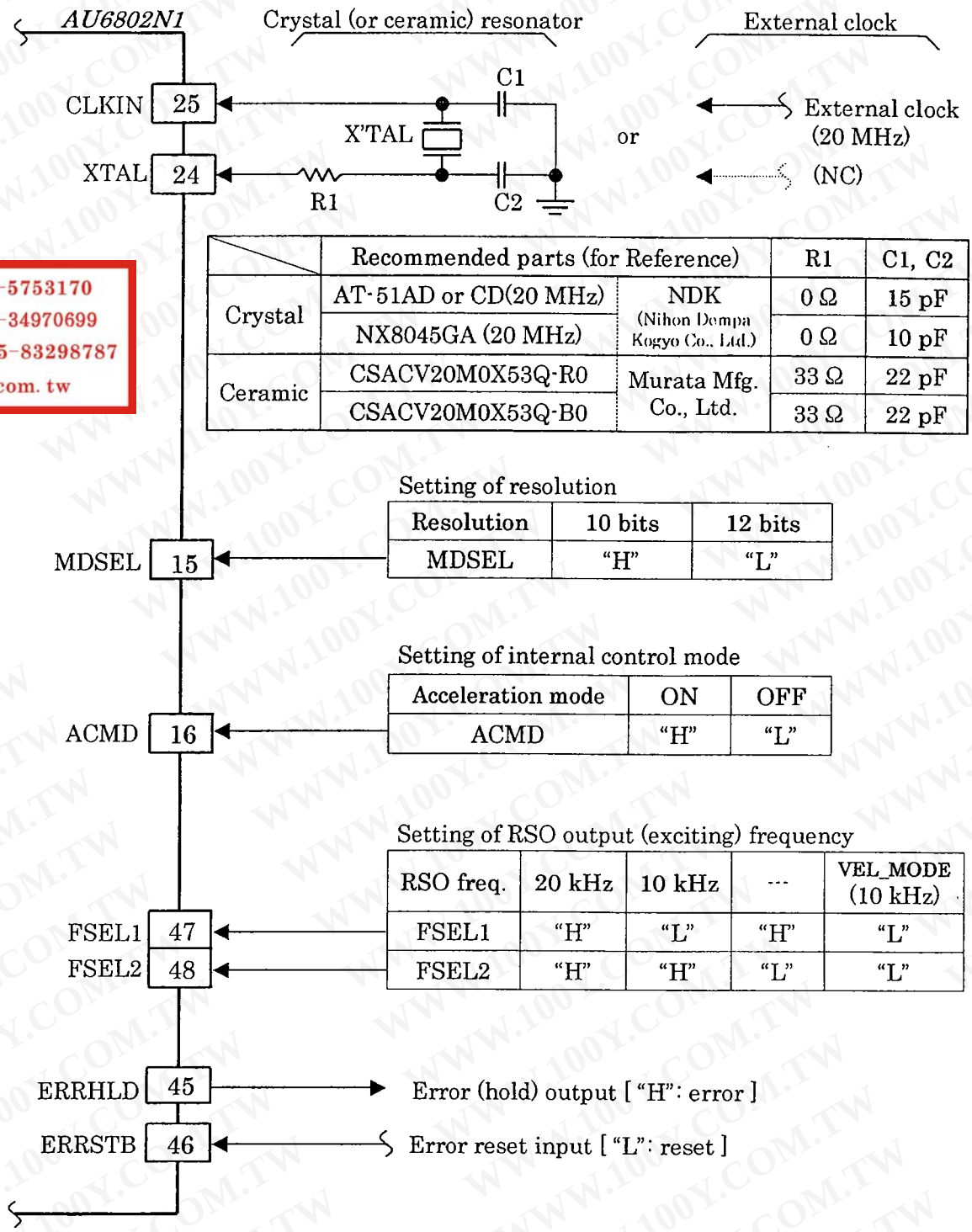
Figure 24. Adjustment method of external input for exciting Resolver
(Leading phase)

(ii) Adjustment method for lagging phase

Insert an adequate capacitor between the R1E and R2E terminals in Figure 23-1 or 23-2.

6.2 System Setting of Smartcoder (AU6802N1)

The procedure for setting the system of *Smartcoder (AU6802N1)* is shown in Figure 25.



	Recommended parts (for Reference)		R1	C1, C2
Crystal	AT-51AD or CD(20 MHz)	NDK (Nihon Dempa Kogyo Co., Ltd.)	0 Ω	15 pF
	NX8045GA (20 MHz)		0 Ω	10 pF
Ceramic	CSACV20M0X53Q-R0	Murata Mfg. Co., Ltd.	33 Ω	22 pF
	CSACV20M0X53Q-B0		33 Ω	22 pF

Setting of resolution

Resolution	10 bits	12 bits
MDSEL	"H"	"L"

Setting of internal control mode

Acceleration mode	ON	OFF
ACMD	"H"	"L"

Setting of RSO output (exciting) frequency

RSO freq.	20 kHz	10 kHz	---	VEL_MODE (10 kHz)
FSEL1	"H"	"L"	"H"	"L"
FSEL2	"H"	"H"	"L"	"L"

Figure 25. System setting of Smartcoder (AU6802N1)

6.3 Output Interface of Smartcoder (AU6802N1)

(1) Pulse (+ Serial data) interface mode

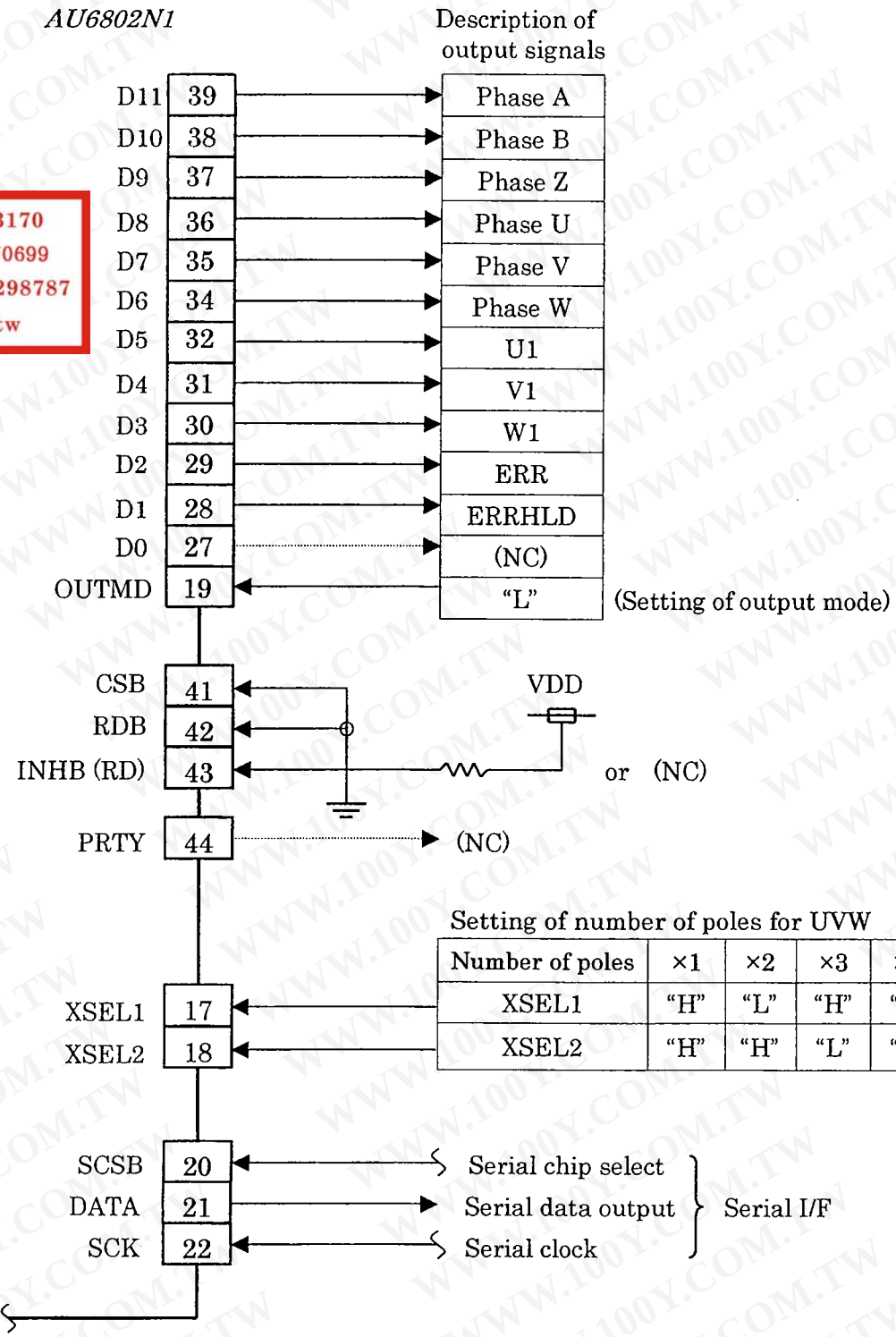


Figure 26. Pulse (+ Serial data) interface mode

参考出図

(2) Parallel I/O interface mode (Stand-alone)

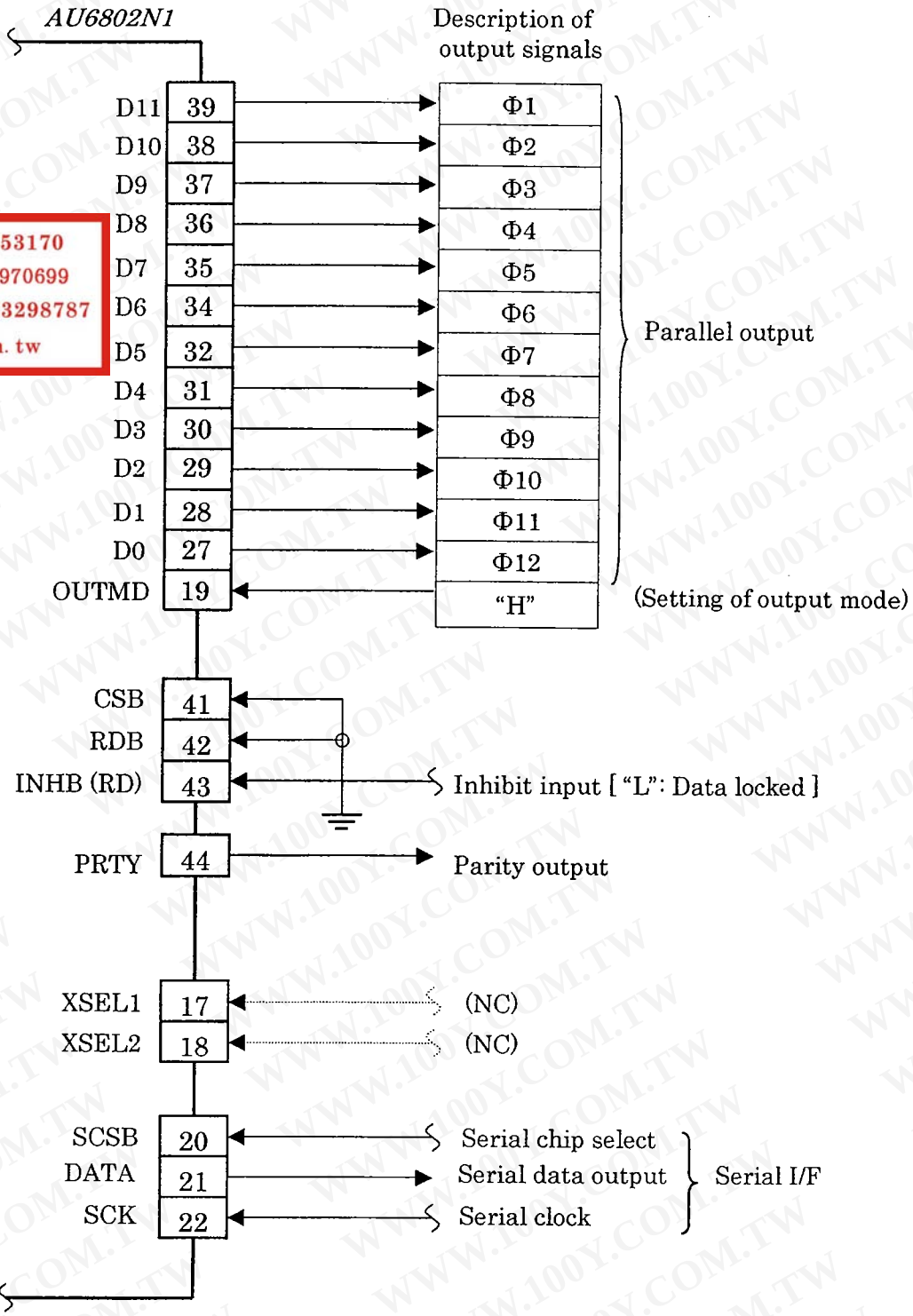


Figure 27. Parallel I/O interface mode (Stand-alone)

参考出図

(3) Parallel bus interface mode

VEL_MODE
[FSEL1= "L"]
[FSEL2= "L"]

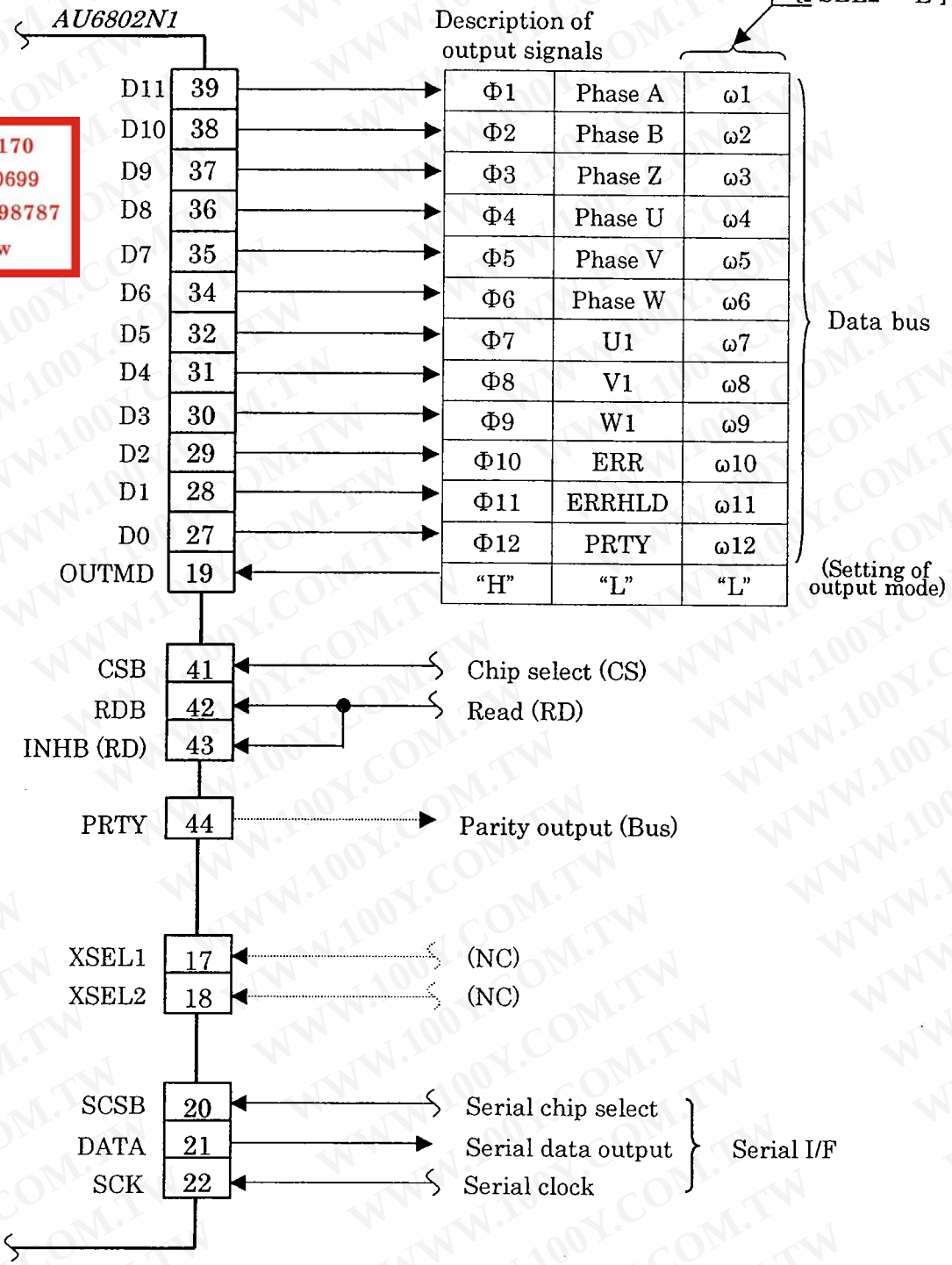


Figure 28. Parallel bus interface mode

DWG No.	3	4	5	6	7	8	9	10	11	12	Sheet
8 0	1	1	0	1	4	1	1	I	4	E	33/

6.4 Countermeasures for Noise

When the Resolver is used as a sensor for an electric motor in particular, various types of noise may affect the system performance depending on the driving control mode of the motor. Therefore, it is necessary to consider some methods to maintain the performance of inherent Resolver signals without overlapped noise and keep the R/D conversion normal.

Smartcoder (AU6802N1) is a fast response R/D conversion IC designed to have considerable noise immunity. However it cannot resist all environments of noise. Depending on the application, some countermeasures to avoid/eliminate noise may be required. Some practical countermeasures against noise are as follows.

(1) Magnetic interference noise

When the leakage flux of the motor passes through the Resolver, the Resolver signal acts as if the angle were changed, which will generate errors.

Countermeasure I When mounting the motor and Resolver, consider the structure and materials to shield them and minimize the magnetic loop by means of cutting the magnetic field off (i.e. magnetic shielding effect).

Countermeasure II When leakage flux cannot be completely prevented, the exciting voltage (i.e.current) of the Resolver should be increased to improve the S/N ratio to its inherent signal. <Refer to Paragraph 6.1.>

(2) Electrical interference noise

The electrical interference noise (i.e. spike noise and others) caused by PWM drive of the motor is extremely strong and affects all circuits of exciting and signal lines of the Resolver, power supply lines and others through various passes. <Refer to Paragraph 6.1.>

Countermeasure III Spike noise is removed by inserting the common mode/normal mode filter into Resolver exciting lines (R1-R2). Generally, these noises are not likely to be induced on low impedance exciting lines and then the countermeasures are needed a few in this case.

Countereasure IV Spike noise is removed by inserting the common mode/normal mode filter into the Resolver signal lines (S1-S3 & S2-S4). It is important to select the time constant of filter to be effective only for noise and not to affect the inherent waveform of Resolver. And it should be considered that these electrical waveforms of noise on S1~ S4 have the same phase to AGND. In case when any error occurs by the electrical interference noise after this countermeasure has been introduced, it is effective to decrease the Resolver signal level.

Countermeasure V For the lines of power supply (VCC, VDD), a by-pass capacitor or equivalent should be inserted in some cases.

(3) Other types of noise

Countermeasure VI Twisted pair lines with shielding each pair should be used for wiring to the Resolver, and the end of the shield should be connected to AGND at the circuit side together. Also the wiring should be separated from any motor cable.

Countermeasure VII GND (Ground) lines should be low impedance type to insure noise reduction from common impedance and to be effective for shielding. It is one method whereby the potential of a driver heat sink, motor case, etc. is made equal to control ground (GND).

Countermeasure VIII Motor driver circuits and sensor circuits should be physically separated and covered with a shield case respectively.

6.5 Switching of Internal Control Mode in R/D Conversion

The type of R/D conversion in Smartcoder (AU6802N1) is based on the negative feedback control system with the closed loop structure referred conventionally as the tracking type, and its control method has the configuration of Type II with the PI (Proportion and Integral) compensation. Therefore any tracking error in constant velocity (i.e. constant velocity deviation) is not principally generated unless the phase difference to the exciting component exists in the signal voltages, but some instantaneous tracking delay or overshooting cannot be avoided at the input of excessive angular acceleration by a sudden change of angular velocity or an external turbulence to the mechanical shaft of Resolver (i.e. shock), etc.

By means of improving the dynamic accuracy in the wide range including unexpected high angular acceleration, more correct sensing is possible to the mechanical angular rotation. In addition to the improvement of inherent dynamic accuracy, the switching of internal control mode is expected to improve the dynamic performance more and to contribute to the improvement of control efficiency in the application of motor control.

The switching of internal control mode in Smartcoder (AU6802N1) is performed as follows.

(1) Control method in R/D converter (Control elements)

The method of internal PI (Proportion and Intergral) control is shown in the following equation:

$$\text{(PI Control elements)} = Kv\{1 + 1/(Ti \cdot s)\}$$

where Kv: Proportional gain; Ti: Integral time constant; s: Raplace operator.

(2) List of internal control modes

No.	Name of control mode	Description of control mode
1	Normal mode	Normal operation mode except the acceleration mode below
2	Acceleration mode	High tracking rate mode by enlarging the proportional gain (Kv) by 32 times of that in normal mode.

(3) Switching conditions entering to/releasing from acceleration mode

Acceleration mode control (ACMD)		"ON"	"OFF"
Condition for entering	When power is turned on	O	---
	At returning from abnormal sensor signal	O	See Note * below.
	At exceeding threshold value	O	---
Condition for releasing		Within the threshold for releasing	

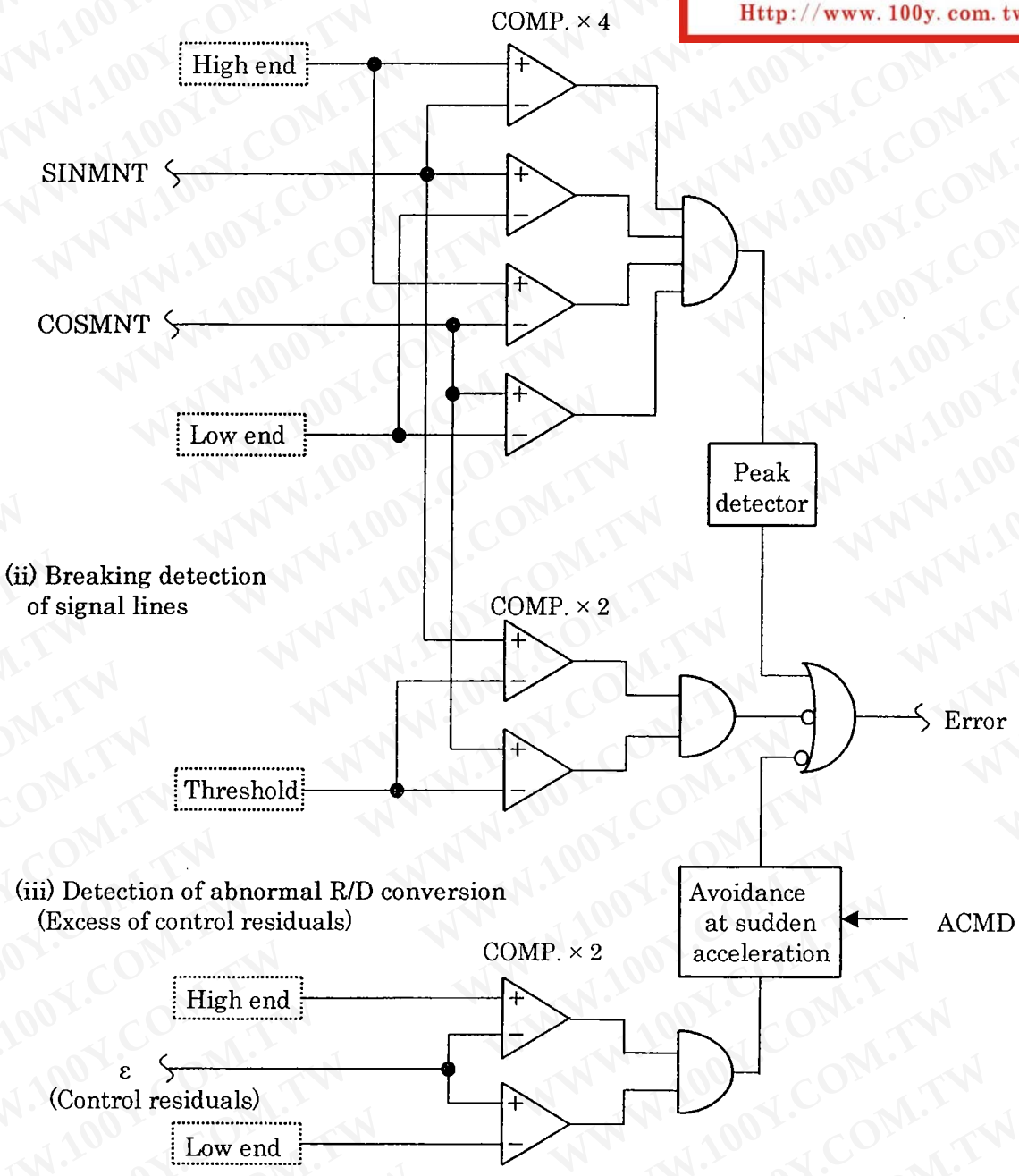
Note *: Only when the deviation of control residual polarity exceeds the threshold value for entering into acceleration mode described below just after returning from the state of abnormal sensor, the mode is in acceleration mode until it first turns into the threshold value for releasing.

(4) Threshold value for switching

Exciting frequency setting (FSEL1, 2)	Decision time	Threshold value for switching (Deviation of control residual polarity)	
		Entered to acceleration mode	Released from acceleration mode
10 kHz	400 μs	±76.8 %	±25.6 %
20 kHz	200 μs	±70.4 %	±25.6 %

Note: It is considered that the acceleration mode does not occur frequently in usual operation except in special cases. But if it occurs in practical operation, it may seem that some abnormal operation has occurred momentarily at observing the output waveform, because the loop gain of control system suddenly changes to 32 times. Note that even in non-actual operation, the deviation of control residual polarity may exceed the said threshold value due to excessive magnetic/electrical distortion of waveform, or an electrical error in the Resolver signals, or some noise, etc., and the acceleration mode may occur.

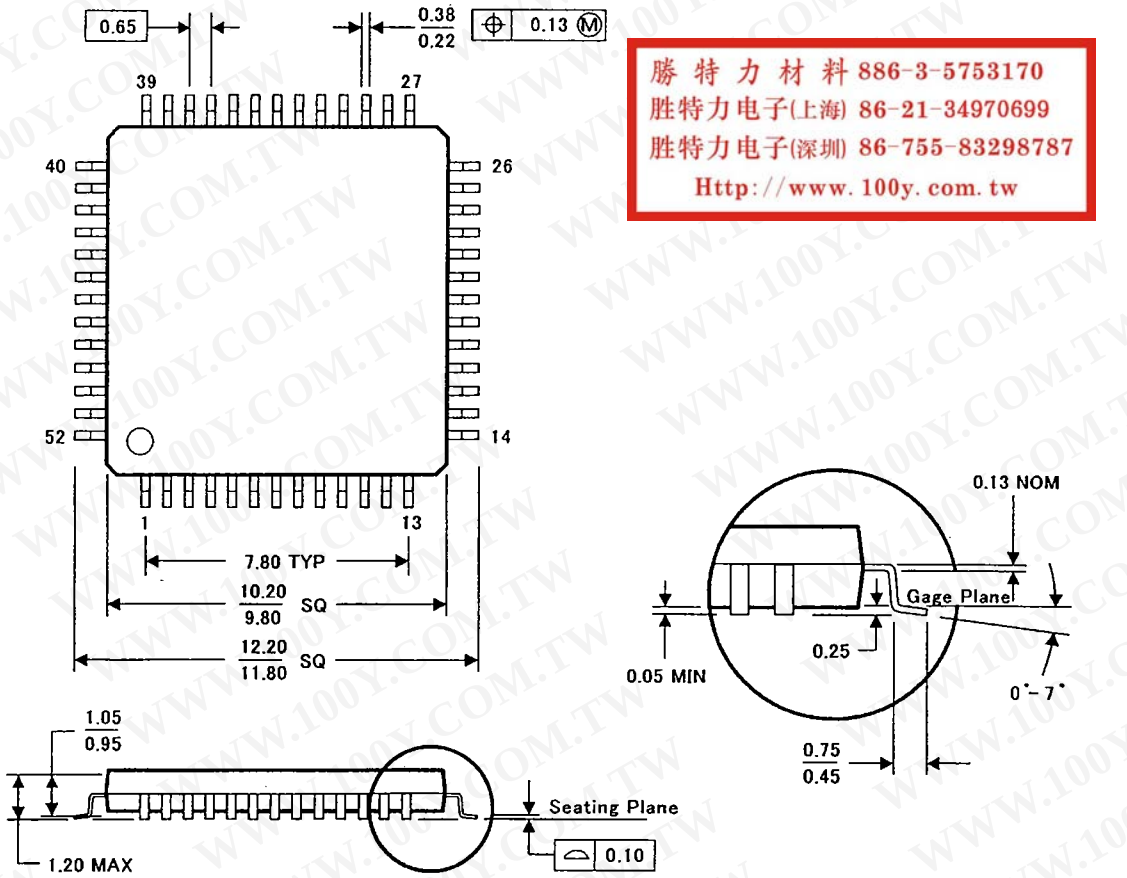
(i) Breaking/Down detection of exciting lines



Attached figure 1. Block diagram of built-in test (Internal error detection) circuit

	DWG No.	3	4	5	6	7	8	9	10	11	12	Sheet
	8	0	1	1	0	1	4	1	1	I	4	E	36/

参考出図



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Attached figure 2. Outline drawing of package

DWG	No.	3	4	5	6	7	8	9	10	11	12	Sheet
8	0	1	1	0	1	4	1	1	I	4	E	37/37