HD49334AF/AHF

CDS/PGA & 10-bit A/D Converter

REJ03F0105-0200
Rev.2.00
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Description

The HD49334AF/AHF is a CMOS IC that provides CDS-PGA analog processing (CDS/PGA) suitable for CCD camera digital signal processing systems together with a 10-bit A/D converter in a single chip.

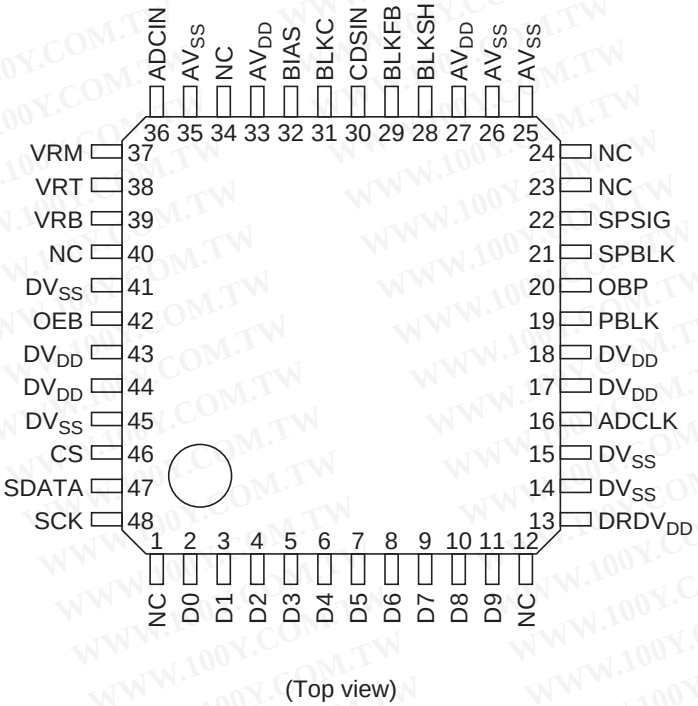
Functions

- Correlated double sampling
- PGA
- Offset compensation
- Serial interface control
- 10-bit ADC
- Operates using only the 3 V voltage
- Corresponds to switching mode of power dissipation and operating frequency
  Power dissipation: 120 mW (Typ), maximum frequency: 36 MHz (HD49334AHF)
  Power dissipation: 60 mW (Typ), maximum frequency: 25 MHz (HD49334AF)
- ADC direct input mode
- QFP 48-pin package

Features

- Suppresses low-frequency noise output from CCD by the S/H type correlated double sampling.
- The S/H response frequency characteristics for the reference level can be adjusted using values of external parts and registers.
- High sensitivity is achieved due to the high S/N ratio and a wide coverage provided by a PG amplifier.
- Feedback is used to compensate and reduce the DC offsets including the output DC offset due to PGA gain change and the CCD offset in the CDS (correlated double sampling) amplifier input.
- PGA, standby mode, etc., is achieved via a serial interface.
- High precision is provided by a 10-bit-resolution A/D converter.

Pin Arrangement



(Top view)

Pin Description

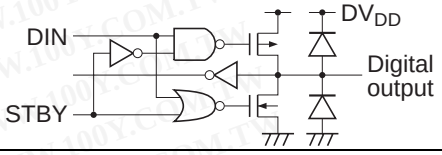
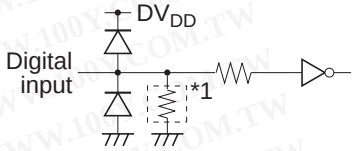
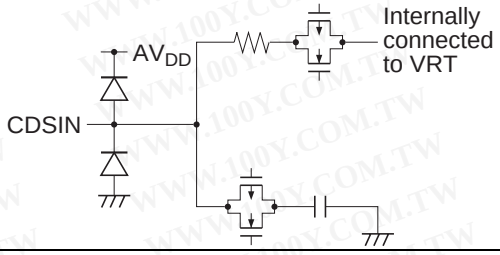
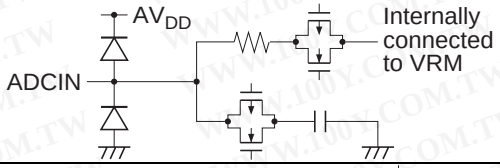
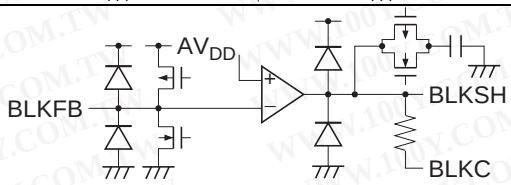
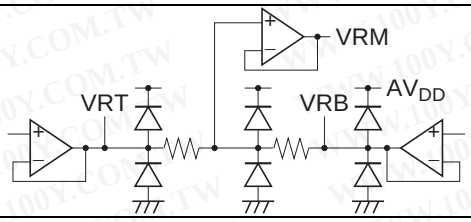
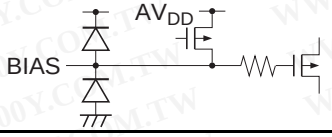
Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
1	NC	No connection pin	—	—
2 to 11	D0 to D9	Digital output	O	D
12	NC	No connection pin	—	—
13	$DRDV_{DD}$	Output buffer power supply (3 V)	—	D
14	DV_{SS}	Digital ground (0 V)	—	D
15	DV_{SS}	Digital ground (0 V)	—	D
16	ADCLK	ADC conversion clock input pin	I	D
17	DV_{DD}	Digital power supply (3 V)	—	D
18	DV_{DD}	Digital power supply (3 V)	—	D
19	PBLK	Preblanking input pin	I	D
20	OBP	Optical black pulse input pin	I	D
21	SPBLK	Black level sampling clock input pin	I	D
22	SPSIG	Signal level sampling clock input pin	I	D
23	NC	No connection pin	—	—
24	NC	No connection pin	—	—
25	AV_{SS}	Analog ground (0 V)	—	A
26	AV_{SS}	Analog ground (0 V)	—	A
27	AV_{DD}	Analog power supply (3 V)	—	A
28	BLKSH	Black level S/H pin	—	A
29	BLKFB	Black level FB pin	—	A
30	CDSIN	CDS input pin	I	A
31	BLKC	Black level C pin	—	A

Pin Description (cont.)

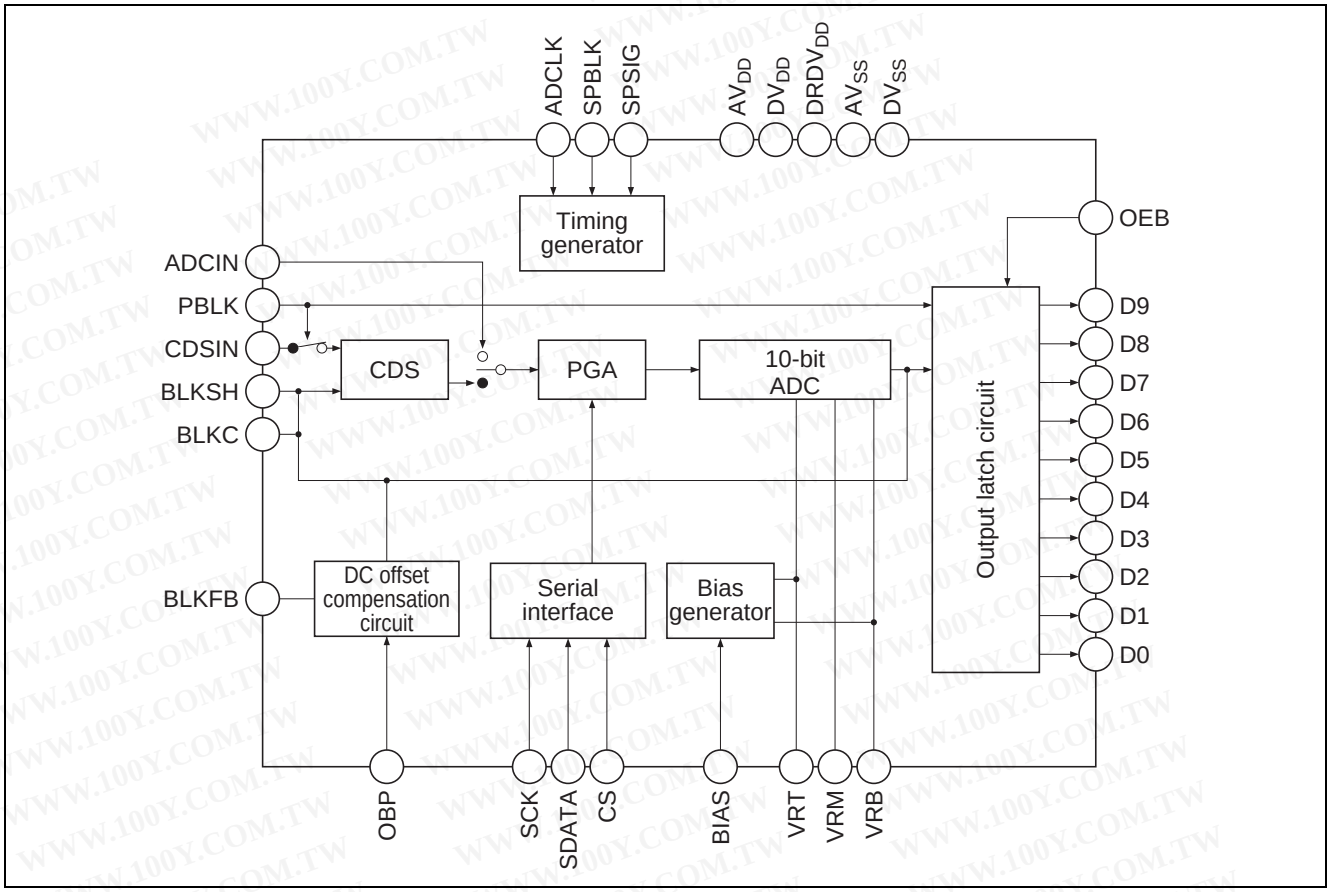
Pin No.	Symbol	Description	I/O	Analog(A) or Digital(D)
32	BIAS	Internal bias pin Connect a 33 kΩ resistor between BIAS and AV_{SS}.	—	A
33	AV_{DD}	Analog power supply (3 V)	—	A
34	NC	No connection pin	—	—
35	AV_{SS}	Analog ground (0 V)	—	A
36	ADCIN	ADC input pin	—	A
37	VRM	Reference voltage pin 1 Connect a 0.1 μF ceramic capacitor between VRM and AV_{SS}.	—	A
38	VRT	Reference voltage pin 3 Connect a 0.1 μF ceramic capacitor between VRT and AV_{SS}.	—	A
39	VRB	Reference voltage pin 2 Connect a 0.1 μF ceramic capacitor between VRB and AV_{SS}.	—	A
40	NC	No connection pin	—	—
41	DV_{SS}	Digital ground (0 V)	—	D
42	OEB *[1]	Digital output enable pin	—	D
43	DV_{DD}	Digital power supply (3 V)	—	D
44	DV_{DD}	Digital power supply (3 V)	—	D
45	DV_{SS}	Digital ground (0 V)	—	D
46	CS	Serial interface control input pin	I	D
47	SDATA	Serial data input pin	I	D
48	SCK	Serial clock input pin	I	D

Note: 1. With pull-down resistor.

Input/Output Equivalent Circuit

Pin Name		Equivalent Circuit
Digital output	D0 to D9	
Digital input	ADCLK, OBP, SPBLK, SPSIG, CS, SCK, SDATA, PBLK, OEB	 Note: Only OEB is pulled down to about 70 kΩ.
Analog	CDSIN	
	ADCIN	
	BLKSH, BLKFB, BLKC	
	VRT, VRM, VRB	
	BIAS	

Block Diagram



Internal Functions

Functional Description

- CDS input
  - — CCD low-frequency noise is suppressed by CDS (correlated double sampling).
  - — The signal level is clamped at 14 LSB to 76 LSB by resister during the OB period. *[1]
  - — Gain can be adjusted using 8 bits of register (0.132 dB steps) within the range from –2.36 dB to 31.40 dB. *[2]
- ADC input
  - — The center level of the input signal is clamped at 512 LSB (Typ).
  - — Gain can be adjusted using 8 bits of register (0.01784 times steps) within the range from 0.57 times (–4.86 dB) to 5.14 times (14.22 dB). *[1]
- Automatic offset calibration of PGA and ADC
- DC offset compensation feedback for CCD and CDS
- Pre-blanking
  - — CDS input operation is protected by separating it from the large input signal.
  - — Digital output is set at clamp level by resister.
- Digital output enable function

Notes: 1. It is not covered by warranty when 14LSB settings
2. Full-scale digital output is defined as 0 dB (one time) when 1 V is input.

Operating Description

Figure 1 shows CDS/PGA + ADC function block.

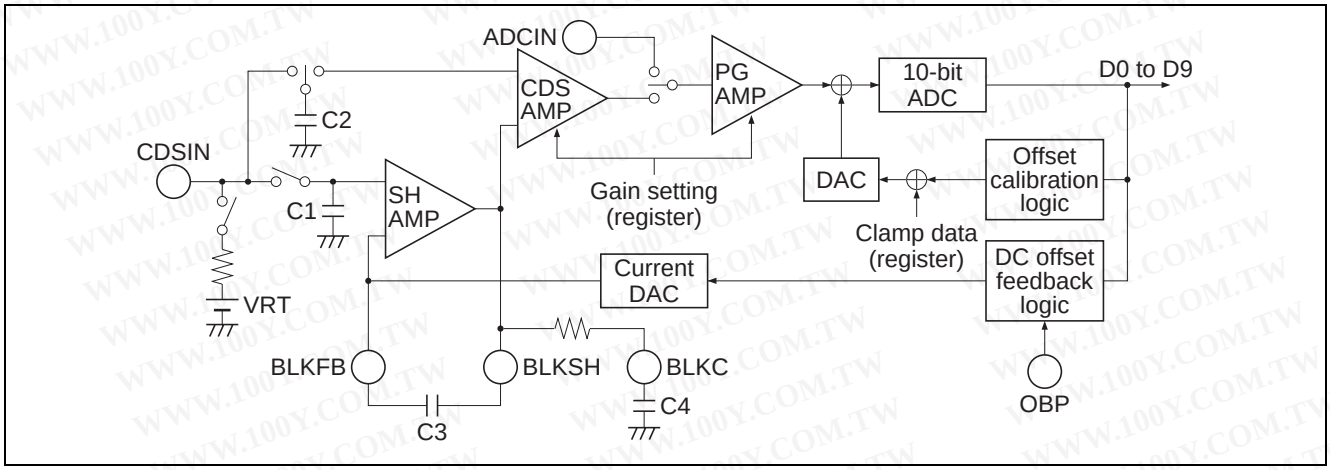


Figure 1 HD49334AF/AHF Functional Block Diagram

1. CDS (Correlated Double Sampling) Circuit
   The CDS circuit extracts the voltage differential between the black level and a signal including the black level. The black level is directly sampled at C1 by using the SPBLK pulse, buffered by the SHAMP, then provided to the CDSAMP.
   The signal level is directly sampled at C2 by using the SPSIG pulse, and provided to CDSAMP (see figure 1). The difference between these two signal levels is extracted by the CDSAMP, which also operates as a programmable gain amplifier at the previous stage. The CDS input is biased with VRT (2 V) during the SPBLK pulse validation period. During the PBLK period, the above sampling and bias operation are paused.

2. PGA Circuit

The PGAMP is the programmable gain amplifier for the latter stage. The PGAMP and the CDSAMP set the gain using 8 bits of register.

The equation below shows how the gain changes when register value N is from 0 to 255.

In CDSIN mode: Gain = (–2.36 dB + 0.132 dB) × N (LOG linear).

In ADCIN mode: Gain = (0.57 times + 0.00446 times) × N (linear).

Full-scale digital output is defined as 0 dB (one time) when 1 V is input.

3. Automatic Offset Calibration Function and Black-Level Clamp Data Setting

The DAC DC voltage added to the output of the PGAMP is adjusted by automatic offset calibration.

The data, which cancels the output offset of the PGAMP and the input offset of the ADC, and the clamp data (14 LSB to 76 LSB) set by register are added and input to the DAC.

The automatic offset calibration starts automatically after the RESET mode set by register 1 is cancelled and terminates after 40000 clock cycles (when fclk = 20 MHz, 2 ms).

4. DC Offset Compensation Feedback Function

Feedback is done to set the black signal level input during the OB period to the DC standard, and all offsets (including the CCD offset and the CDSAMP offset) are compensated for.

The offset from the ADC output is calculated during the OB period, and SHAMP feedback capacitor C3 is charged by the current DAC (see figure 1).

The open-loop differential gain (ΔGain/ΔH) per 1 H of the feedback loop is given by the following equation. 1H is the one cycle of the OBP.

$\Delta Gain/\Delta H = 0.078/(fclk \times C3)$ (fclk: ADCLK frequency, C3: SHAMP external feedback capacitor)

Example:When fclk = 20 MHz and C3 = 1.0 μF, ΔGain/ΔH = 0.0039

When the PGAMP gain setting is changed, the high-speed lead-in operation state is entered, and the feedback loop gain is increased by a multiple of N. Loop gain multiplication factor N can be selected from 4 times, 8 times, 16 times, or 32 times by changing the register settings (see table 1). Note that the open-loop differential gain (ΔGain/ΔH) must be one or lower. If it is two or more, oscillation occurs.

The time from the termination of high-speed lead-in operation to the return of normal loop gain operation can be selected from 1 H, 2 H, 4 H, or 8 H. If the offset error is over 32 LSB, the high-speed lead-in operation continues, and when the offset error is 32 LSB or less, the operation returns to the normal loop-gain operation after 1 H, 2 H, 4 H, or 8 H depending on the register settings. See table 2.

Table 1 Loop Gain Multiplication Factor during High-Speed Lead-In Operation

HGain-Nsel (register settings)		Multiplication Factor N
[0]	[1]	
L	L	4
H	L	8
L	H	16
H	H	32

Table 2 High-Speed Lead-In Operation Cancellation Time

HGstop-Hsel (register settings)		Cancellation Time
[0]	[1]	
L	L	1 H
H	L	2 H
L	H	4 H
H	H	8 H

5. Pre-Blanking Function

During the PBLK input period, the CDS input operation is separated and protected from the large input signal. The ADC digital output is fixed to clamp data (14 to 76 LSB).

6. ADC Digital Output Control Function

The ADC digital output includes the functions output enable, code conversion, and test mode. Tables 3, 4 and 5 show the output functions and the codes.

Table 3 ADC Digital Output Functions

STBY	OEB	TEST0	TEST1	LINV	MINV	PBLK	ADC Digital Output D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Operating Mode
H	X	X	X	X	X	X	Hi-Z										Low-power wait state
L	H	X	X	X	X	X	Hi-Z										Output Hi-Z
	L	L	L	L	L	H	Same as in table 4.										Normal operation
				L	H	H	D9 is inverted in table 4.										
				H	L	H	D8 to D0 are inverted in table 4.										
				H	H	H	D9 to D0 are inverted in table 4.										
				X	X	L	Output code is set up to Clamp Level.										Pre-blanking
			H	L	L	H	Same as in table 5.										Normal operation
				L	H	H	D9 is inverted in table 5.										
				H	L	H	D8 to D0 are inverted in table 5.										
				H	H	H	D9 to D0 are inverted in table 5.										
				X	X	L	Output code is set up to Clamp Level.										Pre-blanking
		H	X	L	L	X	H	L	H	L	H	L	H	L	H	L	Test mode
				L	H	X	L	L	H	L	H	L	H	L	H	L	
				H	L	X	H	H	L	H	L	H	L	H	L	H	
				H	H	X	L	H	L	H	L	H	L	H	L	H	

Notes: 1. STBY, TEST, LINV, and MINV are set by register.
2. Mode setting for the OEB and the PBLK are done by external input pins.
3. The polarity of the PBLK pin when the register setting is SPinv is low.

Table 4 ADC Output Code

Output Pin			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Output codes	Steps	3	L	L	L	L	L	L	L	L	H	H
		4	L	L	L	L	L	L	L	H	L	L
		5	L	L	L	L	L	L	L	H	L	H
		6	L	L	L	L	L	L	L	H	H	L
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		511	L	H	H	H	H	H	H	H	H	H
		512	H	L	L	L	L	L	L	L	L	L
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		1020	H	H	H	H	H	H	H	H	L	L
		1021	H	H	H	H	H	H	H	H	L	H
		1022	H	H	H	H	H	H	H	H	H	L
		1023	H	H	H	H	H	H	H	H	H	H

Table 5 ADC Output Code (TEST1)

Output Pin			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Output codes	Steps	3	L	L	L	L	L	L	L	L	H	L
		4	L	L	L	L	L	L	L	H	H	L
		5	L	L	L	L	L	L	L	H	H	H
		6	L	L	L	L	L	L	L	H	L	H
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		511	L	H	L	L	L	L	L	L	L	L
		512	H	H	L	L	L	L	L	L	L	L
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		1020	H	L	L	L	L	L	L	L	H	L
		1021	H	L	L	L	L	L	L	L	H	H
		1022	H	L	L	L	L	L	L	L	L	H
		1023	H	L	L	L	L	L	L	L	L	L

7. Adjustment of Black-Level S/H Response Frequency Characteristics
   The CR time constant that is used for sampling/hold (S/H) at the black level can be adjusted by changing the register settings, as shown in table 6.

Table 6 SHSW CR Time Constant Setting

	SHSW-fsel (Register setting)																															
	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]
	L	L	L	L	H	L	L	L	L	H	L	L	H	H	L	L	L	L	H	L	H	L	H	L	L	H	H	L	H	H	H	L
CR Time Constant (Typ) (cutoff frequency conversion)	2.20 nsec (72 MHz)				2.30 nsec (69 MHz)				2.51 nsec (63 MHz)				2.64 nsec (60 MHz)				2.93 nsec (54 MHz)				3.11 nsec (51 MHz)				3.52 nsec (45 MHz)				3.77 nsec (42 MHz)			

	SHSW-fsel (Register setting)																															
	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]	[0]	[1]	[2]	[3]
	L	L	L	H	H	L	L	H	L	H	L	H	H	H	L	H	L	L	H	H	H	L	H	H	L	H	H	H	H	H	H	H
CR Time Constant (Typ) (cutoff frequency conversion)	4.40 nsec (36 MHz)				4.80 nsec (33 MHz)				5.87 nsec (27 MHz)				6.60 nsec (24 MHz)				8.80 nsec (18 MHz)				10.6 nsec (15 MHz)				17.6 nsec (9 MHz)				26.4 nsec (6 MHz)			

8. The SHAMP frequency characteristics can be adjusted by changing the register settings and the C4 value of the external 31st pin.
   The settings are shown in table 7.
   Values other than those shown in the table 7 cannot be used.

Table 7 SHAMP Frequency Characteristics Setting

LoPwr (Register setting)	SHA-fsel (Register setting)					
	[0]	[1]	[0]	[1]	[0]	[1]
	H	L	L	H	H	H
"Lo"	116 MHz 10000 pF (270 pF)		75 MHz 13000 pF (300 pF)		56 MHz 18000 pF (360 pF)	
"Hi"	49 MHz 15000 pF (620 pF)		32 MHz 22000 pF (750 pF)		24 MHz 27000 pF (820 pF)	

Note: Upper line : SHAMP cutoff frequency (Typ)
Middle line : Standard value of C4 (maximum value is not defined)
Lower line : Minimum value of C4 (do not set below this value)

Timing Chart

Figure 2 shows the timing chart when CDSIN and ADCIN input modes are used.

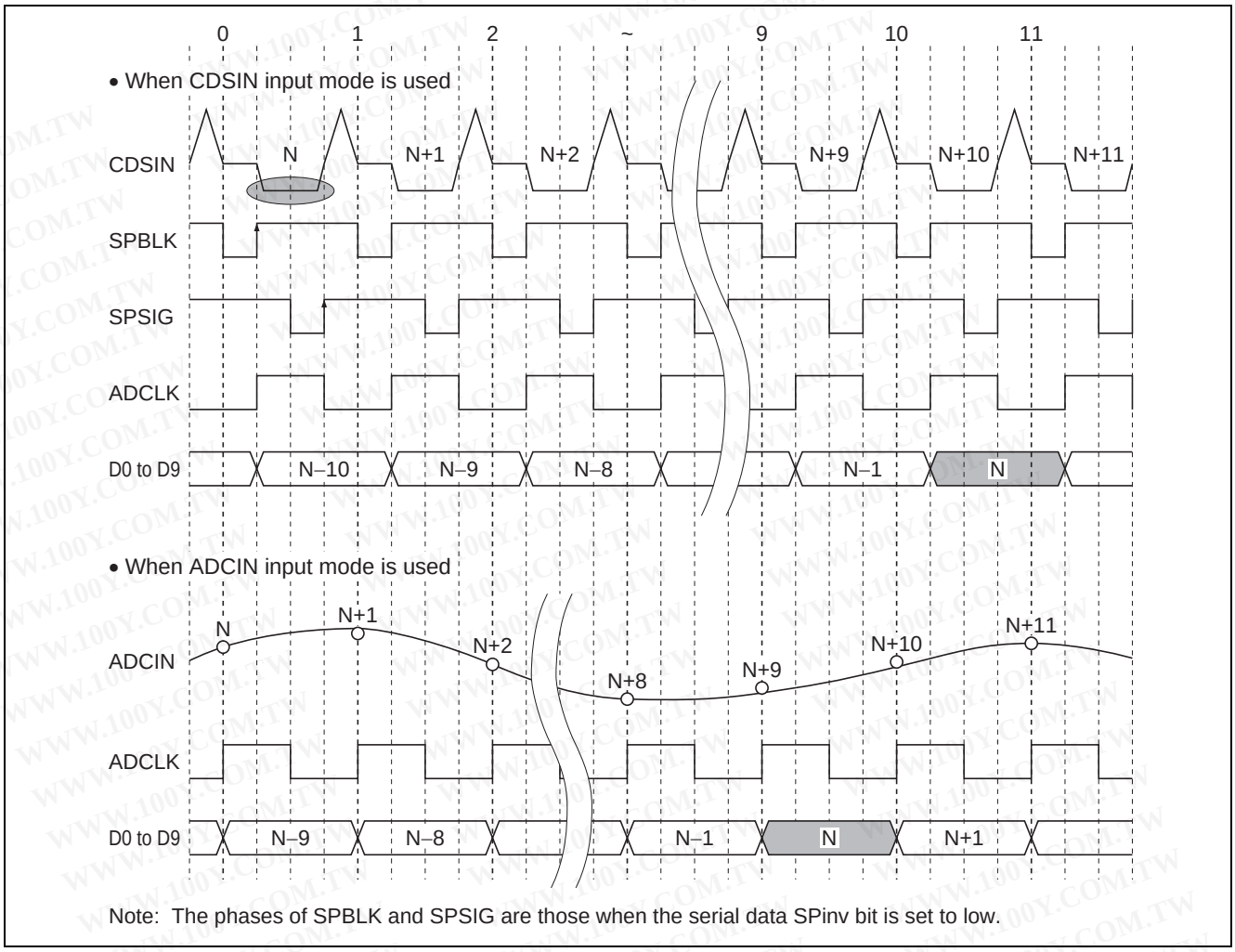


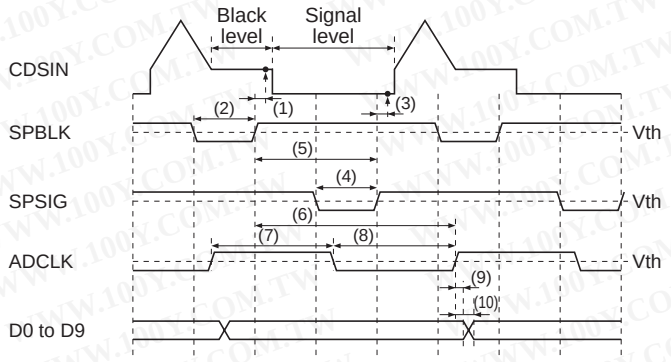
Figure 2 Output Timing Chart when CDSIN and ADCIN Input Modes are Used

- The ADC output (D0 to D9) is output at the rising edge of the ADCLK in both modes.
- Pipe-line delay is ten clock cycles when CDSIN is used and nine when ADCIN is used.
- In ADCIN input mode, the input signal is sampled at the rising edge of the ADCLK.

Detailed Timing Specifications

Detailed Timing Specifications when CDSIN Input Mode is Used

Figure 3 shows the detailed timing specifications when the CDSIN input mode is used, and table 8 shows each timing specification.



Note: 1. When serial data Spinv bit is set to low. (When the Spinv bit is set to high, the polarities of the SPBLK and the SPSIG are inverted.)

Figure 3 Detailed Timing Chart when CDSIN Input Mode is Used

Table 8 Timing Specifications when the CDSIN Input Mode is Used

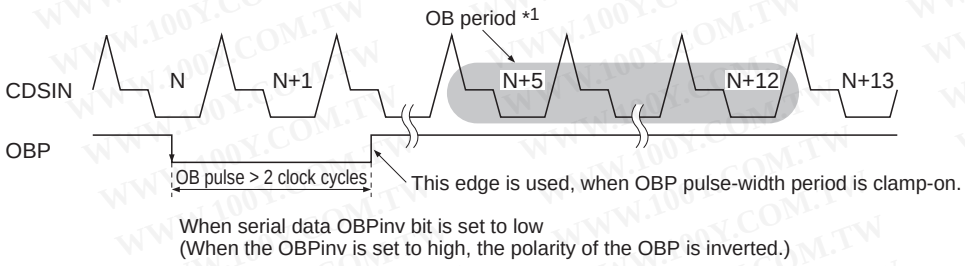
No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Black-level signal fetch time	t_{CDS1}	—	(1.5)	—	ns
(2)	SPBLK low period *1	t_{CDS2}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns
(3)	Signal-level fetch time	t_{CDS3}	—	(1.5)	—	ns
(4)	SPSIG low period *1	t_{CDS4}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns
(5)	SPBLK rising to SPSIG rising time *1	t_{CDS5}	Typ × 0.85	$1/2f_{CLK}$	Typ × 1.15	ns
(6)	SPBLK rising to ADCLK rising inhibition time *1	t_{CDS6}	1	5	11	ns
(7), (8)	ADCLK t_{WH} min./t_{WL} min.	$t_{CDS7, 8}$	11	—	—	ns
(9)	ADCLK rising to digital output hold time	t_{CHLD9}	3	7	—	ns
(10)	ADCLK rising to digital output delay time	t_{COD10}	—	16	24	ns

Note: 1. SPBLK and SPSIG polarities when serial data Spinv bit is set to low.

OBP Detailed Timing Specifications

Figure 4 shows the OBP detailed timing specifications.

The OB period is from the fifth to the twelfth clock cycle after the OB pulse is input. The average of the black signal level is taken for eight input cycles during the OB period and becomes the clamp level (DC standard).



Note: 1. Shifts ±1 clock cycle depending on the OBP input timing.

Figure 4 OBP Detailed Timing Specifications

Detailed Timing Specifications at Pre-Blanking

Figure 5 shows the pre-blanking detailed timing specifications.

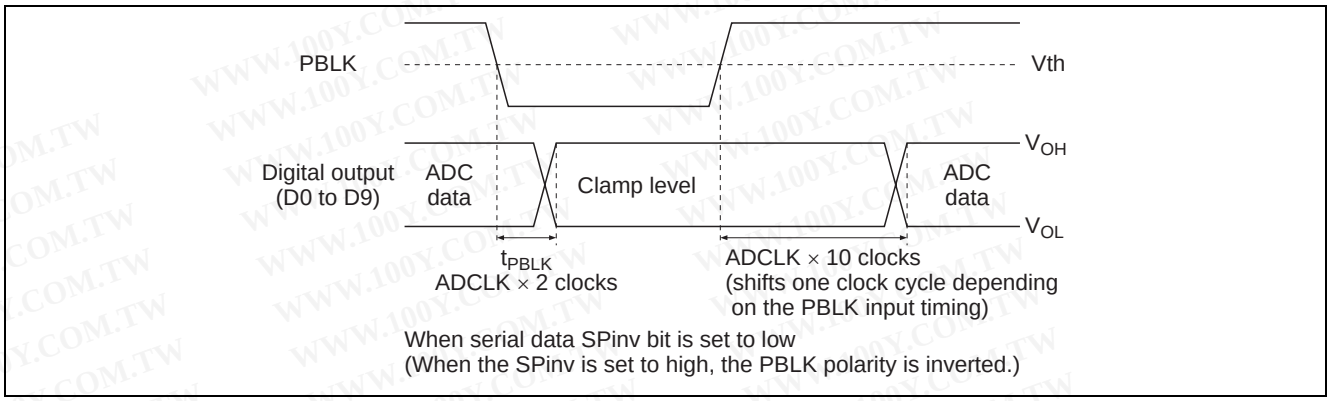


Figure 5 Detailed Timing Specifications at Pre-Blanking

Detailed Timing Specifications when ADCIN Input Mode is Used

Figure 6 shows the detailed timing chart when ADCIN input mode is used, and table 9 shows each timing specification.

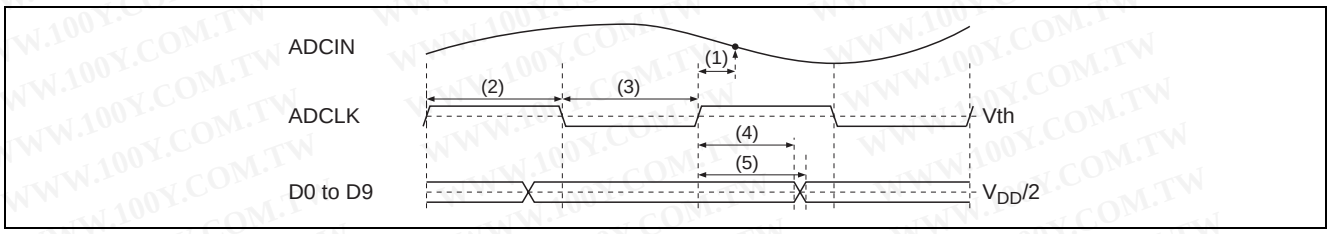


Figure 6 Detailed Timing Chart when ADCIN Input Mode is Used

Table 9 Timing Specifications when ADCIN Input Mode is Used

No.	Timing	Symbol	Min	Typ	Max	Unit
(1)	Signal fetch time	t_{ADC1}	—	(6)	—	ns
(2), (3)	ADCLK t_{WH} min./t_{WL} min.	$t_{ADC2, 3}$	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns
(4)	ADCLK rising to digital output hold time	t_{AHLD4}	10	14.5	—	ns
(5)	ADCLK rising to digital output delay time	t_{AOD5}	—	23.5	31.5	ns

Detailed Timing Specifications for Digital Output-Enable Control

Figure 7 shows the detailed timing specifications for digital output enable control. When the OEB pin is set to high, output disable mode is entered, and the output state becomes High-Z.

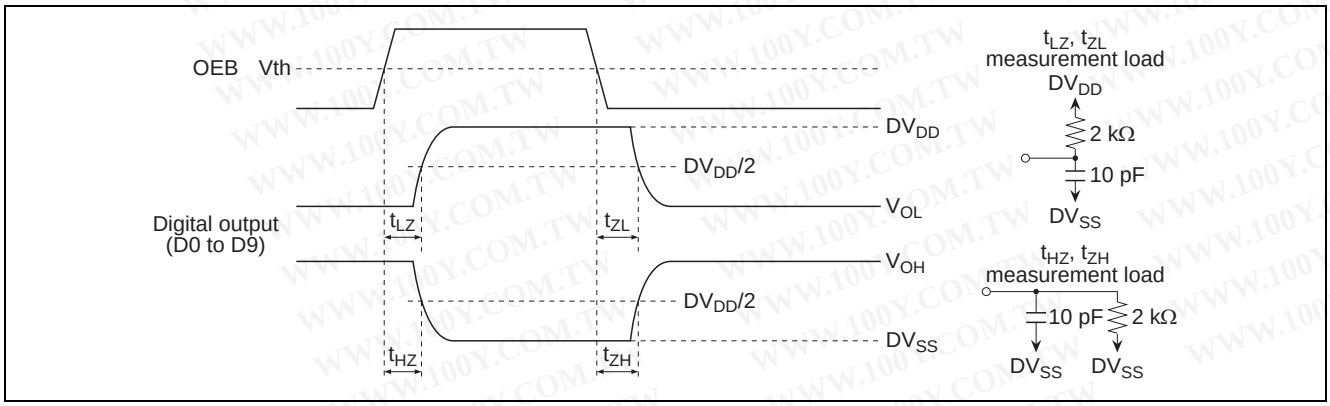


Figure 7 Detailed Timing Specifications for Digital Output Enable Control

Serial Interface Specifications

Table 10 Serial Data Function List

	Resister 0	Resister 1	Resister 2	Resister 3	Resister 4 to 7 Test Mode (can not be used)
DI 00 (LSB)	Low	High	Low	High	Low to High
DI 01	Low	Low	High	High	Low to High
DI 02	Low	Low	Low	Low	High
DI 03	Cannot be used. All low	SLP Low: Normal operation mode High: Sleep mode	Clamp-level [0] (LSB)	C-Bias off	Cannot be used.
DI 04		STBY Low: Normal operation mode High: Standby mode	Clamp-level [1]	Gray code [0] (TEST1)	
DI 05	PGA gain setting (LSB)	Output mode setting (LINV)	Clamp-level [2]	Gray code [1]	
DI 06	PGA gain setting	Output mode setting (MINV)	Clamp-level [3]	Ave_4H	
DI 07	PGA gain setting	Output mode setting (TEST0)	Clamp-level [4] (MSB)	Gray_test [0]	
DI 08	PGA gain setting	SHA-fsel [0] (LSB) (SHAMP frequency characteristics switching)	HGstop-Hsel [0] (High-speed lead-in cancellation time)	Gray_test [1]	
DI 09	PGA gain setting	SHA-fsel [1] (MSB)	HGstop-Hsel [1]	Gray_test [2]	
DI 10	PGA gain setting	SHSW-fsel [0] (LSB) (SHSW frequency characteristics switching)	HGain-Nsel [0] (High-speed lead-in gain multiplication)	0 (Cannot be used.)	
DI 11	PGA gain setting	SHSW-fsel [1]	HGain-Nsel [1]	0	
DI 12	PGA gain setting (MSB)	SHSW-fsel [2]	Low_PWR	1	
DI 13	Cannot be used. All low	SHSW-fsel [3] (MSB)	SPinv, SPSIG/SPBLK/PBLK inversion	0	
DI 14		Cannot be used. All low	OBPinv, OBP inversion	0	
DI 15 (MSB)	CSEL Low: CDSIN input mode High: ADCIN input mode		RESET Low: Reset mode High: Normal operation mode	1	

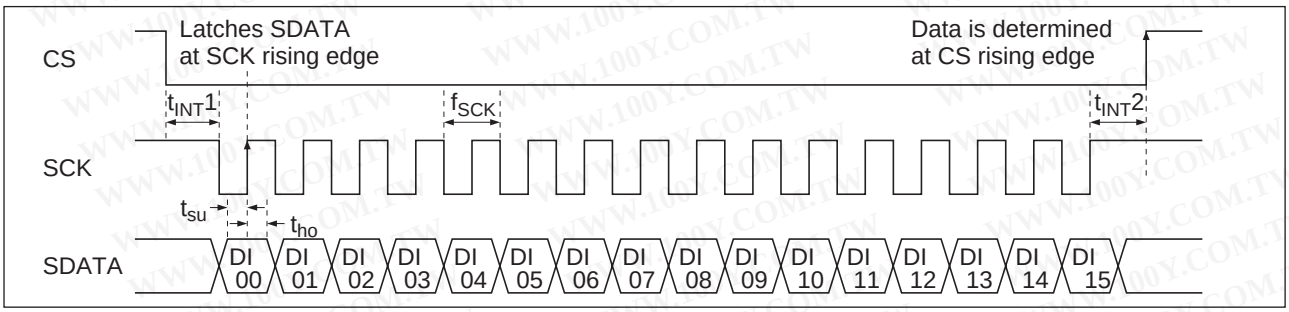


Figure 8 Serial Interface Timing Specifications

Notes: 1. 2 byte continuous communications.
2. SDATA is latched at SCK rising edge.
3. Insert 16 clocks of SCK while CS is low.
4. Data is invalid if data transmission is aborted during transmission.
5. The gain conversion table differs in the CDSIN input mode and the ADCIN input mode.
6. STBY: Reference voltage generator circuit is in the operating state.
SLP: All circuits are in the sleep state.
7. This bit is used for the IC testing, and cannot be used by the user.
The use of this address is prohibited.
8. Circuit current and the frequency characteristic are switched.
Data = 0: 36 MHz guarantee
Data = 1: 25 MHz guarantee

Timing Specifications

	Min	Max
f_{SCK}	—	5 MHz
$t_{INT}1$, 2	50 ns	—
t_{su}	50 ns	—
t_{ho}	50 ns	—

Explanation of Serial Data of CDS Part

Serial data of CDS part has the following functions.

- PGA gain (D5 to D12 of register 0)
  Details are referred to page 5 block diagram.
  At CDS_in mode: –2.36 dB + 0.132 dB × N (Log linear)
  At ADC_in mode: 0.57 times + 0.01784 times × N (Times linear)
  ∗: Full-scale digital output is defined as 0 dB when 1 V is input.
  Above PGA gain definition means input signal 1 Vp-p to CDS_in, and set N = 18 (correspond 2.36 dB), and then PGA outputs the 2 V full-range, and also ADC out puts the full code (1023).
  This mean offset gain of PGA has 6 dB – 2.36 dB = 3.64 dB, therefore it should be decided that how much dB add on.

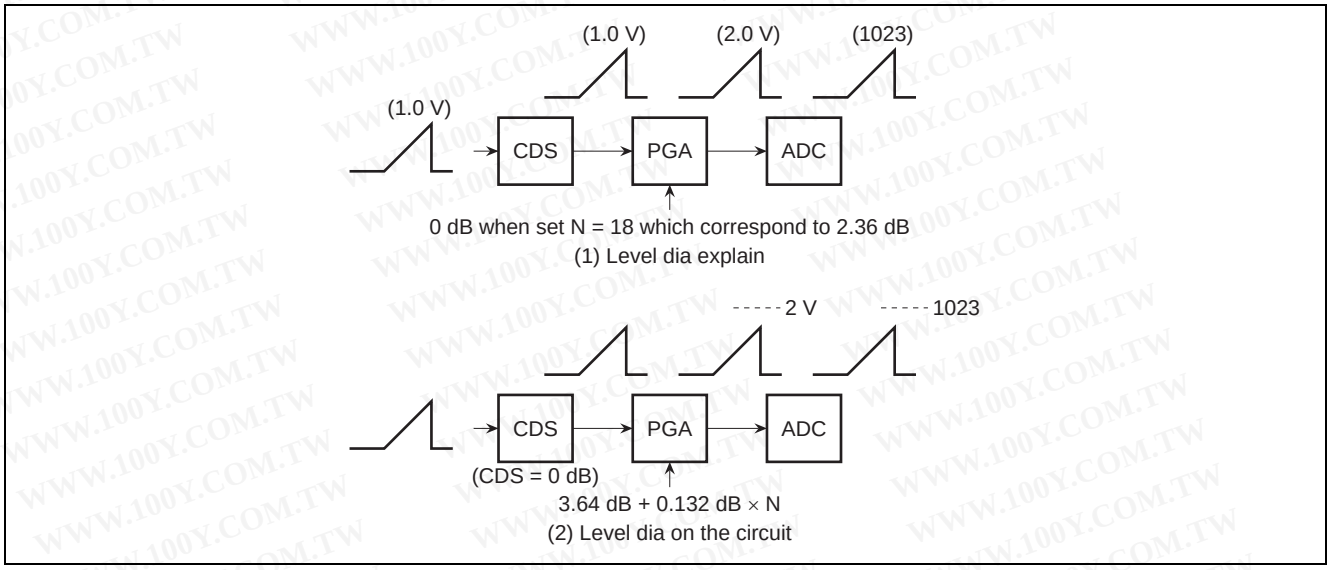


Figure 9 Level Dia of PGA

- CSEL (D15 of register 0)
  Data = 0: Select CDSIN
  Data = 1: Select ADCIN

Address								STD1[7:0] (L)								STD2[15:8] (H)							
1	1	1	1	0	0	0	1				D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
											test0	MINV	LINV	STBY	SLP	test_I2		SHSW_fsel				SHA_fsel	

- SLP and STBY (D3, D4 of register 1)
  SLP: Stop the all circuit. Consumption current of CDS part is less than 10 µA.
  Start up from offset calibration when recover is needed.
  STBY: Only the standard voltage generating circuit is operated. Consumption current of CDS part is about 3 mA.
  Allow 50 H time for feedback clamp is stabilized until recover.
- Output mode (D5 to D7 of register 1 and D4 of register 3)
  It is a test mode. Combination details are table 3 to 5. Normally set to all 0.
- SHA-fsel (D8 to D9 of register 1)
  It is a LPF switching of SH amplifier. Frequency characteristics are referred to page 9. To get rough idea, set the double cut off frequency point with using.
- SHSW-fsel (D10 to D13 of register 1)
  It is a time constant which sampling the black level of SH amplifier. Frequency characteristics are referred to page 9. To get rough idea, set the double cut off frequency point with using. S/N changes by this data, so find the appropriate point with set data to up/down.

- Clamp (D3 to D7 of register 2)
  Determine the OB part level with digital code of ADC output.
  Clamp level = setting data × 2 + 14
  Default data is 9 = 32 LSB.
- HGstop-Hsel, HGain-Nsel (D8 to D11 of register 2)
  Determine the lead-in speed of OB clamp. Details are referred to page 7. PGA gain need to be changed for switch the high speed leading mode. Transfer the gain +1/–1 to previous field, its switch to high speed leading mode.
- Low_PWR (D12 of register 2)
  Switch circuit current and frequency characteristic.
  Data = 0: 36 MHz guarantee
  Data = 1: 25 MHz guarantee
- SPinv (D13 of register 2)
  SPSIG/SPBLK/PBLK input signal inverted switching.
  Data = 1: Normal
  Data = 0: Inverted
- Reset (D15 of register 2)
  Software reset.
  Data = 1: Normal
  Data = 0: Reset
  Offset calibration should be done when starting up with using this bit. Details are referred to page 19.
- C_Bias_off (D3 of register 3)
  Center bias is turned off in ADCIN mode.
  Data = 0: Normally on
  Data = 1: Off
- Ave_4H (D6 of register 3)
  Clamp detection data is averaged 4H.
  Data = 0: 1H
  Data = 1: Averaged 4H

Differential Code and Gray Code (D4 to D5 and D7 to D9 of register 3)

- Gray code (D4 to D5 of register 3)
  DC output code can be change to following type.

Gray Code [1]	Gray Code [0]	Output Code
0	0	Binary code
0	1	Gray code
1	0	Differential encoded binary
1	1	Differential encoded gray

- Serial data setting items (D7 to D9 of register 3)

Setting Bit	Setting Contents
Gray_test[0]	Standard data output timing control signal (Refer to the following table)
Gray_test[1]	
Gray_test[2]	ADCLK polar with OBP. (Lo→Positive edge, HI→Negative edge)

  - Standard data output timing

Gray_test[1]	Gray_test[0]	Standard Data Output Timing
Low	Low	Third and fourth
Low	High	Fourth and fifth
High	Low	Fifth and sixth
High	High	Sixth and seventh

Ripple (pseudo outline made by quantized error) occurres on the point which swithing the ADC output multiple bit in parallel. When switching the several of ADC output at the same time, ripple (pseudo outline caused by miss quantization) occurs to the image.
Differential code and gray code are recommended for this countermeasure.
Figure 10 indicates circuit block. When luminance signal changes are smoothly, the number of bit of switching digital output bit can be reduced and easily to reduce the ripple using this function.
This function is especially effective for longer the settings of sensor more than clk = 30 kHz, and ADC output.
Figure 11 indicates the timing specifications.

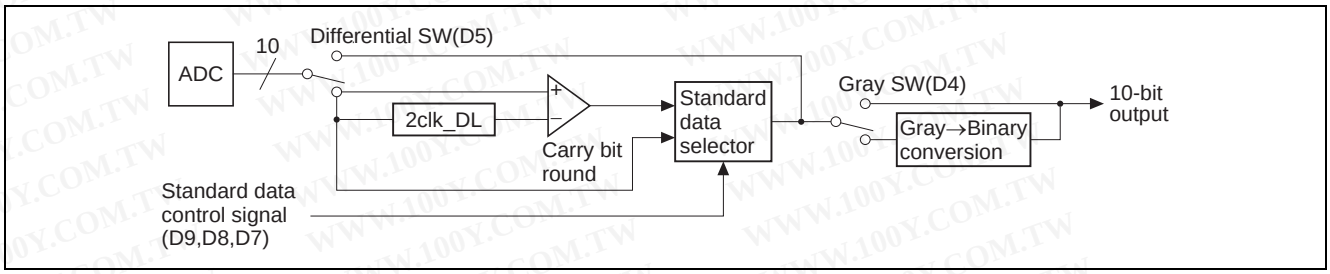


Figure 10 Differential Code, Gray Code Circuit

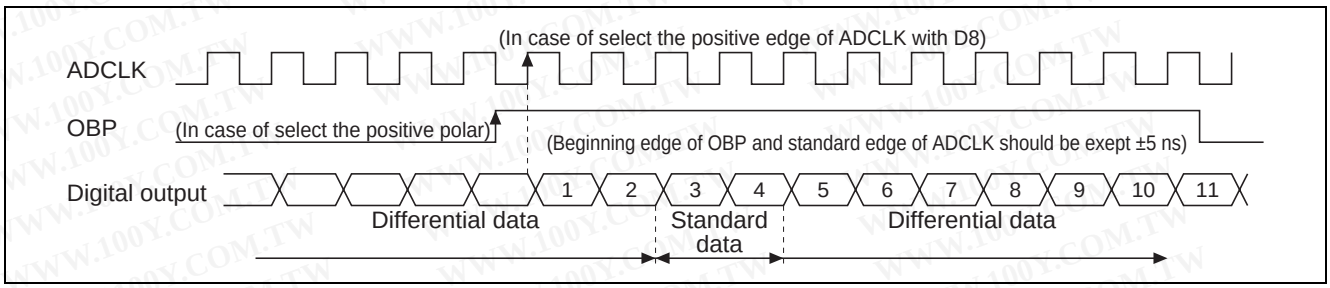


Figure 11 Differential Code Timing Specifications

To use differential code, complex circuit is necessary at DSP side.

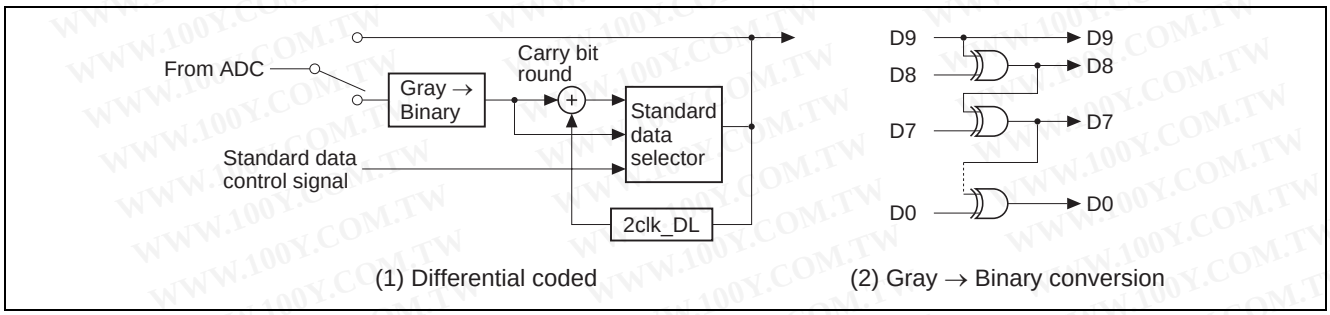


Figure 12 Complex Circuit Example

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Power supply voltage	V_{DD}(max)	4.1	V
Analog input voltage	V_{IN}(max)	–0.3 to AV_{DD} +0.3	V
Digital input voltage	V_I(max)	–0.3 to DV_{DD} +0.3	V
Operating temperature	Topr	–10 to +75	°C
Power dissipation	Pt(max)	400	mW
Storage temperature	Tstg	–55 to +125	°C
Power supply voltage range	Vopr	2.7 to 3.3	V

Notes: 1. V_{DD} indicates AV_{DD} and DV_{DD}.
2. AV_{DD} and DV_{DD} must be commonly connected outside the IC. When they are separated by a noise filter, the potential difference must be 0.3 V or less at power on, and 0.1 V or less during operation.

Electrical Characteristics

(Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, and R_{BIAS} = 33 kΩ)

- Items Common to CDSIN and ADCIN Input Modes

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Power supply voltage range	V_{DD}	2.7	3.0	3.3	V		
Conversion frequency	f_{CLK} hi	20	—	36	MHz	LoPwr = low	HD49334AHF
	f_{CLK} low	5.5	—	25	MHz	LoPwr = high	HD49334AF
Digital input voltage	V_{IH}	$2.0 \times \frac{DV_{DD}}{3.0}$	—	DV_{DD}	V		Digital input pins other than CS, SCK and SDATA
	V_{IL}	0	—	$0.8 \times \frac{DV_{DD}}{3.0}$	V		
	V_{IH2}	$2.25 \times \frac{DV_{DD}}{3.0}$	—	DV_{DD}	V		CS, SCK, SDATA
	V_{IL2}	0	—	$0.6 \times \frac{DV_{DD}}{3.0}$	V		
Digital output voltage	V_{OH}	DV_{DD} –0.5	—	—	V	I_{OH} = –1 mA	
	V_{OL}	—	—	0.5	V	I_{OL} = +1 mA	
Digital input current	I_{IH}	—	—	50	µA	V_{IH} = 3.0 V	
	I_{IH2}	—	—	250	µA	V_{IH} = 3.0 V	
	I_{IL}	–50	—	—	µA	V_{IL} = 0 V	
Digital output current	I_{OZH}	—	—	50	µA	V_{OH} = V_{DD}	
	I_{OZL}	–50	—	—	µA	V_{OL} = 0 V	
ADC resolution	RES	10	10	10	bit		
ADC integral linearity	INL	—	(3)	—	LSBp-p	f_{CLK} = 25 MHz	
ADC differential linearity+	DNL+	—	0.3	0.9	LSB	f_{CLK} = 25 MHz	*1
ADC differential linearity–	DNL–	–0.9	–0.3	—	LSB	f_{CLK} = 25 MHz	*1
Sleep current	I_{SLP}	–100	0	100	µA	Digital input pin is set to 0 V, output pin is open	
Standby current	I_{STBY}	—	3	5	mA	Digital I/O pin is set to 0 V	
Digital output Hi-Z delay time	t_{HZ}	—	—	100	ns	R_L = 2 kΩ, C_L = 10 pF	See figure 7
	t_{LZ}	—	—	100	ns		
	t_{ZH}	—	—	100	ns		
	t_{ZL}	—	—	100	ns		

Notes: 1. Differential linearity is the calculated difference in linearity errors between adjacent codes.
2. Values within parentheses ( ) are for reference.

Electrical Characteristics (cont.)

(Unless othewide specified, Ta = 25°C, AV_{DD} = 3.0 V, DV_{DD} = 3.0 V, and R_{BIAS} = 33 kΩ)

- Items for CDSIN Input Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current (1)	I_{DD1}	—	45.0	54.5	mA	f_{CLK} = 36 MHz	CDSIN mode LoPwr = low
Consumption current (2)	I_{DD2}	—	23.5	31.0	mA	f_{CLK} = 25 MHz	CDSIN mode LoPwr = high
CCD offset tolerance range	V_{CCD}	(–100)	—	(100)	mV		
Timing specifications (1)	t_{CDS1}	—	(1.5)	—	ns		See table 8
Timing specifications (2)	t_{CDS2}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns		
Timing specifications (3)	t_{CDS3}	—	(1.5)	—	ns		
Timing specifications (4)	t_{CDS4}	Typ × 0.8	$1/4f_{CLK}$	Typ × 1.2	ns		
Timing specifications (5)	t_{CDS5}	Typ × 0.85	$1/2f_{CLK}$	Typ × 1.15	ns		
Timing specifications (6)	t_{CDS6}	1	5	9	ns		
Timing specifications (7)	t_{CDS7}	11	—	—	ns		
Timing specifications (8)	t_{CDS8}	11	—	—	ns		
Timing specifications (9)	t_{CHLD9}	3	7	—	ns	C_L = 10 pF	
Timing specifications (10)	t_{COD10}	—	16	24	ns		
Clamp level	CLP(00)	—	(14)	—	LSB		
	CLP(09)	—	(32)	—	LSB		
	CLP(31)	—	(76)	—	LSB		
PGA gain at CDS input	PGA(0)	–4.4	–2.4	–0.4	dB		
	PGA(63)	4.1	6.1	8.1	dB		
	PGA(127)	12.5	14.5	16.5	dB		
	PGA(191)	21.0	23.0	25.0	dB		
	PGA(255)	29.3	31.3	33.3	dB		

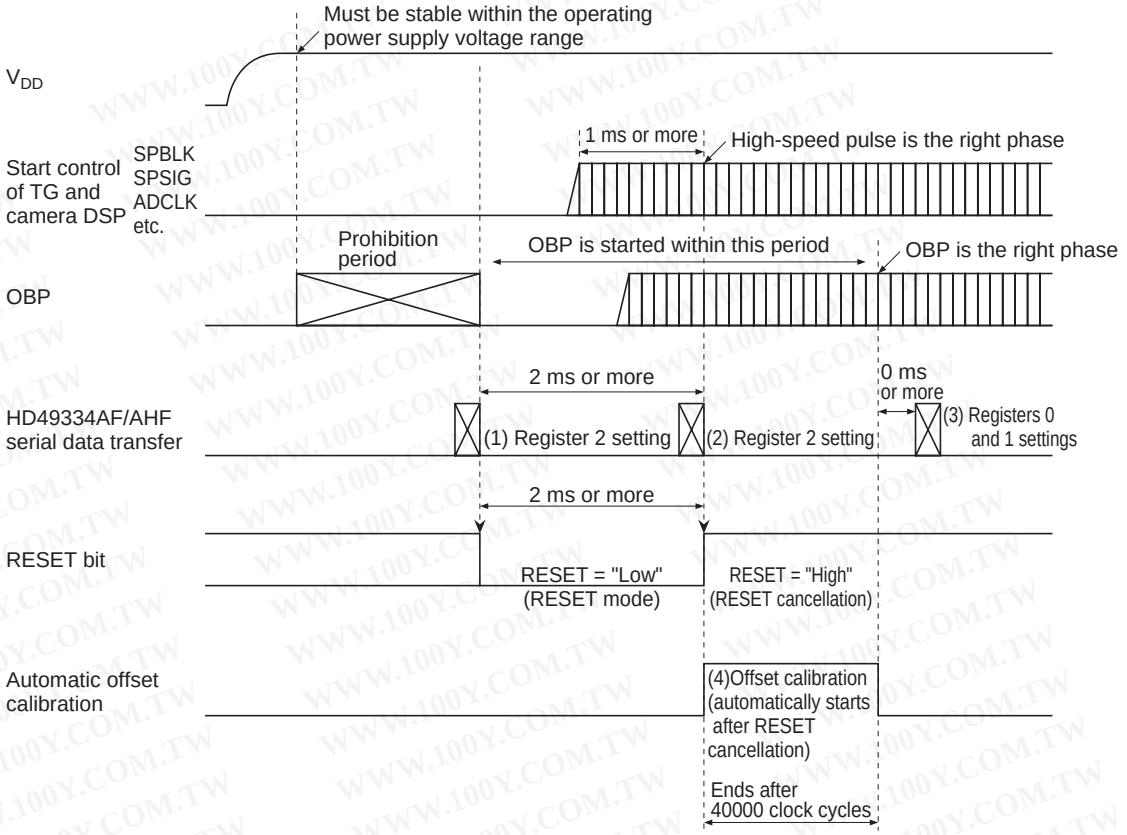
Note : Values within parentheses ( ) are for reference.

- Items for ADCIN Input Mode

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Remarks
Consumption current (3)	I_{DD3}	—	30.0	38.0	mA	f_{CLK} = 36 MHz	ADCIN mode LoPwr = low
Consumption current (4)	I_{DD4}	—	17.0	21.5	mA	f_{CLK} = 25 MHz	ADCIN mode LoPwr = high
Timing specifications (11)	t_{ADC1}	—	(6)	—	ns		See table 9
Timing specifications (12)	t_{ADC2}	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns		
Timing specifications (13)	t_{ADC3}	Typ × 0.85	$1/2f_{ADCLK}$	Typ × 1.15	ns		
Timing specifications (14)	t_{AHLD4}	10	14.5	—	ns	C_L = 10 pF	
Timing specifications (15)	t_{AOD5}	—	23.5	31.5	ns		
Input current at ADC input	IIN_{CIN}	–110	—	110	µA	V_{IN} = 1.0 V to 2.0 V	
Clamp level at ADC input	OF2	—	(512)	—	LSB		
PGA gain at ADC input	GSL(0)	0.45	0.57	0.72	Times		
	GSL(63)	1.36	1.71	2.16	Times		
	GSL(127)	2.26	2.85	3.59	Times		
	GSL(191)	3.18	4.00	5.04	Times		
	GSL(255)	4.06	5.12	6.45	Times		

Note : Values within parentheses ( ) are for reference.

Operation Sequence at Power On

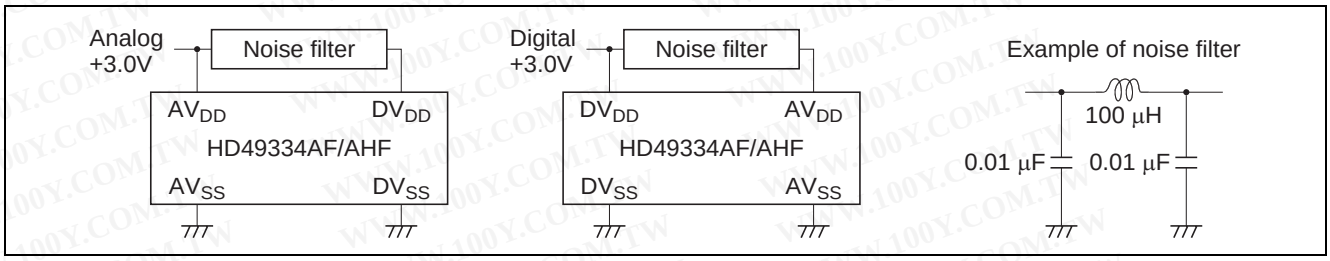


The following describes the above serial data transfer. For details on registers 0, 1, and 2, refer to table 10.

(1) Register 2 setting : Set all bits in register 2 to the usage condition, and set the RESET bit to low.
(2) Register 2 setting : Cancel the RESET mode by setting the register 2 RESET bit to high.
Do not change other register 2 settings. Offset calibration starts automatically.
(3) Register 0 and 1 settings : After the offset calibration is terminated, set registers 0 and 1.
(4) Please perform an offset calibration in the period which avoided PBLK of V.

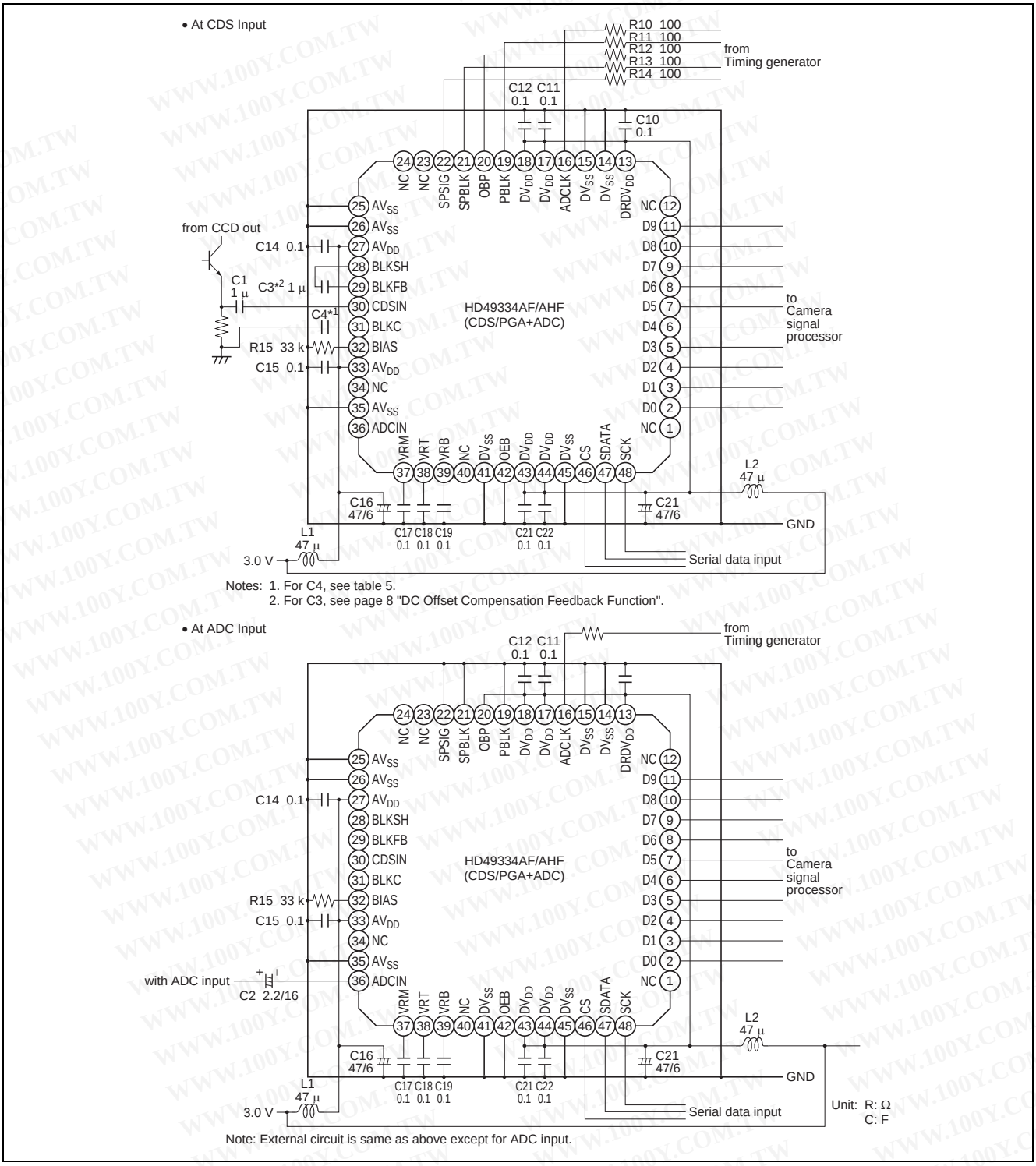
Notice for Use

1. Careful handling is necessary to prevent damage due to static electricity.
2. This product has been developed for consumer applications, and should not be used in non-consumer applications.
3. As this IC is sensitive to power line noise, the ground impedance should be kept as small as possible. Also, to prevent latchup, a ceramic capacitor of 0.1 µF or more and an electrolytic capacitor of 10 µF or more should be inserted between the ground and power supply.
4. Common connection of AV_{DD} and DV_{DD} should be made off-chip. If AV_{DD} and DV_{DD} are isolated by a noise filter, the phase difference should be 0.3 V or less at power-on and 0.1 V or less during operation.
5. If a noise filter is necessary, make a common connection after passage through the filter, as shown in the figure below.



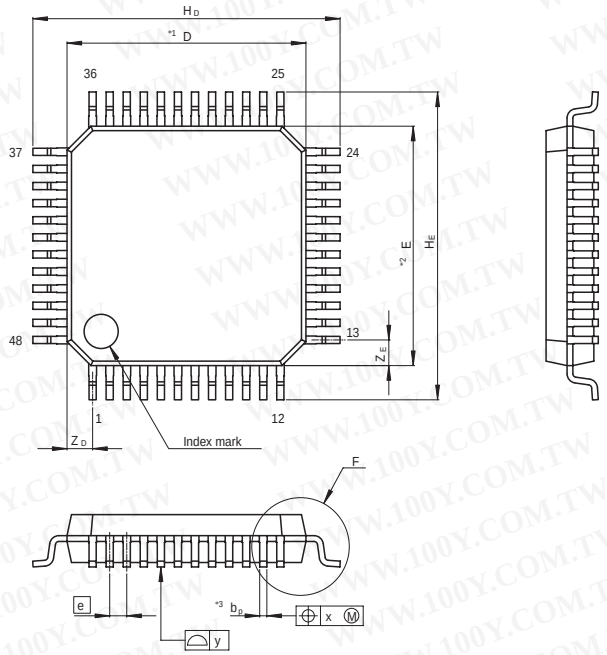
6. Connect AV_{SS} and DV_{SS} off-chip using a common ground. If there are separate analog system and digital system set grounds, connect to the analog system.
7. When V_{DD} is specified in the data sheet, this indicates AV_{DD} and DV_{DD}.
8. No Connection (NC) pins are not connected inside the IC, but it is recommended that they be connected to power supply or ground pins or left open to prevent crosstalk in adjacent analog pins.
9. To ensure low thermal resistance of the package, a Cu-type lead material is used. As this material is less tolerant of bending than Fe-type lead material, careful handling is necessary.
10. The infrared reflow soldering method should be used to mount the chip. Note that general heating methods such as solder dipping cannot be used.
11. Serial communication should not be performed during the effective video period, since this will result in degraded picture quality. Also, use of dedicated ports is recommended for the SCK and SDATA signals used in the HD49330AF. If ports are to be shared with another IC, picture quality should first be thoroughly checked.
12. At power-on, automatic adjustment of the offset voltage generated from PGA, ADC, etc., must be implemented in accordance with the power-on operating sequence (see page 19).

Example of Recommended External Circuit

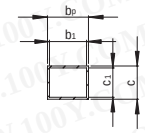


Package Dimensions

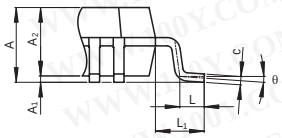
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KD-A	FP-48C/FP-48CV	0.2g



NOTE)
1. DIMENSIONS"*1"AND"*2" DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	7.0	——
E	——	7.0	——
A_2	——	1.40	——
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	——	——	1.70
A_1	0.08	0.13	0.22
b_p	0.16	0.21	0.26
b_1	——	0.19	——
c	0.12	0.17	0.22
c_1	——	0.15	——
θ	0°	——	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.10
Z_D	——	0.75	——
Z_E	——	0.75	——
L	0.40	0.50	0.60
L_1	——	1.00	——