

# HSMP-386J

## High Power RF PIN Diode



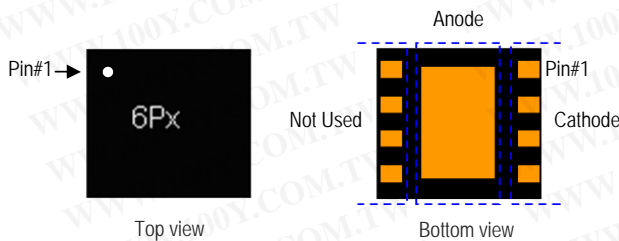
### Data Sheet

#### Description

Avago Technologies' HSMP-386J is a High Power RF PIN Diode specifically design for high power handling and low distortion Transmit/Receive switching application. It is housed in QFN 2x2mm size package which is having good thermal resistance.

The unique with 8 dies in parallel configuration results to low IL performance and low series resistance. The HSMP-386J Power diode is built with match diode to ensure consistency in performance.

#### Package Marking & Orientation



Notes:  
 6P = Device Code  
 x = Month code indicates the month of manufacture

#### Features

- High Power Surface Mount Package QFN 2x2
- Match Diode for Consistent Performance
- Low Bias Current Requirement
- Low Series Resistance
- Low Insertion Loss & High Isolation
- Better Thermal Conductivity for Higher Power Dissipation
- Low Failure in Time (FIT) Rate
- Lead-free Option Available
- MSL1 & Lead Free
- Tape & Reel Option Available

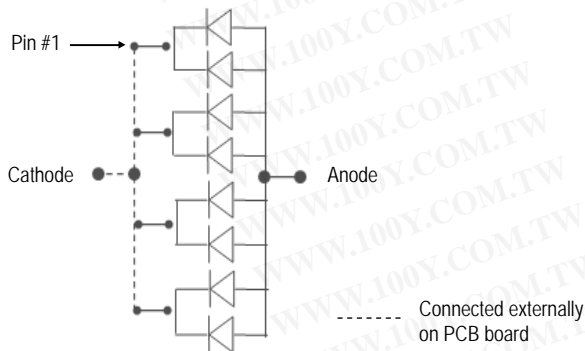
#### Specifications

- Low RS Switching typically  $0.65\Omega$  @ 100MHz, 50mA
- High Power Handling Up to 10W (40dBm) at 2GHz, 50mA

#### Application

- High Power Transmit / Receive Switch for Cellular Infrastructure and Two Way Radio

#### Circuit Diagram of HSMP-386J



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 勝特力电子(上海) 86-21-34970699  
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**Table 1. Absolute Maximum Ratings [1] at T<sub>C</sub> = +25°C**

Symbol	Parameter	Unit	Max Rating
I <sub>F</sub>	Forward Current (1μs Pulse) per die [2]	Amp	1
P <sub>IV</sub>	Peak Inverse Voltage	V	100
T <sub>j</sub>	Junction Temperature	°C	150
T <sub>stg</sub>	Storage Temperature	°C	-60 to 150
θ <sub>jc</sub>	Thermal Resistance [3]	°C/W	45
DC P <sub>diss</sub>	DC Power Dissipation [4]	W	2.0

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. Eight dice are connected in parallel for this device.
3. T<sub>C</sub> = +25°C, where T<sub>C</sub> is defined to be the temperature at the package pins where contact is made to the circuit board.
4. Maximum DC P<sub>diss</sub> measured without RF input and maximum rating is base on device junction temperature.

$$P_{diss} = \frac{T(\text{Max.Operating}) - 25^{\circ}\text{C}}{\text{Thermal Resistance}}$$

**Table 2. Electrical Performance at T<sub>C</sub> = +25°C**

	Minimum Breakdown Voltage V <sub>BR</sub> (V)	Typical Forward Voltage V <sub>f</sub> (V)	Maximum Series Resistance R <sub>S</sub> (Ohm)	Maximum Total Capacitance C <sub>T</sub> (pF)
	100	0.85	0.77	1.25
<b>Test Conditions</b>	V <sub>R</sub> = V <sub>BR</sub> Measure I <sub>R</sub> ≤ 5uA	I <sub>F</sub> = 50mA	I <sub>F</sub> = 50 mA f = 100 MHz	V <sub>R</sub> = 50V f = 1MHz

**Table 3. Typical Performance at T<sub>C</sub> = +25°C**

	Series Resistance R <sub>S</sub> (Ω)	Carrier Lifetime (nS)	Reverse Recovery Time T <sub>rr</sub> (nS)	Total Capacitance C <sub>T</sub> (pF)
	0.65	260	130	0.75
<b>Test Conditions</b>	I <sub>F</sub> = 50mA f = 100MHz	I <sub>F</sub> = 50mA I <sub>R</sub> = 100mA	V <sub>R</sub> = 5V I <sub>F</sub> = 50mA 90% Recovery	V <sub>R</sub> = 50V f = 1MHz

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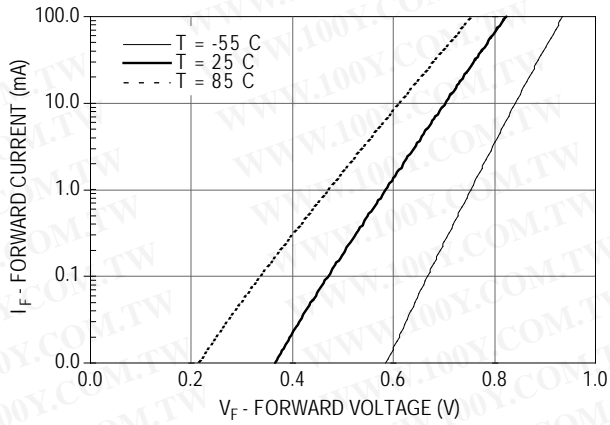


Figure 1. Forward Current vs. Forward Voltage

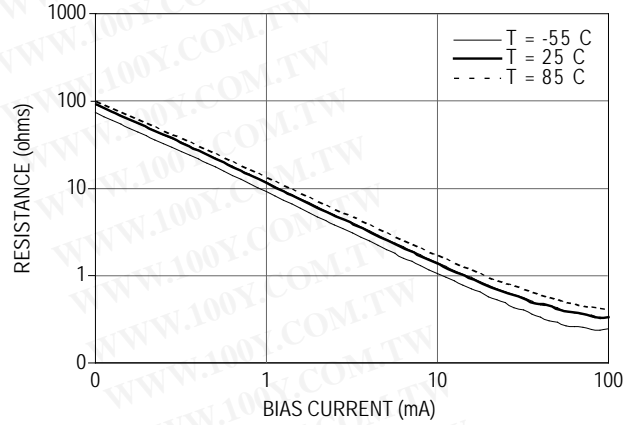


Figure 2. Typical RF Resistance vs. Forward Bias Current.

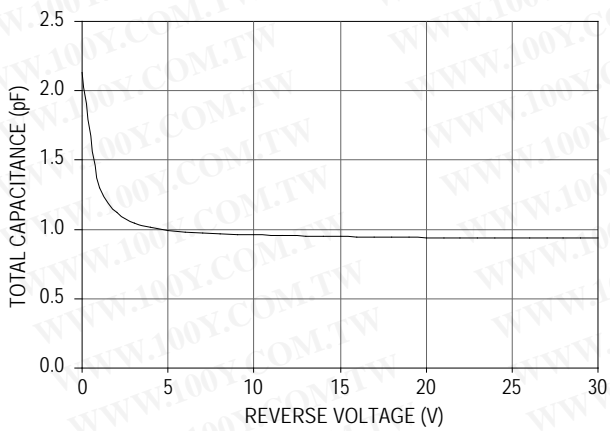


Figure 3. RF Capacitance vs. Reverse Bias Voltage

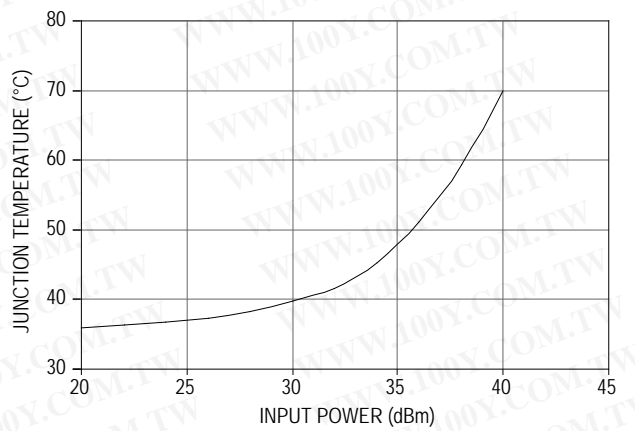


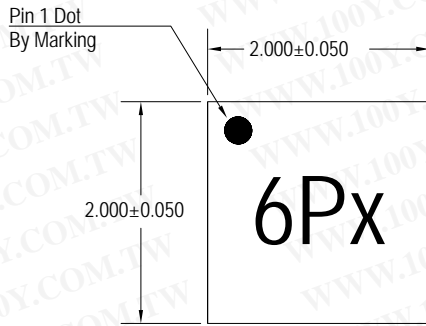
Figure 4. Input Power vs. Junction Temperature [1]

Notes:

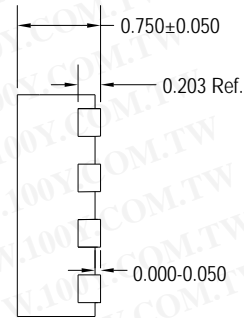
1. Test conditions:  $f = 2.1\text{GHz}$ ,  $I_F = 50\text{mA}$
2. Typical values were derived using limited samples during initial product characterization and may not be representative of the overall distribution.

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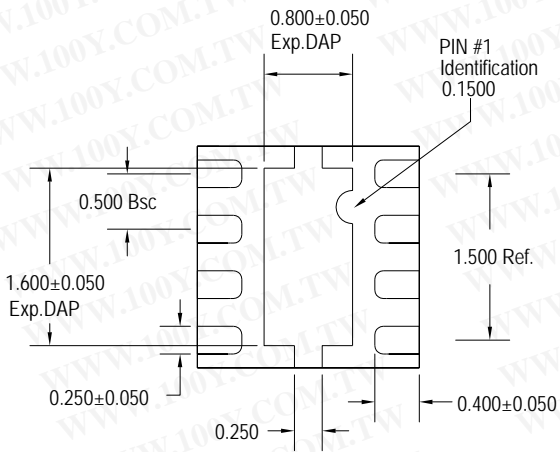
## QFN 2x2 Package Dimension



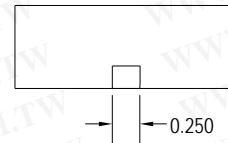
Top View



Side View



Bottom View



Top View

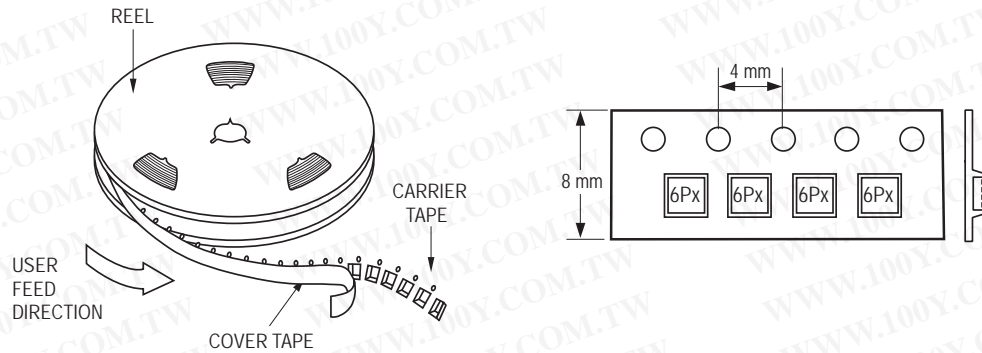
### Note:

1. All dimensions in millimeters.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash and metal burr.

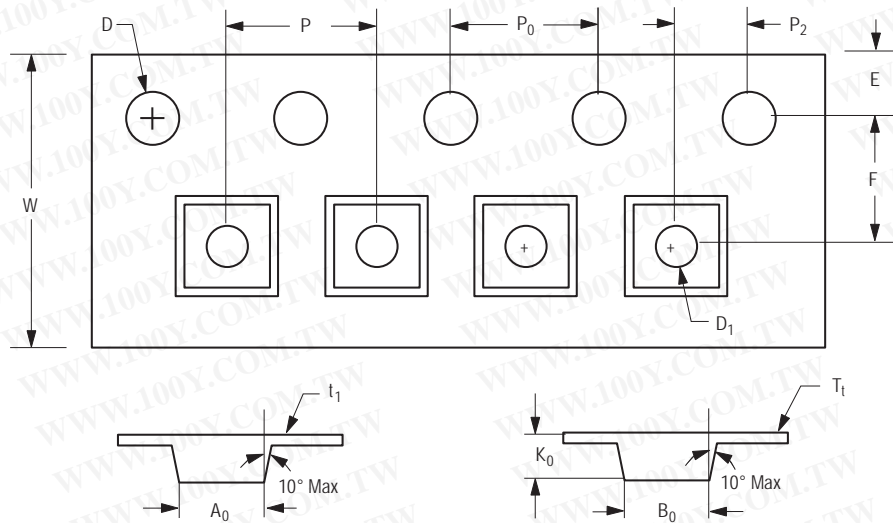
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## Device Orientation



## Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (inches)
CAVITY	LENGTH	$A_0$	$2.30 \pm 0.05$	$0.091 \pm 0.004$
	WIDTH	$B_0$	$2.30 \pm 0.05$	$0.091 \pm 0.004$
	DEPTH	$K_0$	$1.00 \pm 0.05$	$0.039 \pm 0.002$
	PITCH	$P$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	BOTTOM HOLE DIAMETER	$D_1$	$1.00 + 0.25$	$0.039 + 0.002$
PERFORATION	DIAMETER	$D$	$1.50 \pm 0.10$	$0.060 \pm 0.004$
	PITCH	$P_0$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	POSITION	$E$	$1.75 \pm 0.10$	$0.069 \pm 0.004$
CARRIER TAPE	WIDTH	$W$	$8.00 + 0.30$	$0.315 \pm 0.012$
	THICKNESS	$t_1$	$8.00 \pm 0.10$ $0.254 \pm 0.02$	$0.315 \pm 0.004$ $0.010 \pm 0.0008$
COVER TAPE	WIDTH	$C$	$5.4 \pm 0.10$	$0.205 \pm 0.004$
	TAPE THICKNESS	$T_1$	$0.062 \pm 0.001$	$0.0025 \pm 0.0004$
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	$F$	$3.50 \pm 0.05$	$0.138 \pm 0.002$
	CAVITY TO PERFORATION (LENGTH DIRECTION)	$P_2$	$2.00 \pm 0.05$	$0.079 \pm 0.002$

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