

# DATA SHEET

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-54151736  
勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

## 74HC00; 74HCT00 Quad 2-input NAND gate

Product specification  
Supersedes data of 1997 Aug 26

2003 Jun 30

## Quad 2-input NAND gate

## 74HC00; 74HCT00

## FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

## DESCRIPTION

The 74HC00/74HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC00/74HCT00 provide the 2-input NAND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f = 6$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC00	74HCT00	
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 15$ pF; $V_{CC} = 5$ V	7	10	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	22	22	pF

## Notes

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

- For 74HC00 the condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

For 74HCT00 the condition is  $V_I = \text{GND}$  to  $V_{CC} - 1.5$  V.

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## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

## Note

- H = HIGH voltage level;  
L = LOW voltage level.

## Quad 2-input NAND gate

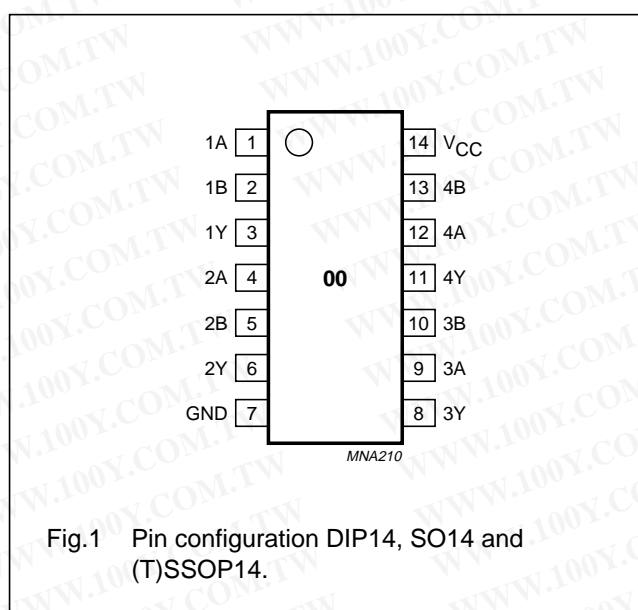
74HC00; 74HCT00

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC00N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT00N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC00D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT00D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HC00DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT00DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC00PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT00PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC00BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT00BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

## PINNING

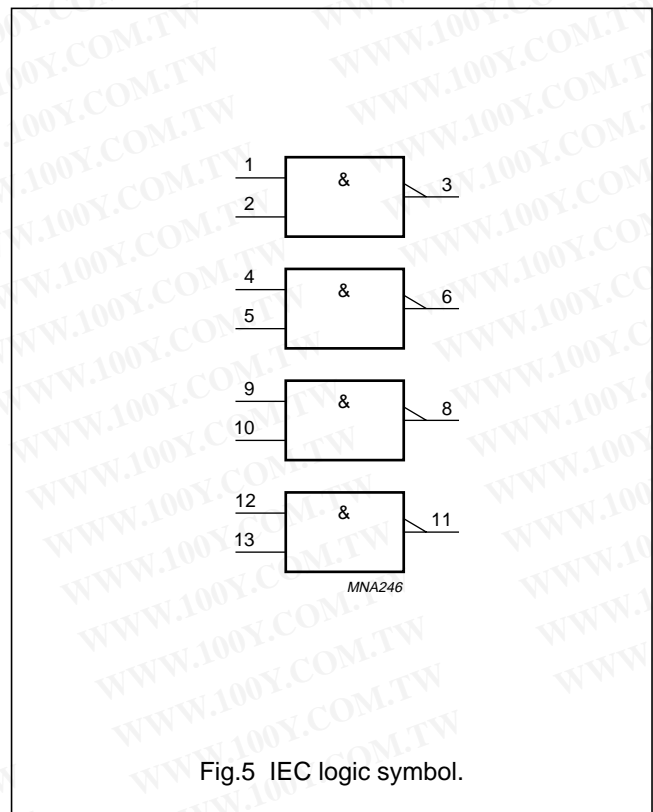
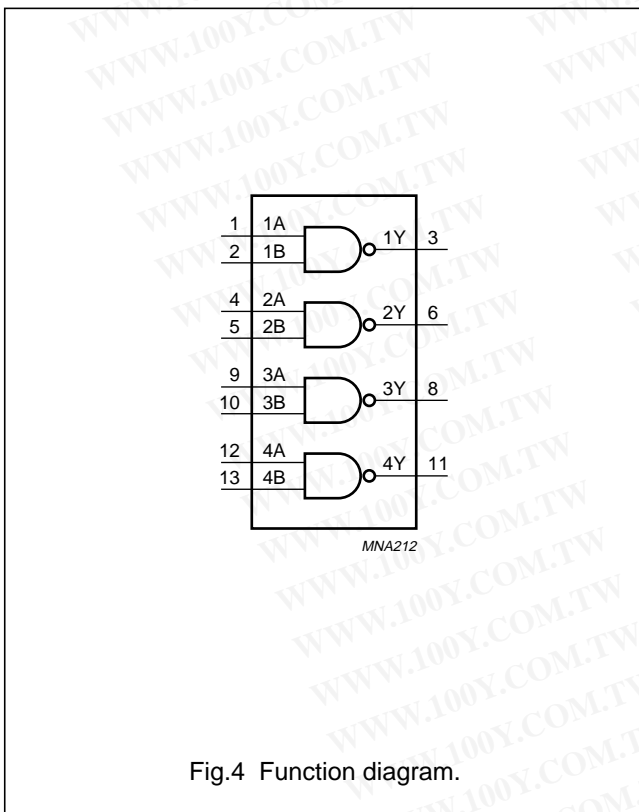
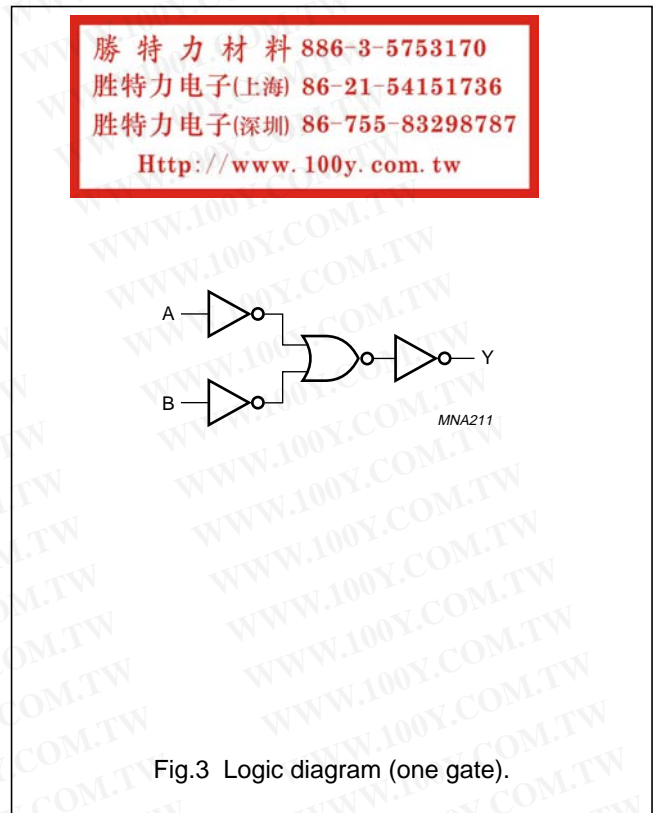
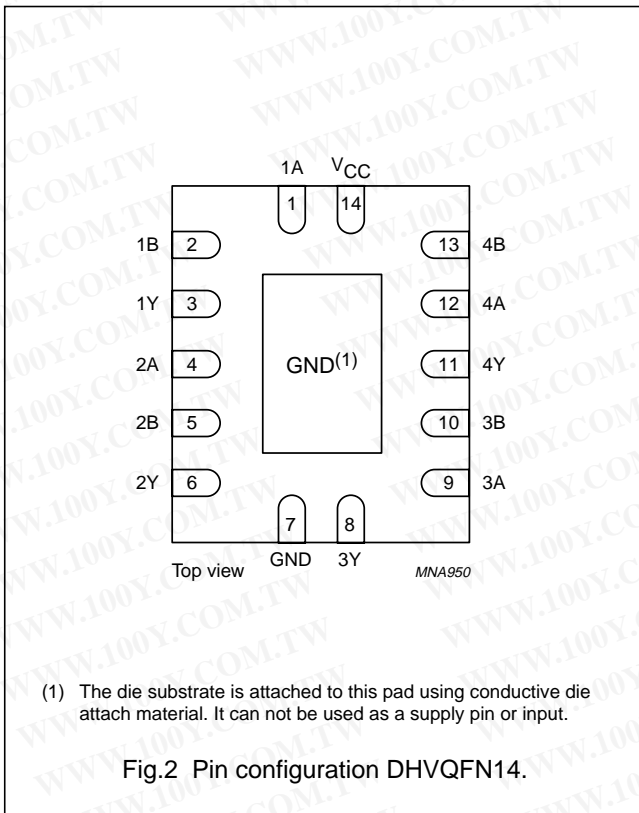
PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V <sub>CC</sub>	supply voltage



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# Quad 2-input NAND gate

# 74HC00; 74HCT00



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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC00			74HCT00			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_O$	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	–	±25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		–	±50	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40\text{ to }+125\text{ °C}$ ; note 1	–	500	mW

## Note

- For DIP14 packages: above 70 °C derate linearly with 12 mW/K.  
For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

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## Quad 2-input NAND gate

## 74HC00; 74HCT00

## DC CHARACTERISTICS

## Type 74HC00

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
T <sub>amb</sub> = -40 to +85 °C; note 1							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	2.0	1.9	2.0	–	V
		I <sub>O</sub> = -20 μA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = -20 μA	6.0	5.9	6.0	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.84	4.32	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.34	5.81	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	2.0	–	0	0.1	V
		I <sub>O</sub> = 20 μA	4.5	–	0	0.1	V
		I <sub>O</sub> = 20 μA	6.0	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.33	V
		I <sub>O</sub> = 5.2 mA	6.0	–	0.16	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	μA
I <sub>oz</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	6.0	–	–	±5.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	20	μA

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## 74HC00; 74HCT00

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	2.0	1.9	–	–	V
		I <sub>O</sub> = -20 μA	4.5	4.4	–	–	V
		I <sub>O</sub> = -20 μA	6.0	5.9	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.2	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	2.0	–	–	0.1	V
		I <sub>O</sub> = 20 μA	4.5	–	–	0.1	V
		I <sub>O</sub> = 20 μA	6.0	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
		I <sub>O</sub> = 5.2 mA	6.0	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	μA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	6.0	–	–	±10.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	40	μA

**Note**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

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## Quad 2-input NAND gate

## 74HC00; 74HCT00

## Type 74HCT00

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.84	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	4.5	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	μA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	±5.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	20	μA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	–	150	675	μA
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 μA	4.5	4.4	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	μA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	40	μA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	–	–	735	μA

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

## Quad 2-input NAND gate

## 74HC00; 74HCT00

### AC CHARACTERISTICS

#### Type 74HC00

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Fig.6	2.0	–	25	115	ns
		see Fig.6	4.5	–	9	23	ns
		see Fig.6	6.0	–	7	20	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time		2.0	–	19	95	ns
			4.5	–	7	19	ns
			6.0	–	6	16	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Fig.6	2.0	–	–	135	ns
		see Fig.6	4.5	–	–	27	ns
		see Fig.6	6.0	–	–	23	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time		2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns

#### Note

- All typical values are measured at T<sub>amb</sub> = 25 °C.

#### Type 74HCT00

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Fig.6	4.5	–	12	24	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time		4.5	–	–	29	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Fig.6	4.5	–	–	29	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time		4.5	–	–	22	ns

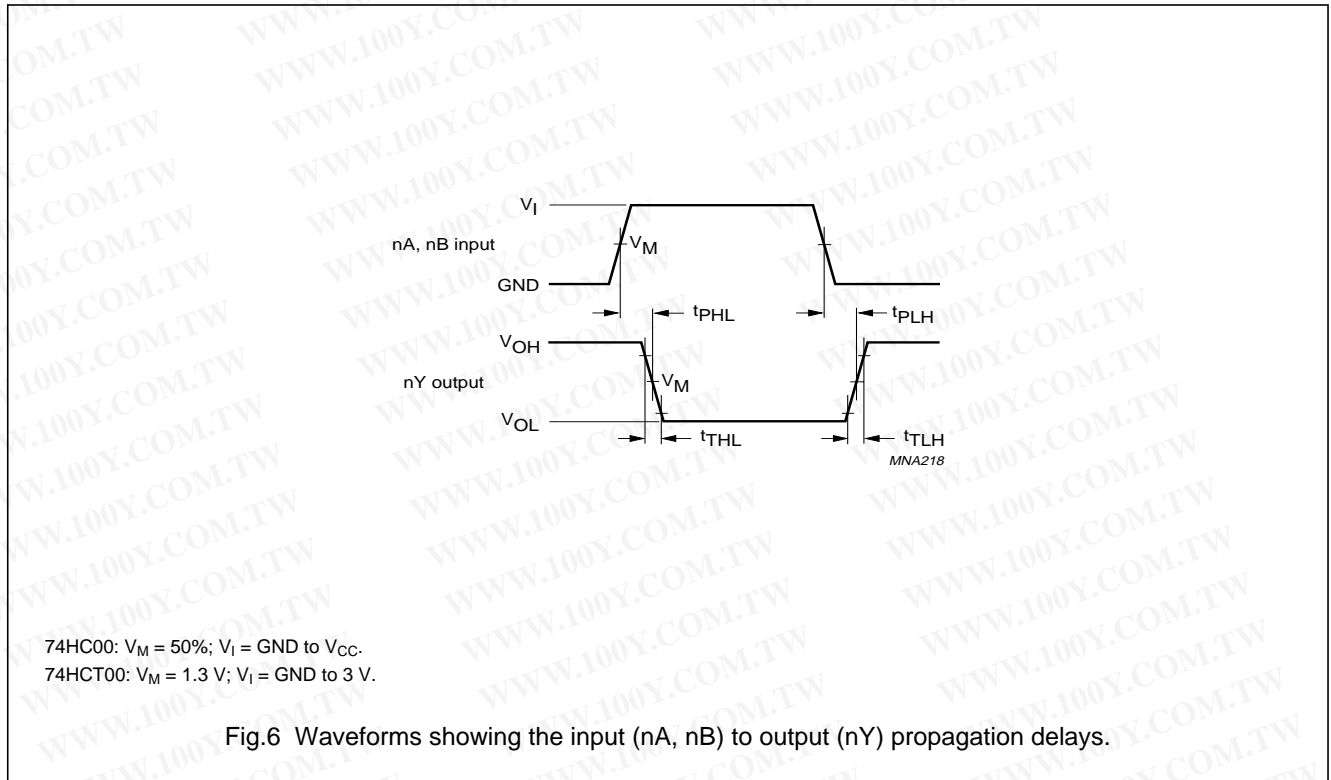
#### Note

- All typical values are measured at T<sub>amb</sub> = 25 °C.

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## AC WAVEFORMS



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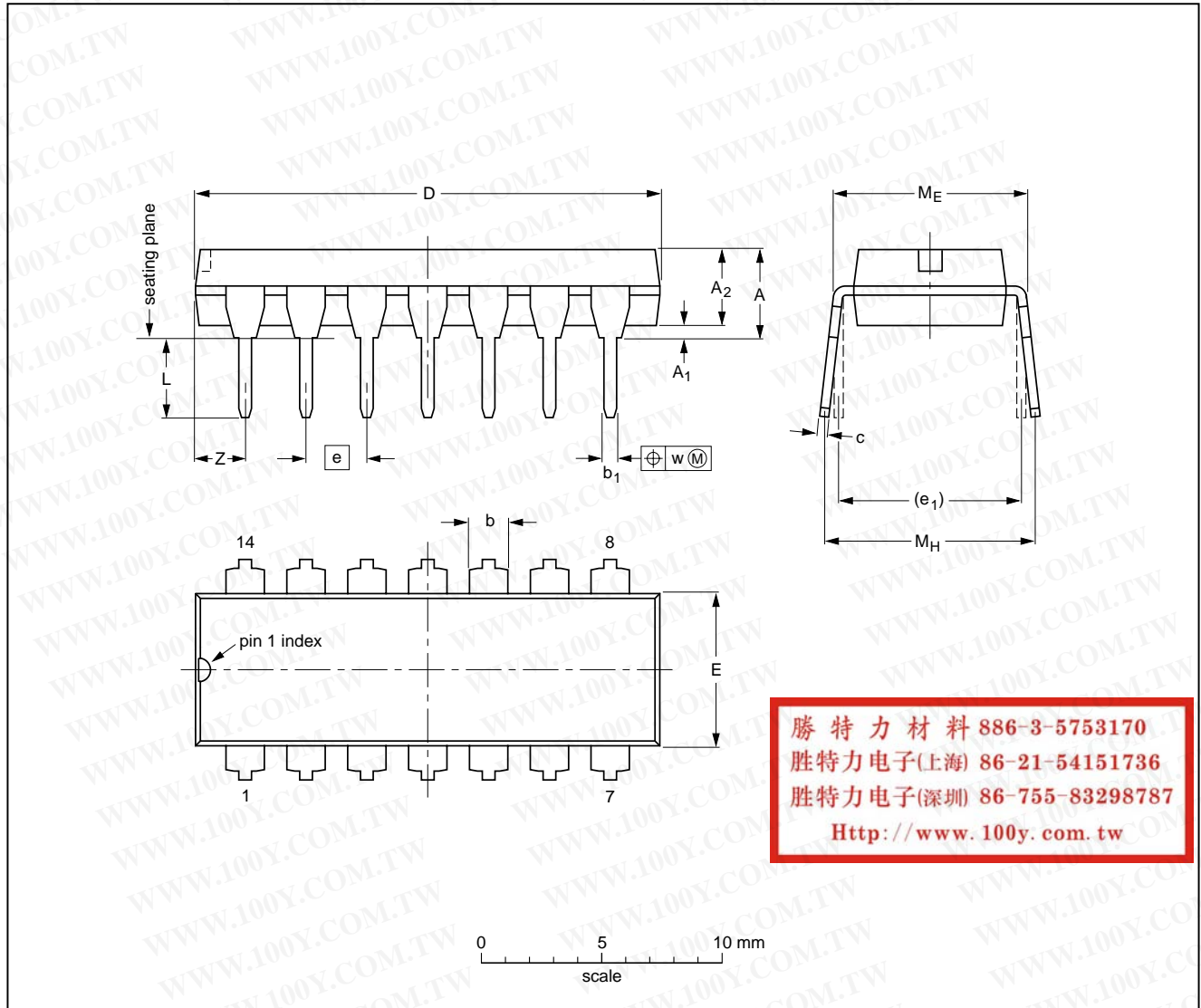
Quad 2-input NAND gate

74HC00; 74HCT00

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



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DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

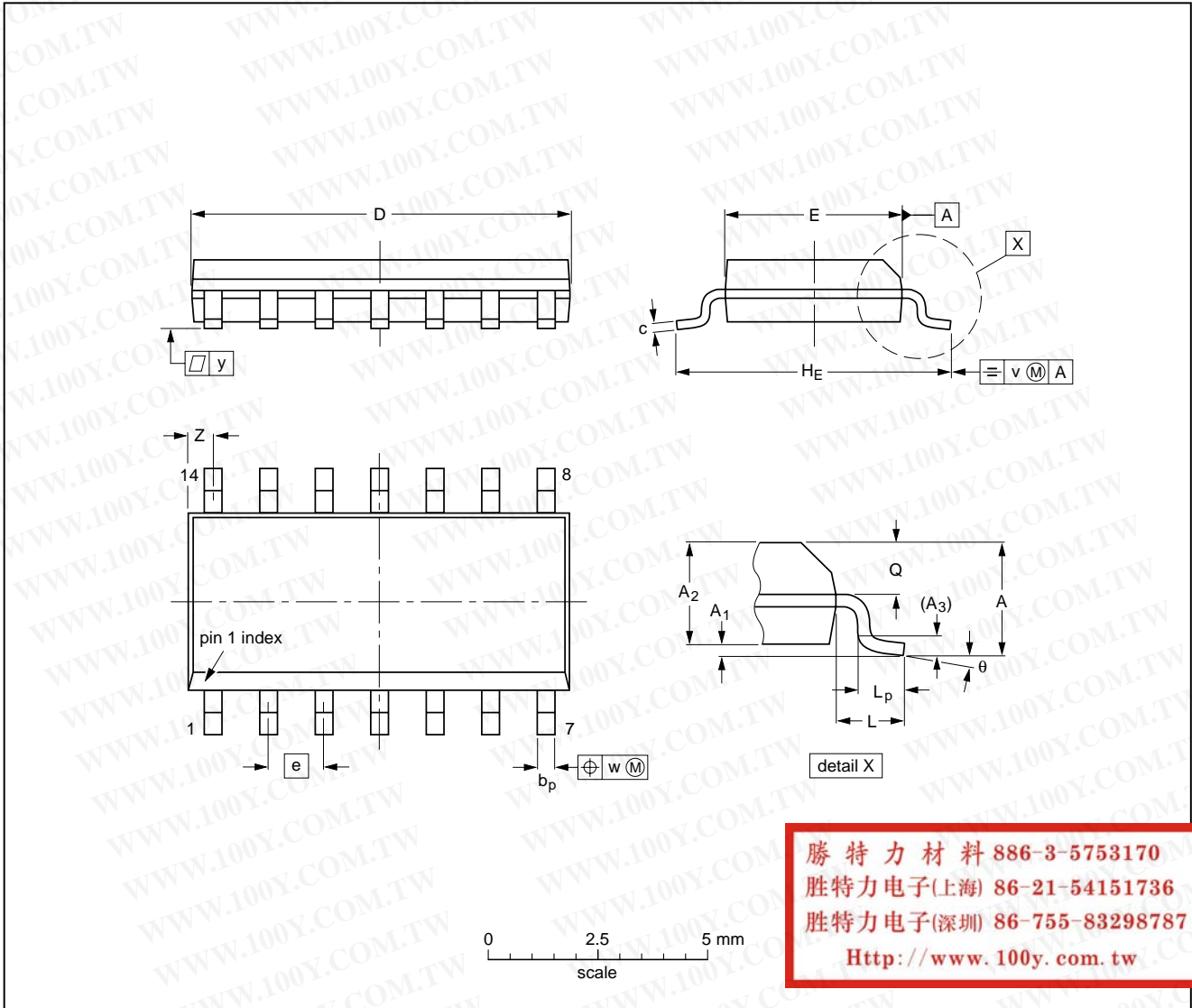
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT27-1	050G04	MO-001	SC-501-14		99-12-27 03-02-13

Quad 2-input NAND gate

74HC00; 74HCT00

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

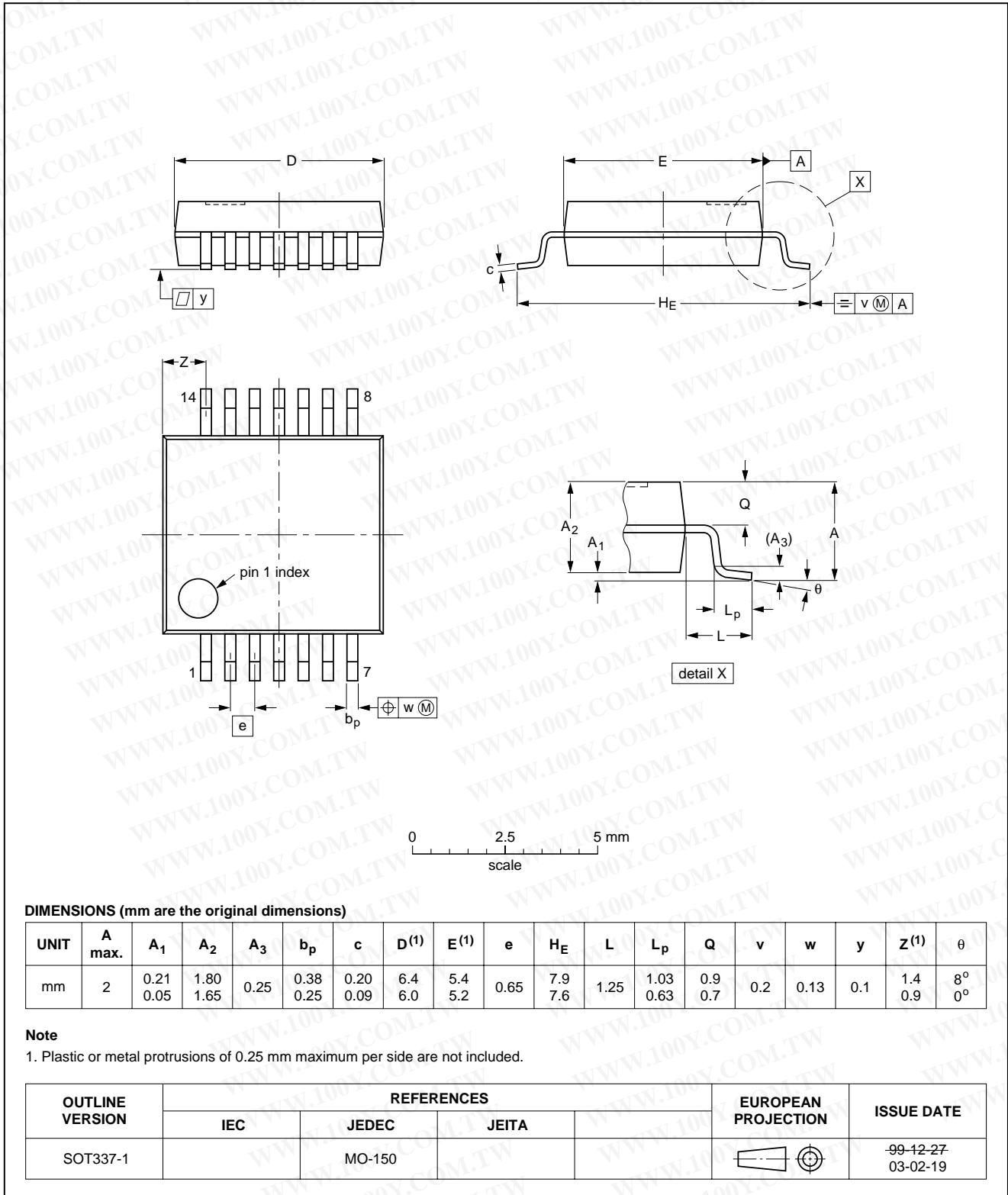
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Quad 2-input NAND gate

74HC00; 74HCT00

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



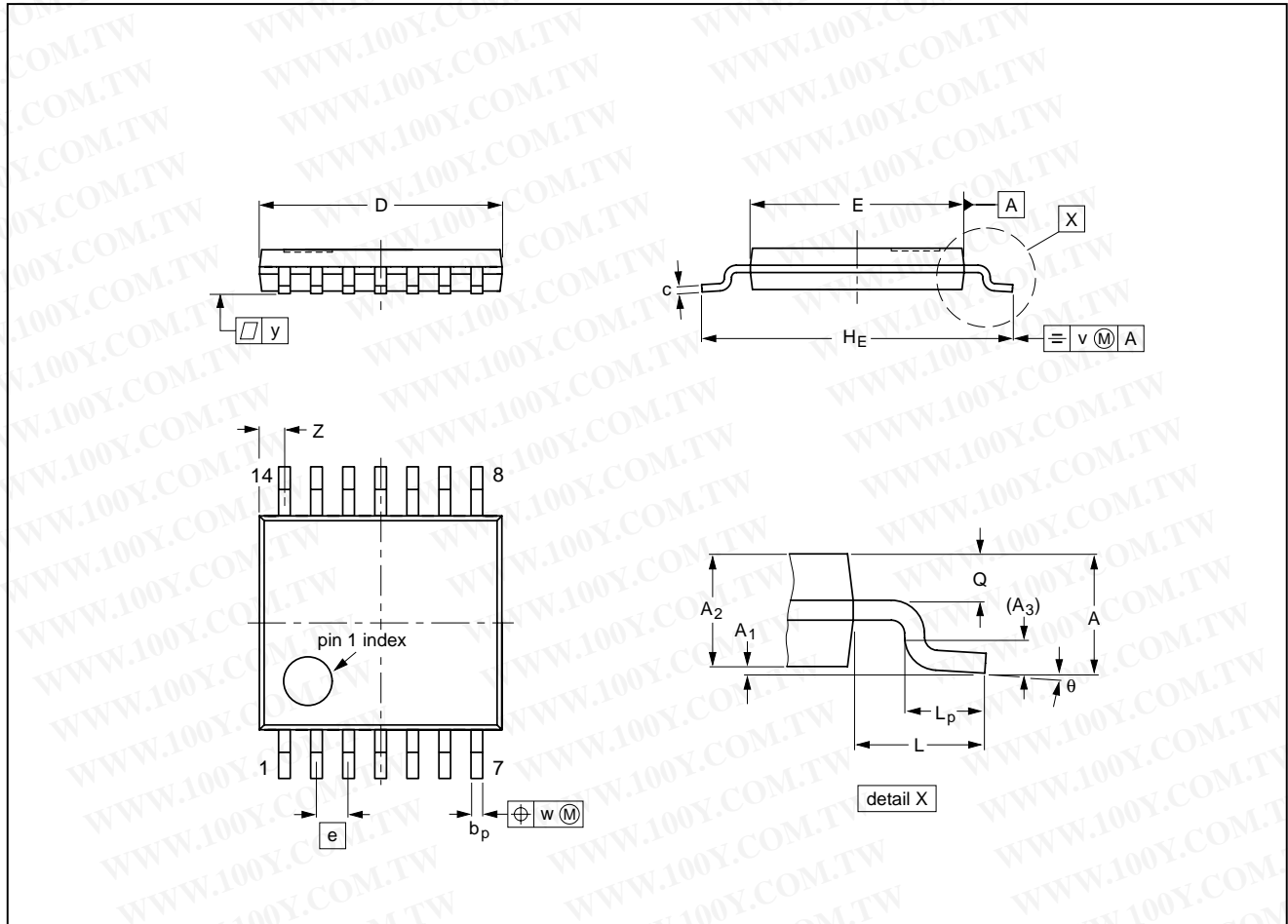
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 勝特力电子(上海) 86-21-54151736  
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Quad 2-input NAND gate

74HC00; 74HCT00

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



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**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

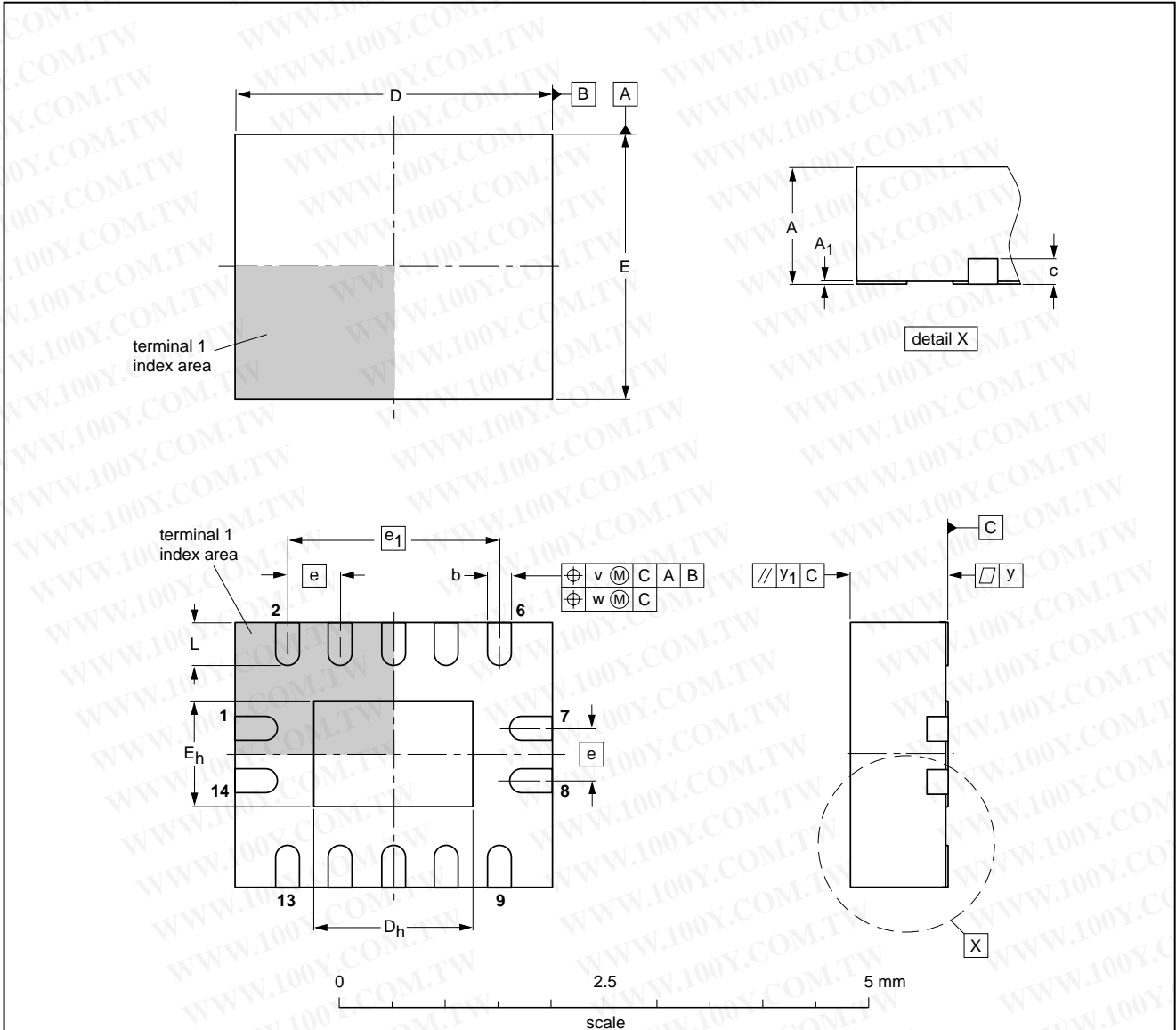
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT402-1		MO-153			99-12-27 03-02-18

Quad 2-input NAND gate

74HC00; 74HCT00

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT762-1	---	MO-241	---		02-10-17 03-01-27

## Quad 2-input NAND gate

74HC00; 74HCT00

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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## Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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