



November 1988
 Revised November 1999

74AC161 • 74ACT161

Synchronous Presettable Binary Counter

General Description

The AC/ACT161 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The AC/ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

Features

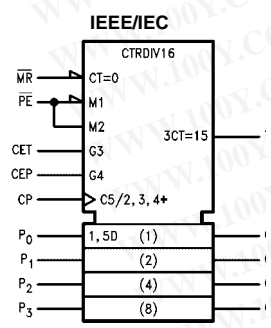
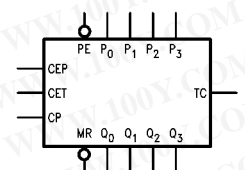
- I_{CC} reduced by 50%
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- ACT161 has TTL-compatible inputs

Ordering Code:

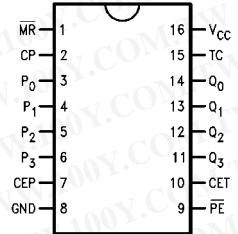
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74AC161SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74AC161SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC161MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC161PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT161SC | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |
| 74ACT161SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ACT161MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT161PC | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|--------------------------------|---------------------------------|
| CEP | Count Enable Parallel Input |
| CET | Count Enable Trickle Input |
| CP | Clock Pulse Input |
| MR | Asynchronous Master Reset Input |
| P ₀ -P ₃ | Parallel Data Inputs |
| PE | Parallel Enable Inputs |
| Q ₀ -Q ₃ | Flip-Flop Outputs |
| TC | Terminal Count Output |

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74AC161 • 74ACT161 Synchronous Presettable Binary Counter

Functional Description

The AC/ACT161 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the AC/ACT161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Five control inputs—Master Reset, Parallel Enable (\overline{PE}), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on \overline{MR} overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \overline{PE} overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With \overline{PE} and \overline{MR} HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The AC/ACT161 use D-type edge-triggered flip-flops and changing the \overline{PE} , CEP, and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle requires 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that lim-

its the clock period is the CP to \overline{TC} delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

$$\text{Logic Equations: Count Enable} = \text{CEP} \cdot \text{CET} \cdot \overline{PE}$$

$$\text{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \text{CET}$$

Mode Select Table

| \overline{PE} | CET | CEP | Action on the Rising Clock Edge (\nearrow) |
|-----------------|-----|-----|--|
| X | X | X | Reset (Clear) |
| L | X | X | Load ($P_n \rightarrow Q_n$) |
| H | H | H | Count (Increment) |
| H | L | X | No Change (Hold) |
| H | X | L | No Change (Hold) |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

State Diagram

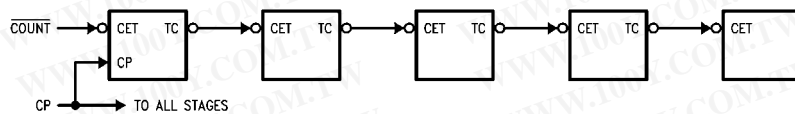
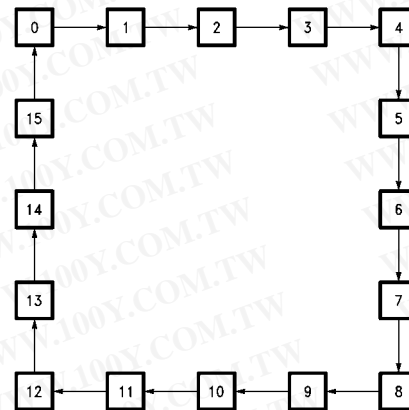


FIGURE 1. Multistage Counter with Ripple Carry

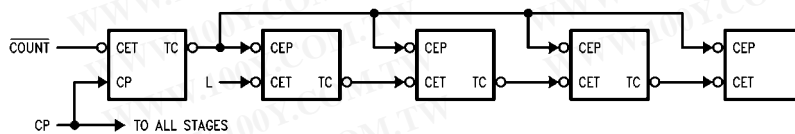
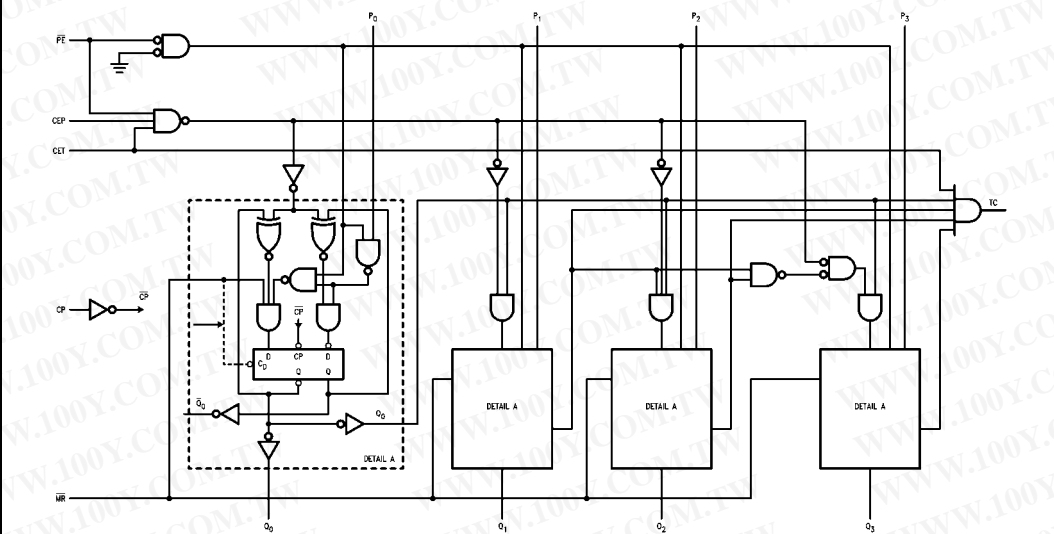


FIGURE 2. Multistage Counter with Lookahead Carry

Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source or Sink Current (I_O) | ±50 mA |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) | ±50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Junction Temperature (T_J) | |
| PDIP | 140°C |

Recommended Operating Conditions

| | |
|---|----------------|
| Supply Voltage (V_{CC}) | |
| AC | 2.0V to 6.0V |
| ACT | 4.5V to 5.5V |
| Input Voltage (V_I) | 0V to V_{CC} |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| AC Devices | |
| V_{IN} from 30% to 70% of V_{CC} | |
| V_{CC} @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| ACT Devices | |
| V_{IN} from 0.8V to 2.0V | |
| V_{CC} @ 4.5V, 5.5V | 125 mV/ns |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-
 out exception, to ensure that the system design is reliable over its power
 supply, temperature, and output/input loading variables. Fairchild does not
 recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ C$ | | $T_A = -40^\circ C$ to $+85^\circ C$ | | Units | Conditions |
|----------------------|--------------------------------------|-----------------|---------------------|-------------------|--------------------------------------|-------------------|---|------------|
| | | | Typ | Guaranteed Limits | Typ | Guaranteed Limits | | |
| V_{IH} | Minimum HIGH Level Input Voltage | 3.0 | 1.5 | 2.1 | 2.1 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 4.5 | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | 3.0 | 1.5 | 0.9 | 0.9 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 4.5 | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | | |
| V_{OH} | Minimum HIGH Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT} = -50 \mu A$ | |
| | | 4.5 | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 3.0 | | 2.56 | 2.46 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 mA$ $I_{OH} = -24 mA$ $I_{OH} = -24 mA$ (Note 2) | |
| | | 4.5 | | 3.86 | 3.76 | | | |
| | | 5.5 | | 4.86 | 4.76 | | | |
| V_{OL} | Maximum LOW Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | | 4.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 3.0 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 mA$ $I_{OL} = 24 mA$ $I_{OL} = 24 mA$ (Note 2) | |
| | | 4.5 | | 0.36 | 0.44 | | | |
| | | 5.5 | | 0.36 | 0.44 | | | |
| I_{IN} (Note 4) | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | µA | $V_I = V_{CC}, GND$ | |
| I_{OLD} | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max | |
| I_{OHD} | Output Current (Note 3) | 5.5 | | | -75 | mA | $V_{OHD} = 3.85V$ Min | |
| I_{CC} (Note 4) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | µA | $V_{IN} = V_{CC}$ or GND | |

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

| DC Electrical Characteristics for ACT | | | | | | | | |
|---------------------------------------|--------------------------------------|------------------------|------------------------|-------------------|---------------------------------|--|-------|---|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -40°C to +85°C | | Units | Conditions |
| | | | Typ | Guaranteed Limits | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | | V | V _{OUT} = 0.1V or V _{CC} - 0.1V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | | V | V _{OUT} = 0.1V or V _{CC} - 0.1V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | | V | I _{OUT} = -50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | | 3.86 | 3.76 | | V | V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 5) |
| | | 5.5 | | 4.86 | 4.76 | | | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | | V | I _{OUT} = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | | 0.36 | 0.44 | | V | V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 5) |
| | | 5.5 | | 0.36 | 0.44 | | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | | μA | V _I = V _{CC} , GND |
| I _{CC} | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.5 | | mA | V _I = V _{CC} - 2.1V |
| I _{OLD} | Minimum Dynamic | 5.5 | | | 75 | | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current (Note 6) | 5.5 | | | -75 | | mA | V _{OHD} = 3.85V Min |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | | μA | V _{IN} = V _{CC} or GND |

Note 5: All outputs loaded; thresholds on input associated with output under test.
Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

| AC Electrical Characteristics for AC | | | | | | | | |
|--------------------------------------|--|------------------------------------|--|-----|------|---|------|-------|
| Symbol | Parameter | V _{CC} (V) (Note 7) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum Count Frequency | 3.3 | 70 | 111 | | 60 | | MHz |
| | | 5.0 | 110 | 167 | | 95 | | |
| t _{PLH} | Propagation Delay CP to Q _n (PE Input HIGH or LOW) | 3.3 | 2.0 | 7.0 | 12 | 1.5 | 13.5 | ns |
| | | 5.0 | 1.5 | 5.0 | 9.0 | 1.0 | 9.5 | |
| t _{PHL} | Propagation Delay CP to Q _n (PE Input HIGH or LOW) | 3.3 | 1.5 | 7.0 | 12 | 1.5 | 13 | ns |
| | | 5.0 | 1.5 | 5.0 | 9.5 | 1.5 | 10 | |
| t _{PLH} | Propagation Delay CP to TC | 3.3 | 3.0 | 9 | 15 | 2.5 | 16.5 | ns |
| | | 5.0 | 2.0 | 6 | 10.5 | 1.5 | 11.5 | |
| t _{PHL} | Propagation Delay CP to TC | 3.3 | 3.5 | 8.5 | 14 | 2.5 | 15.5 | ns |
| | | 5.0 | 2.0 | 6.5 | 11 | 2.0 | 11.5 | |
| t _{PLH} | Propagation Delay CET to TC | 3.3 | 2.0 | 5.5 | 9.5 | 1.5 | 11 | ns |
| | | 5.0 | 1.5 | 3.5 | 6.5 | 1.0 | 7.5 | |
| t _{PHL} | Propagation Delay CET to TC | 3.3 | 2.5 | 6.5 | 11 | 2.0 | 12.5 | ns |
| | | 5.0 | 2.0 | 5 | 8.5 | 1.5 | 9.5 | |
| t _{PHL} | Propagation Delay MR to Q _n | 3.3 | 2.0 | 6.5 | 12 | 1.5 | 13.5 | ns |
| | | 5.0 | 1.5 | 5.5 | 9.5 | 1.5 | 10 | |
| t _{PHL} | Propagation Delay MR to TC | 3.3 | 3.5 | 10 | 15 | 3.0 | 17.5 | ns |
| | | 5.0 | 2.5 | 8.5 | 13 | 2.5 | 13.5 | |

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
 Voltage Range 5.0 is 5.0V ± 0.5V

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| AC Operating Requirements for AC | | | | | | | |
|----------------------------------|--|------------------------------------|--|--------------------|---|--------------------|-------|
| Symbol | Parameter | V _{CC} (V) (Note 8) | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Typ | Guaranteed Minimum | Typ | Guaranteed Minimum | |
| t _S | Setup Time, HIGH or LOW P _n to CP | 3.3 | 6.0 | 13.5 | 16 | ns | |
| | | 5.0 | 3.5 | 8.5 | 10.5 | | |
| t _H | Hold Time, HIGH or LOW P _n to CP | 3.3 | -7.0 | -1 | -0.5 | ns | |
| | | 5.0 | -4.0 | 0 | 0 | | |
| t _S | Setup Time, HIGH or LOW \overline{PE} to CP | 3.3 | 6.5 | 11.5 | 14 | ns | |
| | | 5.0 | 4.0 | 7.5 | 8.5 | | |
| t _H | Hold Time, HIGH or LOW \overline{PE} to CP | 3.3 | -6.0 | 0 | 0 | ns | |
| | | 5.0 | -3.5 | 0.5 | 1 | | |
| t _S | Setup Time, HIGH or LOW CEP or CET to CP | 3.3 | 3.0 | 6.0 | 7 | ns | |
| | | 5.0 | 2.0 | 4.5 | 5 | | |
| t _H | Hold Time, HIGH or LOW CEP or CET to CP | 3.3 | -3.5 | 0 | 0 | ns | |
| | | 5.0 | -2 | 0 | 0.5 | | |
| t _W | Clock Pulse Width (Load) HIGH or LOW | 3.3 | 2.0 | 3.5 | 4 | ns | |
| | | 5.0 | 2.0 | 2.5 | 3 | | |
| t _W | Clock Pulse Width (Count) HIGH or LOW | 3.3 | 2.0 | 4.0 | 4.5 | ns | |
| | | 5.0 | 2.0 | 3.0 | 3.5 | | |
| t _W | \overline{MR} Pulse Width, LOW | 3.3 | 3.0 | 5.5 | 7.5 | ns | |
| | | 5.0 | 2.5 | 4.5 | 6.0 | | |
| t _{REC} | Recovery Time \overline{MR} to CP | | -2 | -0.5 | 0 | ns | |
| | | | -1 | 0 | 0.5 | | |

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V
 Voltage Range 5.0 is 5.0V ± 0.5V

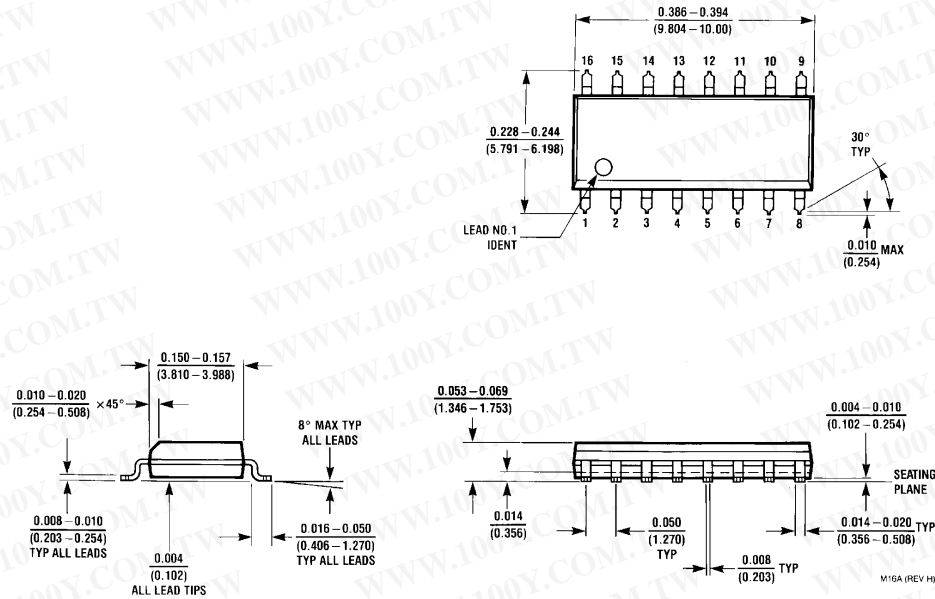
| AC Electrical Characteristics for ACT | | | | | | | | |
|---------------------------------------|--|------------------------------------|--|-----|------|---|------|-------|
| Symbol | Parameter | V _{CC} (V) (Note 9) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Min | Typ | Max | Min | Max | |
| t _{MAX} | Maximum Count Frequency | 5.0 | 115 | 125 | | 100 | | MHz |
| t _{PLH} | Propagation Delay CP to Q _n (\overline{PE} Input HIGH or LOW) | 5.0 | 1.5 | 5.5 | 9.5 | 1.5 | 10.5 | ns |
| t _{PHL} | Propagation Delay CP to Q _n (\overline{PE} Input HIGH or LOW) | 5.0 | 1.5 | 6.0 | 10.5 | 1.5 | 11.5 | ns |
| t _{PLH} | Propagation Delay CP to TC | 5.0 | 2.0 | 7.0 | 11.0 | 1.5 | 12.5 | ns |
| t _{PHL} | Propagation Delay CP to TC | 5.0 | 1.5 | 8.0 | 12.5 | 1.5 | 13.5 | ns |
| t _{PLH} | Propagation Delay CET to TC | 5.0 | 1.5 | 5.5 | 8.5 | 1.5 | 10.0 | ns |
| t _{PHL} | Propagation Delay CET to TC | 5.0 | 1.5 | 6.5 | 9.5 | 1.5 | 10.5 | ns |
| t _{PHL} | Propagation Delay \overline{MR} to Q _n | 5.0 | 1.5 | 6.0 | 10.0 | 1.5 | 11.0 | ns |
| t _{PHL} | Propagation Delay \overline{MR} to TC | 5.0 | 2.5 | 8.0 | 13.5 | 2.0 | 14.5 | ns |

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

| AC Operating Requirements for ACT | | | | | | | |
|--|---|-------------------------------------|--|------------------------|---|--|-------|
| Symbol | Parameter | V _{CC} (V) (Note 10) | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Typ | Guaranteed Minimum | | | |
| t _S | Setup Time, HIGH or LOW P _n to CP | 5.0 | 4.0 | 9.5 | 11.5 | | ns |
| t _H | Hold Time, HIGH or LOW P _n to CP | 5.0 | -5.0 | 0 | 0 | | ns |
| t _S | Setup Time, HIGH or LOW PE to CP | 5.0 | 4.0 | 8.5 | 9.5 | | ns |
| t _H | Hold Time, HIGH or LOW PE to CP | 5.0 | -5.5 | -0.5 | -0.5 | | ns |
| t _S | Setup Time, HIGH or LOW CEP or CET to CP | 5.0 | 2.5 | 5.5 | 6.5 | | ns |
| t _H | Hold Time, HIGH or LOW CEP or CET to CP | 5.0 | -3.0 | 0 | 0 | | ns |
| t _W | Clock Pulse Width, (Load) HIGH or LOW | 5.0 | 2.0 | 3.0 | 3.5 | | ns |
| t _W | Clock Pulse Width, (Count) HIGH or LOW | 5.0 | 2.0 | 3.0 | 3.5 | | ns |
| t _W | MR Pulse Width, LOW | 5.0 | 3.0 | 3.0 | 7.5 | | ns |
| t _{REC} | Recovery Time MR to CP | 5.0 | 0 | 0 | 0.5 | | ns |
| Note 10: Voltage Range 5.0 is 5.0V ± 0.5V | | | | | | | |
| Capacitance | | | | | | | |
| Symbol | Parameter | Typ | Units | Conditions | | | |
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = OPEN | | | |
| C _{PD} | Power Dissipation Capacitance | 45.0 | pF | V _{CC} = 5.0V | | | |

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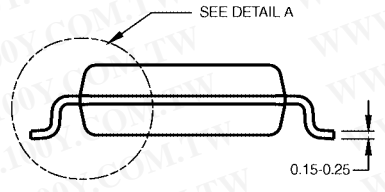
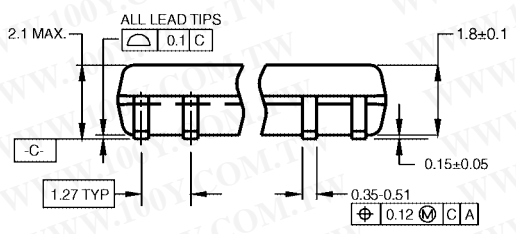
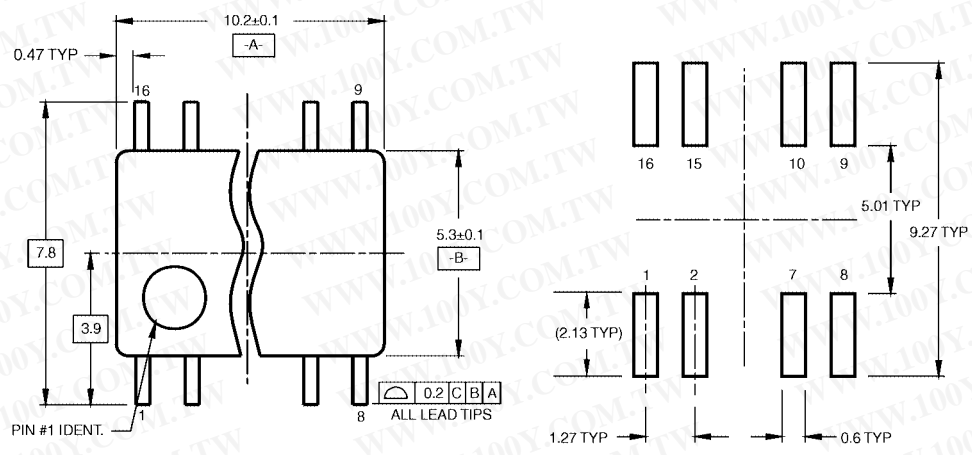
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

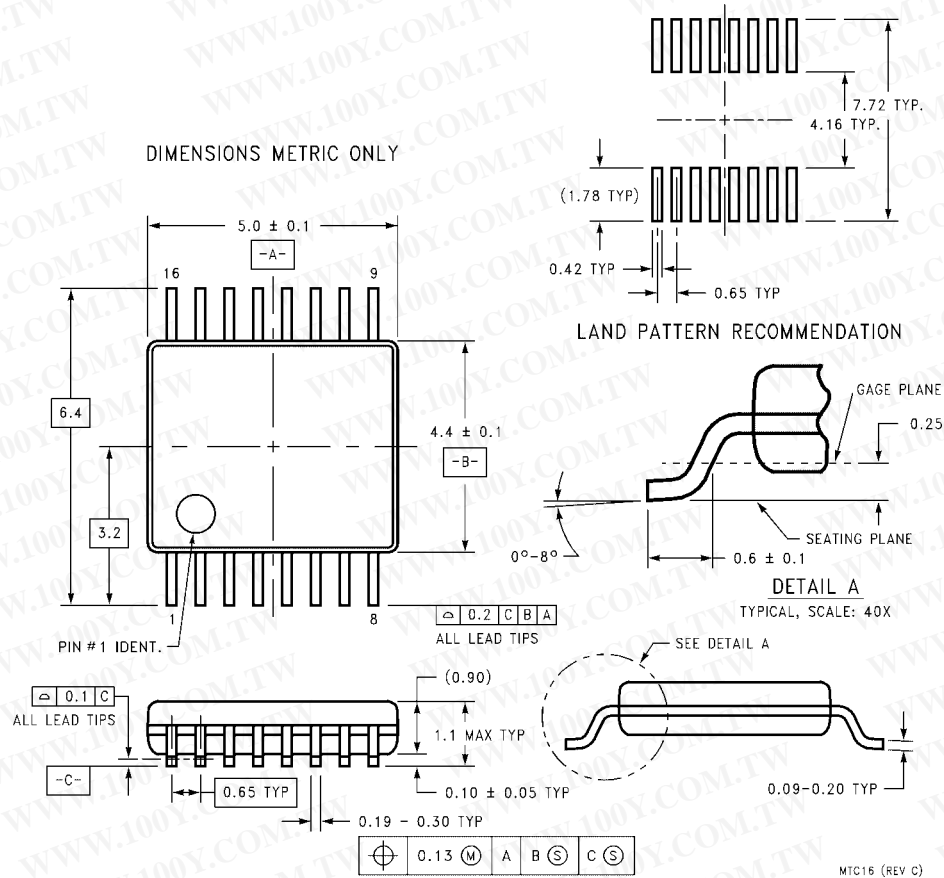
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

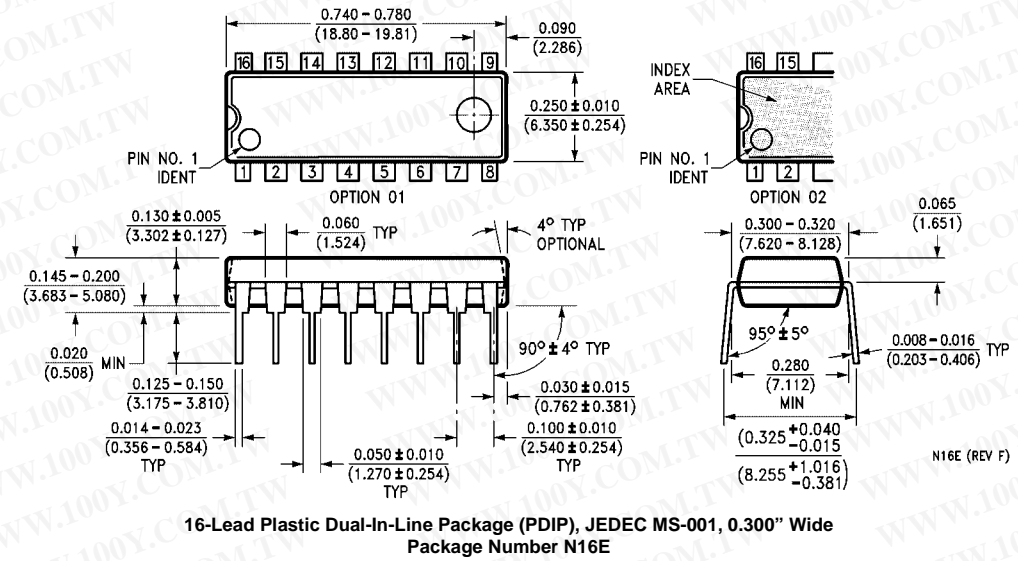
74AC161 • 74ACT161

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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