19-0463; Rev 2; 10/05

Low-Voltage, CMOS Analog Multiplexers/Switches

General Description

The MAX4051/MAX4052/MAX4053 and MAX4051A/MAX4052A/MAX4053A are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4051/A), two 4-channel multiplexers (MAX4052/A), and three single-pole/double-throw (SPDT) switches (MAX4053/A). The A-suffix parts are fully characterized for on-resistance match, on-resistance flatness, and low leakage.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 0.1nA at +25°C or 5nA at +85°C (MAX4051A/MAX4052A/MAX4053A).

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Communications Circuits

Features

- **Pin Compatible with Industry-Standard 74HC4051/74HC4052/74HC4053**
- **Guaranteed On-Resistance: 100Ω with ±5V Supplies**
- **Guaranteed Match Between Channels: 6Ω (MAX4051A–MAX4053A) 12Ω (MAX4051–MAX4053)**
- **Guaranteed Low Off-Leakage Currents: 0.1nA at +25°C (MAX4051A–MAX4053A) 1nA at +25°C (MAX4051–MAX4053)**
- **Guaranteed Low On-Leakage Currents: 0.1nA at +25°C (MAX4051A–MAX4053A) 1nA at +25°C (MAX4051–MAX4053)**
- **Single-Supply Operation from +2.0V to +16V Dual-Supply Operation from ±2.7V to ±8V**
- **TTL/CMOS-Logic Compatible**
- **Low Distortion: < 0.04% (600Ω)**
- **Low Crosstalk: < -90dB (50Ω)**
- **High Off-Isolation: < -90dB (50Ω)**

Ordering Information

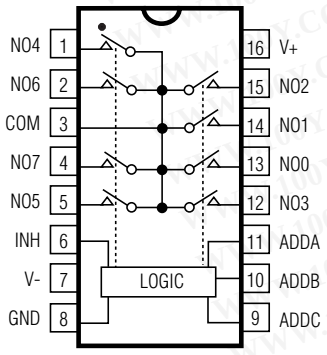
PART	TEMP RANGE	PIN-PACKAGE
MAX4051ACPE	0°C to +70°C	16 Plastic DIP
MAX4051ACSE	0°C to +70°C	16 Narrow SO
MAX4051ACEE	0°C to +70°C	16 QSOP

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams

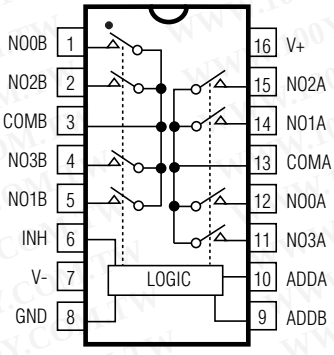
TOP VIEW

MAX4051



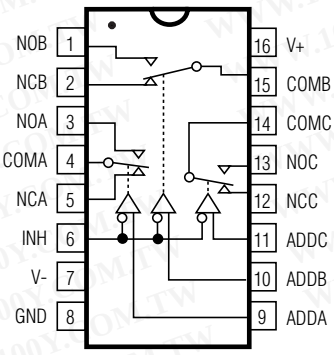
DIP/SO/QSOP

MAX4052



DIP/SO/QSOP

MAX4053



DIP/SO/QSOP

Low-Voltage, CMOS Analog Multiplexers/Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
- V+ .....-0.3V to +17V
- V- .....+0.3V to -17V
- V+ to V- .....-0.3V to +17V
- Voltage into Any Terminal (Note 1) .....(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)

Continuous Current into Any Terminal .....±30mA
Peak Current, NO or COM
- (pulsed at 1ms, 10% duty cycle) .....±100mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 8.70mW/°C above +70°C) 696mW
- QSOP (derate 8.00mW/°C above +70°C) 640mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges
- MAX405_C_ E/MAX405_AC_E .....0°C to +70°C
- MAX405_E_ E/MAX405_AE_E .....-40°C to +85°C
- MAX405_MJE/MAX405_AMJE .....-55°C to +125°C

Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V		T_A = +25°C		60	100	Ω
				C, E, M			125	
COM–NO On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C			6	Ω
				C, E, M			12	
			MAX4051, MAX4052, MAX4053	T_A = +25°C			12	
				C, E, M			18	
COM–NO On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = -3V, 0V, 3V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C			10	Ω
				C, E, M			15	
NO Off-Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{NO} = 4.5V, V_{COM} = -4.5V	MAX4051, MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 5.5V, V- = -5.5V, V_{NO} = -4.5V, V_{COM} = 4.5V	MAX4051A, MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-100		100	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
COM Off-Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{NO} = 4.5V, V_{COM} = -4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-100		100	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V- = -5.5V, V_{NO} = -4.5V, V_{COM} = 4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-50		50	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On-Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = V_{NO} = ±4.5V	MAX4051A	T_A = +25°C	-0.1	0.002	0.1	nA
				C, E	-5		5	
				M	-100		100	
			MAX4051	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052A, MAX4053A	T_A = +25°C	-0.1	0.002	0.1	
				C, E	-2.5		2.5	
				M	-50		50	
			MAX4052, MAX4053	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	

Low-Voltage, CMOS Analog Multiplexers/Switches

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL I/O							
ADD, INH Input Logic Threshold High	V_{IH}		C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}		C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V	C, E, M	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		50	175	ns
			C, E, M			225	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		40	150	ns
			C, E, M			200	
Transition Time	t_{TRANS}	Figure 2	T_A = +25°C		75	250	ns
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C	2	10		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		2	10	pC
NO Off-Capacitance	$C_{NO(OFF)}$	V_{NO} = GND, f = 1MHz, Figure 7	T_A = +25°C		2		pF
COM Off-Capacitance	$C_{COM(OFF)}$	V_{COM} = GND, f = 1MHz, Figure 7	T_A = +25°C		2		pF
Switch On-Capacitance	$C_{(ON)}$	V_{COM} = V_{NO} = GND, f = 1MHz, Figure 7	T_A = +25°C		8		pF
Off-Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E, M	±2.7		±8	V
V+ Supply Current	I+	INH = ADD = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M			10	
V- Supply Current	I-	INH = ADD = 0V or V+	T_A = +25°C	-1	0.1	1	µA
			C, E, M	-10			

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

Note 6: Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	V+ = 5V, I_{NO} = 1mA, V_{COM} = 3.5V		T_A = +25°C		125	225	Ω
				C, E, M			280	
NO Off-Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{NO} = 4.5V, V_{COM} = 0V		T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 5.5V, V_{NO} = 0V, V_{COM} = 4.5V		T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
COM Off-Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 5.5V, V_{NO} = 4.5V, V_{COM} = 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 5.5V, V_{NO} = 0V, V_{COM} = 4.5V or 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On-Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = 4.5V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
DIGITAL I/O								
ADD, INH Input Logic Threshold High	V_{IH}			C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}			C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V		C, E, M	-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	INH = ADD = 0V or V+		T_A = +25°C	-1		1	µA
				C, E, M			10	

Low-Voltage, CMOS Analog Multiplexers/Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		90	200	ns
			C, E, M			275	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		60	125	ns
			C, E, M			175	
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C		30		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		2	10	pC
Off-Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

Note 6: Guaranteed by design, not production tested.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +3.0V to +3.6V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}			C, E, M	V-		V+	V
COM–NO On-Resistance	R_{ON}	I_{NO} = 1mA, V+ = 3V, V_{COM} = 1.5V		T_A = +25°C		250	525	Ω
				C, E, M			700	
NO Off-Leakage Current (Note 5)	$I_{NO(OFF)}$	V+ = 3.6V, V_{NO} = 3V, V_{COM} = 0V		T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
		V+ = 3.6V, V_{NO} = 0V, V_{COM} = 3V		T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
COM Off-Leakage Current (Note 5)	$I_{COM(OFF)}$	V+ = 3.6V, V_{NO} = 3V, V_{COM} = 0V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
		V+ = 3.6V, V_{NO} = 0V, V_{COM} = 3V	MAX4051/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-5		5	
				M	-50		50	
COM On-Leakage Current (Note 5)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} = 3V	MAX4051/A	T_A = +25°C	-1	0.002	1	nA
				C, E	-10		10	
				M	-100		100	
			MAX4052/A, MAX4053/A	T_A = +25°C	-1	0.002	1	
				C, E	-10		10	
				M	-100		100	
DIGITAL I/O								
ADD, INH Input Logic Threshold High	V_{IH}			C, E, M	2.4			V
ADD, INH Input Logic Threshold Low	V_{IL}			C, E, M			0.8	V
ADD, INH Input Current Logic High or Low	I_{IH}, I_{IL}	V_{ADD}, V_{INH} = V+, 0V		C, E, M	-1	0.03	1	µA
POWER SUPPLY								
V+ Supply Current	I+	INH = ADD = 0V or V+		T_A = +25°C	-1		1	µA
				C, E, M			10	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3.0V to +3.6V, V- = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time (Note 6)	t_{ON}	Figure 3	T_A = +25°C		180	600	ns
			C, E, M			700	
Turn-Off Time (Note 6)	t_{OFF}	Figure 3	T_A = +25°C		100	300	ns
			C, E, M			400	
Break-Before-Make Delay	t_{OPEN}	Figure 4	T_A = +25°C		90		ns
Charge Injection (Note 6)	Q	C_L = 1nF, R_S = 0Ω, V_{NO} = 0V, Figure 5	T_A = +25°C		1	10	pC
Off-Isolation	V_{ISO}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB
Channel-to-Channel Crosstalk	V_{CT}	C_L = 15pF, R_L = 50Ω, f = 100kHz, V_{NO} = $1V_{RMS}$, Figure 6	T_A = +25°C		<-90		dB

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V_{NO} = 3V to 0V and 0V to -3V.

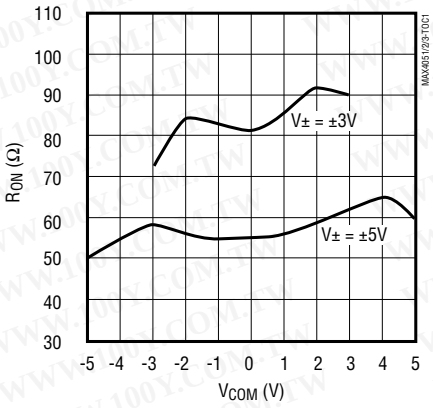
Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

Note 6: Guaranteed by design, not production tested.

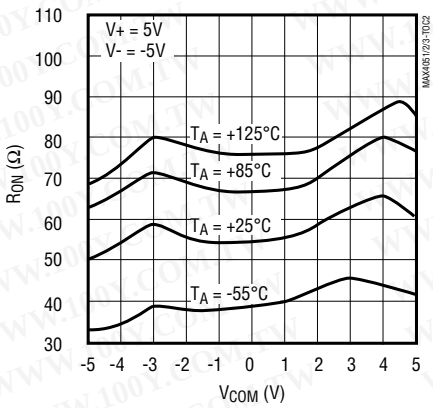
Typical Operating Characteristics

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

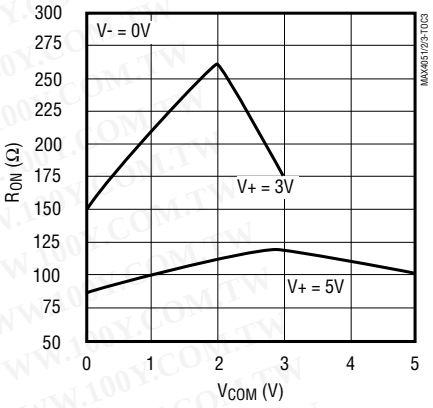
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



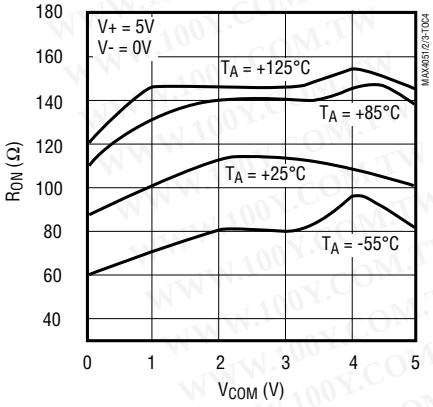
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



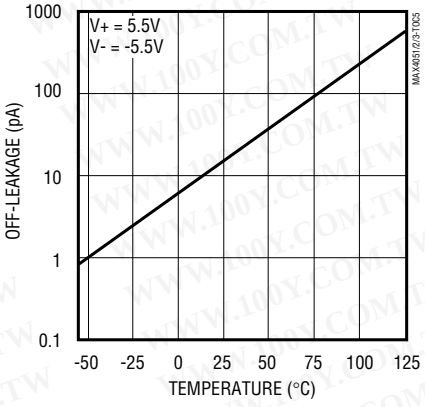
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



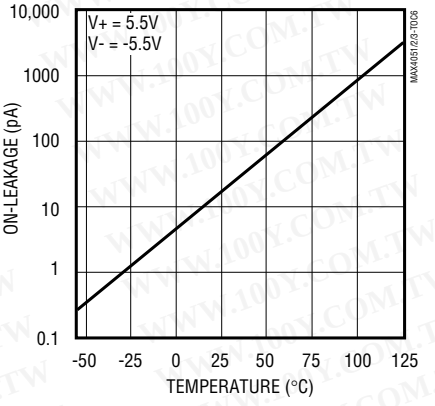
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



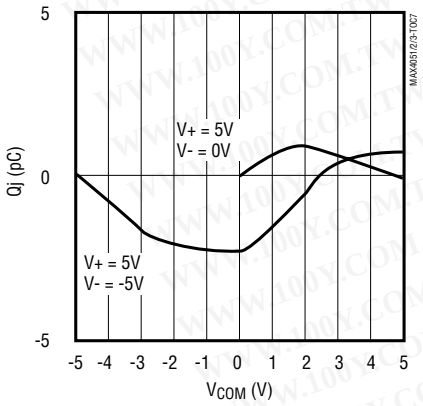
OFF-LEAKAGE vs. TEMPERATURE



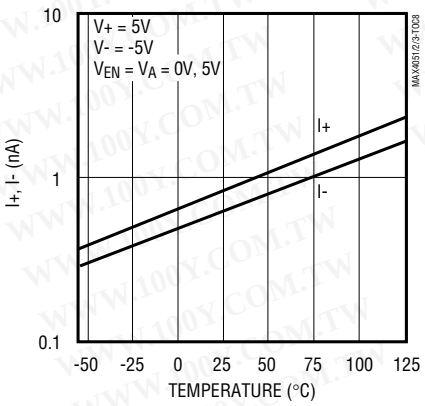
ON-LEAKAGE vs. TEMPERATURE



CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE

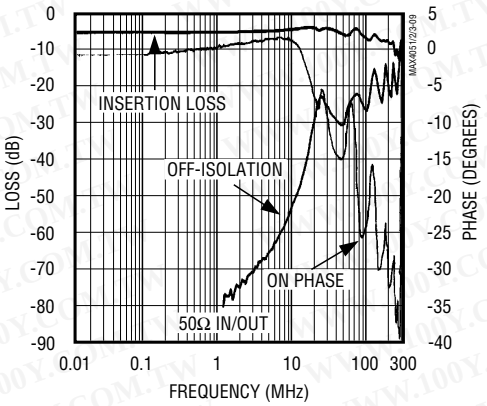


Low-Voltage, CMOS Analog Multiplexers/Switches

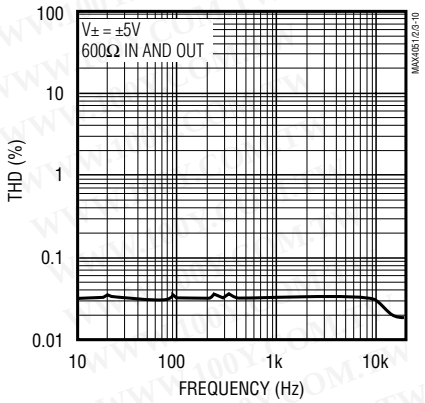
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise noted.)

FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Descriptions

PIN			NAME	FUNCTION
MAX4051/ MAX4051A	MAX4052/ MAX4052A	MAX4053/ MAX4053A		
1, 2, 4, 5, 12, 13, 14, 15	—	—	NO0–NO7	Analog Switch Inputs 0–7
3	—	—	COM	Analog Switch Common
—	1, 2, 4, 5	—	NO0B–NO3B	Analog Switch “B” Inputs 0–3
—	3	15	COMB	Analog Switch “B” Common
—	—	1	NOB	Analog Switch “B” Normally Open Input
—	—	2	NCB	Analog Switch “B” Normally Closed Input
—	—	3	NOA	Analog Switch “A” Normally Open Input
—	—	5	NCA	Analog Switch “A” Normally Closed Input
6	6	6	INH	Digital Inhibit Input. Normally connect to GND. Can be driven to logic high to set all switches off.
7	7	7	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
8	8	8	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
9	—	11	ADDC	Digital Address “C” Input
10	9	10	ADDB	Digital Address “B” Input
11	10	9	ADDA	Digital Address “A” Input
—	11, 12, 14, 15	—	NO0A–NO3A	Analog Switch “A” Inputs 0–3
—	13	4	COMA	Analog Switch “A” Common
—	—	12	NCC	Analog Switch “C” Normally Closed Input
—	—	13	NOC	Analog Switch “C” Normally Open Input
—	—	14	COMC	Analog Switch “C” Common
16	16	16	V+	Positive Analog and Digital Supply Voltage Input

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

Table 1. Truth Table/Switch Programming

INH	ADDRESS BITS			ON SWITCHES		
	ADDC*	ADDB	ADDA	MAX4051/ MAX4051A	MAX4052/ MAX4052A	MAX4053/ MAX4053A
1	X	X	X	All switches open	All switches open	All switches open
0	0	0	0	COM–NO0	COMB–NO0B, COMA–NO0A	COMA–NCA, COMB–NCB, COMC–NCC
0	0	0	1	COM–NO1	COMB–NO1B, COMA–NO1A	COMA–NOA, COMB–NCB, COMC–NCC
0	0	1	0	COM–NO2	COMB–NO2B, COMA–NO2A	COMA–NCA, COMB–NOB, COMC–NCC
0	0	1	1	COM–NO3	COMB–NO3B, COMA–NO3A	COMA–NOA, COMB–NOB, COMC–NCC
0	1	0	0	COM–NO4	COMB–NO0B, COMA–NO0A	COMA–NCA, COMB–NCB, COMC–NOC
0	1	0	1	COM–NO5	COMB–NO1B, COMA–NO1A	COMA–NOA, COMB–NCB, COMC–NOC
0	1	1	0	COM–NO6	COMB–NO2B, COMA–NO2A	COMA–NCA, COMB–NOB, COMC–NOC
0	1	1	1	COM–NO7	COMB–NO3B, COMA–NO3A	COMA–NOA, COMB–NOB, COMC–NOC

X = Don't care * ADDC not present on MAX4052.

Note: NO and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

Applications Information

Power-Supply Considerations

Overview

The MAX4051/MAX4052/MAX4053 and MAX4051A/MAX4052A/MAX4053A construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog signal path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

Low-Voltage, CMOS Analog Multiplexers/Switches

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and V- signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+ and V- have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V+ is +5V. As V+ rises, the threshold increases slightly, so when V+ reaches +12V, the threshold is about 3.1V; above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

These devices operate with bipolar supplies between ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of +17V.

Single Supply

These devices operate from a single supply between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually "work" with a single supply at near or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs (NO) and by COM. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 17V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

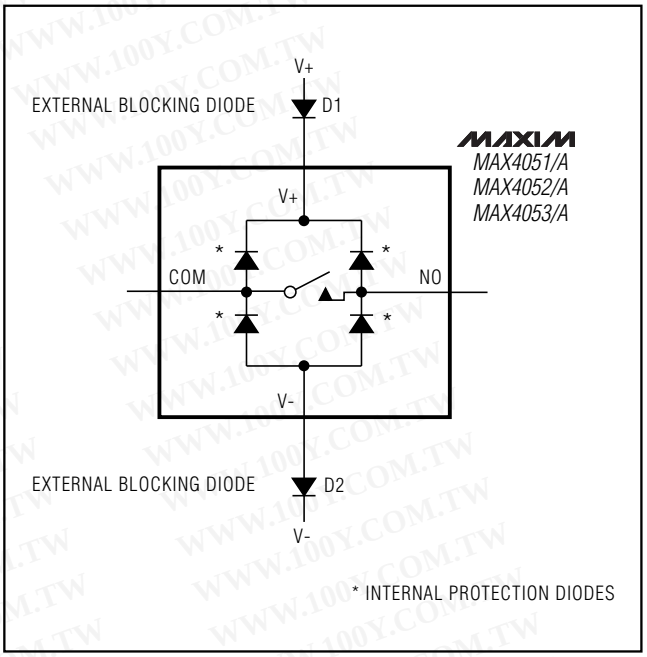
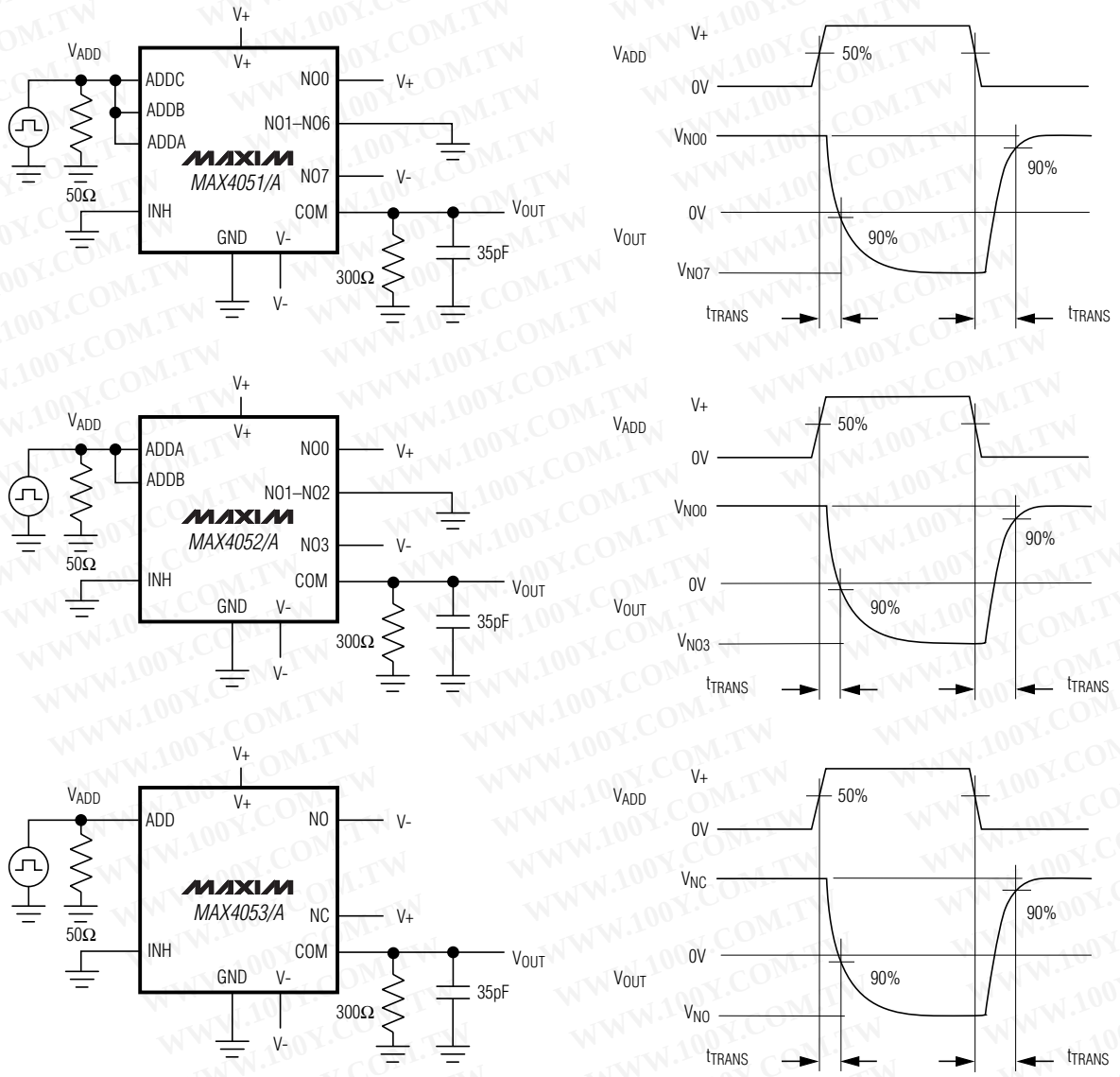


Figure 1. Overvoltage Protection Using External Blocking Diodes

High-Frequency Performance

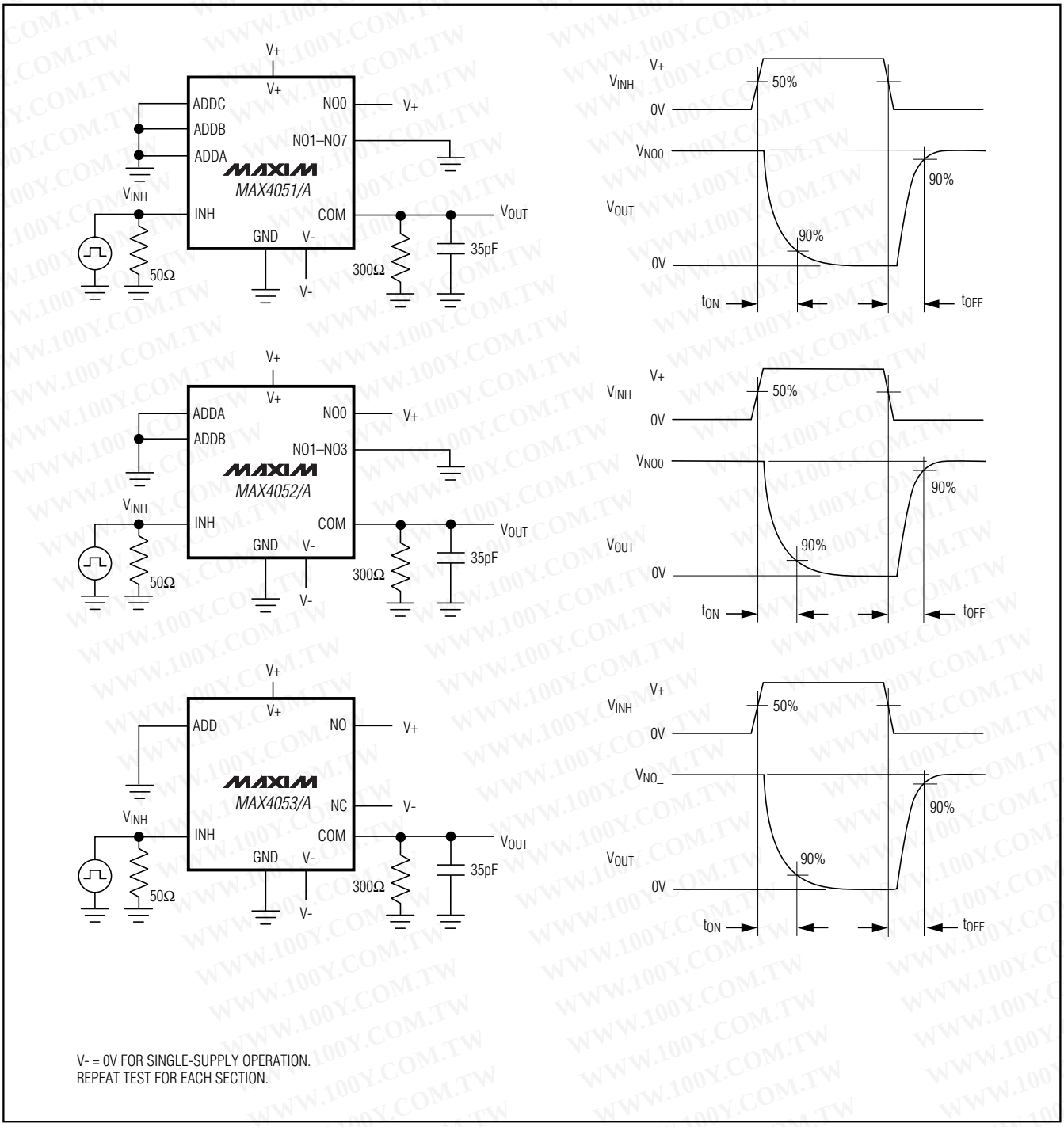
In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor, and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is entirely due to capacitive coupling.

Test Circuits/Timing Diagrams



V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 2. Address Transition Time



V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 3. Enable Switching Time

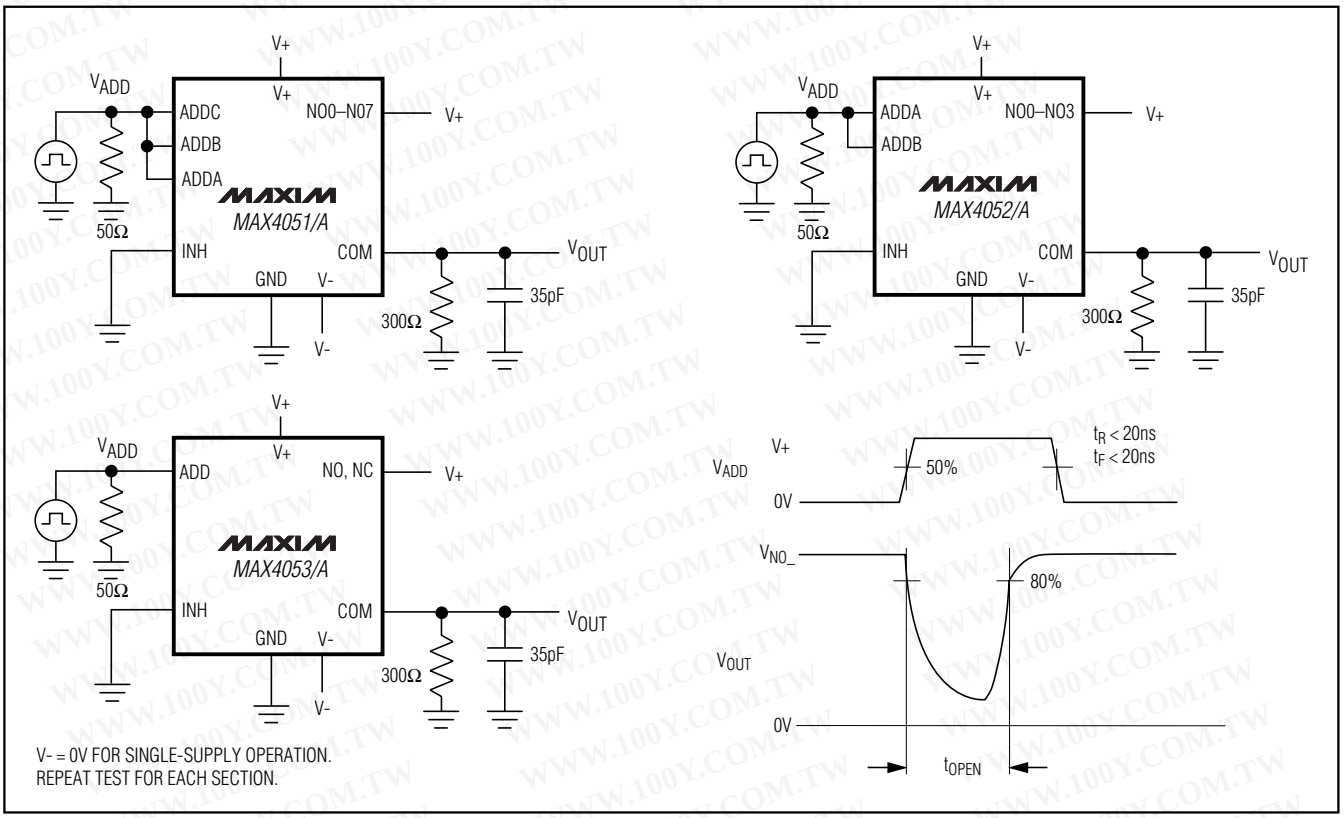


Figure 4. Break-Before-Make Interval

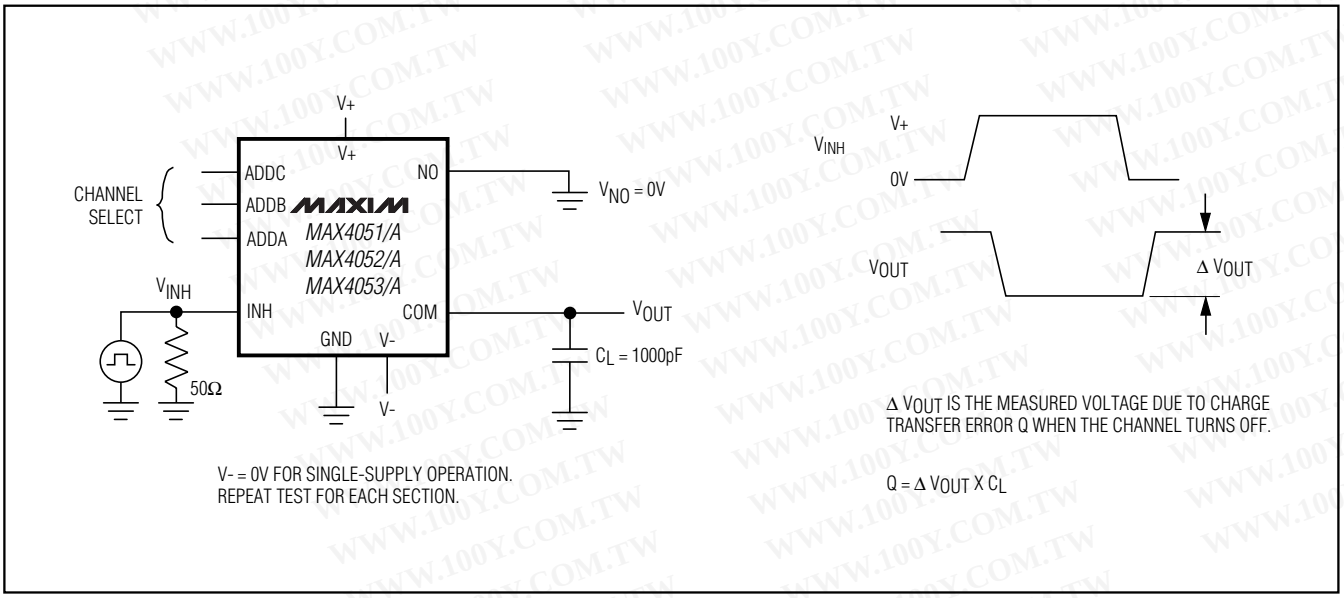


Figure 5. Charge Injection

Low-Voltage, CMOS Analog Multiplexers/Switches

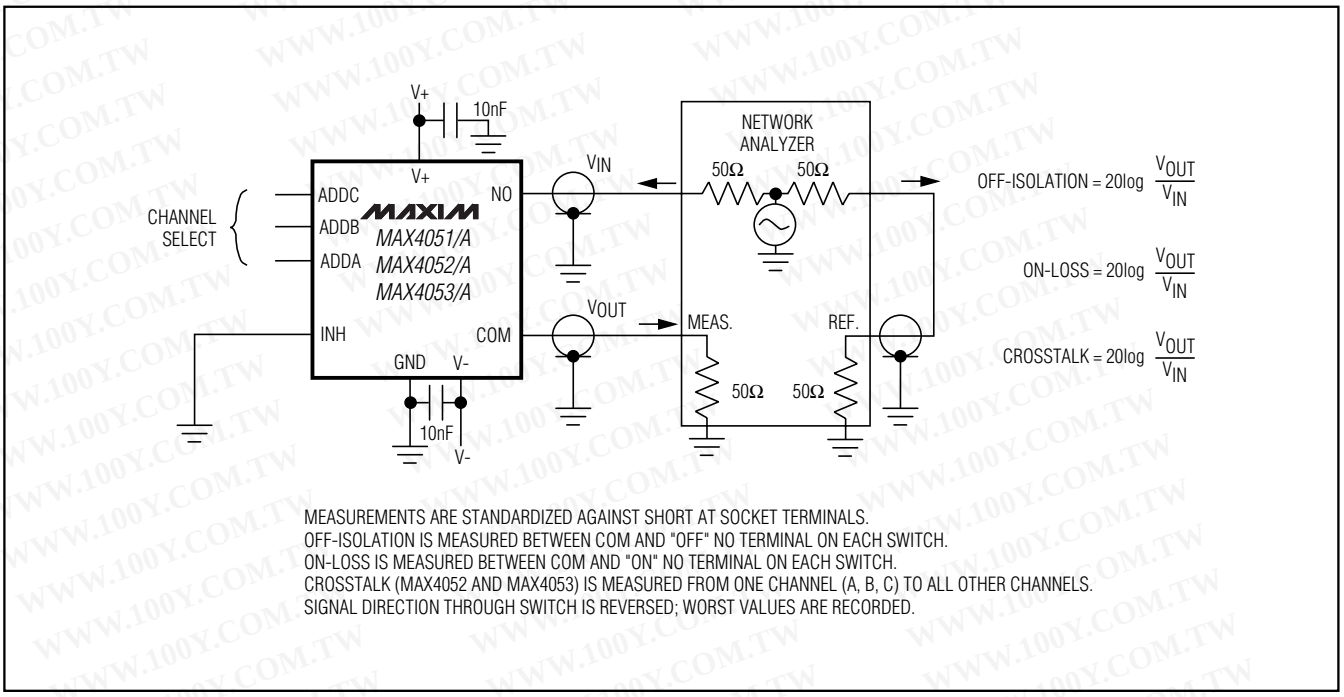


Figure 6. Off-Isolation, On-Loss, and Crosstalk

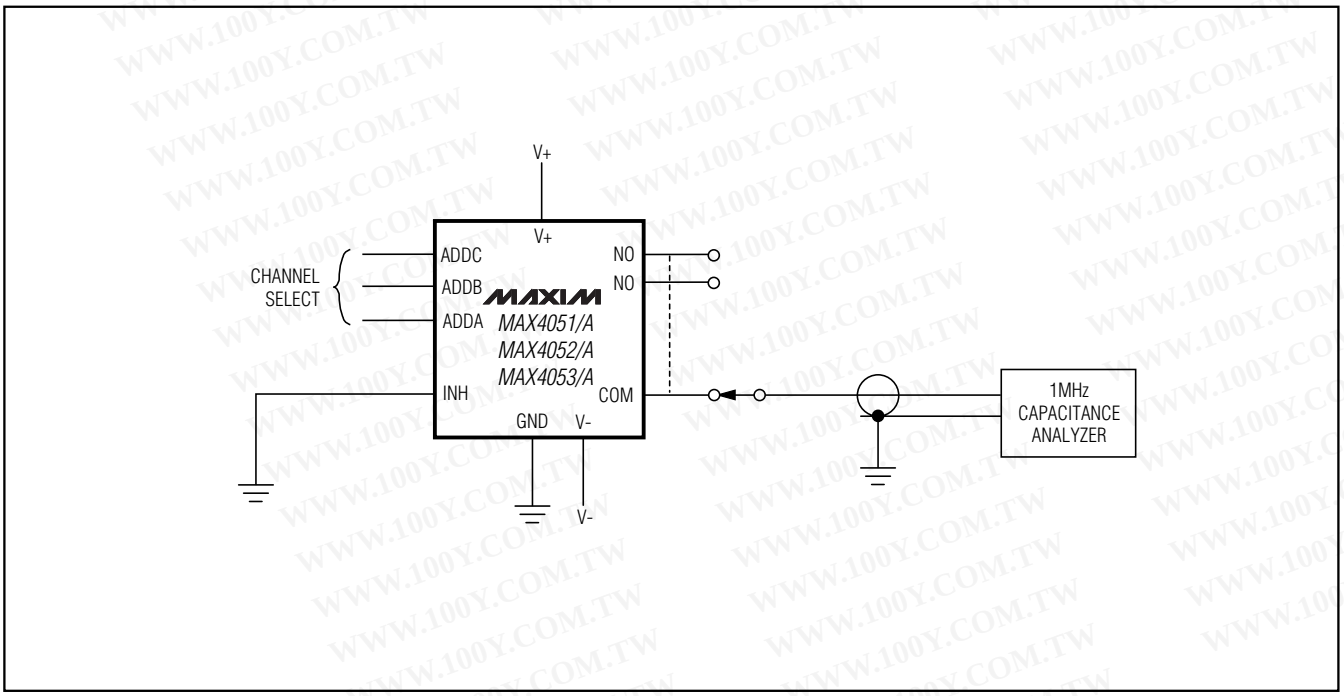


Figure 7. NO/COM Capacitance

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX4051AEPE	-40°C to +85°C	16 Plastic DIP
MAX4051AESE	-40°C to +85°C	16 Narrow SO
MAX4051AEEE	-40°C to +85°C	16 QSOP
MAX4051AMJE	-55°C to +125°C	16 CERDIP**
MAX4051CPE	0°C to +70°C	16 Plastic DIP
MAX4051CSE	0°C to +70°C	16 Narrow SO
MAX4051CEE	0°C to +70°C	16 QSOP
MAX4051C/D	0°C to +70°C	Dice*
MAX4051EPE	-40°C to +85°C	16 Plastic DIP
MAX4051ESE	-40°C to +85°C	16 Narrow SO
MAX4051EEE	-40°C to +85°C	16 QSOP
MAX4051MJE	-55°C to +125°C	16 CERDIP**
MAX4052ACPE	0°C to +70°C	16 Plastic DIP
MAX4052ACSE	0°C to +70°C	16 Narrow SO
MAX4052ACEE	0°C to +70°C	16 QSOP
MAX4052AEPE	-40°C to +85°C	16 Plastic DIP
MAX4052AESE	-40°C to +85°C	16 Narrow SO
MAX4052AEEE	-40°C to +85°C	16 QSOP
MAX4052AMJE	-55°C to +125°C	16 CERDIP**
MAX4052CPE	0°C to +70°C	16 Plastic DIP
MAX4052CSE	0°C to +70°C	16 Narrow SO
MAX4052CEE	0°C to +70°C	16 QSOP
MAX4052C/D	0°C to +70°C	Dice*
MAX4052EPE	-40°C to +85°C	16 Plastic DIP
MAX4052ESE	-40°C to +85°C	16 Narrow SO
MAX4052EEE	-40°C to +85°C	16 QSOP
MAX4052MJE	-55°C to +125°C	16 CERDIP**

PART	TEMP RANGE	PIN-PACKAGE
MAX4053ACPE	0°C to +70°C	16 Plastic DIP
MAX4053ACSE	0°C to +70°C	16 Narrow SO
MAX4053ACEE	0°C to +70°C	16 QSOP
MAX4053AEPE	-40°C to +85°C	16 Plastic DIP
MAX4053AESE	-40°C to +85°C	16 Narrow SO
MAX4053AEEE	-40°C to +85°C	16 QSOP
MAX4053AMJE	-55°C to +125°C	16 CERDIP**
MAX4053CPE	0°C to +70°C	16 Plastic DIP
MAX4053CSE	0°C to +70°C	16 Narrow SO
MAX4053CEE	0°C to +70°C	16 QSOP
MAX4053C/D	0°C to +70°C	Dice*
MAX4053EPE	-40°C to +85°C	16 Plastic DIP
MAX4053ESE	-40°C to +85°C	16 Narrow SO
MAX4053EEE	-40°C to +85°C	16 QSOP
MAX4053MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

Chip Information

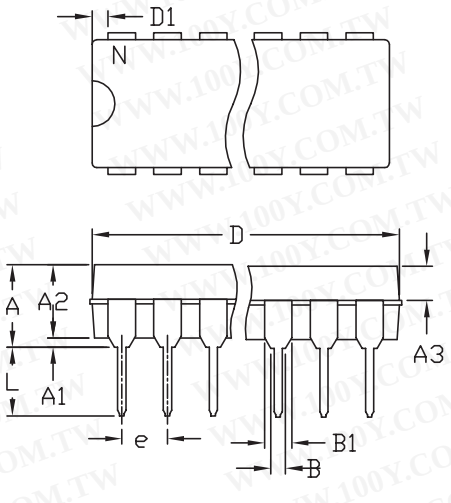
TRANSISTOR COUNT: 161
SUBSTRATE CONNECTED TO V+.

Low-Voltage, CMOS Analog Multiplexers/Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: PDIP .300" TITLE

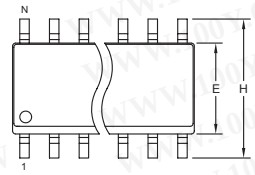
1/1

21-0043 D DOCUMENT CONTROL NUMBER REV

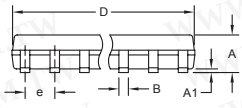
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS



TOP VIEW



FRONT VIEW

SIDE VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

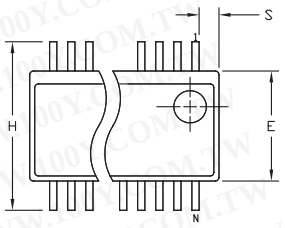
VARIATIONS:

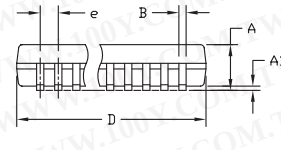
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

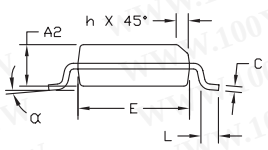
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, .150" SOIC
APPROVAL | DOCUMENT CONTROL NO. 21-0041 | REV. B | 1/1

QSOP.EPS







	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
A	.061	.068	1.55	1.73	
A1	.004	.0098	0.102	0.249	
A2	.055	.061	1.40	1.55	
B	.008	.012	0.20	0.30	
C	.0075	.0098	0.191	0.249	
D	SEE VARIATIONS				
E	.150	.157	3.81	3.99	
e	.025 BSC		0.635 BSC		
H	.230	.244	5.84	6.20	
h	.010	.016	0.25	0.41	
L	.016	.035	0.41	0.89	
N	SEE VARIATIONS				
α	0°	8°	0°	8°	

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV. E | 1/1