

TVP5147PFP

**NTSC/PAL/SECAM 2×10-Bit Digital Video
Decoder With Macrovision™ Detection, YPbPr
Inputs, and 5-Line Comb Filter**

Data Manual

勝特力材料 886-3-5753170
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1 Introduction

The TVP5147 device is a high-quality, single-chip digital video decoder that digitizes and decodes all popular baseband analog video formats into digital component video. The TVP5147 decoder supports the analog-to-digital (A/D) conversion of component YPbPr signals, as well as the A/D conversion and decoding of NTSC, PAL, and SECAM composite and S-video into component YCbCr. This decoder includes two 10-bit 30-MSPS A/D converters (ADCs). Preceding each ADC in the device, the corresponding analog channel contains an analog circuit that clamps the input to a reference voltage and applies a programmable gain and offset. A total of 10 video input terminals can be configured to a combination of YPbPr, CVBS, or S-video video inputs.

Composite or S-video signals are sampled at $2\times$ the square-pixel or ITU-R BT.601 clock frequency, line-locked alignment, and are then decimated to the $1\times$ pixel rate. CVBS decoding uses five-line adaptive comb filtering for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts. A chroma trap filter is also available. On CVBS and S-video inputs, the user can control video characteristics such as contrast, brightness, saturation, and hue via an I²C host port interface. Furthermore, luma peaking (sharpness) with programmable gain is included, as well as a patented chroma transient improvement (CTI) circuit.

The following output formats can be selected: 20-bit 4:2:2 YCbCr or 10-bit 4:2:2 YCbCr.

The TVP5147 decoder generates synchronization, blanking, field, active video window, horizontal and vertical syncs, clock, genlock (for downstream video encoder synchronization), host CPU interrupt and programmable logic I/O signals, in addition to digital video outputs.

The TVP5147 decoder includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor (VDP) slices, parses, and performs error checking on teletext, closed caption (CC), and other VBI data. A built-in FIFO stores up to 11 lines of teletext data, and with proper host port synchronization, full-screen teletext retrieval is possible. The TVP5147 decoder can pass through the output formatter $2\times$ sampled raw luma data for host-based VBI processing.

The main blocks of the TVP5147 decoder include:

- Robust sync detection for weak and noisy signals as well as VCR trick modes
- Y/C separation by 2-D 5-line adaptive comb or chroma trap filter
- Two 10-bit, 30-MSPS A/D converters with analog preprocessors [clamp and automatic gain control (AGC)]
- Analog video output
- Luminance processor
- Chrominance processor
- Clock/timing processor and power-down control
- Software-controlled power-saving standby mode
- Output formatter
- I²C host port interface
- VBI data processor
- Macrovision™ copy protection detection circuit (Type 1, 2, 3, and separate color stripe detection)
- 3.3-V tolerant digital I/O ports

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1.1 Detailed Functionality

- Two 30-MSPS, 10-bit A/D channels with programmable gain control
- Supports NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60) and SECAM (B, D, G, K, K1, L) CVBS, and S-video
- Supports analog component YPbPr video format with embedded sync
- 10 analog video input terminals for multisource connection
- Supports analog video output
- User-programmable video output formats
 - 10-bit ITU-R BT.656 4:2:2 YCbCr with embedded syncs
 - 10-bit 4:2:2 YCbCr with separate syncs
 - 20-bit 4:2:2 YCbCr with separate syncs
 - 2× sampled raw VBI data in active video during a vertical blanking period
 - Sliced VBI data during a vertical blanking period or active video period (full field mode)
- HSYNC/VSYNC outputs with programmable position, polarity, width, and field ID (FID) output
- Composite and S-video processing
 - Adaptive 2-D 5-line adaptive comb filter for composite video inputs; chroma-trap available
 - Automatic video standard detection (NTSC/PAL/SECAM) and switching
 - Luma-peaking with programmable gain
 - Patented chroma transient improvement (CTI)
 - Patented architecture for locking to weak, noisy, or unstable signals
 - Single 14.31818-MHz reference crystal for all standards (ITU-R.BT601 and square pixel sampling)
 - Line-locked internal pixel sampling clock generation with horizontal and vertical lock signal outputs
 - Genlock output RTC format for downstream video encoder synchronization
- Certified Macrovision™ copy protection detection

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- VBI data processor
 - Teletext (NABTS, WST)
 - CC and extended data service (EDS)
 - Wide screen signaling (WSS)
 - Copy generation management system (CGMS)
 - Video program system (VPS/PDC)
 - Vertical interval time code (VITC)
 - Gemstar™ 1×/2× mode
 - V-Chip decoding
 - Register readback of CC, WSS (CGMS), VPS/PDC, VITC and Gemstar 1×/2× sliced data
- I²C host port interface
- Reduced power consumption: 1.8-V digital core, 3.3-V for digital I/O, and 1.8-V/3.3 V analog core with power-save and power-down modes
- 80-terminal TQFP PowerPAD™ package

1.2 TVP5147 Applications

- DLP projectors
- Digital TV
- LCD TV/monitors
- DVD recorders
- PVR
- PC video cards
- Video capture/video editing
- Video conferencing

1.3 Related Products

- *TVP5146 NTSC/PAL/SECAM 2×10-Bit Digital Video Decoder With Macrovision™ Detection, YPbPr/RGB Inputs, and 5-Line Comb Filter (SLES084)*
- *TVP5150A Ultralow Power NTSC/PAL/SECAM Video Decoder With Robust Sync Detector (SLES087)*

1.4 Ordering Information

| T _A | PACKAGED DEVICES |
|----------------|--|
| | 80-TERMINAL PLASTIC FLAT-PACK PowerPAD™ PACKAGE |
| 0°C to 70°C | TVP5147PFP |

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1.5 Functional Block Diagram

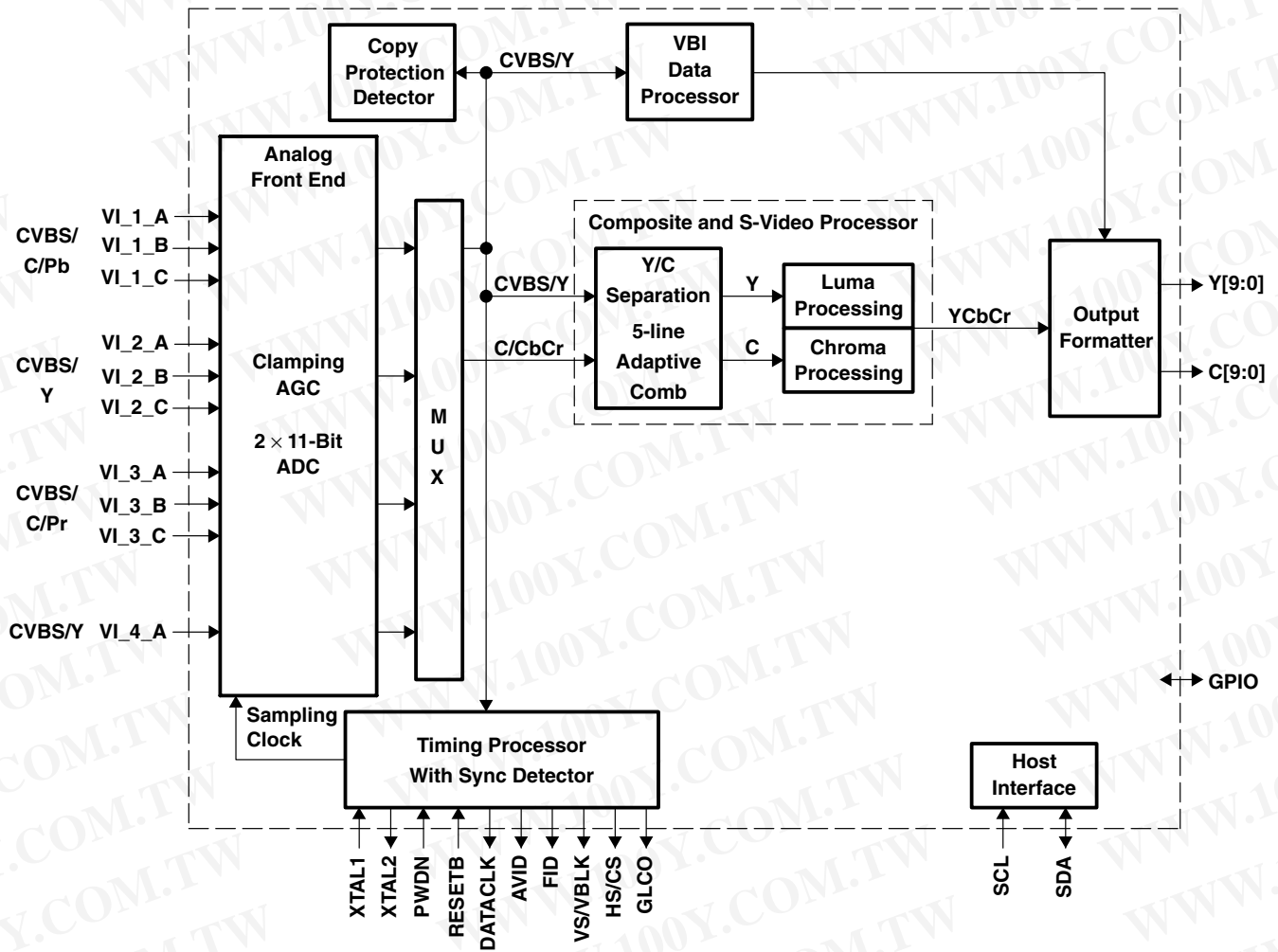


Figure 1-1. Functional Block Diagram

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1.6 Terminal Assignments

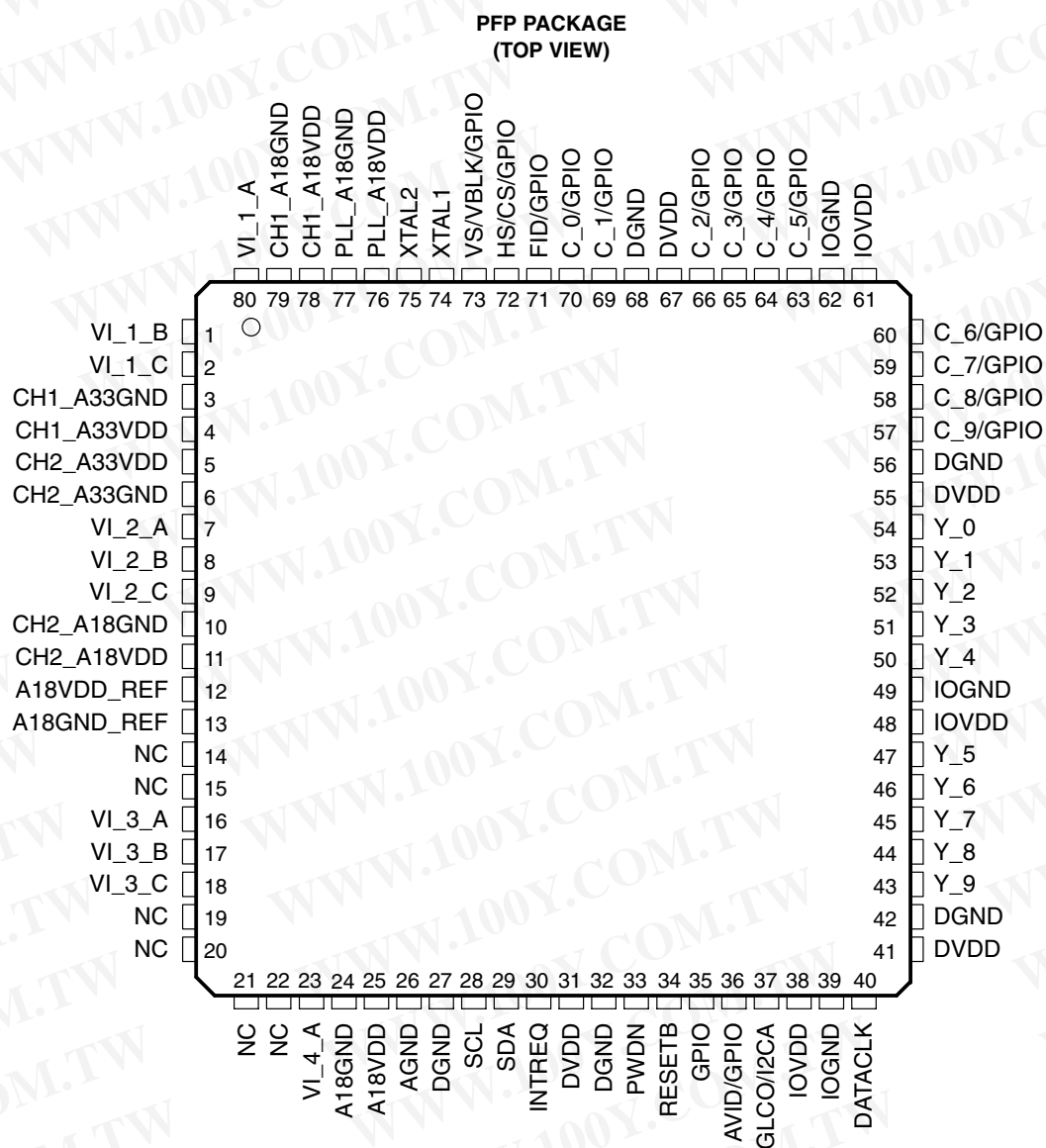


Figure 1–2. Terminal Assignments Diagram

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1.7 Terminal Functions

Table 1–1. Terminal Functions

| TERMINAL NAME | NUMBER | I/O | DESCRIPTION |
|------------------------------|--|-----|--|
| Analog Video | | | |
| VI_1_A | 80 | I/O | VI_1_A: Analog video input for CVBS/Pb/C or analog video output (see Section 2.11.58) |
| VI_1_B | 1 | I | VI_1_x: Analog video input for CVBS/Pb/C |
| VI_1_C | 2 | I | VI_2_x: Analog video input for CVBS/Y |
| VI_2_A | 7 | I | VI_3_x: Analog video input for CVBS/Pr/C |
| VI_2_B | 8 | I | VI_4_A: Analog video input for CVBS/Y |
| VI_2_C | 9 | I | Up to 10 composite, 4 S-video, and 2 composite or 3 component video inputs (or a combination thereof) can be supported. |
| VI_3_A | 16 | I | |
| VI_3_B | 17 | I | The inputs must be ac-coupled. The recommended coupling capacitor is 0.1 μ F. |
| VI_3_C | 18 | I | The possible input configurations are listed in the input select register at I ² C subaddress 00h (see Section 2.11.1). |
| VI_4_A | 23 | I | |
| Clock Signals | | | |
| DATACLK | 40 | O | Line-locked data output clock |
| XTAL1 | 74 | I | External clock reference input. It can be connected to an external oscillator with a 1.8-V compatible clock signal or a 14.31818-MHz crystal oscillator. |
| XTAL2 | 75 | O | External clock reference output. Not connected if XTAL1 is driven by an external single-ended oscillator. |
| Digital Video | | | |
| C_[9:0]/ GPIO[9:0] | 57, 58, 59, 60, 63, 64, 65, 66, 69, 70 | I/O | Digital video output of CbCr, C[9] is MSB and C[0] is LSB. Also, these terminals can be programmable general-purpose I/O. For the 8-bit mode, the two LSBs are ignored. Unused outputs can be left unconnected. The C_1 terminal needs a pulldown resistor (see Figure 5–1). |
| Y[9:0] | 43, 44, 45, 46, 47, 50, 51, 52, 53, 54 | O | Digital video output of Y/YCbCr, Y[9] is MSB and Y[0] is LSB. For the 8-bit mode, the two LSBs are ignored. Unused outputs can be left unconnected. |
| Miscellaneous Signals | | | |
| GPIO | 35 | I/O | Programmable general-purpose I/O |
| GLCO/I2CA | 37 | I/O | Genlock control output (GLCO) uses real time control (RTC) format. During reset, this terminal is an input used to program the I ² C address LSB. |
| INTREQ | 30 | O | Interrupt request |
| NC | 14, 15, 19, 20, 21, 22 | | Not connected. These terminals can be connected to power or ground (compatible with TVP5146 terminals), internally floating. |
| PWDN | 33 | I | Power down input: 1 = Power down 0 = Normal mode |
| RESETB | 34 | I | Reset input, active low (see Section 2.8) |
| Host Interface | | | |
| SCL | 28 | I | I ² C clock input |
| SDA | 29 | I/O | I ² C data bus |

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Table 1–1. Terminal Functions (Continued)

| TERMINAL NAME | NUMBER | I/O | DESCRIPTION |
|-----------------------|-----------------------|-----|--|
| Power Supplies | | | |
| AGND | 26 | | Analog ground. Connect to analog ground. |
| A18GND_REF | 13 | | Analog 1.8-V return |
| A18VDD_REF | 12 | | Analog power for reference 1.8 V |
| CH1_A18GND | 79 | | Analog 1.8-V return |
| CH2_A18GND | 10 | | |
| A18GND | 24 | | |
| CH1_A18VDD | 78 | | Analog power. Connect to 1.8 V. |
| CH2_A18VDD | 11 | | |
| A18VDD | 25 | | |
| CH1_A33GND | 3 | | Analog 3.3-V return |
| CH2_A33GND | 6 | | |
| CH1_A33VDD | 4 | | Analog power. Connect to 3.3 V. |
| CH2_A33VDD | 5 | | |
| DGND | 27, 32, 42, 56, 68 | | Digital return |
| DVDD | 31, 41, 55, 67 | | Digital power. Connect to 1.8 V. |
| IOGND | 39, 49, 62 | | Digital power return |
| IOVDD | 38, 48, 61 | | Digital power. Connect to 3.3 V or less for reduced noise. |
| PLL_A18GND | 77 | | Analog power return |
| PLL_A18VDD | 76 | | Analog power. Connect to 1.8 V. |
| Sync Signals | | | |
| HS/CS/GPIO | 72 | I/O | Horizontal sync output or digital composite sync output Programmable general-purpose I/O |
| VS/VBLK/GPIO | 73 | I/O | Vertical sync output (for modes with dedicated VSYNC) or VBLK output Programmable general-purpose I/O |
| FID/GPIO | 71 | I/O | Odd/even field indicator output. This terminal needs a pulldown resistor (see Figure 5–1). Programmable general-purpose I/O |
| AVID/GPIO | 36 | I/O | Active video indicator output Programmable general-purpose I/O |

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2 Functional Description

2.1 Analog Processing and A/D Converters

Figure 2–1 shows a functional diagram of the analog processors and A/D converters, which provide the analog interface to all video inputs. It accepts up to 10 inputs and performs source selection, video clamping, video amplification, A/D conversion, and gain and offset adjustments to center the digitized video signal. The TVP5147 supports one analog video output for the selected analog input video.

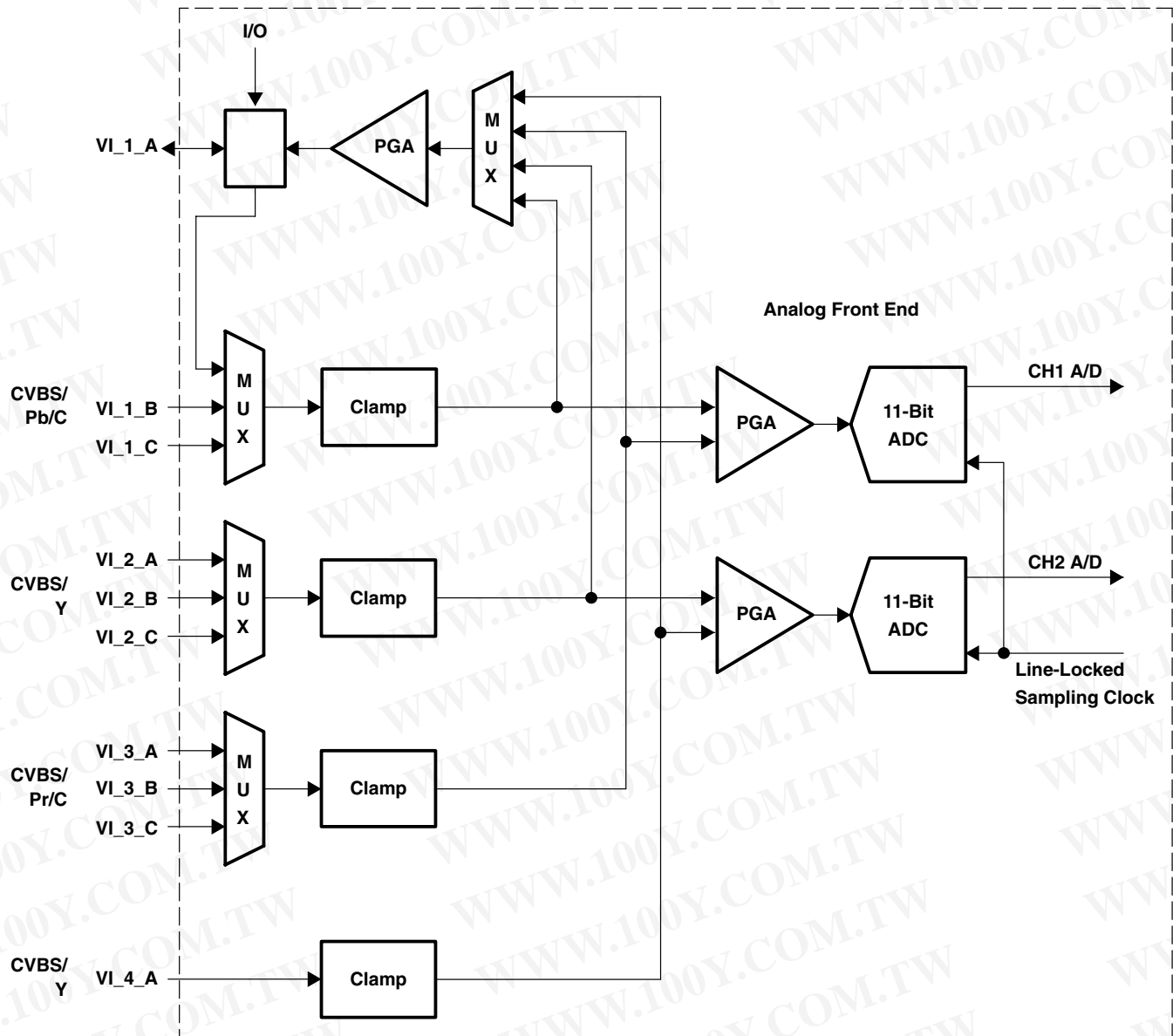


Figure 2–1. Analog Processors and A/D Converters

2.1.1 Video Input Switch Control

The TVP5147 decoder has two analog channels that accept up to 10 video inputs. The user can configure the internal analog video switches via the I²C interface. The 10 analog video inputs can be used for different input configurations, some of which are:

- Up to 10 selectable individual composite video inputs
- Up to four selectable S-video inputs
- Up to three selectable analog YPbPr video inputs and one CVBS input
- Up to two selectable analog YPbPr video inputs, two S-video inputs, and two CVBS inputs

The input selection is performed by the input select register at I²C subaddress 00h (see Section 2.11.1).

2.1.2 Analog Input Clamping

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video sync level to a fixed dc reference voltage. The selection between bottom and mid clamp is performed automatically by the TVP5147 decoder.

2.1.3 Automatic Gain Control

The TVP5147 decoder uses two programmable gain amplifiers (PGAs), one per channel. The PGA can scale a signal with a voltage-input compliance of 0.5-V_{PP} to 2.0-V_{PP} to a full-scale 10-bit A/D output code range. A 4-bit code sets the coarse gain with individual adjustment per channel. Minimum gain corresponds to a code 0x0 (2.0-V_{PP} full-scale input, -6-dB gain) while maximum gain corresponds to code 0xF (0.5 V_{PP} full scale, +6-dB gain). The TVP5147 decoder also has 12-bit fine gain controls for each channel and applies independently to coarse gain controls. For composite video, the input video signal amplitude can vary significantly from the nominal level of 1 V_{PP}. The TVP5147 decoder can adjust its PGA setting automatically: an automatic gain control (AGC) can be enabled and can adjust the signal amplitude such that the maximum range of the ADC is reached without clipping. Some nonstandard video signals contain peak white levels that saturate the ADC. In these cases, the AGC automatically cuts back gain to avoid clipping. If the AGC is on, then the TVP5147 decoder can read the gain currently being used.

The TVP5147 AGC comprises the front-end AGC before Y/C separation and the back-end AGC after Y/C separation. The back-end AGC restores the optimum system gain whenever an amplitude reference such as the composite peak (which is only relevant before Y/C separation) forces the front-end AGC to set the gain too low. The front-end and back-end AGC algorithms can use up to four amplitude references: sync height, color burst amplitude, composite peak, and luma peak.

The specific amplitude references being used by the front-end and back-end AGC algorithms can be independently controlled using the AGC white peak processing register located at subaddress 74h. The TVP5147 gain increment speed and gain increment delay can be controlled using the AGC increment speed register located at subaddress 78h and the AGC increment delay register located at subaddress 79h.

2.1.4 Analog Video Output

One of the analog input signals is available at the analog video output terminal, which is shared with input selected by I²C registers. The signal at this terminal must be buffered by a source follower. The nominal output voltage is 2 V p-p, thus the signal can be used to drive a 75-Ω line. The magnitude is maintained with an AGC in 16 steps controlled by the TVP5147 decoder. In order to use this function, terminal VI_1_A must be set as an output terminal. The input mode selection register also selects an active analog output signal.

2.1.5 A/D Converters

All ADCs have a resolution of 10 bits and can operate up to 30 MSPS. All A/D channels receive an identical clock from the on-chip phase-locked loop (PLL) at a frequency between 24 MHz and 30 MHz. All ADC reference voltages are generated internally.

2.2 Digital Video Processing

Figure 2–2 is a block diagram of the TVP5147 digital video decoder processing. This block receives digitized video signals from the ADCs and performs composite processing for CVBS and S-video inputs and YCbCr signal enhancements for CVBS and S-video inputs. It also generates horizontal and vertical syncs and other output control signals such as genlock for CVBS and S-video inputs. Additionally, it can provide field identification, horizontal and vertical lock, vertical blanking, and active video window indication signals. The digital data output can be programmed to two formats: 20-bit 4:2:2 with external syncs or 10-bit 4:2:2 with embedded/separate syncs. The circuit detects pseudosync pulses, AGC pulses, and color striping in Macrovision-encoded copy-protected material. Information present in the VBI interval can be retrieved and either inserted in the ITU-R BT.656 output as ancillary data or stored in internal FIFO and/or registers for retrieval via the host port interface.

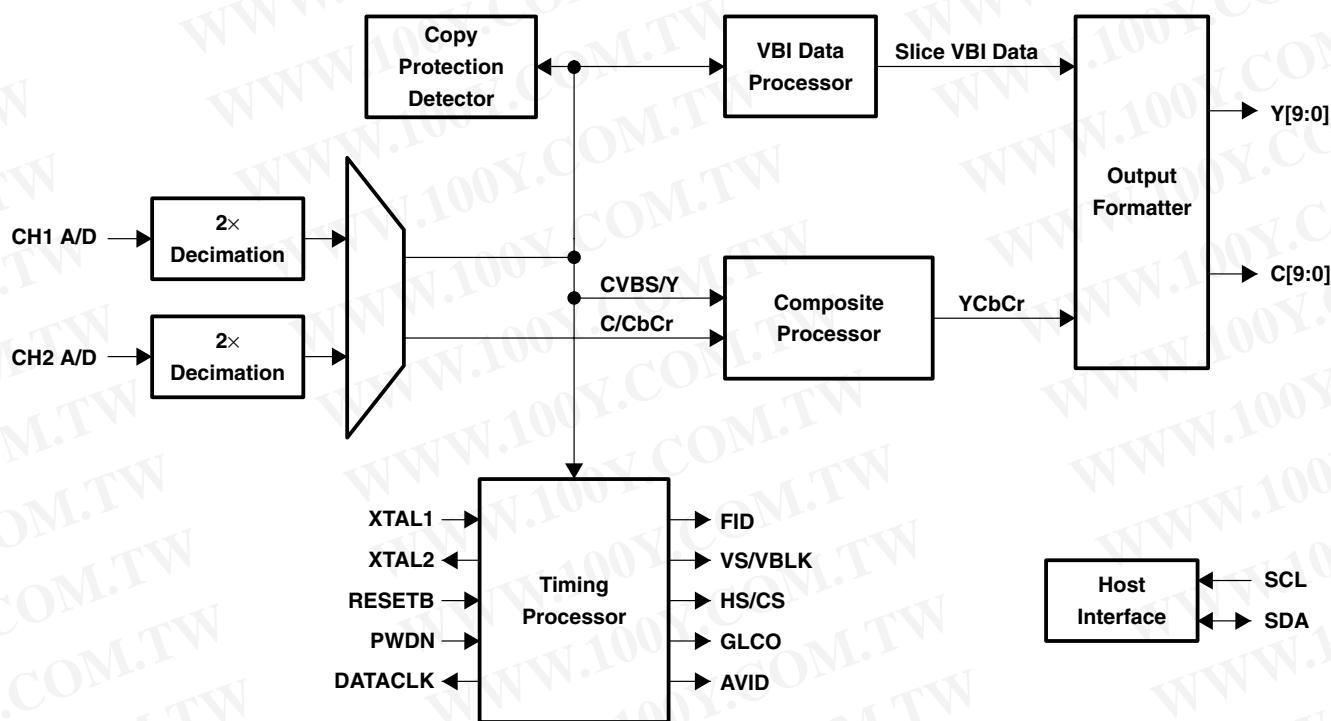


Figure 2–2. Digital Video Processing Block Diagram

2.2.1 2× Decimation Filter

All input signals are typically oversampled by a factor of 2 (27 MHz). The A/D outputs initially pass through decimation filters that reduce the data rate to 1× the pixel rate. The decimation filter is a half-band filter. Oversampling and decimation filtering can effectively increase the overall signal-to-noise ratio by 3 dB.

2.2.2 Composite Processor

Figure 2–3 is a block diagram of the TVP5147 digital composite video processing circuit. This processing circuit receives a digitized composite or S-video signal from the ADCs and performs Y/C separation (bypassed for S-video input), chroma demodulation for PAL/NTSC and SECAM, and YUV signal enhancements.

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The 10-bit composite video is multiplied by the subcarrier signals in the quadrature demodulator to generate color difference signals U and V. The U and V signals are then sent to low-pass filters to achieve the desired bandwidth. An adaptive 5-line comb filter separates UV from Y based on the unique property of color phase shifts from line to line. The chroma is remodulated through a quadrature modulator and subtracted from line-delayed composite video to generate luma. This form of Y/C separation is completely complementary, thus there is no loss of information. However, in some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter is also available in the luma path. Contrast, brightness, sharpness, hue, and saturation controls are programmable through the host port.

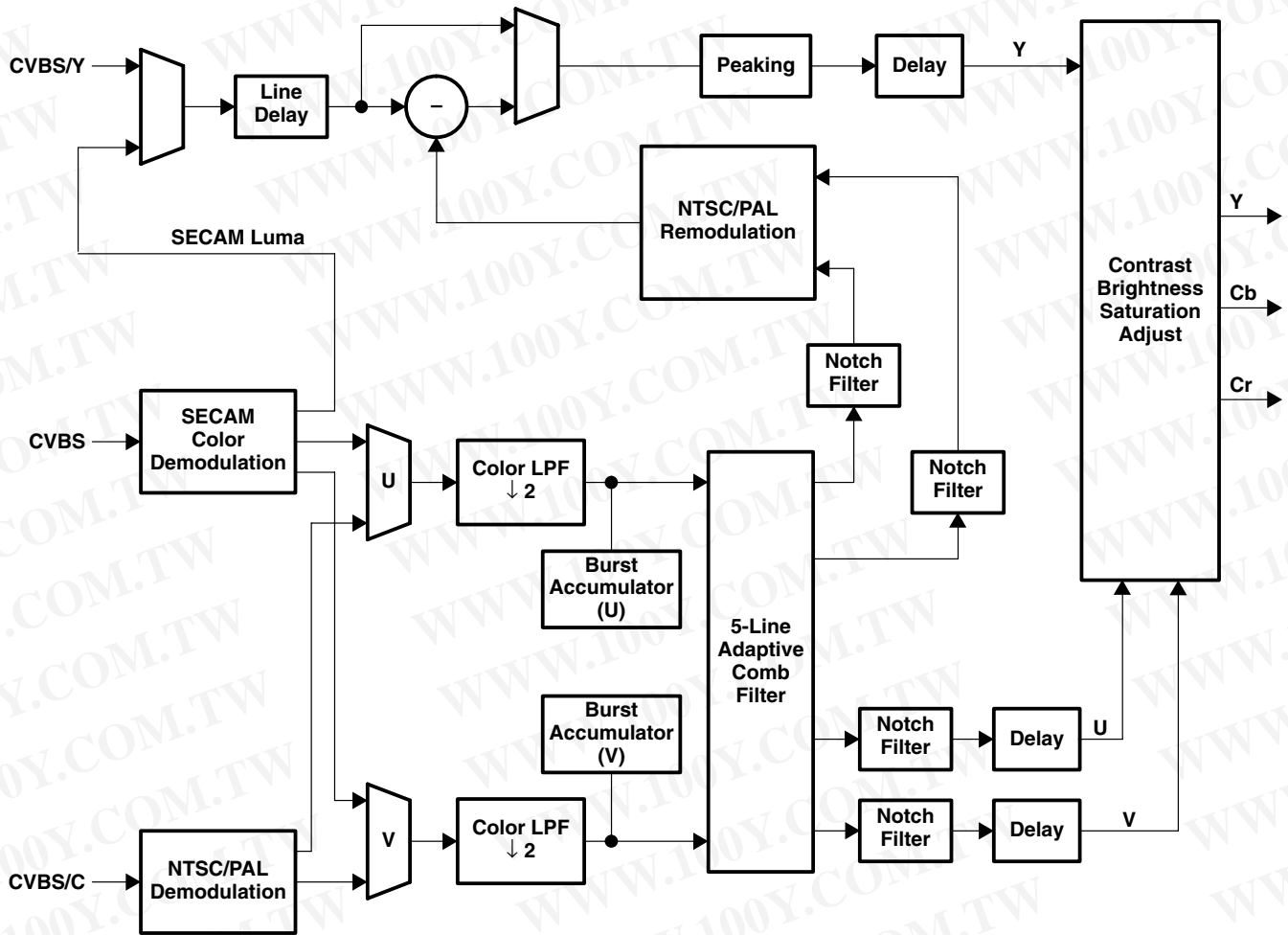


Figure 2-3. Composite and S-Video Processing Block Diagram

2.2.2.1 Color Low-Pass Filter

High filter bandwidth preserves sharp color transitions and produces crisp color boundaries. However, for nonstandard video sources that have asymmetrical U and V side bands, it is desirable to limit the filter bandwidth to avoid UV crosstalk. The color low-pass filter bandwidth is programmable to enable one of the three notch filters. Figure 2-4 through Figure 2-7 represent the frequency responses of the wideband color low-pass filters.

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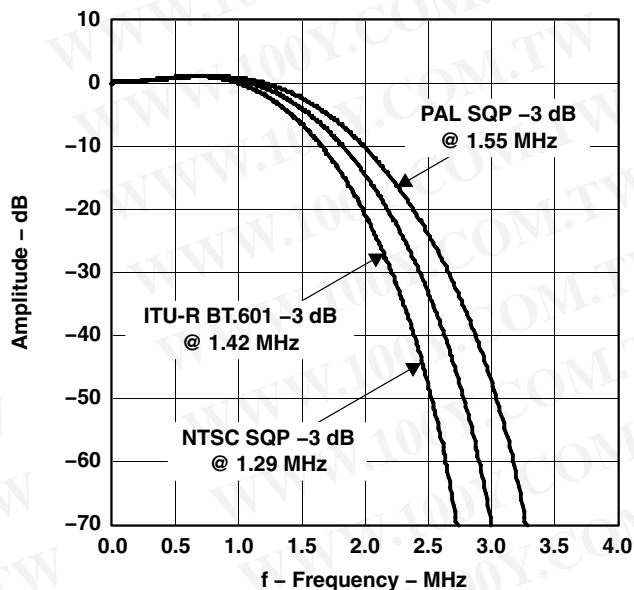


Figure 2-4. Color Low-Pass Filter Frequency Response

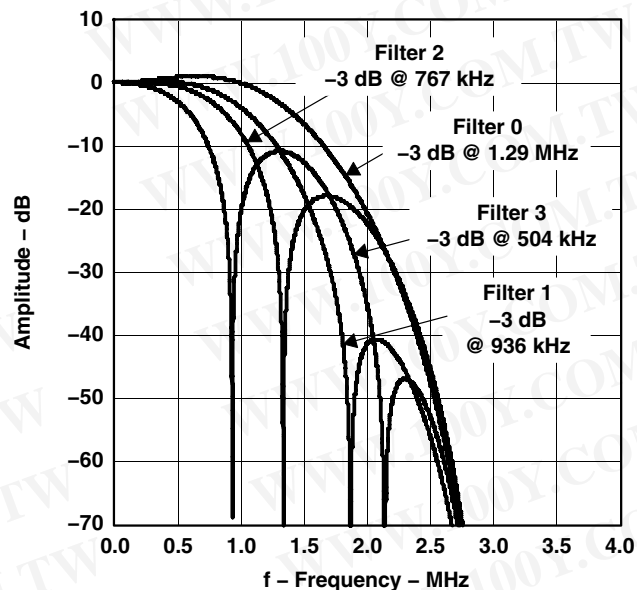


Figure 2-5. Color Low-Pass Filter With Filter Frequency Response, NTSC Square Pixel Sampling

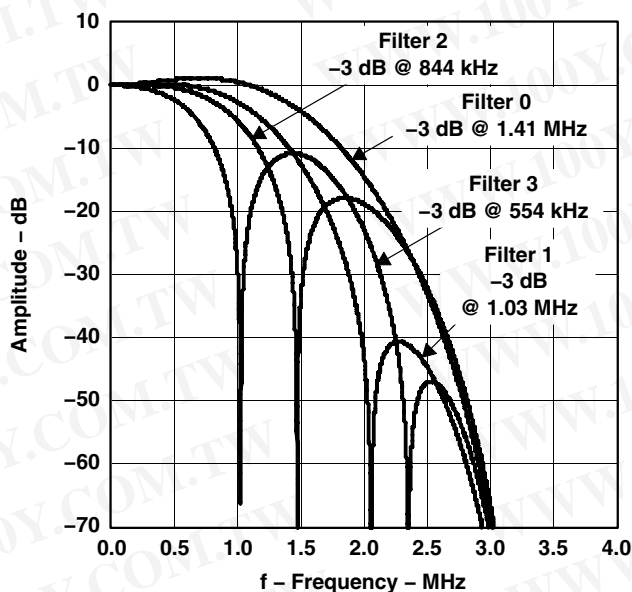


Figure 2-6. Color Low-Pass Filter With Filter Characteristics, NTSC/PAL ITU-R BT.601 Sampling

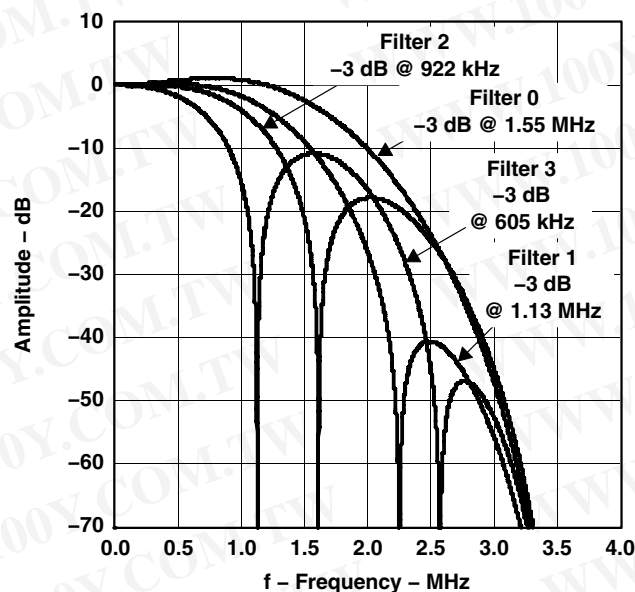


Figure 2-7. Color Low-Pass Filter With Filter Characteristics, PAL Square Pixel Sampling

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2.2.2.2 Y/C Separation

Y/C separation can be done using adaptive 5-line (5-H delay) comb filters or a chroma trap filter. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used which are shown in Figure 2–8 through Figure 2–11. TI's patented adaptive comb filter algorithm reduces artifacts such as hanging dots at color boundaries. It detects and properly handles false colors in high-frequency luminance images such as a multiburst pattern or circle pattern.

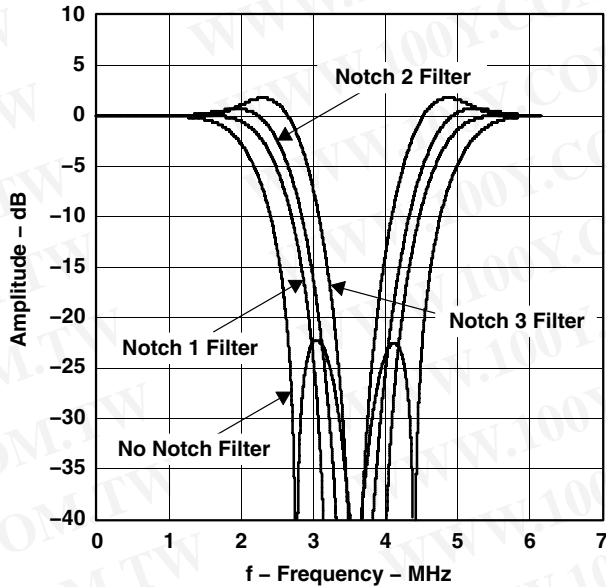


Figure 2–8. Chroma Trap Filter Frequency Response, NTSC Square Pixel Sampling

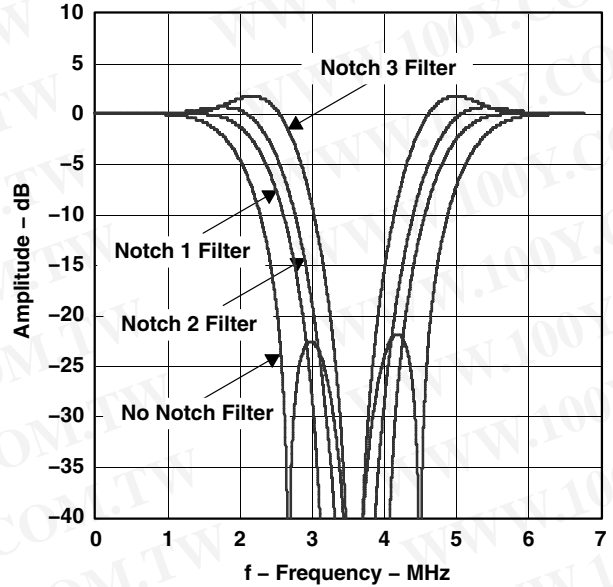


Figure 2–9. Chroma Trap Filter Frequency Response, NTSC ITU-R BT.601 Sampling

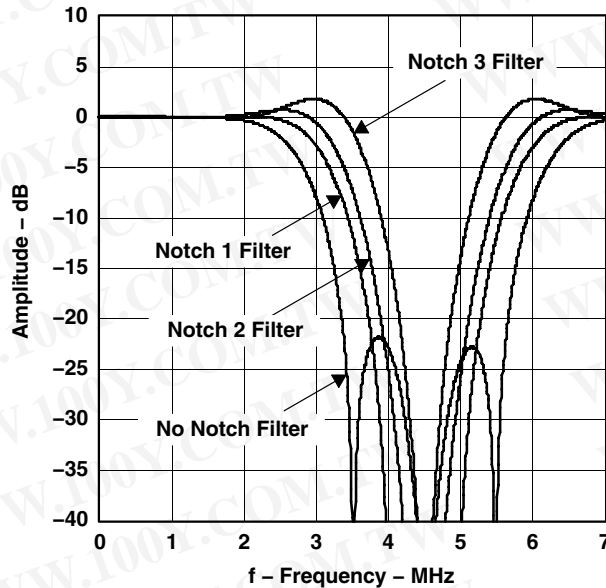


Figure 2–10. Chroma Trap Filter Frequency Response, PAL ITU-R BT.601 Sampling

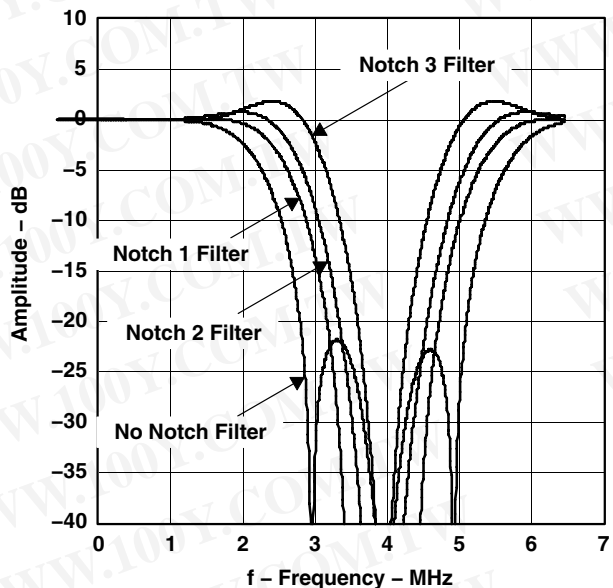


Figure 2–11. Chroma Trap Filter Frequency Response, PAL Square Pixel Sampling

2.2.3 Luminance Processing

The digitized composite video signal passes through either a luminance comb filter or a chroma trap filter, either of which removes chrominance information from the composite signal to generate a luminance signal. The luminance signal is then fed into the input of a peaking circuit. Figure 2–12 illustrates the basic functions of the luminance data path. In the case of S-video, the luminance signal bypasses the comb filter or chroma trap filter and is fed directly to the circuit. A peaking filter (edge enhancer) amplifies high-frequency components of the luminance signal. Figure 2–13, Figure 2–14, and Figure 2–15 show the characteristics of the peaking filter at four different gain settings that are user-programmable via the I²C interface.

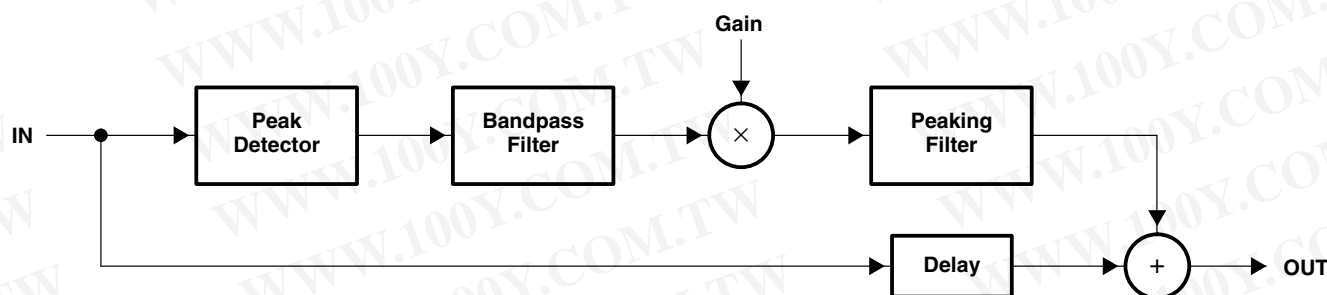


Figure 2–12. Luminance Edge-Enhancer Peaking Block Diagram

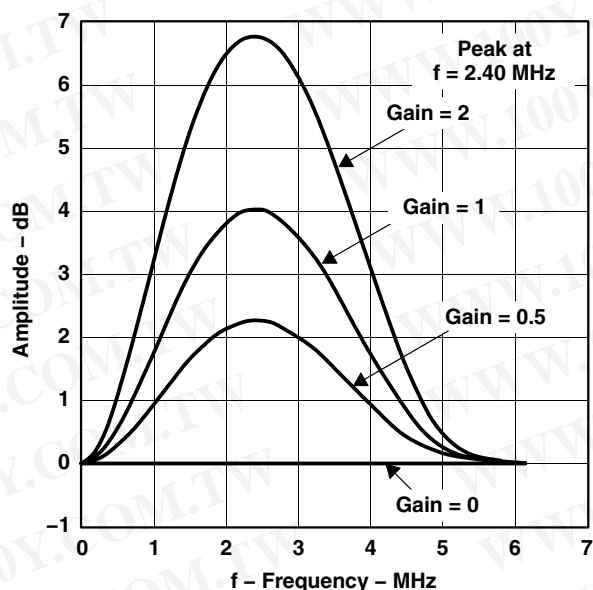


Figure 2–13. Peaking Filter Response, NTSC Square Pixel Sampling

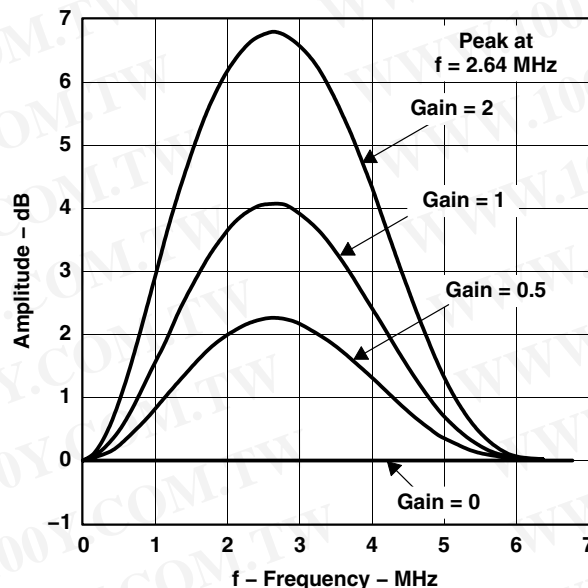


Figure 2–14. Peaking Filter Response, NTSC/PAL ITU-R BT.601 Sampling

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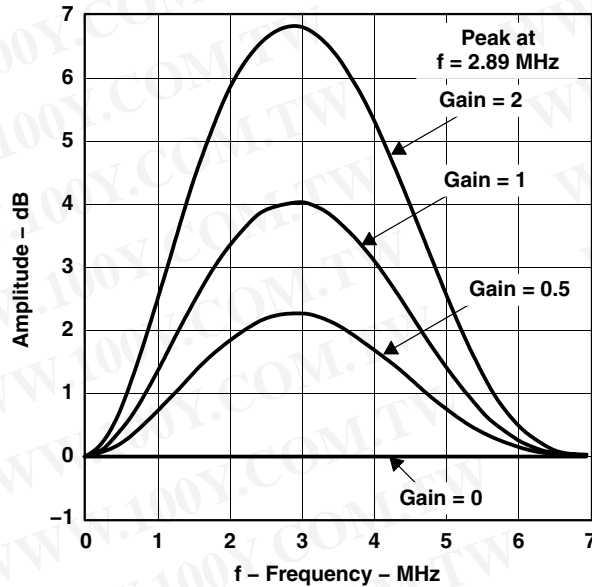


Figure 2–15. Peaking Filter Response, PAL Square Pixel Sampling

2.2.3.1 Color Transient Improvement

Color transient improvement (CTI) enhances horizontal color transients. The color difference signal transition points are maintained, but the edges are enhanced for signals which have bandwidth-limited color components.

2.3 Clock Circuits

An internal line-locked PLL generates the system and pixel clocks. A 14.318-MHz clock is required to drive the PLL. This can be input to the TVP5147 decoder at the 1.8-V level on terminal 74 (XTAL1), or a crystal of 14.318-MHz fundamental resonant frequency can be connected across terminals 74 and 75 (XTAL2). If a parallel resonant circuit is used as shown in Figure 2–16, then the external capacitors must have the following relationship:

$$C_{L1} = C_{L2} = 2C_L - C_{STRAY}$$

where C_{STRAY} is the terminal capacitance with respect to ground. Figure 2–16 shows the reference clock configurations. The TVP5147 decoder generates the DATACLK signal used for clocking data.

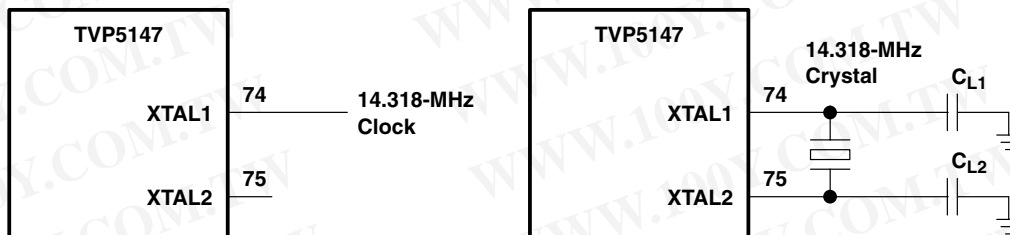


Figure 2–16. Reference Clock Configurations

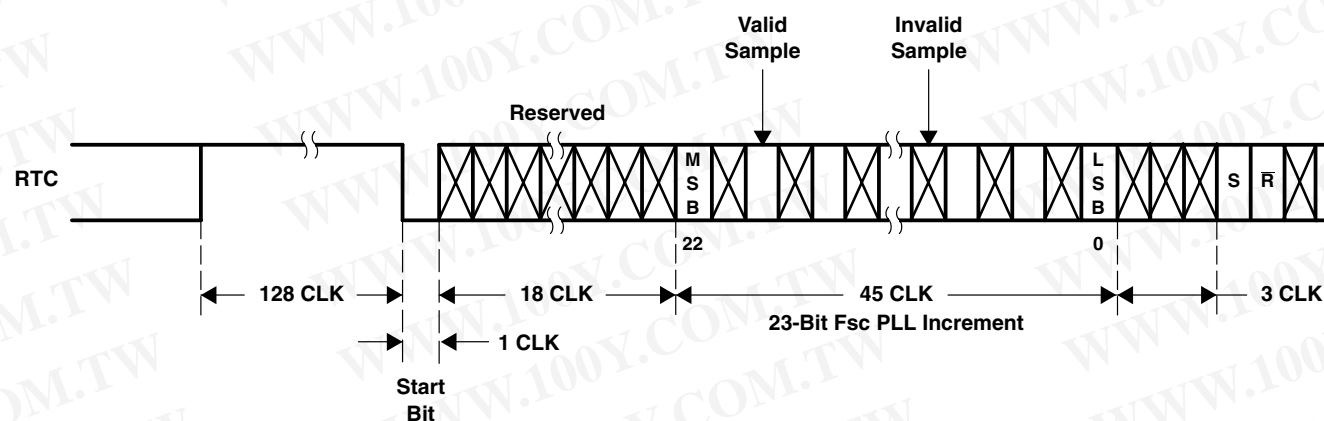
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2.4 Real-Time Control (RTC)

Although the TVP5147 decoder is a line-locked system, the color burst information is used to determine accurately the color subcarrier frequency and phase. This ensures proper operation with nonstandard video signals that do not follow exactly the required frequency multiple between color subcarrier frequency and video line frequency. The frequency control word of the internal color subcarrier PLL and the subcarrier reset bit are transmitted via terminal 37 (GLCO) for optional use in an end system (for example, by a video encoder). The frequency control word is a 23-bit binary number. The instantaneous frequency of the color subcarrier can be calculated using the following equation:

$$F_{PLL} = \frac{F_{ctrl}}{2^{23}} \times F_{sclk}$$

where F_{PLL} is the frequency of the subcarrier PLL, F_{ctrl} is the 23-bit PLL frequency control word, and F_{sclk} is two times the pixel frequency. This information can be generated on the GLCO terminal. Figure 2–17 shows the detailed timing diagram.



NOTE: RTC reset bit (R) is active-low, Sequence bit (S) PAL: 1 = (R-Y) line normal, 0 = (R-Y) line inverted, NTSC: 1 = no change

Figure 2–17. RTC Timing

2.5 Output Formatter

The output formatter sets how the data is formatted for output on the TVP5147 output buses. Table 2–1 shows the available output modes.

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Table 2–1. Output Format

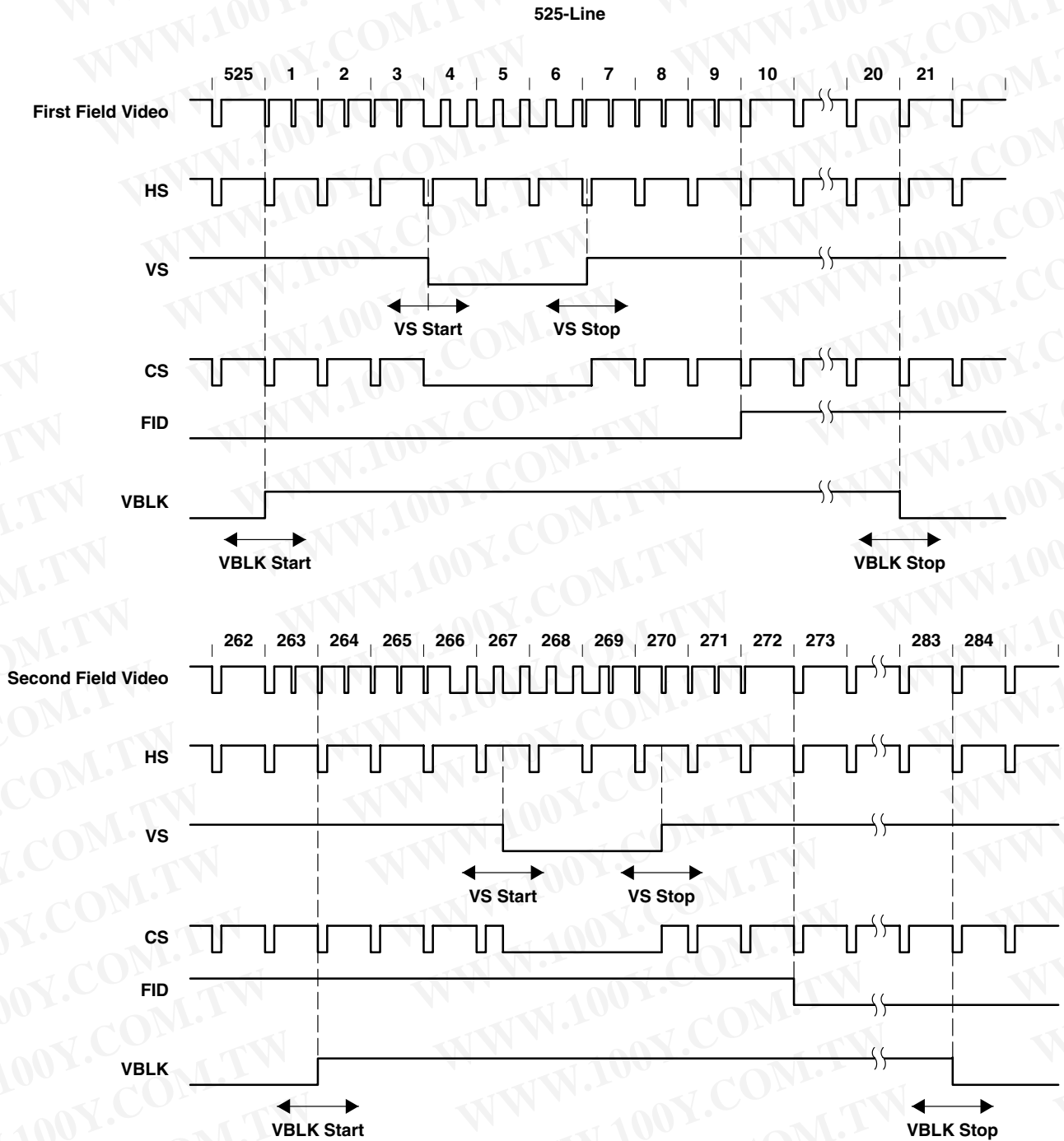
| TERMINAL NAME | TERMINAL NUMBER | 10-Bit 4:2:2 YCbCr | 20-Bit 4:2:2 YCbCr |
|---------------|-----------------|--------------------|--------------------|
| Y_9 | 43 | Cb9, Y9, Cr9 | Y9 |
| Y_8 | 44 | Cb8, Y8, Cr8 | Y8 |
| Y_7 | 45 | Cb7, Y7, Cr7 | Y7 |
| Y_6 | 46 | Cb6, Y6, Cr6 | Y6 |
| Y_5 | 47 | Cb5, Y5, Cr5 | Y5 |
| Y_4 | 50 | Cb4, Y4, Cr4 | Y4 |
| Y_3 | 51 | Cb3, Y3, Cr3 | Y3 |
| Y_2 | 52 | Cb2, Y2, Cr2 | Y2 |
| Y_1 | 53 | Cb1, Y1, Cr1 | Y1 |
| Y_0 | 54 | Cb0, Y0, Cr0 | Y0 |
| C_9 | 57 | | Cb9, Cr9 |
| C_8 | 58 | | Cb8, Cr8 |
| C_7 | 59 | | Cb7, Cr7 |
| C_6 | 60 | | Cb6, Cr6 |
| C_5 | 63 | | Cb5, Cr5 |
| C_4 | 64 | | Cb4, Cr4 |
| C_3 | 65 | | Cb3, Cr3 |
| C_2 | 66 | | Cb2, Cr2 |
| C_1 | 69 | | Cb1, Cr1 |
| C_0 | 70 | | Cb0, Cr0 |

Table 2–2. Summary of Line Frequencies, Data Rates, and Pixel/Line Counts

| STANDARDS | PIXELS PER LINE | ACTIVE PIXELS PER LINE | LINES PER FRAME | PIXEL FREQUENCY (MHz) | COLOR SUBCARRIER FREQUENCY (MHz) | HORIZONTAL LINE RATE (kHz) |
|------------------------|-----------------|------------------------|-----------------|-----------------------|----------------------------------|----------------------------|
| 601 sampling | | | | | | |
| NTSC-J, M | 858 | 720 | 525 | 13.5 | 3.579545 | 15.73426 |
| NTSC-4.43 | 858 | 720 | 525 | 13.5 | 4.43361875 | 15.73426 |
| PAL-M | 858 | 720 | 525 | 13.5 | 3.57561149 | 15.73426 |
| PAL-60 | 858 | 720 | 525 | 13.5 | 4.43361875 | 15.73426 |
| PAL-B, D, G, H, I | 864 | 720 | 625 | 13.5 | 4.43361875 | 15.625 |
| PAL-N | 864 | 720 | 625 | 13.5 | 4.43361875 | 15.625 |
| PAL-Nc | 864 | 720 | 625 | 13.5 | 3.58205625 | 15.625 |
| SECAM | 864 | 720 | 625 | 13.5 | Dr = 4.406250 Db = 4.250000 | 15.625 |
| Square sampling | | | | | | |
| NTSC-J, M | 780 | 640 | 525 | 12.2727 | 3.579545 | 15.73426 |
| NTSC-4.43 | 780 | 640 | 525 | 12.2727 | 4.43361875 | 15.73426 |
| PAL-M | 780 | 640 | 525 | 12.2727 | 3.57561149 | 15.73426 |
| PAL-60 | 780 | 640 | 525 | 12.2727 | 4.43361875 | 15.73426 |
| PAL-B, D, G, H, I | 944 | 768 | 625 | 14.75 | 4.43361875 | 15.625 |
| PAL-N | 944 | 768 | 625 | 14.75 | 4.43361875 | 15.625 |
| PAL-Nc | 944 | 768 | 625 | 14.75 | 3.58205625 | 15.625 |
| SECAM | 944 | 768 | 625 | 14.75 | Dr = 4.406250 Db = 4.250000 | 15.625 |

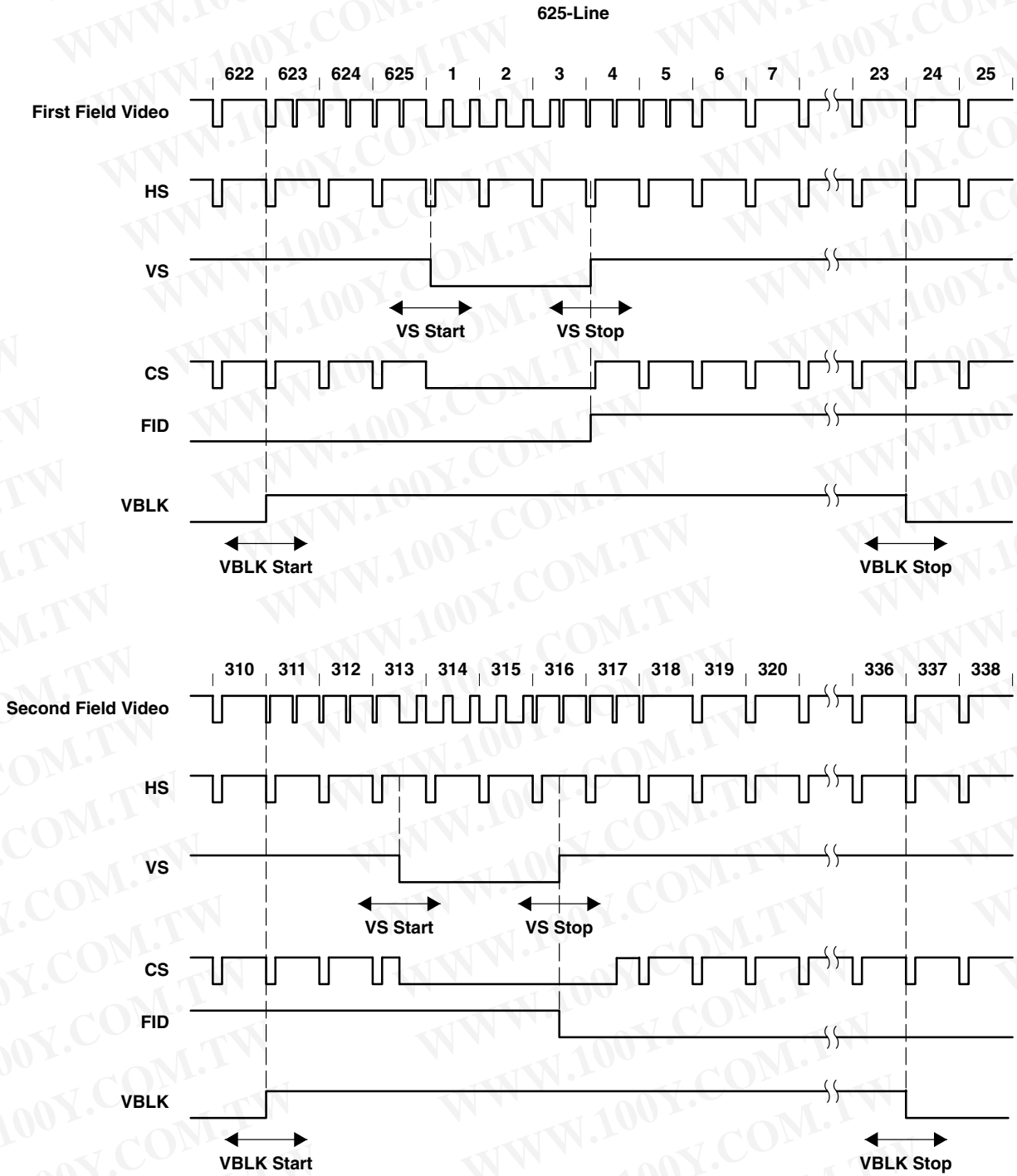
2.5.1 Separate Syncs

VS, HS, and VBLK are independently software programmable to a 1× pixel count. This allows any possible alignment to the internal pixel count and line count. The default settings for 525-line and 625-line video outputs are given as examples below. FID changes at the same transient time when the trailing edge of vertical sync occurs. The polarity of FID is programmable by an I²C interface.



NOTE: Line numbering conforms to ITU-R BT.470

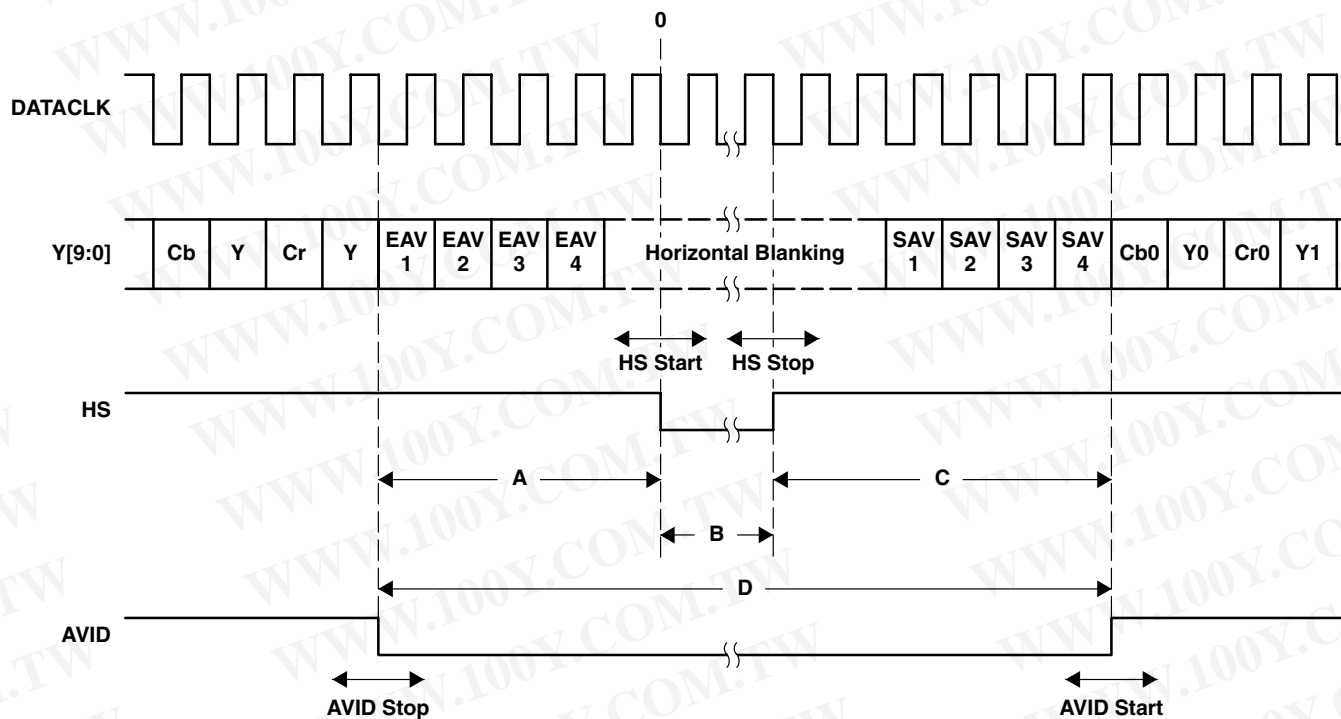
Figure 2-18. Vertical Synchronization Signals for 525-Line System



NOTE: Line numbering conforms to ITU-R BT.470

Figure 2–19. Vertical Synchronization Signals for 625-Line System

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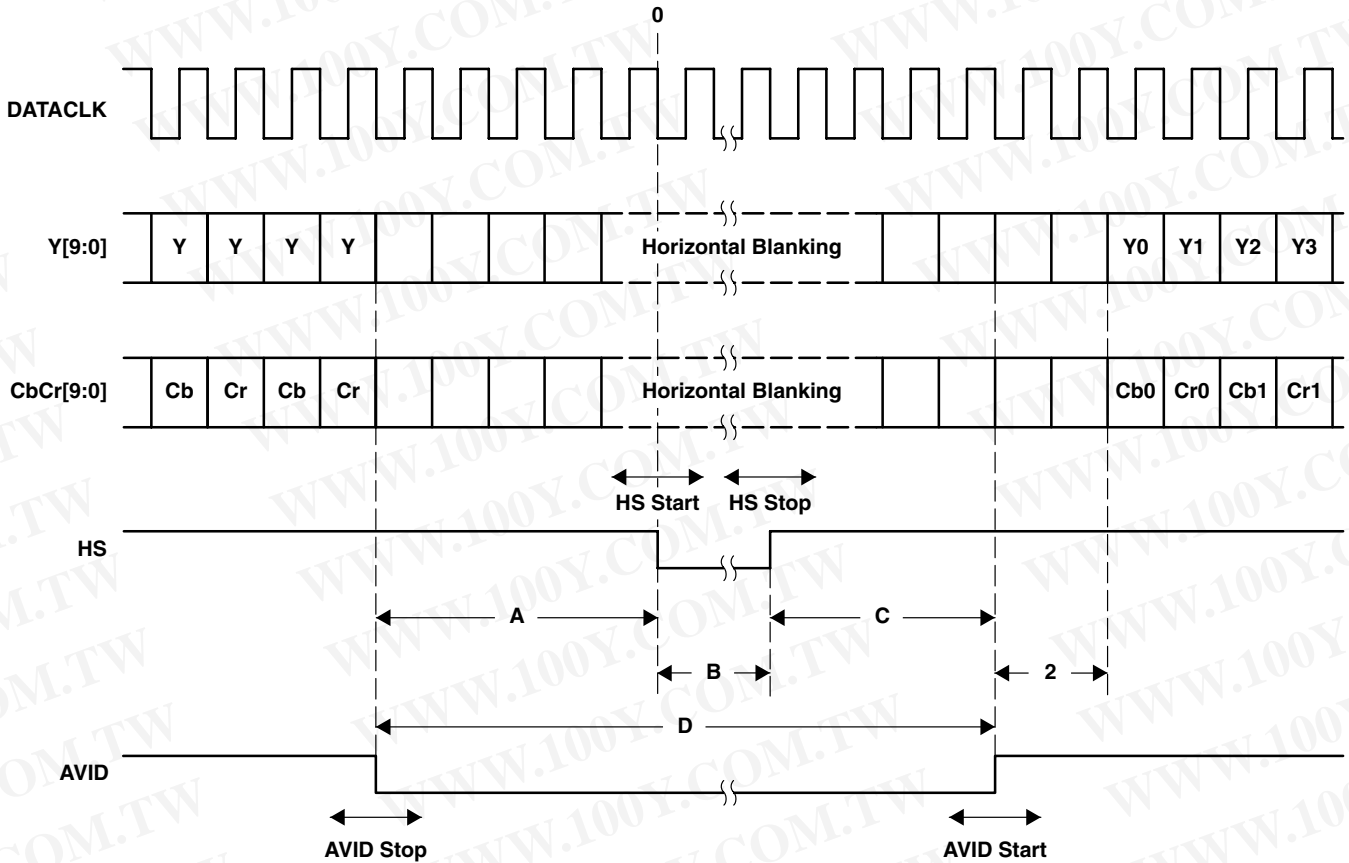
DATACLK = 2x Pixel Clock

| Mode | A | B | C | D |
|----------|-----|-----|----|-----|
| NTSC 601 | 106 | 128 | 42 | 276 |
| PAL 601 | 112 | 128 | 48 | 288 |
| NTSC Sqp | 108 | 128 | 44 | 280 |
| PAL Sqp | 144 | 128 | 80 | 352 |

NOTE: ITU-R BT.656 10-bit 4:2:2 timing with 2x pixel clock reference

Figure 2–20. Horizontal Synchronization Signals for 10-Bit 4:2:2 Mode

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NOTE: AVID rising edge occurs 4 clock cycles early.

DATACLK = 1× Pixel Clock

| Mode | A | B | C | D |
|----------|----|----|----|-----|
| NTSC 601 | 53 | 64 | 19 | 136 |
| PAL 601 | 56 | 64 | 22 | 142 |
| NTSC Sqp | 54 | 64 | 20 | 138 |
| PAL Sqp | 72 | 64 | 38 | 174 |

NOTE: 20-bit 4:2:2 timing with 1× pixel clock reference

Figure 2–21. Horizontal Synchronization Signals for 20-Bit 4:2:2 Mode

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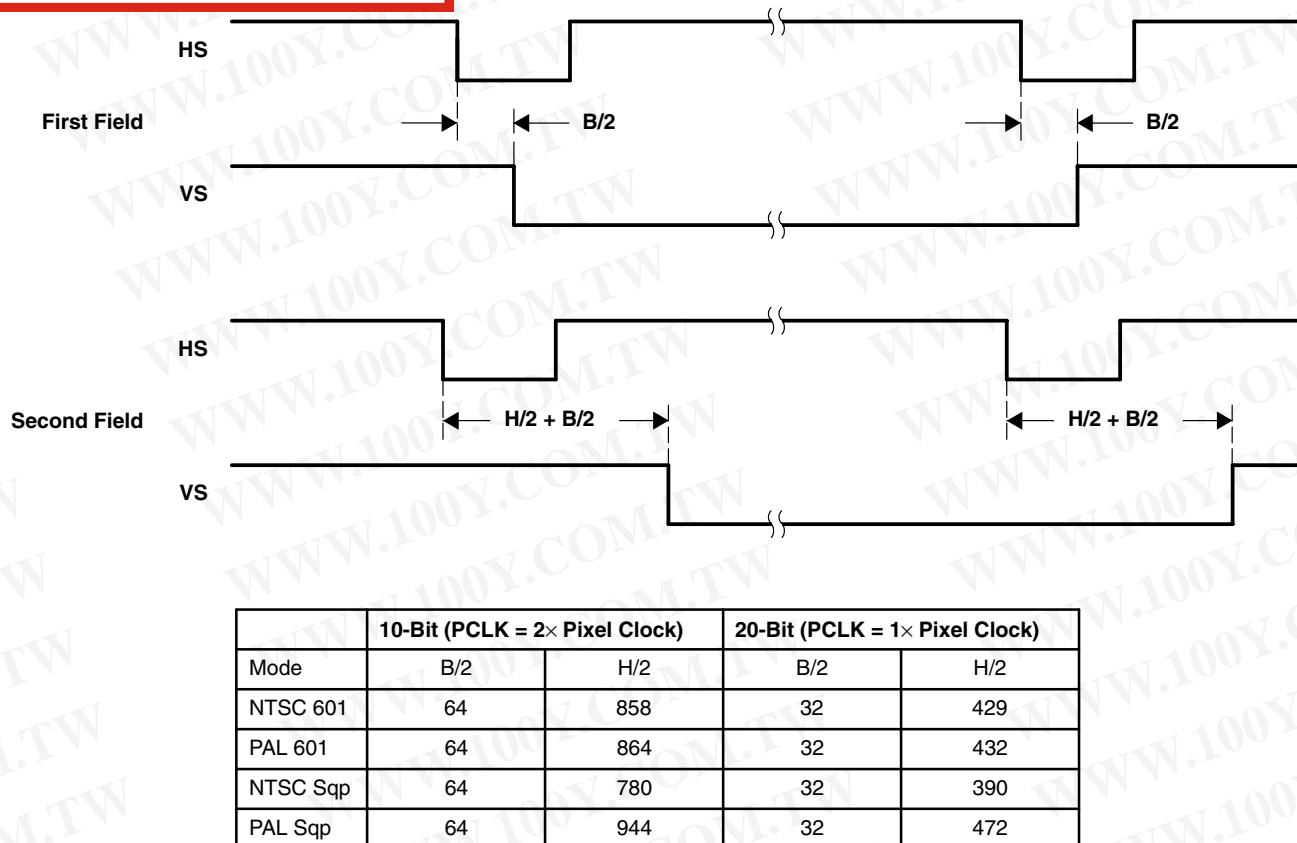


Figure 2–22. VSYNC Position With Respect to HSYNC

2.5.2 Embedded Syncs

Standards with embedded syncs insert the SAV and EAV codes into the data stream on the rising and falling edges of AVID. These codes contain the V and F bits which also define vertical timing. Table 2–3 gives the format of the SAV and EAV codes.

H equals 1 always indicates EAV. H equals 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard.

The P bits are protection bits:

$$P3 = V \text{ xor } H; P2 = F \text{ xor } H; P1 = F \text{ xor } V; P0 = F \text{ xor } V \text{ xor } H$$

Table 2–3. EAV and SAV Sequence

| | D9 (MSB) | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|----|----|----|----|----|----|----|
| Preamble | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Preamble | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Preamble | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Status word | 1 | F | V | H | P3 | P2 | P1 | P0 | 0 | 0 |

2.6 I²C Host Interface

Communication with the TVP5147 decoder is via an I²C host interface. The I²C standard consists of two signals, the serial input/output data (SDA) line and the serial input clock line (SCL), which carry information between the devices connected to the bus. A third signal (I2CA) is used for slave address selection. Although an I²C system can be multimastered, the TVP5147 decoder functions as a slave device only.

Because SDA and SCL are kept open-drain at a logic-high output level or when the bus is not driven, the user must connect SDA and SCL to a positive supply voltage via a pullup resistor on the board. The slave addresses select signal, terminal 37 (I2CA), enables the use of TVP5147 devices tied to the same I²C bus, because it controls the least significant bit of the I²C device address.

Table 2–4. I²C Host Interface Terminal Description

| SIGNAL | TYPE | DESCRIPTION |
|--------|------|-------------------------|
| I2CA | I | Slave address selection |
| SCL | I | Input clock line |
| SDA | I/O | Input/output data line |

2.6.1 Reset and I²C Bus Address Selection

The TVP5147 decoder can respond to two possible chip addresses. The address selection is made at reset by an externally supplied level on the I2CA terminal. The TVP5147 decoder samples the level of terminal 37 at power up or at the trailing edge of RESETB and configures the I²C bus address bit A0. The I2CA terminal has an internal pulldown resistor to pull the terminal low to set a zero.

Table 2–5. I²C Address Selection

| A6 | A5 | A4 | A3 | A2 | A1 | A0 (I2CA) | R/W | HEX |
|----|----|----|----|----|----|-------------|-----|-------|
| 1 | 0 | 1 | 1 | 1 | 0 | 0 (default) | 1/0 | B9/B8 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 † | 1/0 | BB/BA |

† If terminal 37 is strapped to DVDD via a 2.2-kΩ resistor, I²C device address A0 is set to 1.

2.6.2 I²C Operation

Data transfers occur using the following illustrated formats.

| | | | | | | | |
|---|----------|-----|------------|-----|-----------|-----|---|
| S | 10111000 | ACK | Subaddress | ACK | Send data | ACK | P |
|---|----------|-----|------------|-----|-----------|-----|---|

Read from I²C control registers

| | | | | | | | | | | |
|---|----------|-----|------------|-----|---|----------|-----|--------------|-----|---|
| S | 10111000 | ACK | Subaddress | ACK | S | 10111001 | ACK | Receive data | NAK | P |
|---|----------|-----|------------|-----|---|----------|-----|--------------|-----|---|

S = I²C bus start condition

P = I²C bus stop condition

ACK = Acknowledge generated by the slave

NAK = Acknowledge generated by the master, for multiple-byte read master with ACK each byte except last byte

Subaddress = Subaddress byte

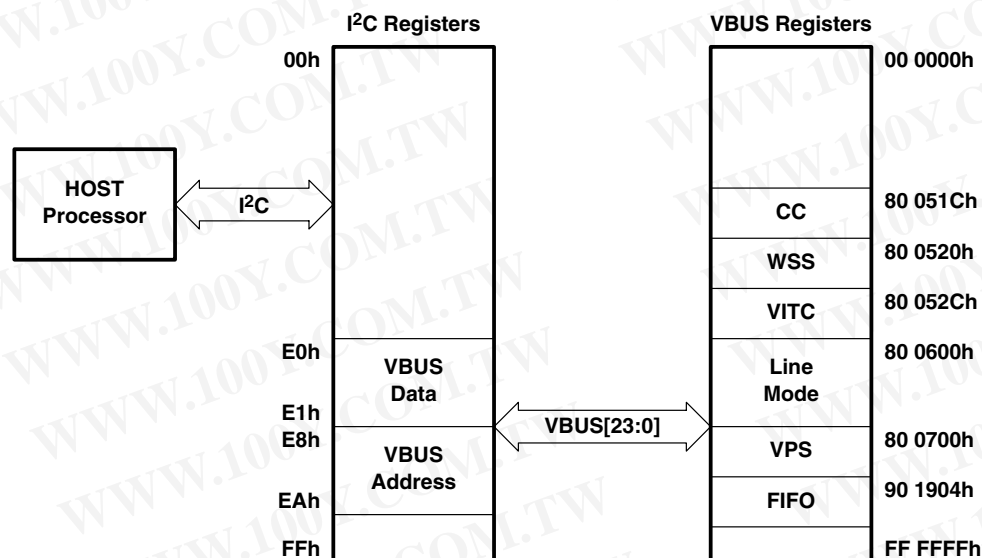
Data = Data byte. If more than one byte of data is transmitted (read and write), the subaddress pointer is automatically incremented.

I²C bus address = Example shown that I²CA is in default mode. Write (B8h), read (B9h)

2.6.3 VBUS Access

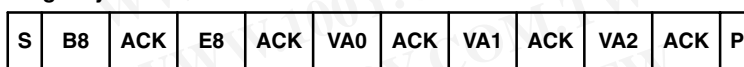
The TVP5147 decoder has additional internal registers accessible through an indirect access to an internal 24-bit address wide VBUS. Figure 2–23 shows the VBUS register access.

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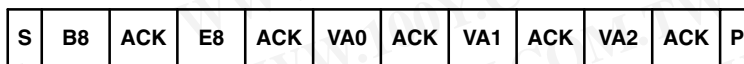


VBUS Write

Single Byte

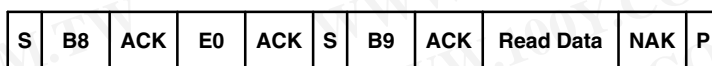
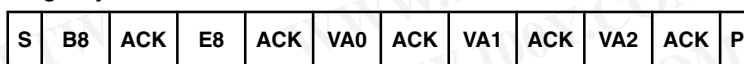


Multiple Bytes



VBUS Read

Single Byte



Multiple Bytes



NOTE: Examples use default I2C address
 ACK = Acknowledge generated by the slave
 NAK = No acknowledge generated by the master

Figure 2–23. VBUS Access

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2.7 VBI Data Processor

The TVP5147 VBI data processor (VDP) slices various data services like teletext (WST, NABTS), closed caption (CC), wide screen signaling (WSS), program delivery control (PDC), vertical interval time code (VITC), video program system (VPS), copy generation management system (CGMS) data, and electronic program guide (Gemstar) 1x/2x. Table 2–6 shows the supported VBI system.

These services are acquired by programming the VDP to enable the reception of one or more vertical blank interval (VBI) data standard(s) during the VBI. The VDP can be programmed on a line-per-line basis to enable simultaneous reception of different VBI formats, one per line. The results are stored in a FIFO and/or registers. Because of the high data bandwidth, teletext results are stored in FIFO only. The TVP5147 decoder provides fully decoded V-Chip data to the dedicated registers at subaddresses 80 0540h–80 0543h.

Table 2–6. Supported VBI System

| VBI SYSTEM | STANDARD | LINE NUMBER | NUMBER OF BYTES |
|------------------|----------|------------------------|-------------------|
| Teletext WST A | SECAM | 6–23 (Fields 1 and 2) | 38 |
| Teletext WST B | PAL | 6–22 (Fields 1 and 2) | 43 |
| Teletext NABTS C | NTSC | 10–21 (Fields 1 and 2) | 34 |
| Teletext NABTS D | NTSC-J | 10–21 (Fields 1 and 2) | 35 |
| Closed Caption | PAL | 22 (Fields 1 and 2) | 2 |
| Closed Caption | NTSC | 21 (Fields 1 and 2) | 2 |
| WSS | PAL | 23 (Fields 1 and 2) | 14 bits |
| WSS-CGMS | NTSC | 20 (Fields 1 and 2) | 20 bits |
| VITC | PAL | 6–22 | 9 |
| VITC | NTSC | 10–20 | 9 |
| VPS (PDC) | PAL | 16 | 13 |
| V-Chip (decoded) | NTSC | 21 (Fields 1 and 2) | 2 |
| Gemstar 1x | NTSC | | 2 |
| Gemstar 2x | NTSC | | 5 with frame byte |
| User | Any | Programmable | Programmable |

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2.7.1 VBI FIFO and Ancillary Data in Video Stream

Sliced VBI data can be output as ancillary data in the video stream in ITU-R BT.656 mode. VBI data is output on the Y[9:2] terminals during the horizontal blanking period. Table 2–7 shows the header format and sequence of the ancillary data inserted into the video stream. This format is also used to store any VBI data into the FIFO. The size of the FIFO is 512 bytes. Therefore, the FIFO can store up to 11 lines of teletext data with the NTSC NABTS standard.

Table 2–7. Ancillary Data Format and Sequence

| BYTE NO. | D7 (MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) | DESCRIPTION | | |
|----------|--------------------|----|----|------------|----------|----------|--------------------|----------|----------------------------|----------------------|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Ancillary data preamble | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | |
| 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | |
| 3 | NEP | EP | 0 | 1 | 0 | DID2 | DID1 | DID0 | Data ID (DID) | | |
| 4 | NEP | EP | F5 | F4 | F3 | F2 | F1 | F0 | Secondary data ID (SDID) | | |
| 5 | NEP | EP | N5 | N4 | N3 | N2 | N1 | N0 | Number of 32-bit data (NN) | | |
| 6 | Video line # [7:0] | | | | | | | | Internal data ID0 (IDID0) | | |
| 7 | 0 | 0 | 0 | Data error | Match #1 | Match #2 | Video line # [9:8] | | Internal data ID1 (IDID1) | | |
| 8 | 1. Data | | | | | | | | Data byte | 1 st word | |
| 9 | 2. Data | | | | | | | | Data byte | | |
| 10 | 3. Data | | | | | | | | Data byte | | |
| 11 | 4. Data | | | | | | | | Data byte | | |
| : | : | | | | | | | | : | : | |
| | m. Data | | | | | | | | Data byte | N th word | |
| | CS[7:0] | | | | | | | | Check sum | | |
| 4N+7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Fill byte | | |

NOTE: The number of bytes (m) varies depending on the VBI data service.

EP: Even parity for D0–D5, NEP: Negated even parity

DID: 91h: Sliced data of VBI lines of first field
53h: Sliced data of line 24 to end of first field
55h: Sliced data of VBI lines of second field
97h: Sliced data of line 24 to end of second field

SDID: This field holds the data format taken from the line mode register bits [2:0] of the corresponding line.

NN: Number of Dwords beginning with byte 8 through 4N+7. Note this value is the number of Dwords where each Dword is 4 bytes.

IDID0: Transaction video line number [7:0]

IDID1: Bit 0/1 = Transaction video line number [9:8]
Bit 2 = Match 2 flag
Bit 3 = Match 1 flag
Bit 4 = 1 if an error was detected in the EDC block. 0 if no error was detected.

CS: Sum of D0–D7 of first data through last data byte.

Fill byte: Fill bytes make a multiple of 4 bytes from byte 0 to last fill byte. For teletext modes, byte 8 is the sync pattern byte. Byte 9 is the first data byte.

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2.7.2 VBI Raw Data Output

The TVP5147 decoder can output raw A/D video data at twice the sampling rate for external VBI slicing. This is transmitted as an ancillary data block, although somewhat differently from the way the sliced VBI data is transmitted in the FIFO format as described in Section 2.7.1. The samples are transmitted during the active portion of the line. VBI raw data uses ITU-R BT.656 format having only luma data. The chroma samples are replaced by luma samples. The TVP5147 decoder inserts a four-byte preamble 000h 3FFh 3FFh 180h before data start. There are no checksum bytes and fill bytes in this mode.

Table 2–8. VBI Raw Data Output Format

| BYTE NO. | D9 (MSB) | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) | DESCRIPTION |
|----------|-----------|----|----|----|----|----|----|----|----|----------|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VBI raw data preamble |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 3 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 4 | 1. Data | | | | | | | | | | 2× pixel rate luma data (i.e., NTSC 601: n = 1707) |
| 5 | 2. Data | | | | | | | | | | |
| : | : | | | | | | | | | | |
| n–1 | n–5. Data | | | | | | | | | | |
| n | n–4. Data | | | | | | | | | | |

2.8 Reset and Initialization

Reset is initiated at power up or any time terminal 34 (RESETB) is brought low. Table 2–9 describes the status of the TVP5147 terminals during and immediately after reset.

Table 2–9. Reset Sequence

| SIGNAL NAME | DURING RESET | RESET COMPLETED |
|--|--------------|-----------------|
| Y[9:0], C[9:0] | Input | High-impedance |
| RESETB, PWDN, SDA, SCL, FSS, AVID, GLCO, HS, VS, FID | Input | Input |
| INTREQ | Input | Output |
| DATACLK | Output | High-impedance |

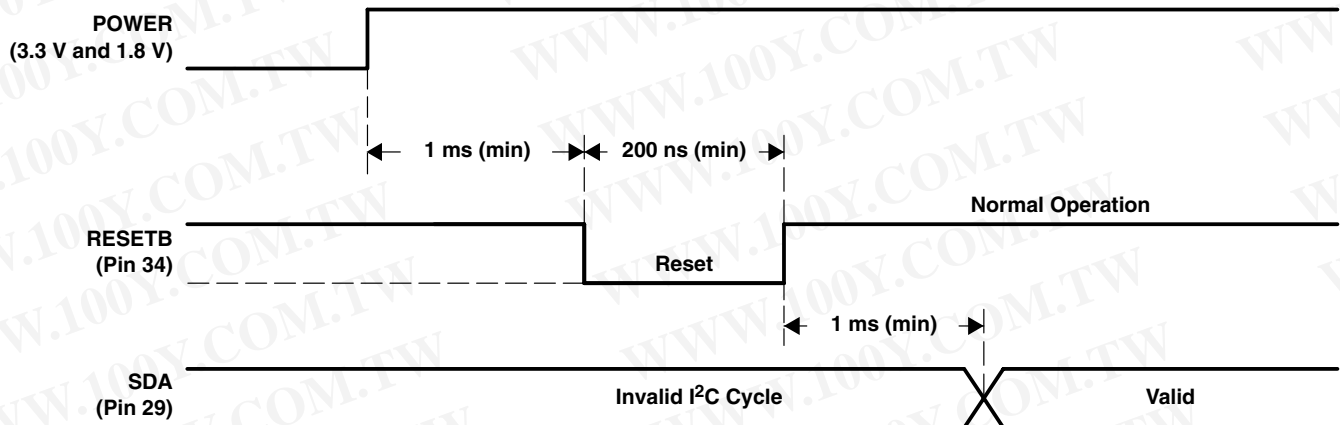


Figure 2–24. Reset Timing

The TVP5147 requires that pin 69 (C₁/GPIO) be held LOW. If using the 20-/16-bit mode or using this pin as GPIO, then this pin must be pulled low through a 2.2-kΩ pulldown resistor (see Figure 5–1). If unused, this pin can be shorted to ground. (Note: If using the 20-/16-bit mode and only using the 16 MSBs, it is possible to short pin 69 to GND, but the current for IOVDD will increase by 2 or 3 mA.)

After reset, the user must write the following I²C commands to the TVP5147:

| STEP | I ² C SUBADDRESS | I ² C DATA |
|------|-----------------------------|-----------------------|
| 1 | 0xE8 | 0x02 |
| 2 | 0xE9 | 0x00 |
| 3 | 0xEA | 0x80 |
| 4 | 0xE0 | 0x01 |
| 5 | 0xE8 | 0x60 |
| 6 | 0xE9 | 0x00 |
| 7 | 0xEA | 0xB0 |
| 8 | 0xE0 | 0x01 |
| 9 | 0xE8 | 0x16 |
| 10 | 0xE9 | 0x00 |
| 11 | 0xEA | 0xA0 |
| 12 | 0xE0 | 0x16 |
| 13 | 0xE8 | 0x60 |
| 14 | 0xE9 | 0x00 |
| 15 | 0xEA | 0xB0 |
| 16 | 0xE0 | 0x00 |
| 17 | 0x03 | 0x01 |
| 18 | 0x03 | 0x00 |

Afterward, the user programs the device as usual.

2.9 Adjusting External Syncs

The proper sequence to program the following external syncs is:

- To set NTSC, PAL-M, NTSC 443, PAL60 (525-line modes):
 - Set the video standard to NTSC (register 02h)
 - Set HSYNC, VSYNC, VBLK, and AVID external syncs (registers 16h through 24h)
- To set PAL, PAL-N, SECAM (625-line modes):
 - Set the video standard to PAL (register 02h)
 - Set HSYNC, VSYNC, VBLK, and AVID external syncs (registers 16h through 24h)
- For autoswitch, set the video standard to autoswitch (register 02h)

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2.10 Internal Control Registers

The TVP5147 decoder is initialized and controlled by a set of internal registers that define the operating parameters of the entire device. Communication between the external controller and the TVP5147 is through a standard I²C host port interface, as described earlier. Table 2–10 shows the summary of these registers. Detailed programming information for each register is described in the following sections. Additional registers are accessible through an indirect procedure involving access to an internal 24-bit address wide VBUS. Table 2–11 shows the summary of the VBUS registers.

NOTE: Do not write to reserved registers. Reserved bits in any defined register must be written with 0s, unless otherwise noted.

Table 2–10. I²C Register Summary

| REGISTER NAME | I ² C SUBADDRESS | DEFAULT | R/W |
|----------------------------------|-----------------------------|---------|-----|
| Input select | 00h | 00h | R/W |
| AFE gain control | 01h | 0Fh | R/W |
| Video standard | 02h | 00h | R/W |
| Operation mode | 03h | 00h | R/W |
| Autoswitch mask | 04h | 23h | R/W |
| Color killer | 05h | 10h | R/W |
| Luminance processing control 1 | 06h | 00h | R/W |
| Luminance processing control 2 | 07h | 00h | R/W |
| Luminance processing control 3 | 08h | 02h | R/W |
| Luminance brightness | 09h | 80h | R/W |
| Luminance contrast | 0Ah | 80h | R/W |
| Chrominance saturation | 0Bh | 80h | R/W |
| Chroma hue | 0Ch | 00h | R/W |
| Chrominance processing control 1 | 0Dh | 00h | R/W |
| Chrominance processing control 2 | 0Eh | 0Eh | R/W |
| Reserved | 0Fh–15h | | |
| AVID start pixel | 16h–17h | 055h | R/W |
| AVID stop pixel | 18h–19h | 325h | R/W |
| HSYNC start pixel | 1Ah–1Bh | 000h | R/W |
| HSYNC stop pixel | 1Ch–1Dh | 040h | R/W |
| VSYNC start line | 1Eh–1Fh | 004h | R/W |
| VSYNC stop line | 20h–21h | 007h | R/W |
| VBLK start line | 22h–23h | 001h | R/W |
| VBLK stop line | 24h–25h | 015h | R/W |
| Reserved | 26h–2Ah | | |
| Overlay delay | 2Bh | 00h | R/W |
| Reserved | 2Ch | | |
| CTI delay | 2Dh | 00h | R/W |
| CTI control | 2Eh | 00h | R/W |
| Reserved | 2Fh–30h | | |
| GLCO/RTC | 31h | 05h | R/W |
| Sync control | 32h | 00h | R/W |
| Output formatter 1 | 33h | 40h | R/W |
| Output formatter 2 | 34h | 00h | R/W |
| Output formatter 3 | 35h | FFh | R/W |
| Output formatter 4 | 36h | FFh | R/W |
| Output formatter 5 | 37h | FFh | R/W |
| Output formatter 6 | 38h | FFh | R/W |
| Clear lost lock detect | 39h | 00h | R/W |
| Status 1 | 3Ah | | R |
| Status 2 | 3Bh | | R |

NOTE: R = Read only
 W = Write only
 R/W = Read and write
 Reserved register addresses must not be written to.

Table 2–10. I²C Register Summary (Continued)

| REGISTER NAME | I ² C SUBADDRESS | DEFAULT | R/W |
|-----------------------------|-----------------------------|---------|-----|
| AGC gain status | 3Ch–3Dh | | R |
| Reserved | 3Eh | | |
| Video standard status | 3Fh | | R |
| GPIO input 1 | 40h | | R |
| GPIO input 2 | 41h | | R |
| Vertical line count | 42h–43h | | R |
| Reserved | 44h–45h | | |
| AFE coarse gain for CH1 | 46h | 20h | R/W |
| AFE coarse gain for CH2 | 47h | 20h | R/W |
| AFE coarse gain for CH3 | 48h | 20h | R/W |
| AFE coarse gain for CH4 | 49h | 20h | R/W |
| AFE fine gain for Pb | 4Ah–4Bh | 900h | R/W |
| AFE fine gain for chroma | 4Ch–4Dh | 900h | R/W |
| AFE fine gain for Pr | 4Eh–4Fh | 900h | R/W |
| AFE fine gain for CVBS_Luma | 50h–51h | 900h | R/W |
| Reserved | 52h–56h | | |
| Field ID control | 57h | 00h | R/W |
| Reserved | 58h–6Fh | | |
| ROM version | 70h | | R |
| Reserved | 71h–73h | | |
| AGC white peak processing | 74h | 00h | R/W |
| F and V bit control | 75h | 12h | R/W |
| VCR trick mode control | 76h | 8Ah | R/W |
| Horizontal shake increment | 77h | 64h | R/W |
| AGC increment speed | 78h | 05h | R/W |
| AGC increment delay | 79h | 1Eh | R/W |
| Reserved | 7Ah–7Eh | | |
| Analog output control 1 | 7Fh | 00h | R/W |
| Chip ID MSB | 80h | 51h | R |
| Chip ID LSB | 81h | 47h | R |
| Reserved | 82h–B0h | | |
| VDP TTX filter 1 mask 1 | B1h | 00h | R/W |
| VDP TTX filter 1 mask 2 | B2h | 00h | R/W |
| VDP TTX filter 1 mask 3 | B3h | 00h | R/W |
| VDP TTX filter 1 mask 4 | B4h | 00h | R/W |
| VDP TTX filter 1 mask 5 | B5h | 00h | R/W |
| VDP TTX filter 2 mask 1 | B6h | 00h | R/W |
| VDP TTX filter 2 mask 2 | B7h | 00h | R/W |
| VDP TTX filter 2 mask 3 | B8h | 00h | R/W |
| VDP TTX filter 2 mask 4 | B9h | 00h | R/W |
| VDP TTX filter 2 mask 5 | BAh | 00h | R/W |

NOTE: R = Read only
 W = Write only
 R/W = Read and write
 Reserved register addresses must not be written to.

Table 2–10. I²C Register Summary (Continued)

| REGISTER NAME | I ² C SUBADDRESS | DEFAULT | R/W |
|---|-----------------------------|----------|-----|
| VDP TTX filter control | BBh | 00h | R/W |
| VDP FIFO word count | BCh | | R |
| VDP FIFO interrupt threshold | BDh | 80h | R/W |
| Reserved | BEh | | |
| VDP FIFO reset | BFh | 00h | R/W |
| VDP FIFO output control | C0h | 00h | R/W |
| VDP line number interrupt | C1h | 00h | R/W |
| VDP pixel alignment | C2h–C3h | 01Eh | R/W |
| Reserved | C4h–D5h | | |
| VDP line start | D6h | 06h | R/W |
| VDP line stop | D7h | 1Bh | R/W |
| VDP global line mode | D8h | FFh | R/W |
| VDP full field enable | D9h | 00h | R/W |
| VDP full field mode | DAh | FFh | R/W |
| Reserved | DBh–DFh | | |
| VBUS data access with no VBUS address increment | E0h | 00h | R/W |
| VBUS data access with VBUS address increment | E1h | 00h | R/W |
| FIFO read data | E2h | | R |
| Reserved | E3h–E7h | | |
| VBUS address access | E8h–EAh | 00 0000h | R/W |
| Reserved | EBh–EFh | | |
| Interrupt raw status 0 | F0h | | R |
| Interrupt raw status 1 | F1h | | R |
| Interrupt status 0 | F2h | | R |
| Interrupt status 1 | F3h | | R |
| Interrupt mask 0 | F4h | 00h | R/W |
| Interrupt mask 1 | F5h | 00h | R/W |
| Interrupt clear 0 | F6h | 00h | R/W |
| Interrupt clear 1 | F7h | 00h | R/W |
| Reserved | F8h–FFh | | |

NOTE: R = Read only
W = Write only
R/W = Read and write
Reserved register addresses must not be written to.

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Table 2–11. VBUS Register Summary

| REGISTER NAME | I ² C SUBADDRESS | DEFAULT | R/W |
|--|-----------------------------|----------|-----|
| Reserved | 00 0000h–80 051Bh | | |
| VDP closed caption data | 80 051Ch–80 051Fh | | R |
| VDP WSS data | 80 0520h–80 0526h | | R |
| Reserved | 80 0527h–80 052Bh | | |
| VDP VITC data | 80 052Ch–80 0534h | | R |
| Reserved | 80 0535h–80 053Fh | | |
| VDP V-Chip data | 80 0540h–80 0543h | | R |
| Reserved | 80 0544h–80 05FFh | | |
| VDP general line mode and line address | 80 0600h–80 0611h | 00h, FFh | R/W |
| Reserved | 80 0612h–80 06FFh | | |
| VDP VPS (PDC)/Gemstar data | 80 0700h–80 070Ch | | R |
| Reserved | 80 070Dh–90 1903h | | |
| VDP FIFO read | 90 1904h | | R |
| Reserved | 90 1905h–A0 005Dh | | |
| Analog output control 2 | A0 005Eh | B2h | R/W |
| Reserved | A0 005Fh–B0 005Fh | | |
| Interrupt configuration | B0 0060h | 00h | R/W |
| Reserved | B0 0061h–FF FFFFh | | |

NOTE: Writing any value to a reserved register may cause erroneous operation of the TVP5147 decoder. It is recommended not to access any data to/from reserved registers.

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2.11 Register Definitions

2.11.1 Input Select Register

| | |
|------------|-----|
| Subaddress | 00h |
| Default | 00h |

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| | | | | | | | |
|--------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Input select [7:0] | | | | | | | |

Table 2–12. Analog Channel and Video Mode Selection

| MODE | INPUT(S) SELECTED | INPUT SELECT [7:0] | | | | | | | | | OUTPUT (see Note 1) | |
|---------|-----------------------------------|--------------------|---|---|---|---|---|---|---|-----|------------------------|-----------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX | | |
| CVBS | VI_1_A (default) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | N/A |
| | VI_1_B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | VI_1_B |
| | VI_1_C | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 02 | VI_1_C |
| | VI_2_A | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 04 | VI_2_A |
| | VI_2_B | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 05 | VI_2_B |
| | VI_2_C | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 06 | VI_2_C |
| | VI_3_A | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 08 | VI_3_A |
| | VI_3_B | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 09 | VI_3_B |
| | VI_3_C | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0A | VI_3_C |
| | VI_4_A | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0C | VI_4_A |
| S-video | VI_2_A(Y), VI_1_A(C) | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 44 | N/A |
| | VI_2_B(Y), VI_1_B(C) | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 45 | VI_2_B(Y) |
| | VI_2_C(Y), VI_1_C(C) | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 46 | VI_2_C(Y) |
| | VI_2_A(Y), VI_3_A(C) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 54 | VI_2_A(Y) |
| | VI_2_B(Y), VI_3_B(C) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 55 | VI_2_B(Y) |
| | VI_2_C(Y), VI_3_C(C) | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 56 | VI_2_C(Y) |
| | VI_4_A(Y), VI_1_A(C) | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 4C | N/A |
| | VI_4_A(Y), VI_1_B(C) | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 4D | VI_4_A(Y) |
| | VI_4_A(Y), VI_1_C(C) | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 4E | VI_4_A(Y) |
| | VI_4_A(Y), VI_3_A(C) | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 5C | VI_4_A(Y) |
| | VI_4_A(Y), VI_3_B(C) | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 5D | VI_4_A(Y) |
| | VI_4_A(Y), VI_3_C(C) | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 5E | VI_4_A(Y) |
| YPbPr | VI_1_A(Pb), VI_2_A(Y), VI_3_A(Pr) | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 94 | N/A |
| | VI_1_B(Pb), VI_2_B(Y), VI_3_B(Pr) | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 95 | VI_2_B(Y) |
| | VI_1_C(Pb), VI_2_C(Y), VI_3_C(Pr) | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 96 | VI_2_C(Y) |

NOTE 1: When VI_1_A is set to output, the total number of inputs is nine. The video output can be either CVBS or luma.

Ten input terminals can be configured to support composite, S-video, and component YPbPr as listed in Table 2–12. User must follow this table properly for S-video and component applications because only the terminal configurations listed in Table 2–12 are supported.

2.11.2 AFE Gain Control Register

| | |
|------------|-----|
| Subaddress | 01h |
| Default | 0Fh |

| | | | | | | | |
|----------|---|---|---|---|---|------------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | 1 | 1 | AGC chroma | AGC luma |

Bit 3: 1 must be written to this bit.

Bit 2: 1 must be written to this bit.

AGC chroma enable: Controls automatic gain in the chroma/PbPr channel:

- 0 = Manual (if AGC luma is set to manual, AGC chroma is forced to be in manual)
- 1 = Enabled auto gain, applied a gain value acquired from the sync channel for S-video and component mode. When AGC luma is set, this state is valid. (default)

AGC luma enable: Controls automatic gain in the embedded sync channel of CVBS, S-video, component video:

- 0 = Manual gain, AFE coarse and fine gain frozen to the previous gain value set by AGC when this bit is set to 0.
- 1 = Enabled auto gain applied to only the embedded sync channel (default)

These settings only affect the analog front-end (AFE). The brightness and contrast controls are not affected by these settings.

2.11.3 Video Standard Register

| | |
|------------|-----|
| Subaddress | 02h |
| Default | 00h |

| | | | | | | | |
|----------|---|---|---|----------------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | Video standard [2:0] | | | |

Video standard [2:0]:

| CVBS and S-Video | | Component Video |
|------------------|-----------------------------|---------------------------|
| 000 | = Autoswitch mode (default) | Autoswitch mode (default) |
| 001 | = (M, J) NTSC | Component 525 |
| 010 | = (B, D, G, H, I, N) PAL | Component 625 |
| 011 | = (M) PAL | Reserved |
| 100 | = (Combination-N) PAL | Reserved |
| 101 | = NTSC 4.43 | Reserved |
| 110 | = SECAM | Reserved |
| 111 | = PAL 60 | Reserved |

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With the autoswitch code running, the user can force the decoder to operate in a particular video standard mode by writing the appropriate value into this register. Changing these bits causes the register settings to be reinitialized.

NOTE: Sampling rate (either square pixel or ITU-R BT.601) can be set by bit 7 (sampling rate) in the output formatter 1 register at I²C subaddress 33h (see Section 2.11.28).

2.11.4 Operation Mode Register

| | |
|------------|-----|
| Subaddress | 03h |
| Default | 00h |

| | | | | | | | |
|----------|---|---|---|---|---|---|------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | Power save |

Power save:

0 = Normal operation (default)

1 = Power-save mode. Reduces the clock speed of the internal processor and switches off the ADCs. I²C interface is active and all current operating settings are preserved.

2.11.5 Autoswitch Mask Register

| | |
|------------|-----|
| Subaddress | 04h |
| Default | 23h |

| | | | | | | | |
|----------|--------|-------|-----------|----------|---------|-----|-------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | PAL 60 | SECAM | NTSC 4.43 | (Nc) PAL | (M) PAL | PAL | (M, J) NTSC |

Autoswitch mode mask: Limits the video formats between which autoswitch is possible.

PAL 60:

0 = Autoswitch does not include PAL 60 (default)

1 = Autoswitch includes PAL60

SECAM:

0 = Autoswitch does not include SECAM

1 = Autoswitch includes SECAM (default)

NTSC 4.43:

0 = Autoswitch does not include NTSC 4.43 (default)

1 = Autoswitch includes NTSC 4.43

(Nc) PAL:

0 = Autoswitch does not include (Nc) PAL (default)

1 = Autoswitch includes (Nc) PAL

(M) PAL:

0 = Autoswitch does not include (M) PAL (default)

1 = Autoswitch includes (M) PAL

PAL:

0 = Reserved

1 = Autoswitch includes (B, D, G, H, I, N) PAL (default)

(M, J) NTSC:

0 = Reserved

1 = Autoswitch includes (M, J) NTSC (default)

NOTE: Bits 1 and 0 must always be 1.

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2.11.6 Color Killer Register

| | |
|------------|-----|
| Subaddress | 05h |
| Default | 10h |

| | | | | | | | |
|----------|------------------------|---|------------------------------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Automatic color killer | | Color killer threshold [4:0] | | | | |

Automatic color killer:

- 00 = Automatic mode (default)
- 01 = Reserved
- 10 = Color killer enabled, the UV terminals are forced to a zero color state.
- 11 = Color killer disabled

Color killer threshold [4:0]:

- 1 1111 = 31 (maximum)
- 1 0000 = 16 (default)
- 0 0000 = 0 (minimum)

2.11.7 Luminance Processing Control 1 Register

| | |
|------------|-----|
| Subaddress | 06h |
| Default | 00h |

| | | | | | | | |
|----------|----------------------|----------|---------|------------------------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Pedestal not present | Reserved | VBI raw | Luminance signal delay [3:0] | | | |

Pedestal not present:

- 0 = 7.5 IRE pedestal is present on the analog video input signal (default)
- 1 = Pedestal is not present on the analog video input signal

VBI raw:

- 0 = Disabled (default)
- 1 = Enabled

During the duration of the vertical blanking as defined by the VBLK start and stop line registers at subaddresses 22h through 25h (see Sections 2.11.22 and 2.11.23), the chroma samples are replaced by luma samples. This feature can be used to support VBI processing performed by an external device during the vertical blanking interval. In order to use this bit, the output format must be 10-bit ITU-R BT.656 mode.

Luminance signal delay [3:0]: Luminance signal delays with respect to the chroma signal in 1× pixel clock increments.

- 0111 = Reserved
- 0110 = 6-pixel delay
- 0001 = 1-pixel delay
- 0000 = 0 delay (default)
- 1111 = -1-pixel delay
- 1000 = -8-pixel delay

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2.11.8 Luminance Processing Control 2 Register

| | |
|------------|-----|
| Subaddress | 07h |
| Default | 00h |

| | | | | | | | |
|--------------------------|---|----------|---|--------------------|---|----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Luma filter select [1:0] | | Reserved | | Peaking gain [1:0] | | Reserved | |

Luma filter selected [1:0]:

- 00 = Luminance adaptive comb enabled (default on CVBS)
- 01 = Luminance adaptive comb disabled (trap filter selected)
- 10 = Luma comb/trap filter bypassed (default on S-video, component mode, and SECAM)
- 11 = Reserved

Peaking gain [1:0]:

- 00 = 0 (default)
- 01 = 0.5
- 10 = 1
- 11 = 2

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2.11.9 Luminance Processing Control 3 Register

| | |
|------------|-----|
| Subaddress | 08h |
| Default | 02h |

| | | | | | | | |
|----------|---|---|---|---|---|--------------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | Trap filter select [1:0] | |

Trap filter select [1:0] selects one of the four trap filters to produce the luminance signal by removing the chrominance signal from the composite video signal. The stop band of the chroma trap filter is centered at the chroma subcarrier frequency with the stop-band bandwidth controlled by the two control bits.

Trap filter stop-band bandwidth (MHz):

| Filter select [1:0] | NTSC ITU-R BT.601 | NTSC square pixel | PAL ITU-R BT.601 | PAL square pixel |
|---------------------|-------------------|-------------------|------------------|------------------|
| 00 = | 1.2129 | 1.1026 | 1.2129 | 1.3252 |
| 01 = | 0.8701 | 0.7910 | 0.8701 | 0.9507 |
| 10 = (default) | 0.7183 | 0.6712 | 0.7383 | 0.8066 |
| 11 = | 0.5010 | 0.4554 | 0.5010 | 0.5474 |

2.11.10 Luminance Brightness Register

| | |
|------------|-----|
| Subaddress | 09h |
| Default | 80h |

| | | | | | | | |
|------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Brightness [7:0] | | | | | | | |

Brightness [7:0]: This register works for CVBS, S-video, and component video luminance.

- 1111 1111 = 255 (bright)
- 1000 0000 = 128 (default)
- 0000 0000 = 0 (dark)

2.11.11 Luminance Contrast Register

| | |
|------------|-----|
| Subaddress | 0Ah |
| Default | 80h |

| | | | | | | | |
|----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Contrast [7:0] | | | | | | | |

Contrast [7:0]: This register works for CVBS, S-video, and component video luminance.

1111 1111 = 255 (maximum contrast)

1000 0000 = 128 (default)

0000 0000 = 0 (minimum contrast)

2.11.12 Chrominance Saturation Register

| | |
|------------|-----|
| Subaddress | 0Bh |
| Default | 80h |

| | | | | | | | |
|------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Saturation [7:0] | | | | | | | |

Saturation [7:0]: This register works for CVBS, S-video, and component video luminance.

1111 1111 = 255 (maximum)

1000 0000 = 128 (default)

0000 0000 = 0 (no color)

2.11.13 Chroma Hue Register

| | |
|------------|-----|
| Subaddress | 0Ch |
| Default | 00h |

| | | | | | | | |
|-----------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Hue [7:0] | | | | | | | |

Hue [7:0] (does not apply to component video)

0111 1111 = +180 degrees

0000 0000 = 0 degrees (default)

1000 0000 = -180 degrees

2.11.14 Chrominance Processing Control 1 Register

| | |
|------------|-----|
| Subaddress | 0Dh |
| Default | 00h |

| | | | | | | | |
|----------|---|---|-----------------|-------------------------------------|----------|------------------------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | Color PLL reset | Chrominance adaptive comb enable | Reserved | Automatic color gain control [1:0] | |

Color PLL reset:

0 = Color subcarrier PLL not reset (default)

1 = Color subcarrier PLL reset

Chrominance adaptive comb enable: This bit is effective on composite video only.

0 = Enabled (default)

1 = Disabled

Automatic color gain control (ACGC) [1:0]:

00= ACGC enabled (default)

01 = Reserved

10= ACGC disabled, ACGC set to the nominal value

11= ACGC frozen to the previous set value

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2.11.15 Chrominance Processing Control 2 Register

| | |
|------------|-----|
| Subaddress | 0Eh |
| Default | 0Eh |

| | | | | | | | |
|----------|---|---|---|------------------|-----|---------------------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | PAL compensation | WCF | Chrominance filter select [1:0] | |

PAL compensation:

- 0 = Disabled
- 1 = Enabled (default)

Wideband chroma LPF filter (WCF):

- 0 = Disabled
- 1 = Enabled (default)

Chrominance filter select [1:0]:

- 00 = Disabled
- 01 = Notch 1
- 10 = Notch 2 (default)
- 11 = Notch 3

See Figure 2–8 through Figure 2–11 for characteristics.

2.11.16 AVID Start Pixel Register

| | |
|------------|---------|
| Subaddress | 16h–17h |
| Default | 055h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------------|---|---|-------------|----------|---|------------------|---|
| 16h | AVID start [7:0] | | | | | | | |
| 17h | Reserved | | | AVID active | Reserved | | AVID start [9:8] | |

AVID active:

- 0 = AVID out active in VBLK (default)
- 1 = AVID out inactive in VBLK

AVID start [9:0]: AVID start pixel number, this is an absolute pixel location from HSYNC start pixel 0.

| | | | | |
|---------|-----------------|-----------------|----------------|----------------|
| | <u>NTSC 601</u> | <u>NTSC Sqp</u> | <u>PAL 601</u> | <u>PAL Sqp</u> |
| default | 85 (55h) | 86 (56h) | 88 (58h) | 103 (67h) |

The TVP5147 decoder updates the AVID start only when the AVID start MSB byte is written to. If the user changes these registers, then the TVP5147 decoder retains values in different modes until this device resets. The AVID start pixel register also controls the position of the SAV code.

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2.11.17 AVID Stop Pixel Register

| | |
|------------|---------|
| Subaddress | 18h–19h |
| Default | 325h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----------------|---|---|---|---|---|-----------------|---|
| 18h | AVID stop [7:0] | | | | | | | |
| 19h | Reserved | | | | | | AVID stop [9:8] | |

AVID stop [9:0]: AVID stop pixel number. The number of pixels of active video must be an even number. This is an absolute pixel location from HSYNC start pixel 0.

| | NTSC 601 | NTSC Sq | PAL 601 | PAL Sq |
|---------|------------|------------|------------|------------|
| default | 805 (325h) | 726 (2D6h) | 808 (328h) | 696 (2B8h) |

The TVP5147 decoder updates the AVID stop only when the AVID stop MSB byte is written to. If the user changes these registers, then the TVP5147 decoder retains values in different modes until this device resets. The AVID start pixel register also controls the position of the EAV code.

2.11.18 HSYNC Start Pixel Register

| | |
|------------|---------|
| Subaddress | 1Ah–1Bh |
| Default | 000h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-------------------|---|---|---|---|---|-------------------|---|
| 1Ah | HSYNC start [7:0] | | | | | | | |
| 1Bh | Reserved | | | | | | HSYNC start [9:8] | |

HSYNC start pixel [9:0]: This is an absolute pixel location from HSYNC start pixel 0.

The TVP5147 decoder updates the HSYNC start only when the HSYNC start MSB is written to. If the user changes these registers, then the TVP5147 decoder retains values in different modes until this device resets.

2.11.19 HSYNC Stop Pixel Register

| | |
|------------|---------|
| Subaddress | 1Ch–1Dh |
| Default | 040h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------------|---|---|---|---|---|------------------|---|
| 1Ch | HSYNC stop [7:0] | | | | | | | |
| 1Dh | Reserved | | | | | | HSYNC stop [9:8] | |

HSYNC stop [9:0]: This is an absolute pixel location from HSYNC start pixel 0.

The TVP5147 decoder updates the HSYNC stop only when the HSYNC stop MSB is written to. If the user changes these registers, then the TVP5147 decoder retains values in different modes until this device resets.

2.11.20 VSYNC Start Line Register

| | |
|------------|---------|
| Subaddress | 1Eh–1Fh |
| Default | 004h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-------------------|---|---|---|---|---|-------------------|---|
| 1Eh | VSYNC start [7:0] | | | | | | | |
| 1Fh | Reserved | | | | | | VSYNC start [9:8] | |

VSYNC start [9:0]: This is an absolute line number. The TVP5147 decoder updates the VSYNC start only when the VSYNC start MSB is written to. If the user changes these registers, then the TVP5147 decoder retains values in different modes until this decoder resets.

NTSC: default 004h PAL: default 001h

2.11.21 VSYNC Stop Line Register

| | |
|------------|---------|
| Subaddress | 20h–21h |
| Default | 007h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------------|---|---|---|---|---|------------------|---|
| 20h | VSYNC stop [7:0] | | | | | | | |
| 21h | Reserved | | | | | | VSYNC stop [9:8] | |

VSYNC stop [9:0]: This is an absolute line number. The TVP5147 decoder updates the VSYNC stop only when the VSYNC stop MSB is written to. If the user changes these registers, the TVP5147 decoder retains values in different modes until this decoder resets.

NTSC: default 007h PAL: default 004h

2.11.22 VBLK Start Line Register

| | |
|------------|---------|
| Subaddress | 22h–23h |
| Default | 001h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------------|---|---|---|---|---|------------------|---|
| 22h | VBLK start [7:0] | | | | | | | |
| 23h | Reserved | | | | | | VBLK start [9:8] | |

VBLK start [9:0]: This is an absolute line number. The TVP5147 decoder updates the VBLK start line only when the VBLK start MSB is written to. If the user changes these registers, the TVP5147 decoder retains values in different modes until this resets (see Section 2.11.16)

NTSC: default 001h PAL: default 623 (26Fh)

2.11.23 VBLK Stop Line Register

| | |
|------------|---------|
| Subaddress | 24h–25h |
| Default | 015h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----------------|---|---|---|---|---|-----------------|---|
| 24h | VBLK stop [7:0] | | | | | | | |
| 25h | Reserved | | | | | | VBLK stop [9:8] | |

VBLK stop [9:0]: This is an absolute line number. The TVP5147 decoder updates the VBLK stop only when the VBLK stop MSB is written to. If the user changes these registers, then the TVP5147 decoder retains values in different modes until this device resets (see Section 2.11.16).

NTSC: default 21 (015h) PAL: default 23 (017h)

2.11.24 CTI Delay Register

| | |
|------------|-----|
| Subaddress | 2Dh |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|-----------------|---|
| Reserved | | | | | | CTI delay [2:0] | |

CTI delay [2:0]: Sets the delay of the Y channel with respect to Cb/Cr in the CTI block

- 011 = 3-pixel delay
- 001 = 1-pixel delay
- 000 = 0 delay (default)
- 111 = –1-pixel delay
- 100 = –4-pixel delay

2.11.25 CTI Control Register

| | |
|------------|-----|
| Subaddress | 2Eh |
| Default | 00h |

| | | | | | | | |
|------------------|---|---|---|----------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CTI coring [3:0] | | | | CTI gain [3:0] | | | |

CTI coring [3:0]: 4-bit CTI coring limit control value, unsigned linear control range from 0 to ± 60 , step size = 4

1111 = ± 60

0001 = ± 4

0000 = 0 (default)

CTI gain [3:0]: 4-bit CTI gain control values, unsigned linear control range from 0 to 15/16, step size = 1/16

1111 = 15/16

0001 = 1/16

0000 = 0 disabled (default)

2.11.26 RTC Register

| | |
|------------|-----|
| Subaddress | 31h |
| Default | 05h |

| | | | | | | | |
|----------|---|---|---|---------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | Genlock [2:0] | | | |

Genlock [2:0]:

000 = Reserved

001 = Reserved

010 = Reserved

011 = Reserved

100 = Reserved

101 = RTC mode

110 = Reserved

111 = Reserved

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2.11.27 Sync Control Register

| | |
|------------|-----|
| Subaddress | 32h |
| Default | 00h |

| | | | | | | | |
|----------|---|---|--------------|-------------|-------------|---------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | Polarity FID | Polarity VS | Polarity HS | VS/VBLK | HS/CS |

Polarity FID: determines polarity of FID terminal

- 0 = First field high, second field low (default)
- 1 = First field low, second field high

Polarity VS: determines polarity of VS terminal

- 0 = Active low (default)
- 1 = Active high

Polarity HS: determines polarity of HS terminal

- 0 = Active low (default)
- 1 = Active high

VS or VBLK:

- 0 = VS terminal outputs vertical sync (default)
- 1 = VS terminal outputs vertical blank

HS or CS:

- 0 = HS terminal outputs horizontal sync (default)
- 1 = HS terminal outputs composite sync

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2.11.28 Output Formatter 1 Register

| | |
|------------|-----|
| Subaddress | 33h |
| Default | 40h |

| | | | | | | | |
|---------------|------------------|-----------|----------|---|---------------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Sampling rate | YCbCr code range | CbCr code | Reserved | | Output format [2:0] | | |

Sampling rate (changing this bit causes the register settings to be reinitialized):

- 0 = ITU-R BT.601 sampling rate (default)
- 1 = Square pixel sampling rate

YCbCr output code range:

- 0 = ITU-R BT.601 coding range (Y ranges from 64 to 940. Cb and Cr range from 64 to 960.)
- 1 = Extended coding range (Y, Cb, and Cr range from 4 to 1016.) (default)

CbCr code format:

- 0 = Offset binary code (2s complement + 512) (default)
- 1 = Straight binary code (2s complement)

Output format [2:0]:

- 000 = 10-bit 4:2:2 (pixel x 2 rate) with embedded syncs (ITU-R BT.656) (default)
- 001 = 20-bit 4:2:2 (pixel rate) with separate syncs
- 010 = Reserved
- 011 = 10-bit 4:2:2 with separate syncs
- 100–111 = Reserved

NOTE: 10-bit mode is also used for the raw VBI output mode when bit 4 (VBI raw) in the luminance processing control 1 register at subaddress 06h is set (see Section 2.11.7).

2.11.29 Output Formatter 2 Register

| | |
|------------|-----|
| Subaddress | 34h |
| Default | 00h |

| | | | | | | | |
|----------|---|---|-------------|--------------------|---|--------------|--------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | Data enable | Black Screen [1:0] | | CLK polarity | Clock enable |

Data enable: Y[9:0] AND C[9:0] output enable

0 = Y[9:0] and C[9:0] high impedance (default)

1 = Y [9:0] and C[9:0] active

Black Screen [1:0]:

00 = Normal operation (default)

01 = Black screen out when TVP5147 detects lost lock (using with tuner input but not with VCR)

10 = Black screen out

11 = Black screen out

CLK polarity:

0 = Data clocked out on the falling edge of DATACLK (default)

1 = Data clocked out on the rising edge of DATACLK

Clock enable:

0 = DATACLK outputs are high-impedance (default).

1 = DATACLK outputs are enabled.

2.11.30 Output Formatter 3 Register

| | |
|------------|-----|
| Subaddress | 35h |
| Default | FFh |

| | | | | | | | |
|------------|---|------------|---|------------|---|-----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GPIO [1:0] | | AVID [1:0] | | GLCO [1:0] | | FID [1:0] | |

GPIO [1:0]: FSS terminal function select

00 = GPIO is logic 0 output.

01 = GPIO is logic 1 output.

10 = Reserved

11 = GPIO is logic input (default).

AVID [1:0]: AVID terminal function select

00 = AVID is logic 0 output.

01 = AVID is logic 1 output.

10 = AVID is active video indicator output.

11 = AVID is logic input (default).

GLCO [1:0]: GLCO terminal function select

00 = GLCO is logic 0 output.

01 = GLCO is logic 1 output.

10 = GCLO is genlock output.

11 = GCLO is logic input (default).

FID [1:0]: FID terminal function select

00 = FID is logic 0 output.

01 = FID is logic 1 output.

10 = FID is FID output.

11 = FID is logic input (default).

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2.11.31 Output Formatter 4 Register

| | |
|------------|-----|
| Subaddress | 36h |
| Default | FFh |

| | | | | | | | |
|---------------|---|-------------|---|-----------|---|-----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VS/VBLK [1:0] | | HS/CS [1:0] | | C_1 [1:0] | | C_0 [1:0] | |

VS/VBLK [1:0]: VS terminal function select

00 = VS/VBLK is logic 0 output.

01 = VS/VBLK is logic 1 output.

10 = VS/VBLK is vertical sync or vertical blank output corresponding to bit 1 (VS/VBLK) in the sync control register at subaddress 32h (see Section 2.11.27).

11 = VS/VBLK is logic input (default).

HS/CS [1:0]: HS terminal function select

00 = HS/CS is logic 0 output.

01 = HS/CS is logic 1 output.

10 = HS/CS is horizontal sync or composite sync output corresponding to bit 0 (HS/CS) in the sync control register at subaddress 32h (see Section 2.11.27).

11 = HS/CS is logic input (default).

C_1 [1:0]: C_1 terminal function select

00 = C_1 is logic 0 output.

01 = C_1 is logic 1 output.

10 = Reserved

11 = C_1 is logic input (default).

C_0 [1:0]: C_0 terminal function select

00 = C_0 is logic 0 output.

01 = C_0 is logic 1 output.

10 = Reserved

11 = C_0 is logic input (default).

C_x functions are only available in the 10-bit output mode.

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2.11.32 Output Formatter 5 Register

| | |
|------------|-----|
| Subaddress | 37h |
| Default | FFh |

| | | | | | | | |
|-----------|---|-----------|---|-----------|---|-----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| C_5 [1:0] | | C_4 [1:0] | | C_3 [1:0] | | C_2 [1:0] | |

C_5 [1:0]: C_5 terminal function select

- 00 = C_5 is logic 0 output.
- 01 = C_5 is logic 1 output.
- 10 = Reserved
- 11 = C_5 is logic input (default).

C_4 [1:0]: C_4 terminal function select

- 00 = C_4 is logic 0 output.
- 01 = C_4 is logic 1 output.
- 10 = Reserved
- 11 = C_4 is logic input (default).

C_3 [1:0]: C_3 terminal function select

- 00 = C_3 is logic 0 output.
- 01 = C_3 is logic 1 output.
- 10 = Reserved
- 11 = C_3 is logic input (default).

C_2 [1:0]: C_2 terminal function select

- 00 = C_2 is logic 0 output.
- 01 = C_2 is logic 1 output.
- 10 = Reserved
- 11 = C_2 is logic input (default).

C_x functions are only available in the 10-bit output mode.

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2.11.33 Output Formatter 6 Register

| | |
|------------|-----|
| Subaddress | 38h |
| Default | FFh |

| | | | | | | | |
|-----------|---|-----------|---|-----------|---|-----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| C_9 [1:0] | | C_8 [1:0] | | C_7 [1:0] | | C_6 [1:0] | |

C_9 [1:0]: C_9 terminal function select

- 00 = C_9 is logic 0 output.
- 01 = C_9 is logic 1 output.
- 10 = Reserved
- 11 = C_9 is logic input (default).

C_8 [1:0]: C_8 terminal function select

- 00 = C_8 is logic 0 output.
- 01 = C_8 is logic 1 output.
- 10 = Reserved
- 11 = C_8 is logic input (default).

C_7 [1:0]: C_7 terminal function select

- 00 = C_7 is logic 0 output.
- 01 = C_7 is logic 1 output.
- 10 = Reserved
- 11 = C_7 is logic input (default).

C_6 [1:0]: C_6 terminal function select

- 00 = C_6 is logic 0 output.
- 01 = C_6 is logic 1 output.
- 10 = Reserved
- 11 = C_6 is logic input (default).

C_x functions are only available in the 10-bit output mode.

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2.11.34 Clear Lost Lock Detect Register

| | |
|------------|-----|
| Subaddress | 39h |
| Default | 00h |

| | | | | | | | |
|----------|---|---|---|---|---|---|------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | Clear lost lock detect |

Clear lost lock detect: Clear bit 4 (lost lock detect) in the status 1 register at subaddress 3Ah (see Section 2.11.35)

- 0 = No effect (default)
- 1 = Clears bit 4 in the status 1 register

2.11.35 Status 1 Register

| | |
|------------|-----|
| Subaddress | 3Ah |
|------------|-----|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|-------------------------|-------------------|------------------|------------------------------|---------------------------|-----------------------------|---------------|
| Peak white detect status | Line-alternating status | Field rate status | Lost lock detect | Color subcarrier lock status | Vertical sync lock status | Horizontal sync lock status | TV/VCR status |

Peak white detect status:

- 0 = Peak white is not detected.
- 1 = Peak white is detected.

Line-alternating status:

- 0 = Nonline-alternating
- 1 = Line-alternating

Field rate status:

- 0 = 60 Hz
- 1 = 50 Hz

Lost lock detect:

- 0 = No lost lock since this bit was cleared.
- 1 = Lost lock since this bit was cleared.

Color subcarrier lock status:

- 0 = Color subcarrier is not locked.
- 1 = Color subcarrier is locked.

Vertical sync lock status:

- 0 = Vertical sync is not locked.
- 1 = Vertical sync is locked.

Horizontal sync lock status:

- 0 = Horizontal sync is not locked.
- 1 = Horizontal sync is locked.

TV/VCR status:

- 0 = TV
- 1 = VCR

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2.11.36 Status 2 Register

| | |
|------------|-----|
| Subaddress | 3Bh |
|------------|-----|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|-----------------------|---------------------|-----------------------|----------|-----------------------------|---|---|
| Signal present | Weak signal detection | PAL switch polarity | Field sequence status | Reserved | Macrovision detection [2:0] | | |

Signal present detection:

- 0 = Signal not present
- 1 = Signal present

Weak signal detection:

- 0 = No weak signal
- 1 = Weak signal mode

PAL switch polarity of first line of odd field:

- 0 = PAL switch is zero.
- 1 = PAL switch is one.

Field sequence status:

- 0 = Even field
- 1 = Odd field

Macrovision detection [2:0]:

- 000 = No copy protection
- 001 = AGC pulses/pseudo syncs present (type 1)
- 010 = 2-line color stripe only present
- 011 = AGC pulses/pseudo syncs and 2-line color stripe present (type 2)
- 100 = Reserved
- 101 = Reserved
- 110 = 4-line color stripe only present
- 111 = AGC pulses/pseudo syncs and 4-line color stripe present (type 3)

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2.11.37 AGC Gain Status Register

| | |
|------------|---------|
| Subaddress | 3Ch-3Dh |
|------------|---------|

Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-------------------|---|---|---|------------------|---|---|---|
| 3Ch | Fine gain [7:0] | | | | | | | |
| 3Dh | Coarse gain [3:0] | | | | Fine gain [11:8] | | | |

Fine gain [11:0]: This register provides the fine gain value of sync channel.

- 1111 1111 1111 = 1.9995
- 1000 0000 0000 = 1
- 0010 0000 0000 = 0.5

Coarse gain [3:0]: This register provides the coarse gain value of sync channel.

- 1111 = 2
- 0101 = 1
- 0000 = 0.5

These AGC gain status registers are updated automatically by the TVP5147 decoder with AGC on. In manual gain control mode, these register values are not updated by the TVP5147 decoder.

2.11.38 Video Standard Status Register

| | |
|------------|-----|
| Subaddress | 3Fh |
|------------|-----|

Read only

| | | | | | | | |
|------------|----------|---|---|----------------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Autoswitch | Reserved | | | Video standard [2:0] | | | |

Autoswitch mode:

- 0 = Stand-alone (forced video standard) mode
- 1 = Autoswitch mode

Video standard [2:0]:

| CVBS and S-video | Component video |
|------------------------------|-----------------|
| 000 = Reserved | Reserved |
| 001 = (M, J) NTSC | Component 525 |
| 010 = (B, D, G, H, I, N) PAL | Component 625 |
| 011 = (M) PAL | Reserved |
| 100 = (Combination-N) PAL | Reserved |
| 101 = NTSC 4.43 | Reserved |
| 110 = SECAM | Reserved |
| 111 = PAL 60 | Reserved |

This register contains information about the detected video standard that the device is currently operating. When autoswitch code is running, this register must be tested to determine which video standard has been detected.

2.11.39 GPIO Input 1 Register

| | |
|------------|-----|
| Subaddress | 40h |
|------------|-----|

Read only

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| C_7 | C_6 | C_5 | C_4 | C_3 | C_2 | C_1 | C_0 |

C_x input status:

- 0 = Input is a low.
- 1 = Input is a high.

These status bits are only valid when terminals are used as input and its states updated at every line.

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2.11.40 GPIO Input 2 Register

| | |
|------------|-----|
| Subaddress | 41h |
|------------|-----|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|----|----|-----|-----|-----|
| GPIO | AVID | GLCO | VS | HS | FID | C_9 | C_8 |

GPIO input terminal status:

- 0 = Input is a low.
- 1 = Input is a high.

AVID input terminal status:

- 0 = Input is a low.
- 1 = Input is a high.

GLCO input terminal status:

- 0 = Input is a low.
- 1 = Input is a high.

VS input terminal status:

- 0 = Input is a low.
- 1 = Input is a high.

HS input status:

- 0 = Input is a low.
- 1 = Input is a high.

FID input status:

- 0 = Input is a low.
- 1 = Input is a high.

C_x input status:

- 0 = Input is a low.
- 1 = Input is a high.

These status bits are only valid when terminals are used as input and its states updated at every line.

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2.11.41 Vertical Line Count Register

| | |
|------------|---------|
| Subaddress | 42h–43h |
|------------|---------|

Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---------------------|---|---|---|---|---------------------|---|---|
| 42h | Vertical line [7:0] | | | | | | | |
| 43h | Reserved | | | | | Vertical line [9:8] | | |

Vertical line [9:0] represents the detected total number of lines from the previous frame. This can be used with nonstandard video signals, such as a VCR in trick mode, to synchronize downstream video circuitry.

2.11.42 AFE Coarse Gain for CH 1 Register

| | |
|------------|-----|
| Subaddress | 46h |
| Default | 20h |

| | | | | | | | |
|---------------|---|---|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CGAIN 1 [3:0] | | | | Reserved | | | |

CGAIN 1 [3:0]: Coarse_Gain = 0.5 + (CGAIN 1)/10, where $0 \leq \text{CGAIN 1} \leq 15$

This register works only in manual gain control mode. When AGC is active, writing to any value is ignored.

1111 = 2
 1110 = 1.9
 1101 = 1.8
 1100 = 1.7
 1011 = 1.6
 1010 = 1.5
 1001 = 1.4
 1000 = 1.3
 0111 = 1.2
 0110 = 1.1
 0101 = 1
 0100 = 0.9
 0011 = 0.8
 0010 = 0.7 (default)
 0001 = 0.6
 0000 = 0.5

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2.11.43 AFE Coarse Gain for CH 2 Register

| | |
|------------|-----|
| Subaddress | 47h |
| Default | 20h |

| | | | | | | | |
|---------------|---|---|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CGAIN 2 [3:0] | | | | Reserved | | | |

CGAIN 2 [3:0]: Coarse_Gain = 0.5 + (CGAIN 2)/10, where $0 \leq \text{CGAIN 2} \leq 15$

This register works only in manual gain control mode. When AGC is active, writing to any value is ignored.

1111 = 2
 1110 = 1.9
 1101 = 1.8
 1100 = 1.7
 1011 = 1.6
 1010 = 1.5
 1001 = 1.4
 1000 = 1.3
 0111 = 1.2
 0110 = 1.1
 0101 = 1
 0100 = 0.9
 0011 = 0.8
 0010 = 0.7 (default)
 0001 = 0.6
 0000 = 0.5

2.11.44 AFE Coarse Gain for CH 3 Register

| | |
|------------|-----|
| Subaddress | 48h |
| Default | 20h |

| | | | | | | | |
|---------------|---|---|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CGAIN 3 [3:0] | | | | Reserved | | | |

CGAIN 3 [3:0]: Coarse_Gain = 0.5 + (CGAIN 3)/10, where 0 ≤ CGAIN 3 ≤ 15

This register works only in the manual gain control mode. When AGC is active, writing to any value is ignored.

- 1111 = 2
- 1110 = 1.9
- 1101 = 1.8
- 1100 = 1.7
- 1011 = 1.6
- 1010 = 1.5
- 1001 = 1.4
- 1000 = 1.3
- 0111 = 1.2
- 0110 = 1.1
- 0101 = 1
- 0100 = 0.9
- 0011 = 0.8
- 0010 = 0.7 (default)
- 0001 = 0.6
- 0000 = 0.5

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2.11.45 AFE Coarse Gain for CH 4 Register

| | |
|------------|-----|
| Subaddress | 49h |
| Default | 20h |

| | | | | | | | |
|---------------|---|---|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CGAIN 4 [3:0] | | | | Reserved | | | |

CGAIN 4 [3:0]: Coarse_Gain = 0.5 + (CGAIN 4)/10, where 0 ≤ CGAIN 4 ≤ 15

This register works only in the manual gain control mode. When AGC is active, writing to any value is ignored.

- 1111 = 2
- 1110 = 1.9
- 1101 = 1.8
- 1100 = 1.7
- 1011 = 1.6
- 1010 = 1.5
- 1001 = 1.4
- 1000 = 1.3
- 0111 = 1.2
- 0110 = 1.1
- 0101 = 1
- 0100 = 0.9
- 0011 = 0.8
- 0010 = 0.7 (default)
- 0001 = 0.6
- 0000 = 0.5

2.11.46 AFE Fine Gain for Pb Register

| | |
|------------|---------|
| Subaddress | 4Ah–4Bh |
| Default | 900h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---------------|---|---|---|----------------|---|---|---|
| 4Ah | FGAIN 1 [7:0] | | | | | | | |
| 4Bh | Reserved | | | | FGAIN 1 [11:8] | | | |

FGAIN 1 [11:0]: This fine gain applies to component Pb.

Fine_Gain = (1/2048) * FGAIN 1, where $0 \leq \text{FGAIN 1} \leq 4095$

This register works only in manual gain control mode. When AGC is active, writing to any value is ignored.

1111 1111 1111 = 1.9995
 1100 0000 0000 = 1.5
 1001 0000 0000 = 1.125 (default)
 1000 0000 0000 = 1
 0100 0000 0000 = 0.5
 0011 1111 1111 to 0000 0000 0000 = Reserved

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2.11.47 AFE Fine Gain for Y_Chroma Register

| | |
|------------|---------|
| Subaddress | 4Ch–4Dh |
| Default | 900h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---------------|---|---|---|----------------|---|---|---|
| 4Ch | FGAIN 2 [7:0] | | | | | | | |
| 4Dh | Reserved | | | | FGAIN 2 [11:8] | | | |

FGAIN 2 [11:0]: This gain applies to component Y channel or S-video chroma (see AFE fine gain for Pb register, Section 2.11.46).

This register works only in manual gain control mode. When AGC is active, writing to any value is ignored.

1111 1111 1111 = 1.9995
 1100 0000 0000 = 1.5
 1001 0000 0000 = 1.125 (default)
 1000 0000 0000 = 1
 0100 0000 0000 = 0.5
 0011 1111 1111 to 0000 0000 0000 = Reserved

2.11.48 AFE Fine Gain for Pr Register

| | |
|------------|---------|
| Subaddress | 4Eh–4Fh |
| Default | 900h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---------------|---|---|---|----------------|---|---|---|
| 4Eh | FGAIN 3 [7:0] | | | | | | | |
| 4Fh | Reserved | | | | FGAIN 3 [11:8] | | | |

FGAIN 3 [11:0]: This fine gain applies to component Pr (see AFE fine gain for Pb register, Section 2.11.46).

This register works only in manual gain control mode. When AGC is active, writing to any value is ignored.

1111 1111 1111 = 1.9995
 1100 0000 0000 = 1.5
 1001 0000 0000 = 1.125 (default)
 1000 0000 0000 = 1
 0100 0000 0000 = 0.5
 0011 1111 1111 to 0000 0000 0000 = Reserved

2.11.49 AFE Fine Gain for CVBS_Luma Register

| | |
|------------|---------|
| Subaddress | 50h–51h |
| Default | 900h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---------------|---|---|---|----------------|---|---|---|
| 50h | FGAIN 4 [7:0] | | | | | | | |
| 51h | Reserved | | | | FGAIN 4 [11:8] | | | |

FGAIN 4 [11:0]: This fine gain applies to CVBS or S-video luma (see AFE fine gain for Pb register, Section 2.11.46).

This register works only in manual gain control mode. When AGC is active, writing to any value is ignored.

- 1111 1111 1111 = 1.9995
- 1100 0000 0000 = 1.5
- 1001 0000 0000 = 1.125 (default)
- 1000 0000 0000 = 1
- 0100 0000 0000 = 0.5
- 0011 1111 1111 to 0000 0000 0000 = Reserved

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2.11.50 Field ID Control Register

| | |
|------------|-----|
| Subaddress | 57h |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|-------------|-------------|
| | | | | | | 656 version | FID control |

656 Version

- 0 = ITU-R BT.656-4 (default)
- 1 = ITU-R BT.656-3

FID control

- 0 = 0→1 adapts to field 1, 1→0 adapts to field 1+ field 2 (default)
- 1 = 0→1 adapts to field 2, 1→0 adapts to field 1+ field 2 (for TVP5147 EVM)

2.11.51 ROM Version Register

| | |
|------------|-----|
| Subaddress | 70h |
|------------|-----|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|---|---|---|---|---|---|
| ROM version [7:0] | | | | | | | |

ROM Version [7:0]: ROM revision number

2.11.52 AGC White Peak Processing Register

| | |
|------------|-----|
| Subaddress | 74h |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|---------------|---------------|-------------|----------------|---------------|---------------|
| Luma peak A | Reserved | Color burst A | Sync height A | Luma peak B | Composite peak | Color burst B | Sync height B |

Luma peak A: Use of the luma peak as a video amplitude reference for the back-end feed-forward type AGC algorithm.

- 0 = Enabled (default)
- 1 = Disabled

Color burst A: Use of the color burst amplitude as a video amplitude reference for the back end.

NOTE: Not available for SECAM, component, and B/W video sources.

- 0 = Enabled (default)
- 1 = Disabled

Sync height A: Use of the sync height as a video amplitude reference for the back-end feed-forward type AGC algorithm.

- 0 = Enabled (default)
- 1 = Disabled

Luma peak B: Use of the luma peak as a video amplitude reference for the front-end feedback type AGC algorithm.

- 0 = Enabled (default)
- 1 = Disabled

Composite peak: Use of the composite peak as a video amplitude reference for the front-end feedback type AGC algorithm.

NOTE: Required for CVBS video sources.

- 0 = Enabled (default)
- 1 = Disabled

Color burst B: Use of the color burst amplitude as a video amplitude reference for the front-end feedback type AGC algorithm.

NOTE: Not available for SECAM, component, and B/W video sources.

- 0 = Enabled (default)
- 1 = Disabled

Sync height B:

Use of the sync height as a video amplitude reference for the front-end feedback type AGC algorithm.

- 0 = Enabled (default)
- 1 = Disabled

NOTE: If all 4 bits of the lower nibble are set to logic 1 (that is, no amplitude reference selected), then the front-end analog and digital gains are automatically set to nominal values of 2 and 2304, respectively.

If all 4 bits of the upper nibble are set to logic 1 (that is, no amplitude reference selected), then the back-end gain is set automatically to unity.

If the input sync height is greater than 100% and the AGC-adjusted output video amplitude becomes less than 100%, then the back-end scale factor attempts to increase the contrast in the back end to restore the video amplitude to 100%.

2.11.53 F and V Bit Control Register

| | |
|------------|-----|
| Subaddress | 75h |
| Default | 12h |

| | | | | | | | |
|--------------|-----------|------------|-----------|---------------|----------|------------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 2 line delay | Stable HS | Line limit | Fast lock | F and V [1:0] | | Phase Det. | HPLL |

2-line delay: Enable bypass of internal 2-line delay when in VCR mode

- 0 = Disabled (default)
- 1 = Enabled

Stable HSYNC: Enable work around code which stabilizes horizontal sync in VCR mode

- 0 = Disabled (default)
- 1 = Enabled

Line limit: Enable ± 30 line limit from standard lines per frame on vertical sync PLL adjustment when vertical lock is true.

- 0 = Disabled (default)
- 1 = Enabled

Fast lock: Enable fast lock where vertical PLL is reset and a 2 sec timer is initialized when vertical lock is lost; during time-out the detected input VSYNC is output.

- 0 = Disabled
- 1 = Enabled (default)

F and V [1:0]

| F and V | Lines per frame | F bit | V bit |
|----------------|------------------|--------------|--------------------------|
| 00 = (default) | Standard | ITU-R BT 656 | ITU-R BT 656 |
| | Nonstandard-even | Forced to 1 | Switch at field boundary |
| | Nonstandard-odd | Toggles | Switch at field boundary |
| 01 = | Standard | ITU-R BT 656 | ITU-R BT 656 |
| | Nonstandard | Toggles | Switch at field boundary |
| 10 = | Standard | ITU-R BT 656 | ITU-R BT 656 |
| | Nonstandard | Pulsed mode | Switch at field boundary |
| 11 = | Reserved | | |

Phase Detector: Enable integral window phase detector

- 0 = Disabled
- 1 = Enabled (default)

HPLL Enable horizontal PLL to free run

- 0 = Disabled (default)
- 1 = Enabled

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2.11.54 VCR Trick Mode Control Register

| | |
|------------|-----|
| Subaddress | 76h |
| Default | 8Ah |

| | | | | | | | |
|---------------|---|----------------------------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Switch header | | Horizontal shake threshold [6:0] | | | | | |

Switch header: When in VCR trick mode, the header noisy area around the head switch is skipped.

0 = Disabled

1 = Enabled (default)

Horizontal shake threshold [6:0]:

000 0000 = Zero threshold

000 1010 = 0Ah (default)

111 1111 = Largest threshold

2.11.55 Horizontal Shake Increment Register

| | |
|------------|-----|
| Subaddress | 77h |
| Default | 64h |

| | | | | | | | |
|----------------------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Horizontal shake increment [7:0] | | | | | | | |

Horizontal shake increment [7:0]:

000 0000 = 0

000 1010 = 64h (default)

111 1111 = FFh

2.11.56 AGC Increment Speed Register

| | |
|------------|-----|
| Subaddress | 78h |
| Default | 06h |

| | | | | | | | |
|----------|---|---|---|---|---------------------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | AGC increment speed [3:0] | | |

AGC increment speed: Adjusts gain increment speed.

111 = 7 (slowest)

110 = 6 (default)

⋮

000 = 0 (fastest)

2.11.57 AGC Increment Delay Register

| | |
|------------|-----|
| Subaddress | 79h |
| Default | 1Eh |

| | | | | | | | |
|---------------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AGC increment delay [7:0] | | | | | | | |

AGC increment delay: Number of frames to delay gain increments

1111 1111 = 255

⋮

0001 1110 = 30 (default)

⋮

0000 0000 = 0

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2.11.58 Analog Output Control 1 Register

| | |
|------------|-----|
| Subaddress | 7Fh |
| Default | 00h |

| | | | | | | | |
|----------|---|---|---|------------|---|--------------|----------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | AGC enable | | Input select | Analog Output enable |

AGC enable:

- 0 = Enabled (default)
- 1 = Disabled, manual gain mode (see Section 2.12.10)

Input select:

- 00 = Input selected by TVP5147 decoder, (see Section 2.11.1) (default)
- 01 = Input selected manually (see Section 2.12.10)

Analog output enable:

- 0 = VI_1_A is input (default).
- 1 = VI_1_A is analog video output.

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2.11.59 Chip ID MSB Register

| | |
|------------|-----|
| Subaddress | 80h |
|------------|-----|

Read only

| | | | | | | | |
|-------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Chip ID MSB [7:0] | | | | | | | |

Chip ID MSB [7:0]: This register identifies the MSB of the device ID. Value = 51h

2.11.60 Chip ID LSB Register

| | |
|------------|-----|
| Subaddress | 81h |
|------------|-----|

Read only

| | | | | | | | |
|-------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Chip ID LSB [7:0] | | | | | | | |

Chip ID LSB [7:0]: This register identifies the LSB of the device ID. Value = 47h

2.11.61 VDP TTX Filter And Mask Registers

| | | | | | | | | | | |
|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Subaddress | B1h | B2h | B3h | B4h | B5h | B6h | B7h | B8h | B9h | BAh |
| Default | 00h | 00h | 00h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|------------|-----------------|---|---|---|---|--------------------|---|---|--|
| B1h | Filter 1 mask 1 | | | | | Filter 1 pattern 1 | | | |
| B2h | Filter 1 mask 2 | | | | | Filter 1 pattern 2 | | | |
| B3h | Filter 1 mask 3 | | | | | Filter 1 pattern 3 | | | |
| B4h | Filter 1 mask 4 | | | | | Filter 1 pattern 4 | | | |
| B5h | Filter 1 mask 5 | | | | | Filter 1 pattern 5 | | | |
| B6h | Filter 2 mask 1 | | | | | Filter 2 pattern 1 | | | |
| B7h | Filter 2 mask 2 | | | | | Filter 2 pattern 2 | | | |
| B8h | Filter 2 mask 3 | | | | | Filter 2 pattern 3 | | | |
| B9h | Filter 2 mask 4 | | | | | Filter 2 pattern 4 | | | |
| BAh | Filter 2 mask 5 | | | | | Filter 2 pattern 5 | | | |

For an NABTS system, the packet prefix consists of five bytes. Each byte contains 4 data bits (D[3:0]) interlaced with 4 Hamming protection bits (H[3:0]):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D[3] | H[3] | D[2] | H[2] | D[1] | H[1] | D[0] | H[0] |

Only data portion D[3:0] from each byte is applied to a teletext filter function with corresponding pattern bits P[3:0] and mask bits M[3:0]. The filter ignores the Hamming protection bits.

For WST system (PAL or NTSC), the packet prefix consists of two bytes. The two bytes contain three bits of magazine number (M[2:0]) and five bits of row address (R[4:0]), interlaced with eight Hamming protection bits H[7:0]:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R[0] | H[3] | M[2] | H[2] | M[1] | H[1] | M[0] | H[0] |
| R[4] | H[7] | R[3] | H[6] | R[2] | H[5] | R[1] | H[4] |

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of mask 1 means that the filter module must compare the LSB of nibble 1 in the pattern register to the first data bit on the transaction. If these match, then a true result is returned. A 0 in a bit of mask means that the filter module must ignore that data bit of the transaction. If all 0s are programmed in the mask bits, then the filter matches all patterns returning a true result (default 00h).

2.11.62 VDP TTX Filter Control Register

| | |
|------------|-----|
| Subaddress | BBh |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|--------------------|---|------|---------------------|---------------------|
| Reserved | | | Filter logic [1:0] | | Mode | TTX filter 2 enable | TTX filter 1 enable |

Filter logic [1:0]: Allow different logic to be applied when combining the decision of filter 1 and filter 2 as follows:

- 00 = NOR (default)
- 01 = NAND
- 10 = OR
- 11 = AND

Mode: indicates which teletext mode is in use.

- 0 = Teletext filter applies to 2 header bytes (default)
- 1 = Teletext filter applies to 5 header bytes

TTX filter 2 enable: provides for enabling the teletext filter function within the VDP.

- 0 = Disabled (default)
- 1 = Enabled

TTX filter 1 enable: provides for enabling the teletext filter function within the VDP.

- 0 = Disabled (default)
- 1 = Enabled

If the filter matches or if the filter mask is all 0s, then a true result is returned.

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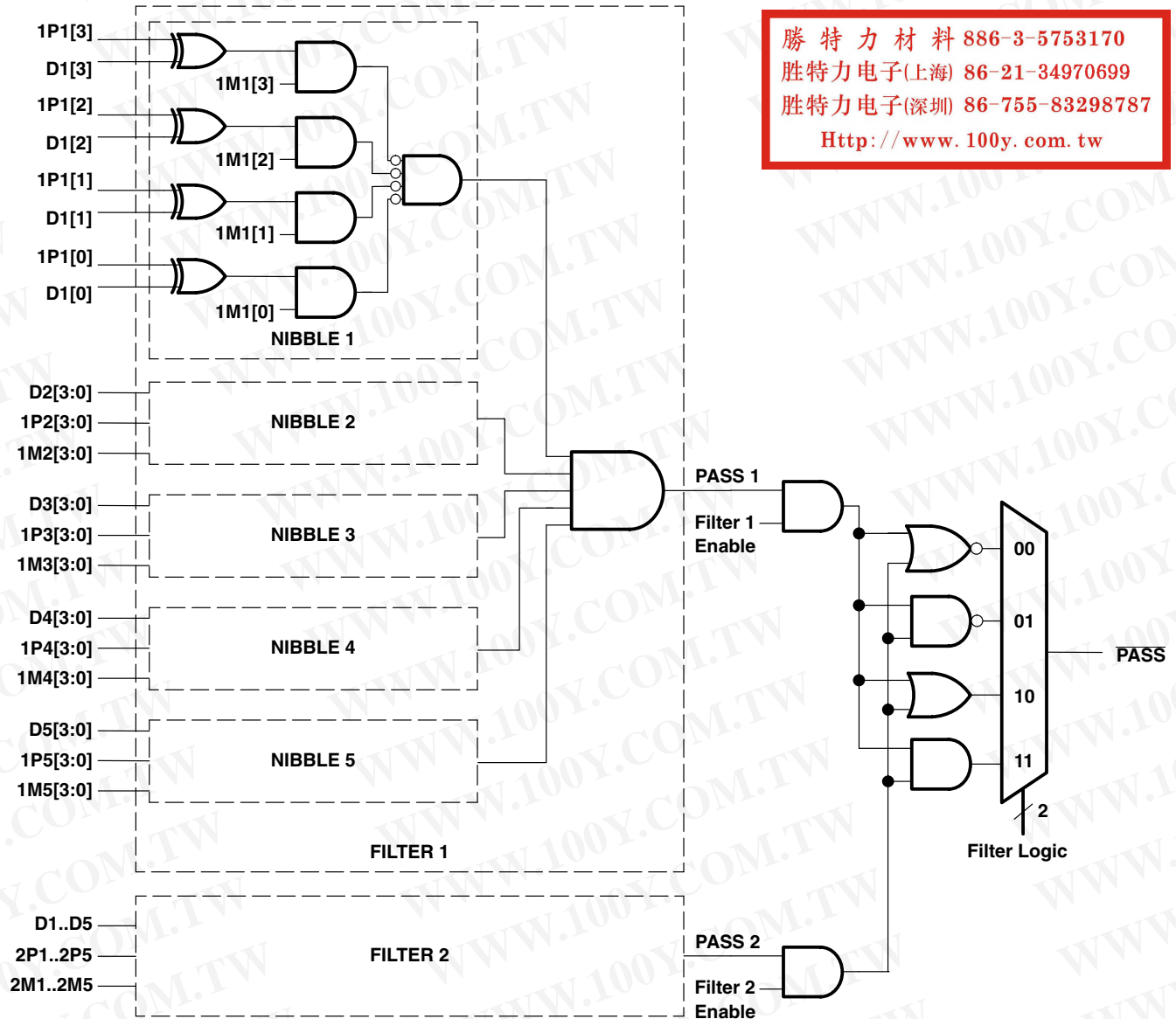


Figure 2–25. Teletext Filter Function

2.11.63 VDP FIFO Word Count Register

| | |
|------------|-----|
| Subaddress | BCh |
|------------|-----|

Read only

| | | | | | | | |
|-----------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIFO word count [7:0] | | | | | | | |

FIFO word count [7:0]: This register provides the number of words in the FIFO.

NOTE: 1 word equals 2 bytes.

2.11.64 VDP FIFO Interrupt Threshold Register

| | |
|------------|-----|
| Subaddress | BDh |
| Default | 80h |

| | | | | | | | |
|-----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Threshold [7:0] | | | | | | | |

Threshold [7:0]: This register is programmed to trigger an interrupt when the number of words in the FIFO exceeds this value.

NOTE: 1 word equals 2 bytes.

2.11.65 VDP FIFO Reset Register

| | |
|------------|-----|
| Subaddress | BFh |
| Default | 00h |

| | | | | | | | |
|----------|---|---|---|---|---|---|------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | FIFO reset |

FIFO reset: Writing any data to this register clears the FIFO and VDP data register (CC, WSS, VITC and VPS). After clearing, this register is automatically cleared.

2.11.66 VDP FIFO Output Control Register

| | |
|------------|-----|
| Subaddress | C0h |
| Default | 00h |

| | | | | | | | |
|----------|---|---|---|---|---|---|--------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | Host access enable |

Host access enable: This register is programmed to allow the host port access to the FIFO or to allow all VDP data to go out the video output.

0 = Output FIFO data to the video output Y[9:2] (default)

1 = Allow host port access to the FIFO data

2.11.67 VDP Line Number Interrupt Register

| | |
|------------|-----|
| Subaddress | C1h |
| Default | 00h |

| | | | | | | | |
|----------------|----------------|-------------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field 1 enable | Field 2 enable | Line number [5:0] | | | | | |

Field 1 interrupt enable:

0 = Disabled (default)

1 = Enabled

Field 2 interrupt enable:

0 = Disabled (default)

1 = Enabled

Line number [5:0]: Interrupt line number (default 00h)

This register is programmed to trigger an interrupt when the video line number exceeds this value in bits [5:0]. This interrupt must be enabled at address F4h.

NOTE: The line number value of 0 or 1 is invalid and does not generate an interrupt.

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Functional Description

2.11.68 VDP Pixel Alignment Register

| | |
|------------|---------|
| Subaddress | C2h–C3h |
| Default | 01Eh |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----------------------|---|---|---|---|---|-----------------------|---|
| C2h | Pixel alignment [7:0] | | | | | | | |
| C3h | Reserved | | | | | | Pixel alignment [9:8] | |

Pixel alignment [9:8]: These registers form a 10-bit horizontal pixel position from the falling edge of horizontal sync, where the VDP controller initiates the program from one line standard to the next line standard, for example, the previous line of teletext to the next line of closed caption. This value must be set so that the switch occurs after the previous transaction has cleared the delay in the VDP, but early enough to allow the new values to be programmed before the current settings are required.

The default value is 0x1E and has been tested with every standard supported here. A new value is needed only if a custom standard is in use.

2.11.69 VDP Line Start Register

| | |
|------------|-----|
| Subaddress | D6h |
| Default | 06h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|---|---|---|---|---|---|---|
| VDP line start [7:0] | | | | | | | |

VDP line start [7:0]: Set the VDP line starting address
 This register must be set properly before enabling the line mode registers. The VDP processor works only the VBI region set by this register and the VDP line stop register.

2.11.70 VDP Line Stop Register

| | |
|------------|-----|
| Subaddress | D7h |
| Default | 1Bh |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|---|---|---|---|---|---|---|
| VDP line stop [7:0] | | | | | | | |

VDP line stop [7:0]: Set the VDP stop line address

2.11.71 VDP Global Line Mode Register

| | |
|------------|-----|
| Subaddress | D8h |
| Default | FFh |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------------|---|---|---|---|---|---|---|
| Global line mode [7:0] | | | | | | | |

Global line mode [7:0]: VDP processing for multiple lines set by the VDP start line register at subaddress D6h and the VDP stop line register at subaddress D7h.
 Global line mode register has the same bit definition as the general line mode registers.
 General line mode has priority over the global line mode.

2.11.72 VDP Full Field Enable Register

| | |
|------------|-----|
| Subaddress | D9h |
| Default | 00h |

| | | | | | | | |
|----------|---|---|---|---|---|---|-------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | Full field enable |

Full field enable:

- 0 = Disabled full field mode (default)
- 1 = Enabled full field mode

This register enables the full field mode. In this mode, all lines outside the vertical blank area and all lines in the line mode register programmed with FFh are sliced with the definition of the VDP full field mode register at subaddress DAh. Values other than FFh in the line mode registers allow a different slice mode for that particular line.

2.11.73 VDP Full Field Mode Register

| | |
|------------|-----|
| Subaddress | DAh |
| Default | FFh |

| | | | | | | | |
|-----------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Full field mode [7:0] | | | | | | | |

Full field mode [7:0]:

This register programs the specific VBI standard for full field mode. It can be any VBI standard. Individual line settings take priority over the full field register. This allows each VBI line to be programmed independently but have the remaining lines in full field mode. The full field mode register has the same bit definition as line mode registers (default FFh).

Global line mode has priority over the full field mode.

2.11.74 VBUS Data Access With No VBUS Address Increment Register

| | |
|------------|-----|
| Subaddress | E0h |
| Default | 00h |

| | | | | | | | |
|-----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBUS data [7:0] | | | | | | | |

VBUS data [7:0]: VBUS data register for VBUS single-byte read/write transaction.

2.11.75 VBUS Data Access With VBUS Address Increment Register

| | |
|------------|-----|
| Subaddress | E1h |
| Default | 00h |

| | | | | | | | |
|-----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBUS data [7:0] | | | | | | | |

VBUS data [7:0]: VBUS data register for VBUS multibyte read/write transaction. VBUS address is autoincremented after each data byte read/write.

2.11.76 FIFO Read Data Register

| | |
|------------|-----|
| Subaddress | E2h |
|------------|-----|

Read only

| | | | | | | | |
|----------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIFO read data [7:0] | | | | | | | |

FIFO read data [7:0]: This register is provided to access VBI FIFO data through the I²C interface. All forms of teletext data come directly from the FIFO, while all other forms of VBI data can be programmed to come from registers or from the FIFO. If the host port is to be used to read data from the FIFO, then bit 0 (host access enable) in the VDP FIFO output control register at subaddress C0h must be set to 1 (see Section 2.11.66).

2.11.77 VBUS Address Access Register

| | | | |
|------------|-----|-----|-----|
| Subaddress | E8h | E9h | EAh |
| Default | 00h | 00h | 00h |

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|----------------------|---|---|---|---|---|---|---|
| E8h | VBUS address [7:0] | | | | | | | |
| E9h | VBUS address [15:8] | | | | | | | |
| EAh | VBUS address [23:16] | | | | | | | |

VBUS address [23:0]: VBUS is a 24-bit wide internal bus. The user needs to program in these registers the 24-bit address of the internal register to be accessed via host port indirect access mode.

2.11.78 Interrupt Raw Status 0 Register

| | |
|------------|-----|
| Subaddress | F0h |
|------------|-----|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|-----|-----|------|-------|-------|------|
| FIFO THRS | TTX | WSS | VPS | VITC | CC F2 | CC F1 | Line |

FIFO THRS: FIFO threshold passed, unmasked

- 0 = Not passed
- 1 = Passed

TTX: Teletext data available unmasked

- 0 = Not available
- 1 = Available

WSS: WSS data available unmasked

- 0 = Not available
- 1 = Available

VPS: VPS data available unmasked

- 0 = Not available
- 1 = Available

VITC: VITC data available unmasked

- 0 = Not available
- 1 = Available

CC F2: CC field 2 data available unmasked

- 0 = Not available
- 1 = Available

CC F1: CC field 1 data available unmasked

- 0 = Not available
- 1 = Available

Line: Line number interrupt unmasked

- 0 = Not available
- 1 = Available

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The host interrupt raw status 0 and 1 registers represent the interrupt status without applying mask bits.

2.11.79 Interrupt Raw Status 1 Register

| | |
|------------|-----|
| Subaddress | F1h |
|------------|-----|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|----------|----------------------------|------------------|-----------|
| Reserved | | | | H/V lock | Macrovision status changed | Standard changed | FIFO full |

H/V lock: unmasked

- 0 = H/V lock status unchanged
- 1 = H/V lock status changed

Macrovision status changed: unmasked

- 0 = Macrovision status unchanged
- 1 = Macrovision status changed

Standard changed: unmasked

- 0 = Video standard unchanged
- 1 = Video standard changed

FIFO full: unmasked

- 0 = FIFO not full
- 1 = FIFO was full during write to FIFO

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The FIFO full error flag is set when the current line of VBI data cannot enter the FIFO. For example, if the FIFO has only 10 bytes left and teletext is the current VBI line, then the FIFO full error flag is set, but no data is written because the entire teletext line does not fit. However, if the next VBI line is closed caption requiring only 2 bytes of data plus the header, then this goes into the FIFO even if the full error flag is set.

2.11.80 Interrupt Status 0 Register

| | |
|------------|-----|
| Subaddress | F2h |
|------------|-----|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|-----|-----|------|-------|-------|------|
| FIFO THRS | TTX | WSS | VPS | VITC | CC F2 | CC F1 | Line |

FIFO THRS: FIFO threshold passed, masked

- 0 = Not passed
- 1 = Passed

TTX: Teletext data available masked

- 0 = Not available
- 1 = Available

WSS: WSS data available masked

- 0 = Not available
- 1 = Available

VPS: VPS data available masked

- 0 = Not available
- 1 = Available

VITC: VITC data available masked

- 0 = Not available
- 1 = Available

CC F2: CC field 2 data available masked

- 0 = Not available
- 1 = Available

CC F1: CC field 1 data available masked

- 0 = Not available
- 1 = Available

Line: Line number interrupt masked

- 0 = Not available
- 1 = Available

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The interrupt status 0 and 1 registers represent the interrupt status after applying mask bits. Therefore, the status bits are the result of a logical AND between the raw status and mask bits. The external interrupt terminal is derived from this register as an OR function of all nonmasked interrupts in this register.

Reading data from the corresponding register does not clear the status flags automatically. These flags are reset using the corresponding bits in interrupt clear 0 and 1 registers.

2.11.81 Interrupt Status 1 Register

| | |
|------------|-----|
| Subaddress | F3h |
|------------|-----|

Read only

| | | | | | | | |
|----------|---|---|---|----------|----------------------------|------------------|-----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | H/V lock | Macrovision status changed | Standard changed | FIFO full |

H/V lock: H/V lock status changed mask

- 0 = H/V lock status unchanged
- 1 = H/V lock status changed

Macrovision status changed: Macrovision status changed masked

- 0 = Macrovision status not changed
- 1 = Macrovision status changed

Standard changed: Standard changed masked

- 0 = Video standard not changed
- 1 = Video standard changed

FIFO full: full status of FIFO masked

- 0 = FIFO not full
- 1 = FIFO was full during write to FIFO, see the interrupt mask 1 register at subaddress F5h for details (see Section 2.11.83)

2.11.82 Interrupt Mask 0 Register

| | |
|------------|-----|
| Subaddress | F4h |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|-----|-----|------|-------|-------|------|
| FIFO THRS | TTX | WSS | VPS | VITC | CC F2 | CC F1 | Line |

FIFO THRS: FIFO threshold passed mask

- 0 = Disabled (default)
- 1 = Enabled FIFO_THRES interrupt

TTX: Teletext data available mask

- 0 = Disabled (default)
- 1 = Enabled TTX available interrupt

WSS: WSS data available mask

- 0 = Disabled (default)
- 1 = Enabled WSS available interrupt

VPS: VPS data available mask

- 0 = Disabled (default)
- 1 = Enabled VPS available interrupt

VITC: VITC data available mask

- 0 = Disabled (default)
- 1 = Enabled VITC available interrupt

CC F2: CC field 2 data available mask

- 0 = Disabled (default)
- 1 = Enabled CC_field 2 available interrupt

CC F1: CC field 1 data available mask

- 0 = Disabled (default)
- 1 = Enabled CC_field 1 available interrupt

Line: Line number interrupt mask

- 0 = Disabled (default)
- 1 = Enabled Line_INT interrupt

The host interrupt mask 0 and 1 registers can be used by the external processor to mask unnecessary interrupt sources for the interrupt status 0 and 1 register bits, and for the external interrupt terminal. The external interrupt is generated from all nonmasked interrupt flags.

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2.11.83 Interrupt Mask 1 Register

| | |
|------------|-----|
| Subaddress | F5h |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|----------|----------------------------|------------------|-----------|
| Reserved | | | | H/V lock | Macrovision status changed | Standard changed | FIFO full |

H/V lock: H/V lock status changed masked

- 0 = H/V lock status unchanged (default)
- 1 = H/V lock status changed

Macrovision status changed: Macrovision status changed mask

- 0 = Macrovision status unchanged
- 1 = Macrovision status changed

Standard changed: Standard changed mask

- 0 = Disabled (default)
- 1 = Enabled video standard changed

FIFO full: FIFO full mask

- 0 = Disabled (default)
- 1 = Enabled FIFO full interrupt

2.11.84 Interrupt Clear 0 Register

| | |
|------------|-----|
| Subaddress | F6h |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----|-----|-----|------|-------|-------|------|
| FIFO THRS | TTX | WSS | VPS | VITC | CC F2 | CC F1 | Line |

FIFO THRS: FIFO threshold passed clear

- 0 = No effect (default)
- 1 = Clear bit 7 (FIFO_THRS) in the interrupt status 0 register at subaddress F2h

TTX: Teletext data available clear

- 0 = No effect (default)
- 1 = Clear bit 6 (TTX available) in the interrupt status 0 register at subaddress F2h

WSS: WSS data available clear

- 0 = No effect (default)
- 1 = Clear bit 5 (WSS available) in the interrupt status 0 register at subaddress F2h

VPS: VPS data available clear

- 0 = No effect (default)
- 1 = Clear bit 4 (VPS available) in the interrupt status 0 register at subaddress F2h

VITC: VITC data available clear

- 0 = Disabled (default)
- 1 = Clear bit 3 (VITC available) in the interrupt status 0 register at subaddress F2h

CC F2: CC field 2 data available clear

- 0 = Disabled (default)
- 1 = Clear bit 2 (CC field 2 available) in the interrupt status 0 register at subaddress F2h

CC F1: CC field 1 data available clear

- 0 = Disabled (default)
- 1 = Clear bit 1 (CC field 1 available) in the interrupt status 0 register at subaddress F2h

Line: Line number interrupt clear

0 = Disabled (default)

1 = Clear bit 0 (line interrupt available) in the interrupt status 0 register at subaddress F2h

The host interrupt clear 0 and 1 registers are used by the external processor to clear the interrupt status bits in the host interrupt status 0 and 1 registers. When no nonmasked interrupts remain set in the registers, the external interrupt terminal also becomes inactive.

2.11.85 Interrupt Clear 1 Register

| | |
|------------|-----|
| Subaddress | F7h |
| Default | 00h |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|----------|----------------------------|------------------|-----------|
| Reserved | | | | H/V lock | Macrovision status changed | Standard changed | FIFO full |

H/V lock: Clear H/V lock status changed flag

0 = H/V lock status unchanged

1 = H/V lock status changed

Macrovision status changed: Clear Macrovision status changed flag

0 = No effect (default)

1 = Clear bit 2 (Macrovision status changed) in the interrupt status 1 register at subaddress F3h and the interrupt raw status 1 register at subaddress F1h

Standard changed: Clear standard changed flag

0 = No effect (default)

1 = Clear bit 1 (video standard changed) in the interrupt status 1 register at subaddress F3h and the interrupt raw status 1 register at subaddress F1h

FIFO full: Clear FIFO full flag

0 = No effect (default)

1 = Clear bit 0 (FIFO full flag) in the interrupt status 1 register at subaddress F3h and the interrupt raw status 1 register at subaddress F1h

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2.12 VBUS Register Definitions

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2.12.1 VDP Closed Caption Data Register

| | |
|------------|-------------------|
| Subaddress | 80 051Ch–80 051Fh |
|------------|-------------------|

Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-------------------------------|---|---|---|---|---|---|---|
| 80 051Ch | Closed caption field 1 byte 1 | | | | | | | |
| 80 051Dh | Closed caption field 1 byte 2 | | | | | | | |
| 80 051Eh | Closed caption field 2 byte 1 | | | | | | | |
| 80 051Fh | Closed caption field 2 byte 2 | | | | | | | |

These registers contain the closed caption data arranged in bytes per field.

2.12.2 VDP WSS Data Register

| | |
|------------|-------------------|
| Subaddress | 80 0520h–80 0526h |
|------------|-------------------|

WSS NTSC (CGMS):

Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte |
|------------|----------|-----|-----|-----|-----|-----|-----|-----|--------------------|
| 80 0520h | | | b5 | b4 | b3 | b2 | b1 | b0 | WSS field 1 byte 1 |
| 80 0521h | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | WSS field 1 byte 2 |
| 80 0522h | | | b19 | b18 | b17 | b16 | b15 | b14 | WSS field 1 byte 3 |
| 80 0523h | Reserved | | | | | | | | |
| 80 0524h | | | b5 | b4 | b3 | b2 | b1 | b0 | WSS field 2 byte 1 |
| 80 0525h | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | WSS field 2 byte 2 |
| 80 0526h | | | b19 | b18 | b17 | b16 | b15 | b14 | WSS field 2 byte 3 |

These registers contain the wide screen signaling data for NTSC.

- Bits 0–1 represent word 0, aspect ratio
- Bits 2–5 represent word 1, header code for word 2
- Bits 6–13 represent word 2, copy control
- Bits 14–19 represent word 3, CRC

PAL/SECAM:

Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Byte |
|------------|----------|----|-----|-----|-----|-----|----|----|--------------------|
| 80 0520h | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | WSS field 1 byte 1 |
| 80 0521h | | | b13 | b12 | b11 | b10 | b9 | b8 | WSS field 1 byte 2 |
| 80 0522h | Reserved | | | | | | | | |
| 80 0523h | Reserved | | | | | | | | |
| 80 0524h | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | WSS field 2 byte 1 |
| 80 0525h | | | b13 | b12 | b11 | b10 | b9 | b8 | WSS field 2 byte 2 |
| 80 0526h | Reserved | | | | | | | | |

PAL/SECAM:

- Bits 0–3 represent group 1, aspect ratio
- Bits 4–7 represent group 2, enhanced services
- Bits 8–10 represent group 3, subtitles
- Bits 11–13 represent group 4, others

2.12.3 VDP VITC Data Register

| | |
|------------|-------------------|
| Subaddress | 80 052Ch-80 0534h |
|------------|-------------------|

Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---------------------|---|---|---|---|---|---|---|
| 80 052Ch | VITC frame byte 1 | | | | | | | |
| 80 052Dh | VITC frame byte 2 | | | | | | | |
| 80 052Eh | VITC seconds byte 1 | | | | | | | |
| 80 052Fh | VITC seconds byte 2 | | | | | | | |
| 80 0530h | VITC minutes byte 1 | | | | | | | |
| 80 0531h | VITC minutes byte 2 | | | | | | | |
| 80 0532h | VITC hours byte 1 | | | | | | | |
| 80 0533h | VITC hours byte 2 | | | | | | | |
| 80 0534h | VITC CRC byte | | | | | | | |

These registers contain the VITC data.

2.12.4 VDP V-Chip TV Rating Block 1 Register

| | |
|------------|----------|
| Subaddress | 80 0540h |
|------------|----------|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|------|------|----------|------|------|------|----------|
| Reserved | 14-D | PG-D | Reserved | MA-L | 14-L | PG-L | Reserved |

TV parental guidelines rating block 1:

- 14-D: When incoming video program is TV-14-D rated then this bit is set high
- PG-D: When incoming video program is TV-PG-D rated then this bit is set high
- MA-L: When incoming video program is TV-MA-L rated then this bit is set high
- 14-L: When incoming video program is TV-14-L rated then this bit is set high
- PG-L: When incoming video program is TV-PG-L rated then this bit is set high

2.12.5 VDP V-Chip TV Rating Block 2 Register

| | |
|------------|----------|
| Subaddress | 80 0541h |
|------------|----------|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|----------|------|------|------|-------|
| MA-S | 14-S | PG-S | Reserved | MA-V | 14-V | PG-V | Y7-FV |

TV parental guidelines rating block 2:

- MA-S: When incoming video program is TV-MA-S rated then this bit is set high
- 14-S: When incoming video program is TV-14-S rated then this bit is set high
- PG-S: When incoming video program is TV-PG-S rated then this bit is set high
- MA-V: When incoming video program is TV-MA-V rated then this bit is set high
- 14-V: When incoming video program is TV-14-V rated then this bit is set high
- PG-V: When incoming video program is TV-PG-S rated then this bit is set high
- Y7-FV: When incoming video program is TV-Y7-FV rated then this bit is set high

Functional Description

2.12.6 VDP V-Chip TV Rating Block 3 Register

| | |
|------------|----------|
| Subaddress | 80 0542h |
|------------|----------|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------|-------|-------|------|-------|------|------|
| None | TV-MA | TV-14 | TV-PG | TV-G | TV-Y7 | TV-Y | None |

TV parental guidelines rating block 3:

None: no block intended

TV-MA: When incoming video program is TV-MA rated in TV parental guidelines rating then this bit is set high

TV-14: When incoming video program is TV-14 rated in TV parental guidelines rating then this bit is set high

TV-PG: When incoming video program is TV-PG rated in TV parental guidelines rating then this bit is set high

TV-G: When incoming video program is TV-G rated in TV parental guidelines rating then this bit is set high

TV-Y7: When incoming video program is TV-Y7 rated in TV parental guidelines rating then this bit is set high

TV-Y: When incoming video program is TV-G rated in TV parental guidelines rating then this bit is set high

None: no block intended

2.12.7 VDP V-CHIP MPAA Rating Data Register

| | |
|------------|----------|
| Subaddress | 80 0543h |
|------------|----------|

Read only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|-------|---|-------|----|---|-----|
| Not Rated | X | NC-17 | R | PG-13 | PG | G | N/A |

MPAA rating block (E5h):

Not rated: When incoming video program is not rated in MPAA rating then this bit is set high

X: When incoming video program is X rated in MPAA rating then this bit is set high

NC-17: When incoming video program is NC-17 rated in MPAA rating then this bit is set high

R: When incoming video program is R rated in MPAA rating then this bit is set high

PG-13: When incoming video program is PG-13 rated in MPAA rating then this bit is set high

PG: When incoming video program is PG rated in MPAA rating then this bit is set high

G: When incoming video program is G rated in MPAA rating then this bit is set high

N/A: When incoming video program is N/A rated in MPAA rating then this bit is set high

2.12.8 VDP General Line Mode and Line Address Register

| | |
|------------|-------------------|
| Subaddress | 80 0600h–80 0611h |
|------------|-------------------|

(default line mode = FFh, address = 00h)

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|----------------|
| 80 0600h | | | | | | | | Line address 1 |
| 80 0601h | | | | | | | | Line mode 1 |
| 80 0602h | | | | | | | | Line address 2 |
| 80 0603h | | | | | | | | Line mode 2 |
| 80 0604h | | | | | | | | Line address 3 |
| 80 0605h | | | | | | | | Line mode 3 |
| 80 0606h | | | | | | | | Line address 4 |
| 80 0607h | | | | | | | | Line mode 4 |
| 80 0608h | | | | | | | | Line address 5 |
| 80 0609h | | | | | | | | Line mode 5 |
| 80 060Ah | | | | | | | | Line address 6 |
| 80 060Bh | | | | | | | | Line mode 6 |
| 80 060Ch | | | | | | | | Line address 7 |
| 80 060Dh | | | | | | | | Line mode 7 |
| 80 060Eh | | | | | | | | Line address 8 |
| 80 060Fh | | | | | | | | Line mode 8 |
| 80 0610h | | | | | | | | Line address 9 |
| 80 0611h | | | | | | | | Line mode 9 |

Line address [7:0]: Line number to be processed by a VDP set by a line mode register (default 00h)

Line mode register [7:0]:

- Bit 7: 0 = Disabled filters
 1 = Enabled filters for teletext and CC (null byte filter) (default)
- Bit 6: 0 = Send sliced VBI data to registers only (default)
 1 = Send sliced VBI data to FIFO and registers, teletext data only goes to FIFO (default)
- Bit 5: 0 = Allow VBI data with errors in the FIFO
 1 = Do not allow VBI data with errors in the FIFO (default)
- Bit 4: 0 = Disabled error detection and correction
 1 = Enabled error detection and correction (teletext only) (default)
- Bit 3: 0 = Field 1
 1 = Field 2 (default)
- Bits [2:0]: 000 = Teletext (WST625, Chinese teletext, NABTS 525)
 001 = CC (US, Europe, Japan, China)
 010 = WSS (525, 625)
 011 = VITC
 100 = VPS/PDC (PAL only), Gemstar (NTSC only)
 101 = USER 1
 110 = USER 2
 111 = Reserved (active video) (default)

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2.12.9 VDP VPS/Gemstar Data Register

| | |
|------------|-------------------|
| Subaddress | 80 0700h–80 070Ch |
|------------|-------------------|

VPS: Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-------------|---|---|---|---|---|---|---|
| 80 0700h | VPS byte 1 | | | | | | | |
| 80 0701h | VPS byte 2 | | | | | | | |
| 80 0702h | VPS byte 3 | | | | | | | |
| 80 0703h | VPS byte 4 | | | | | | | |
| 80 0704h | VPS byte 5 | | | | | | | |
| 80 0705h | VPS byte 6 | | | | | | | |
| 80 0706h | VPS byte 7 | | | | | | | |
| 80 0707h | VPS byte 8 | | | | | | | |
| 80 0708h | VPS byte 9 | | | | | | | |
| 80 0709h | VPS byte 10 | | | | | | | |
| 80 070Ah | VPS byte 11 | | | | | | | |
| 80 070Bh | VPS byte 12 | | | | | | | |
| 80 070Ch | VPS byte 13 | | | | | | | |

These registers contain the entire VPS data line except the clock run-in code or the start code.

Gemstar: Read only

| Subaddress | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|--------------------|---|---|---|---|---|---|---|
| 80 0700h | Gemstar frame code | | | | | | | |
| 80 0701h | Gemstar byte 1 | | | | | | | |
| 80 0702h | Gemstar byte 2 | | | | | | | |
| 80 0703h | Gemstar byte 3 | | | | | | | |
| 80 0704h | Gemstar byte 4 | | | | | | | |
| 80 0705h | Reserved | | | | | | | |
| 80 0706h | Reserved | | | | | | | |
| 80 0707h | Reserved | | | | | | | |
| 80 0708h | Reserved | | | | | | | |
| 80 0709h | Reserved | | | | | | | |
| 80 070Ah | Reserved | | | | | | | |
| 80 070Bh | Reserved | | | | | | | |
| 80 070Ch | Reserved | | | | | | | |

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2.12.10 Analog Output Control 2 Register

| | |
|------------|----------|
| Subaddress | A0 005Eh |
| Default | B2h |

| | | | | | | | |
|----------|----------|--------------------|---|------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Input Select [1:0] | | Gain [3:0] | | | |

Analog input select [1:0]: These bits are effective when manual input select bit is set to 1 at subaddress 7Fh, bit 1.

- 00 = CH1 selected
- 01 = CH2 selected
- 10 = CH3 selected
- 11 = CH4 selected (default)

Analog output PGA gain [3:0]: These bits are effective when analog output AGC is set to 1 at subaddress 7Fh, bit 2.

| Gain [3:0] | Mode 1 |
|------------------|--------|
| 0000 = | 1.30 |
| 0001 = | 1.56 |
| 0010 = (default) | 1.82 |
| 0011 = | 2.08 |
| 0100 = | 2.34 |
| 0101 = | 2.60 |
| 0110 = | 2.86 |
| 0111 = | 3.12 |
| 0000 = | 3.38 |
| 0001 = | 3.64 |
| 0010 = | 3.90 |
| 0011 = | 4.16 |
| 0100 = | 4.42 |
| 0101 = | 4.68 |
| 0110 = | 4.94 |
| 0111 = | 5.20 |

2.12.11 Interrupt Configuration Register

| | |
|------------|----------|
| Subaddress | B0 0060h |
| Default | 00h |

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| | | | | | | | |
|----------|---|---|---|---|----------|----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | Polarity | Reserved | |

Polarity: Interrupt terminal polarity

- 0 = Active high (default)
- 1 = Active low

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3 Electrical Specifications

3.1 Absolute Maximum Ratings[†]

| | |
|--|-----------------|
| Supply voltage range: IOV _{DD} to I/O GND | 0.5 V to 4 V |
| DV _{DD} to DGND | -0.2 V to 2 V |
| A33VDD (see Note 1) to A18GND (see Note 2) | -0.3 V to 3.6 V |
| A18VDD (see Note 3) to A33GND (see Note 4) | -0.2 V to 2 V |
| Digital input voltage, V _I to DGND | -0.5 V to 4.5 V |
| Digital output voltage, V _O to DGND | -0.5 V to 4.5 V |
| Analog input voltage range AIN to AGND | -0.2 V to 2 V |
| Operating free-air temperature, T _A | 0°C to 70°C |
| Storage temperature, T _{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. CH1_A33VDD, CH2_A33VDD
 2. CH1_A33GND, CH2_A33GND
 3. CH1_A18VDD, CH2_A18VDD, A18VDD_REF, PLL_A18VDD
 4. CH1_A18GND, CH2_A18GND, A18GND

3.2 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------|--|-----------------------|-----|-----------------------|------|
| IOV _{DD} | Digital supply voltage | 3 | 3.3 | 3.6 | V |
| DV _{DD} | Digital supply voltage | 1.65 | 1.8 | 1.95 | V |
| AV _{DD33} | Analog supply voltage | 3 | 3.3 | 3.6 | V |
| AV _{DD18} | Analog supply voltage | 1.65 | 1.8 | 1.95 | V |
| V _{I(P-P)} | Analog input voltage (ac-coupling necessary) | 0.5 | 1 | 2 | V |
| V _{IH} | Digital input voltage, high (Note 1) | 0.7 IOV _{DD} | | | V |
| V _{IL} | Digital input voltage, low (Note 2) | | | 0.3 IOV _{DD} | V |
| I _{OH} | Output current, V _{out} = 2.4 V | -4 | | | mA |
| I _{OL} | Output current, V _{out} = 0.4 V | 4 | | | mA |
| T _A | Operating free-air temperature | 0 | | 70 | °C |

- NOTES:
1. Exception: 0.7 AV_{DD18} for XTAL1 terminal
 2. Exception: 0.3 AV_{DD18} for XTAL1 terminal

3.2.1 Crystal Specifications

| CRYSTAL SPECIFICATIONS | MIN | NOM | MAX | UNIT |
|------------------------|-----|----------|-----|------|
| Frequency | | 14.31818 | | MHz |
| Frequency tolerance | | | ±50 | ppm |

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3.3 Electrical Characteristics

For minimum/maximum values: IOV_{DD} = 3 V to 3.6 V, DV_{DD} = 1.65 V to 1.95 V, AV_{DD33} = 3 V to 3.6 V, AV_{DD18} = 1.65 V to 1.95 V, T_A = 0°C to 70°C

For typical values: IOV_{DD} = 3.3 V, DV_{DD} = 1.8 V, AV_{DD33} = 3.3 V, AV_{DD18} = 1.8 V, T_A = 25°C

3.3.1 DC Electrical Characteristics (see Note 1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|-----------------|-----------------------|-----|-----------------------|------|
| I _{DDIO(D)} | 3.3-V IO digital supply current | CVBS | | 6 | | mA |
| | | S-video | | 6 | | |
| I _{DD(D)} | 1.8-V digital supply current | CVBS | | 55 | | mA |
| | | S-video | | 55 | | |
| I _{DD33(A)} | 3.3-V analog supply current | CVBS | | 24 | | mA |
| | | S-video | | 39 | | |
| I _{DD18(A)} | 1.8-V analog supply current | CVBS | | 79 | | mA |
| | | S-video | | 135 | | |
| P _{TOT} | Total power dissipation (normal operation) | S-video | | 490 | | mW |
| P _{SAVE} | Total power dissipation (power save) | | | 100 | | mW |
| P _{DOWN} | Total power dissipation (power down) | | | 10 | | mW |
| I _{lkg} | Input leakage current | | | | 10 | μA |
| C _i | Input capacitance | By design | | | 8 | pF |
| V _{OH} | Output voltage high | | 0.8 IOV _{DD} | | | V |
| V _{OL} | Output voltage low | | | | 0.2 IOV _{DD} | V |

NOTE 1: Measured with a load of 10 kΩ in parallel to 15 pF.

3.3.2 Analog Processing and A/D Converters

3.3.2.1 F_s = 30 MSPS for CH1, CH2

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--|-----|-------|-----|------|
| Z _i | Input impedance, analog video inputs | By design | 200 | | | kΩ |
| C _i | Input capacitance, analog video inputs | By design | | | 10 | pF |
| V _{i(pp)} | Input voltage range | C _{coupling} = 0.1 μF | 0.5 | 1 | 2 | V |
| ΔG | Gain control range | | -6 | | 6 | dB |
| DNL | Differential nonlinearity | AFE only | | 0.75 | 1 | LSB |
| INL | Integral nonlinearity | AFE only | | 1 | 2.5 | LSB |
| Fr | Frequency response | Multiburst (60 IRE) | | -0.9 | | dB |
| XTALK | Crosstalk | 1 MHz | | | -50 | dB |
| SNR | Signal-to-noise ratio, all channels | 1 MHz, 1 V _{p-p} | | 54 | | dB |
| GM | Gain match (Note 1) | Full scale, 1 MHz | | 1.5% | | |
| NS | Noise spectrum | Luma ramp (100 kHz to full, tilt-null) | | -58 | | dB |
| DP | Differential phase | Modulated ramp | | 0.5 | | ° |
| DG | Differential gain | Modulated ramp | | ±1.5% | | |
| V _O | Output voltage | C _L = 10 pF | | 2 | 2.4 | V |

NOTE 1: Component inputs only

3.3.3 Timing

3.3.3.1 Clocks, Video Data, Sync Timing

| PARAMETER | | TEST CONDITIONS (see NOTE 1) | MIN | TYP | MAX | UNIT |
|--------------------|--------------------|---------------------------------|-----|------|-----|------|
| Duty cycle DATACLK | | | 45% | 50% | 55% | |
| t_1 | High time, DATACLK | | | 18.5 | | ns |
| t_2 | Low time, DATACLK | | | 18.5 | | ns |
| t_3 | Fall time, DATACLK | 90% to 10% | | | 4 | ns |
| t_4 | Rise time, DATACLK | 10% to 90% | | | 4 | ns |
| t_5 | Output delay time | | | | 10 | ns |

NOTE 1: $C_L = 15$ pF

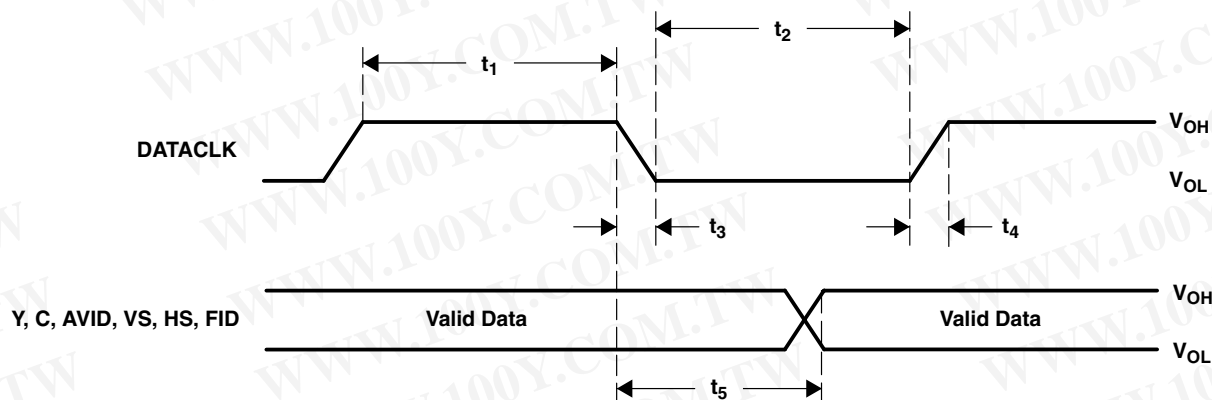


Figure 3-1. Clocks, Video Data, and Sync Timing

3.3.3.2 I²C Host Port Timing

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----------------|-----|-----|-----|---------|
| t_1 | Bus free time between STOP and START | | 1.3 | | | μ s |
| t_2 | Data hold time | | 0 | | 0.9 | μ s |
| t_3 | Data setup time | | 100 | | | ns |
| t_4 | Setup time for a (repeated) START condition | | 0.6 | | | μ s |
| t_5 | Setup time for a STOP condition | | 0.6 | | | ns |
| t_6 | Hold time for a (repeated) START condition | | 0.6 | | | μ s |
| t_7 | Rise time VC1(SDA) and VC0(SCL) signal | | | | 250 | ns |
| t_8 | Fall time VC1(SDA) and VC0(SCL) signal | | | | 250 | ns |
| C_b | Capacitive load for each bus line | | | | 400 | pF |
| f_{I2C} | I ² C clock frequency | | | | 400 | kHz |

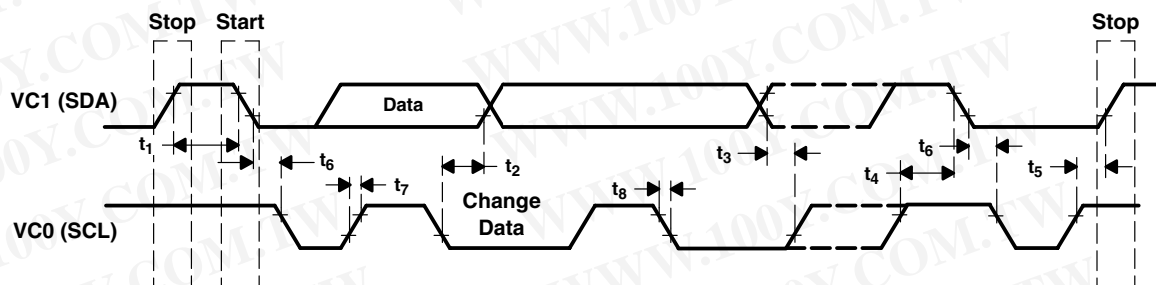


Figure 3-2. I²C Host Port Timing

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4 Example Register Settings

The following example register settings are provided only as a reference. These settings, given the assumed input connector, video format, and output format, set up the TVP5147 decoder and provide video output. Example register settings for other features and the VBI data processor are not provided here.

4.1 Example 1

4.1.1 Assumptions

Input connector: Composite (VI_1_A) (default)

Video format: NTSC (J, M), PAL (B, G, H, I, N) or SECAM (default)

NOTE: NTSC-443, PAL-Nc, and PAL-M are masked from the autoswitch process by default. See the autoswitch mask register at address 04h.

Output format: 10-bit ITU-R BT.656 with embedded syncs (default)

4.1.2 Recommended Settings

Recommended I²C writes: For the given assumptions, only one write is required. All other registers are set up by default.

I²C register address 08h = Luminance processing control 3 register

I²C data 00h = Optimizes the trap filter selection for NTSC and PAL

I²C register address 0Eh = Chrominance processing control 2 register

I²C data 04h = Optimizes the chrominance filter selection for NTSC and PAL

I²C register address 34h = Output formatter 2 register

I²C data 11h = Enables YCbCr output and the clock output

NOTE: HS/CS, VS/VBLK, AVID, FID, and GLCO are logic inputs by default. See output formatter 3 and 4 registers at addresses 35h and 36h, respectively.

4.2 Example 2

4.2.1 Assumptions

Input connector: S-video [VI_2_C (luma), VI_1_C (chroma)]

Video format: NTSC (J, M, 443), PAL (B, D, G, H, I, N, Nc, 60) or SECAM (default)

Output format: 10-bit ITU-R BT.656 with discrete sync outputs

4.2.2 Recommended Settings

Recommended I²C writes: This setup requires additional writes to output the discrete sync 10-bit 4:2:2 data, HS, and VS, and to autoswitch between all video formats mentioned above.

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- I²C register address 00h = Input select register
 - I²C data 46h = Sets luma to VI_2_C and chroma to VI_1_C
- I²C register address 04h = Autoswitch mask register
 - I²C data 3Fh = Includes NTSC 443 and PAL (M, Nc, 60) in the autoswitch
- I²C register address 08h = Luminance processing control 3 register
 - I²C data 00h = Optimizes the trap filter selection for NTSC and PAL
- I²C register address 0Eh = Chrominance processing control 2 register
 - I²C data 04h = Optimizes the chrominance filter selection for NTSC and PAL
- I²C register address 33h = Output formatter 1 register
 - I²C data 41h = Selects the 10-bit 4:2:2 output format
- I²C register address 34h = Output formatter 2 register
 - I²C data 11h = Enables YCbCr output and the clock output
- I²C register address 36h = Output formatter 4 register
 - I²C data 11h = Enables HS and VS sync outputs

4.3 Example 3

4.3.1 Assumptions

- Input connector: Component [VI_1_B (Pb), VI_2_B (Y), VI_3_B (Pr)]
- Video format: NTSC (J, M, 443), PAL (B, D, G, H, I, N, Nc, 60) or SECAM (default)
- Output format: 20-bit ITU-R BT.656 with discrete sync outputs

4.3.2 Recommended Settings

Recommended I²C writes: This setup requires additional writes to output the discrete sync 20-bit 4:2:2 data, HS, and VS, and to autoswitch between all video formats mentioned above.

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- I²C register address 00h = Input select register
I²C data 95h = Sets Pb to VI_1_B, Y to VI_2_B, and Pr to VI_3_B
- I²C register address 04h = Autoswitch mask register
I²C data 3Fh = Includes NTSC 443 and PAL (M, Nc, 60) in the autoswitch
- I²C register address 08h = Luminance processing control 3 register
I²C data 00h = Optimizes the trap filter selection for NTSC and PAL
- I²C register address 0Eh = Chrominance processing control 2 register
I²C data 04h = Optimizes the chrominance filter selection for NTSC and PAL
- I²C register address 33h = Output formatter 1 register
I²C data 41h = Selects the 20-bit 4:2:2 output format
- I²C register address 34h = Output formatter 2 register
I²C data 11h = Enables YCbCr output and the clock output
- I²C register address 36h = Output formatter 4 register
I²C data AFh = Enables HS and VS sync outputs

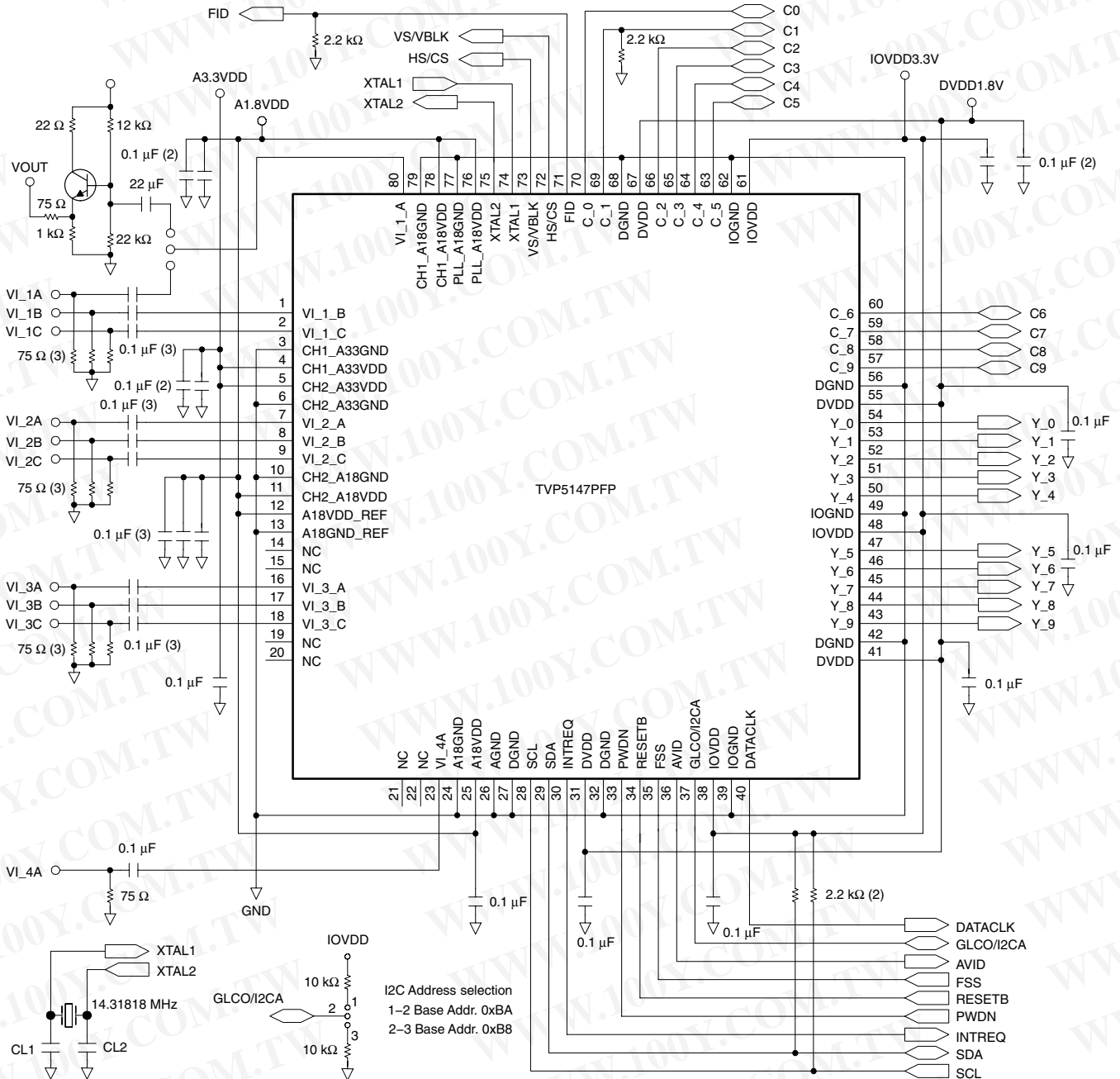
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5 Application Information

5.1 Application Example

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NOTE: If XTAL1 is connected to clock source, input voltage high must be 1.8 V.
 TVP5147 can be a drop-in replacement for TVP5146.
 Terminals 69 and 71 must be connected to ground through pulldown resistors.

Figure 5-1. Example Application Circuit

5.2 Designing With PowerPAD™ Devices

The TVP5147 device is housed in a high-performance, thermally enhanced, 80-terminal PowerPAD package (TI package designator: 80PFP). Use of the PowerPAD package does not require any special considerations except to note that the thermal pad, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing the PowerPAD PCB features, the use of solder masks (or other assembly techniques) can be required to prevent any inadvertent shorting by the exposed thermal pad of connection etches or vias under the package. The recommended option, however, is not to run any etches or signal vias under the device, but to have only a grounded thermal land as in the following explanation. Although the actual size of the exposed die pad may vary, the minimum size required for the keep-out area for the 80-terminal PFP PowerPAD package is 8 mm × 8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size, depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for using thermal lands and thermal vias are detailed in the TI application note PowerPAD™ *Thermally Enhanced Package Application Report*, (SLMA002), available via the TI Web pages beginning at URL: <http://www.ti.com>

For the TVP5147 device, this thermal land must be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size must be as large as possible without shorting device signal terminals. The thermal land can be soldered to the exposed thermal pad using standard reflow soldering techniques.

While the thermal land can be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low-impedance ground plane for the device. More information can be obtained from the TI application note *PHY Layout* (SLLA020).

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|------------------------------|
| TVP5147PFP | NRND | HTQFP | PFP | 80 | 96 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | Replaced by TVP5147M1PFP |
| TVP5147PFPR | NRND | HTQFP | PFP | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | Replaced by TVP5147M1PFPR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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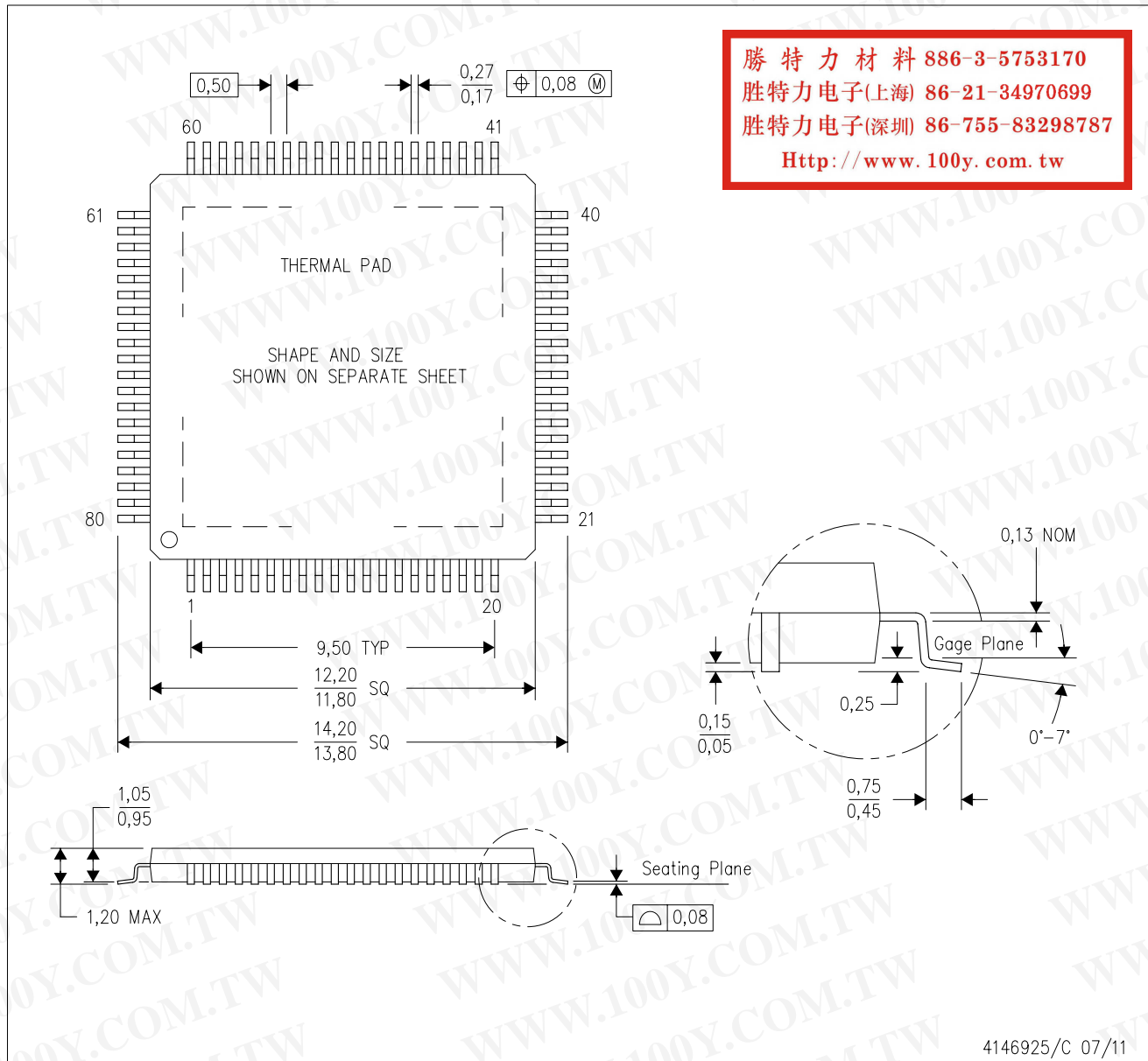
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MECHANICAL DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PFP (S-PQFP-G80)

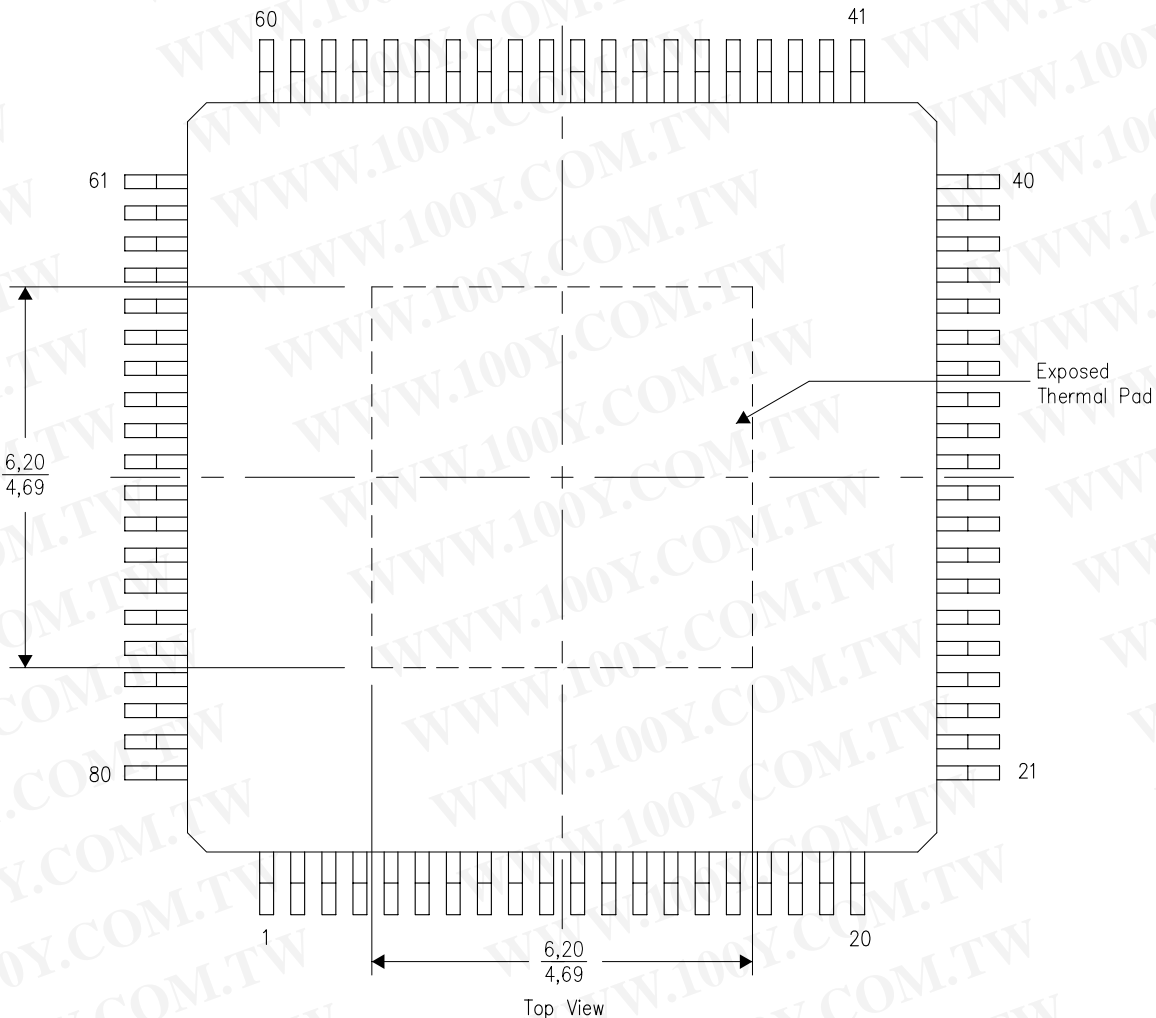
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206327-3/N 09/11

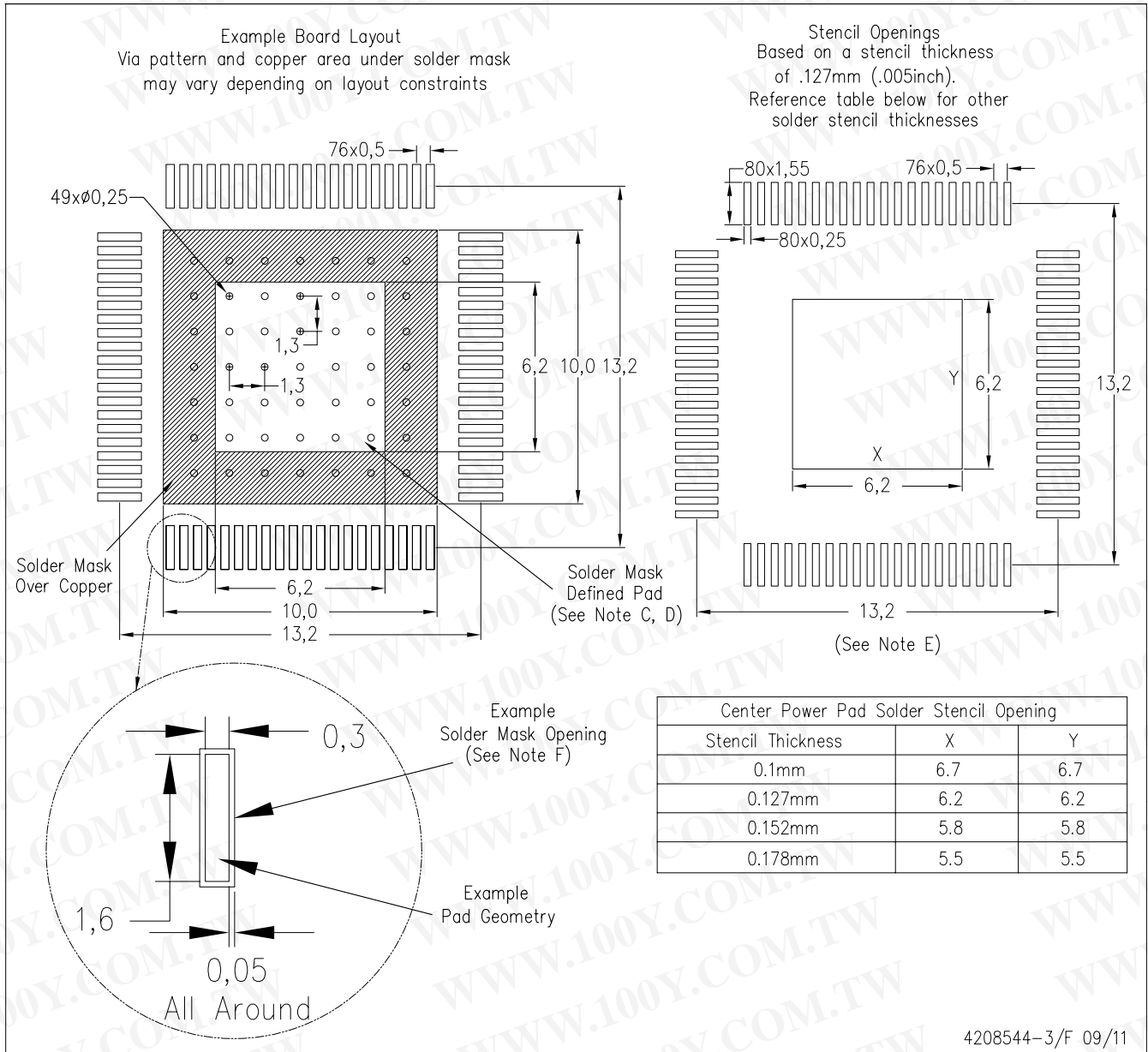
NOTE: A. All linear dimensions are in millimeters

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LAND PATTERN DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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