High Speed Deserialization Board (HSDB)

HSC-ADC-FPGA

FEATURES

- Used with buffer memory board for capturing and converting high speed serial LVDS digital data to parallel CMOS logic levels
- Used with high speed ADC evaluation boards that have serial LVDS outputs
- Features Xilinx® XC2V250-5FG256C FPGA, Virtex-II FPGA
- Can switch up to four channels of output data (two at a time)
- Easily configurable, supporting 8-bit to 14-bit ADCs
- Allows standard JTAG user connection for additional code modifications

EQUIPMENT NEEDED

- Any high speed ADC evaluation board that supports serial LVDS digital output format
- HSC-ADC-EVALA/B-DC, ADI data capture FIFO board

GENERAL DESCRIPTION

The high speed deserialization board (HSDB) captures up to four channels of serial LVDS digital outputs and converts the outputs to standard parallel CMOS format. It supports quad analog-to-digital converter (ADC) evaluation boards, enabling the user to connect to the Analog Devices FIFO board (HSC-ADC-EVALA/B-DC). Together, these boards can be connected to a PC through a USB port and used with the ADC Analyzer™ to evaluate the performance of high speed quad ADCs. Users can view both time and frequency information for a specific analog input and encode rate and analyze SNR, SINAD, SFDR, and harmonic information.

The evaluation kit, which includes a wall-mount switching power supply, is easy to set up. Additional equipment required: an Analog Devices high speed quad ADC evaluation board, dual-channel FIFO board, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is enabled instantly on the PC.

The HSC-ADC-FPGA supports up to four ADC channels, providing two parallel CMOS outputs simultaneously.

FUNCTIONAL BLOCK DIAGRAM

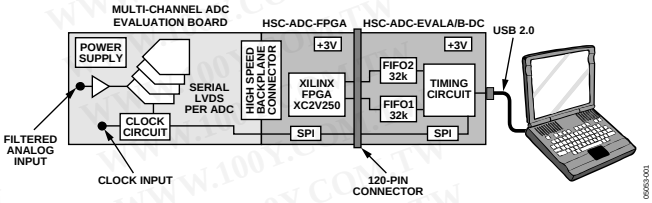

Figure 1. Simplified Functional Block Diagram

PRODUCT HIGHLIGHTS

1. Easy to set up.
   Connect the power supply and signal sources to the two evaluation boards. Then connect to the PC and evaluate the performance instantly.
2. JTAG user interface.
   With the supplied JTAG connection, users can implement unique features in the FPGA.
3. Up to 840 MBPS available on each channel.
   14-bit quad ADCs with encode rates as high as 60 MSPS can be used with the deserialization board.

Rev. B

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REVISION HISTORY

11/05—Rev. A to Rev. B

Changed HSC-ADC-EVALA-DC to HSC-ADC-EVALA/B-DC ..... Universal
Changes to Figure 1 1
Changes to Table 1 4
Changes to the Theory of Operation Section and Figure 3 5
Added the SPI Interface Section 7
Changes to Figure 5 8
Changes to Figure 6 9
Updated Schematic and Layout to Rev D 9-17
Changes to Table 6 17
Changes to Ordering Guide 20

02/05—Rev. 0 to Rev. A

Updated Bill of Materials 15
Changes to Ordering Guide 16

10/04—Revision 0: Initial Version

HSDB QUICK START

The HSDB is used to create an interface from a quad ADC evaluation board that has serial LVDS outputs to the FIFO data capture board.

REQUIREMENTS

The following equipment is needed to set up the HSDB:

- FIFO evaluation board, ADC Analyzer, USB cable, and FIFO data sheet
- High speed ADC evaluation board and ADC data sheet
- Power supply for ADC evaluation board, HSDB, and FIFO
- Analog signal source and appropriate filtering
- Low jitter clock source applicable for specific ADC evaluation, typically <1 ps rms
- PC with Windows® 98 (2nd edition), Windows 2000, Windows ME, or Windows XP for the ADC Analyzer
- PC with a USB 2.0 port recommended for FIFO connection

ADDITIONAL INFORMATION AND UPDATES

For more information on the ADC Analyzer and the FIFO data capture board, and for software updates, visit www.analog.com/FIFO.

For more information on LVDS data output, see the *LVDS Data Outputs for High Speed Analog-to-Digital Converters* Application Note (AN-586) on www.analog.com.

QUICK START STEPS

Connect the quad ADC evaluation board to the high speed backplane connector side of the HSDB. Then connect the other side of the HSDB to the 120-pin connector header that mates to the FIFO board.

1. Connect the USB cable to the FIFO evaluation board and to a USB port on the PC.
2. Set the FIFO jumper settings in dual-channel configuration as shown in the HSC-ADC-EVALA/B-DC datasheet, located at www.analog.com/FIFO.
3. Verify and connect the appropriate power supplies to the FIFO, HSDB, and ADC evaluation boards.
4. Apply power to the evaluation boards and check the voltage levels at the board level. Separate supplies may be necessary.
5. Connect the appropriate analog input (which should be filtered with a band-pass filter) and low jitter clock signal.
6. Start the ADC Analyzer to begin the evaluation.

DESERIALIZATION BOARD

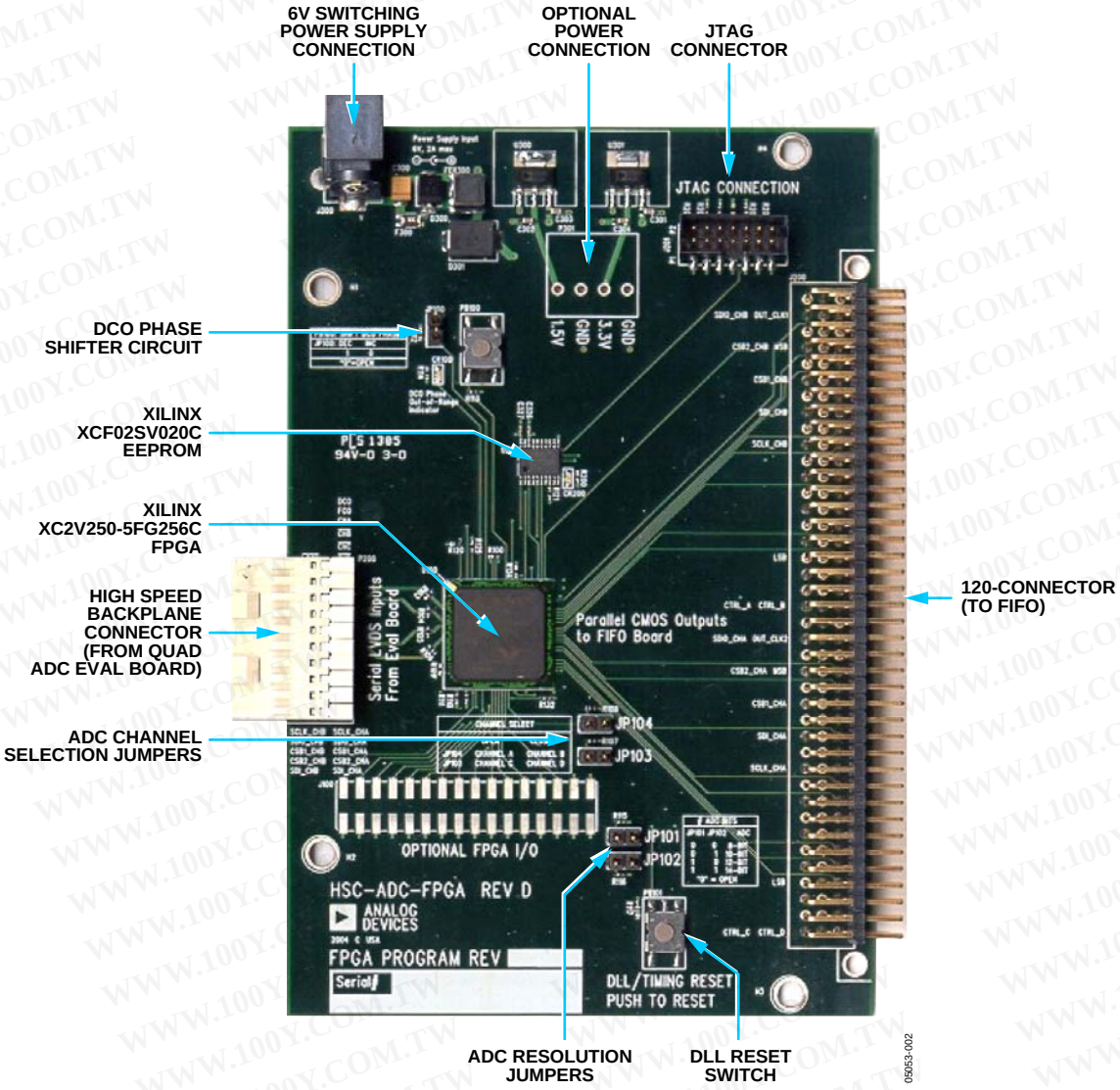

Figure 2. HSC-ADC-FPGA Components

SUPPORTED ADC EVALUATION BOARDS

The evaluation boards in Table 1 can be used with the high speed ADC deserialization board.

Table 1. Supported ADC Evaluation Boards

Evaluation Board Model	Description of ADC	Comments
AD9289-65EB	8-bit, 65 MSPS quad ADC	Requires HSC-ADC-FPGA-9289 and HSC-ADC-EVALA/B-DC (dual-channel)
AD9229-65EB	12-bit, 65 MSPS quad ADC	Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)
AD9287-100EB	8-bit, 100 MSPS quad ADC	Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)
AD9219-65EB	10-bit, 65 MSPS quad ADC	Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)
AD9228-65EB	12-bit, 65 MSPS quad ADC	Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)
AD9259-50EB	14-bit, 50 MSPS quad ADC	Requires HSC-ADC-FPGA-4 and HSC-ADC-EVALA/B-DC (dual-channel)

THEORY OF OPERATION

The HSDB, featuring the Xilinx Virtex™-II FPGA, accepts four ADC channels of LVDS serial data and the data output and frame align clocks (DCO and FCO). The FPGA then converts all of these signals from LVDS to single-ended CMOS signals.

The HSDB can support 8-bit to 14-bit ADCs. The DCO signal is used to clock the incoming data through 14 shift registers. Seven of these registers are clocked on the rising edge of DCO, and the other seven are clocked on the falling edge (DDR), as shown in Figure 3. The ADC resolution is selectable using Jumper Connection JP101 and Jumper Connection JP102.

Both the DCO and FCO are used inside the FPGA to set up all necessary clock edges to take the parallel data from the shift registers to the output of the FPGA. The **DLL/Timing Reset** button (PB101) is used to set the data capture timing to the default setting (see Table 4).

Once the parallel data has been transferred completely to the FCO clock domain, the data is multiplexed for use with the 2-channel FIFO board (HSC-ADC-EVALA/B-DC). ADC Channel A and Channel B are selected using the JP104 jumper connection. Channel C and Channel D are selected using the JP103 jumper connection. Data clock outputs (CLK_AB and CLK_CD) are also provided to clock the FIFO board.

CODE DESCRIPTION

The FPGA on the HSDB comes with Verilog code preinstalled and tested. It is designed to help evaluate the performance of an Analog Devices quad ADC quickly and easily by providing the user with familiar CMOS logic-level outputs.

MANUAL INSTALLATION AND CUSTOMIZATION

Users can manually customize or update the necessary code through a JTAG connector provided on the deserialization board, as shown in Figure 2. However, Analog Devices provides no guarantee of performance if the code is customized.

A Zip file containing all of the necessary default configuration files to implement manual changes or to add custom module blocks for further computation is at www.analog.com/FIFO.

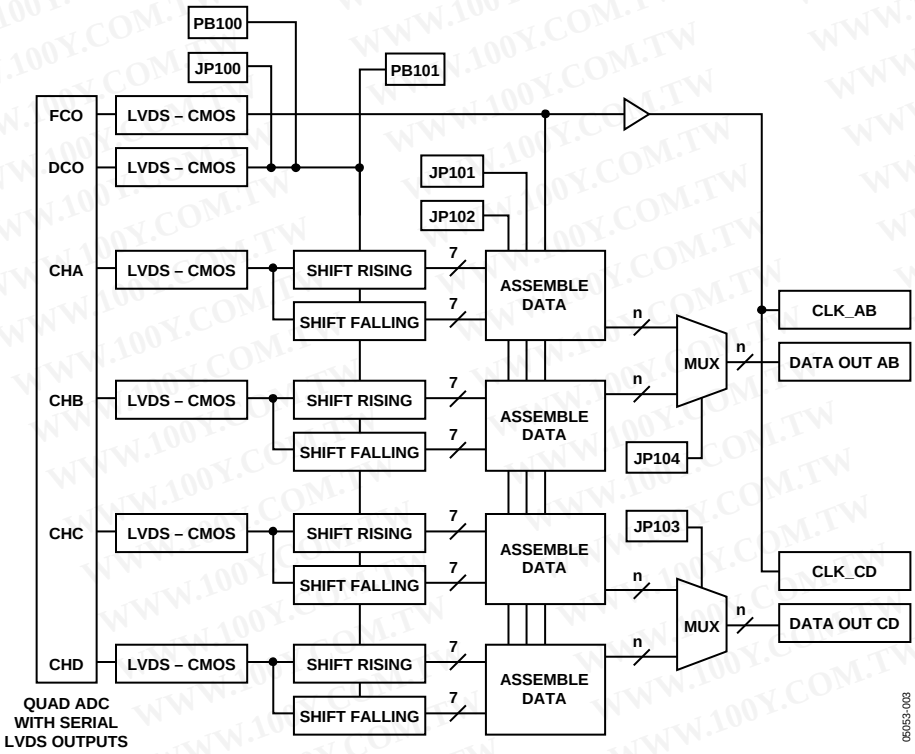

Figure 3. Internal FPGA Functional Block Diagram

JUMPERS

RESOLUTION SETTINGS

The HSDB supports ADCs with 8 bits to 14 bits of resolution. Use Table 2 to configure the appropriate jumpers. In Table 2, 0 indicates an open jumper, and 1 indicates a shorted jumper.

Table 2. Resolution Jumper Settings

Number of Bits	JP101	JP102
8	0	0
10	0	1
12	1	0
14	1	1

CHANNEL SELECTION SETTINGS

The ADC Channel A and Channel B are associated with the top IDT FIFO chip, the one closest to the Analog Devices logo; Channel B; or ADC Analyzer Channel B. ADC Channel C and Channel D are associated with the bottom IDT FIFO chip, Channel A, or ADC Analyzer Channel A. Use Table 3 to configure the jumper settings for channel selection. In Table 3, 0 indicates an open jumper, and 1 indicates a shorted jumper.

Table 3. Channel Selection Jumper Settings

ADC Channel	FIFO Channel/ ADC Analyzer Channel	Channel Select
A	Channel B/Channel B	JP104 = 0
B	Channel B/Channel B	JP104 = 1
C	Channel A/Channel A	JP103 = 0
D	Channel A/Channel A	JP103 = 1

DATA ALIGNMENT

The **DLL/Timing Reset** button (**PB101**) must be pressed to operate the HSDB after initial power-up. Data alignment is automatic; however, the **DLL/Timing Reset** button must be pressed any time the ADC sample clock rate is changed, or data outputs become corrupted.

After pressing the **DLL/Timing Reset** button, the FPGA digital clock manager (DCM) DLL is reset to its default setting. This value (PHASE_SHIFT) is defined in the user constraints file of the FPGA software and is shown in Table 4.

Table 4. Default PHASE_SHIFT User Constraint Settings

Product	PHASE_SHIFT User Constraint
AD9289	+50
AD9229	−10
AD9219/AD9228/ AD9259/AD9287	−10

DCO PHASE ALIGNMENT

The **DCO Phase Shift** button (**PB100**) can be used in conjunction with the DCO Phase Shift jumper (JP100) to adjust the phase relationship between the incoming DCO signal and the FPGA DLL signal.

The output of the FPGA DLL is used to capture the incoming serial data streams. The rising edge and falling edge of this signal must be aligned, so that they occur during the center of the data eye as shown in Figure 4.

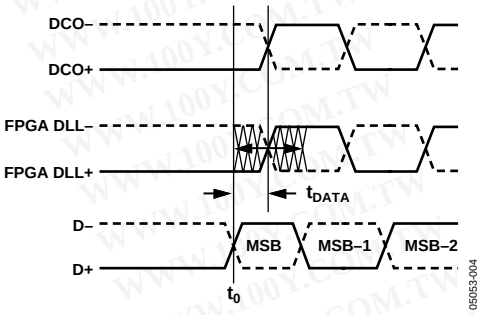

Figure 4. DCO Phase Shifting Alignment Example

After activating the **DLL/Timing Reset** button (**PB101**), the phase of the DLL is set to its default value. If this phase alignment setting is not compatible with the current configuration of the ADC under test, it can be adjusted.

The phase shift operation is activated by pressing the **DLL Phase Shift** button (**PB100**). The direction of this adjustment is determined by the setting of the DLL Phase Shift jumper (JP100); see **Table 5**.

Table 5. DCO Phase Shift Alignment Settings

DCO Phase Shift	JP100
Increment	0
Decrement	1

While the **DLL Phase Shift** button is clicked, the phase is adjusted continuously over the range of the PHASE_SHIFT user constraint. The PHASE_SHIFT variable can be set to any integer value between ±255. The actual setting of this variable is lost when using this function. However, an out-of-range condition is indicated by LED CR100. If the phase has gone out of range, it can be set back in range either by using the **DLL/Timing Reset** button (**PB101**) or by changing the adjustment direction using Jumper **JP100** and clicking the **PB100** button again.

The rate of phase change while the **PB100** button is clicked is determined by multiplying the FCO clock period by 2^{27} (256 steps × 2^{19}). This gives the amount of time in seconds that it takes to slew from PHASE_SHIFT = 0 to the minimum or maximum value. For example, if FCO = 65 MHz, it takes approximately 2 sec to slew from PHASE_SHIFT = 0 to out-of-range (2^{27} × 1/65M). Refer to the Xilinx Virtex-II datasheet for further details on DCM phase shifting.

SPI® INTERFACE

The HSDB fully supports ADCs that have an SPI interface. The HSDB does not interact with any of the SPI signals; it provides a path for the SPI interface to be connected from the HSC-ADC-EVALB-DC data capture board to the corresponding product evaluation board.

FIFO JUMPER SETTINGS

The HSDB requires the interface of the HSC-ADC-EVALA/B-DC (dual-channel FIFO4 or FIFO4.1) for data to be captured and displayed in the ADC Analyzer. The default settings for the FIFO dual-channel configuration can be found in the HSC-ADC-EVALA/B-DC datasheet at www.analog.com/FIFO. To align the timing properly, some evaluation boards require modifications to these settings. For proper operation, the FIFO timing setting should be configured for dual-channel configuration. For more details, see the Theory of Operation section in the HSC-ADC-EVALA/B-SC/HSC-ADC-EVALA/B-DC data sheet at www.analog.com/FIFO.

Another easy way to determine if the proper jumper settings between the HSDB, FIFO, and ADC Analyzer have already been installed is to consult the help menu in the ADC Analyzer software:

1. From the **Help** menu, select **About HSC_ADC_EVALA.**
2. Click **Setup Default Jumper Wizard**.
3. Click **Dual Channel**. A picture of the FIFO board for that application appears, showing the correct jumper settings already in place.

EVALUATION BOARD

The HSDB (HSC-ADC-FPGA, Rev. D) provides all of the support circuitry required to accept quad ADC digital serial LVDS outputs. Each of the various functions and configurations can be selected by proper connection of various jumpers (see Figure 6 to Figure 8). When using this in conjunction with an ADC evaluation board and FIFO, it is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the ultimate performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 6 to Figure 8 for complete schematics and layout plots.

POWER SUPPLIES

The HSDB board is supplied with a wall mount switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 to 240 ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J300. On the PC board, the 6 V supply is then fused and conditioned before connecting to two low dropout linear regulators that supply the proper bias to each of the various sections on the board (see Figure 5).

When operating the evaluation board in a nondefault condition, L302 and L303 can be removed to disconnect the switching power supply. This enables the user to individually bias each section of the board. Use P301 to connect a different supply for each section. The 3.3 V supply is needed with a 1 A current capability to bias the FPGA's I/O supply ring pins. The 1.5 V supply will also be needed in addition to the other 3.3 V supply to bias the FPGA's core supply pins. The 1.5 V supply should have a 1 A current capability, as well.

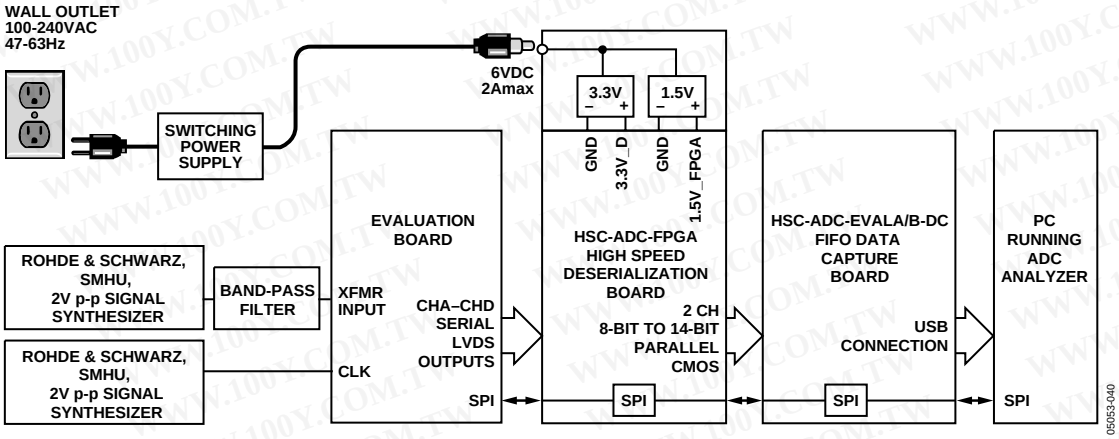

Figure 5. Example Setup Using Quad ADC Evaluation Board and FIFO Data Capture Board

HSDB SCHEMATICS AND PCB LAYOUT

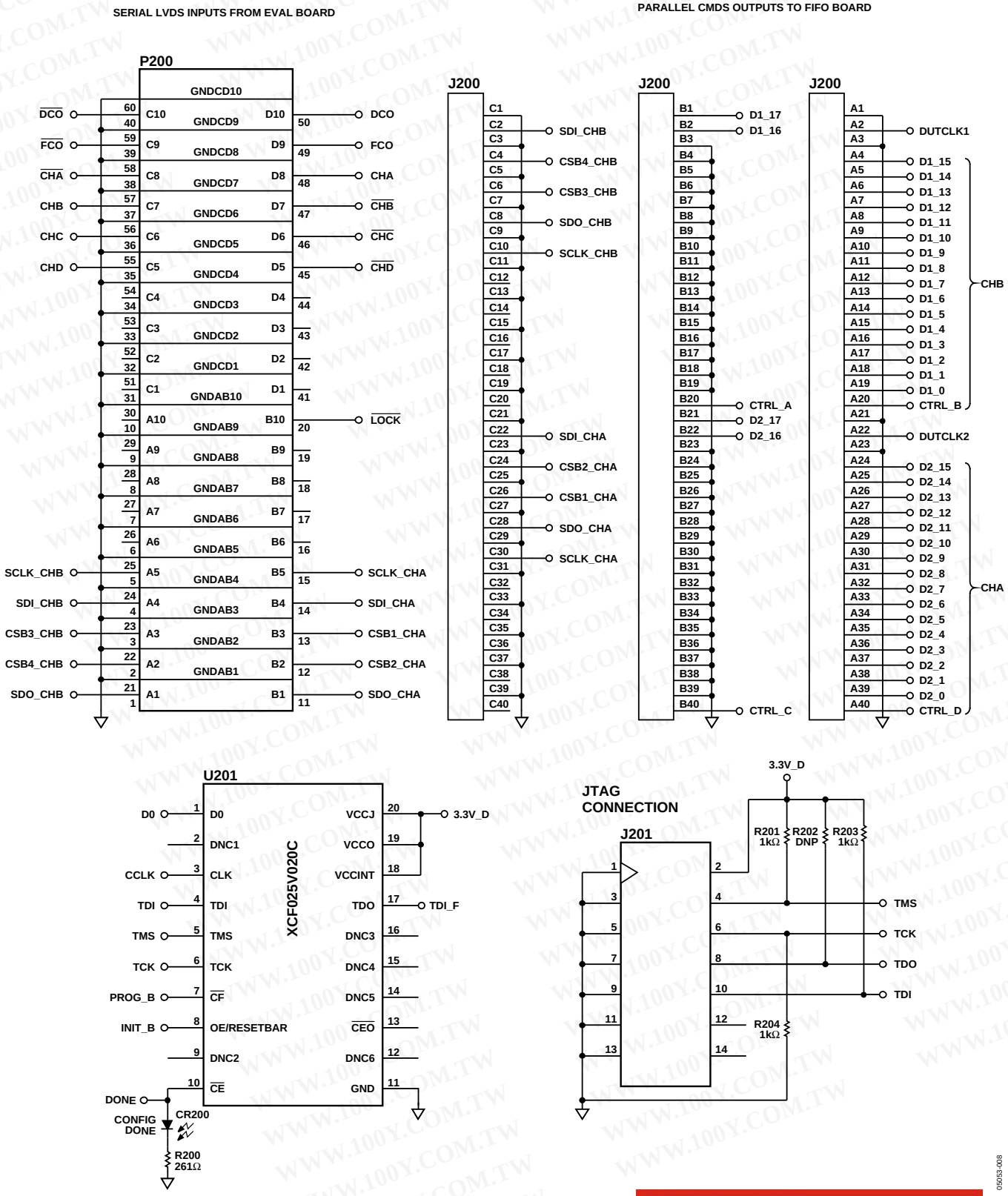

Figure 6. PCB Schematic

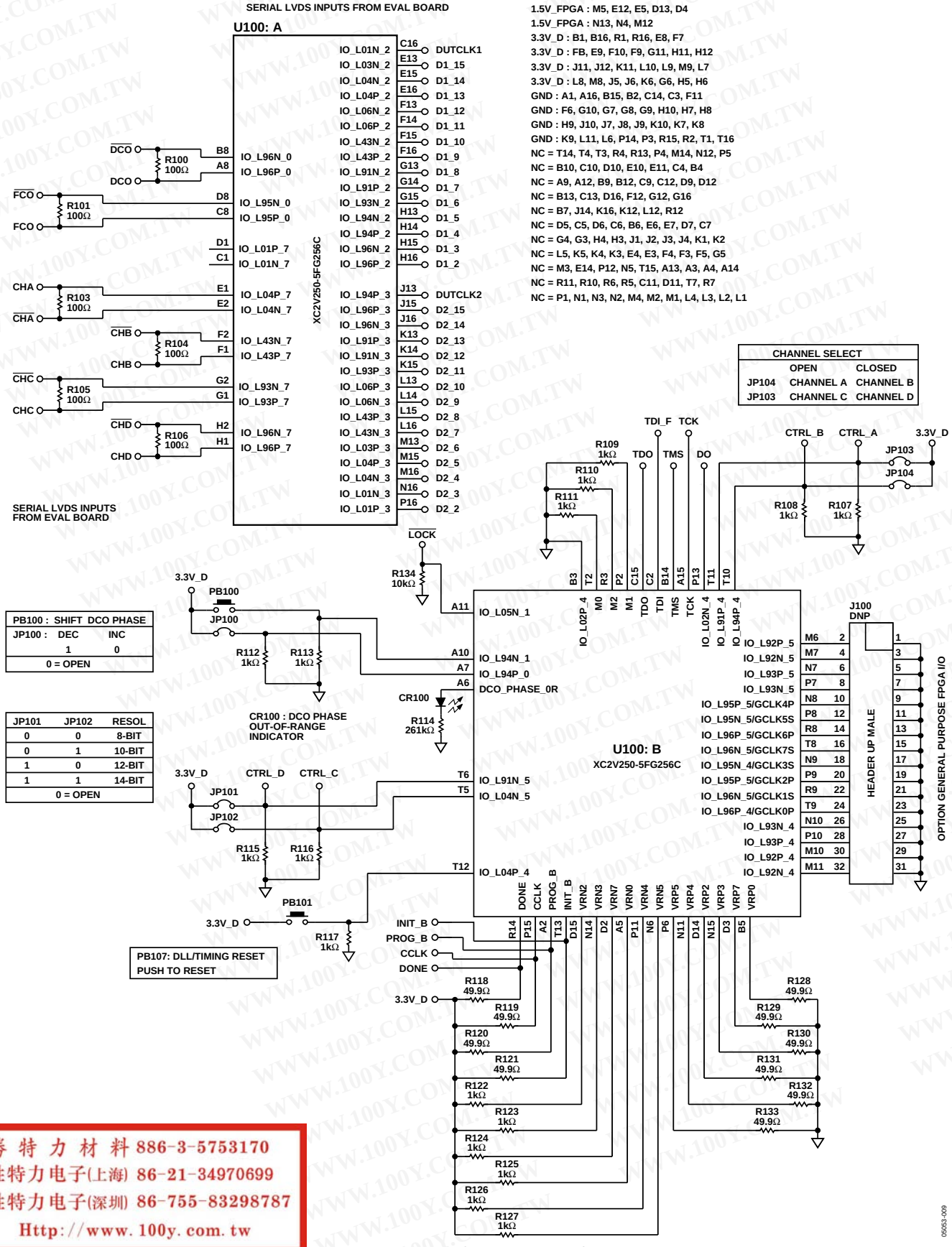

Figure 7. PCB Schematic (Continued)

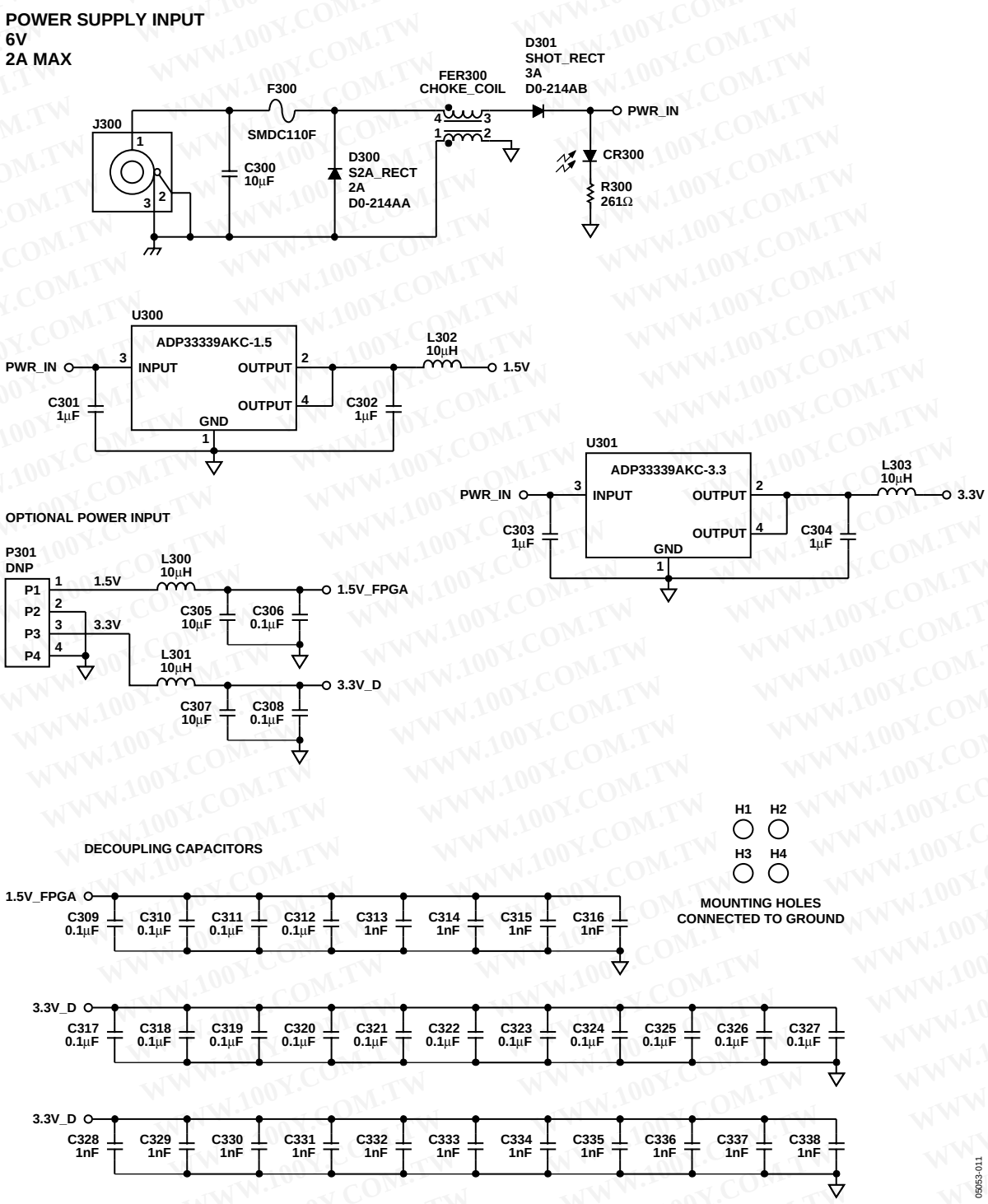

Figure 8. PCB Schematic (Continued)

LAYER 1—PRIMARY SIDE

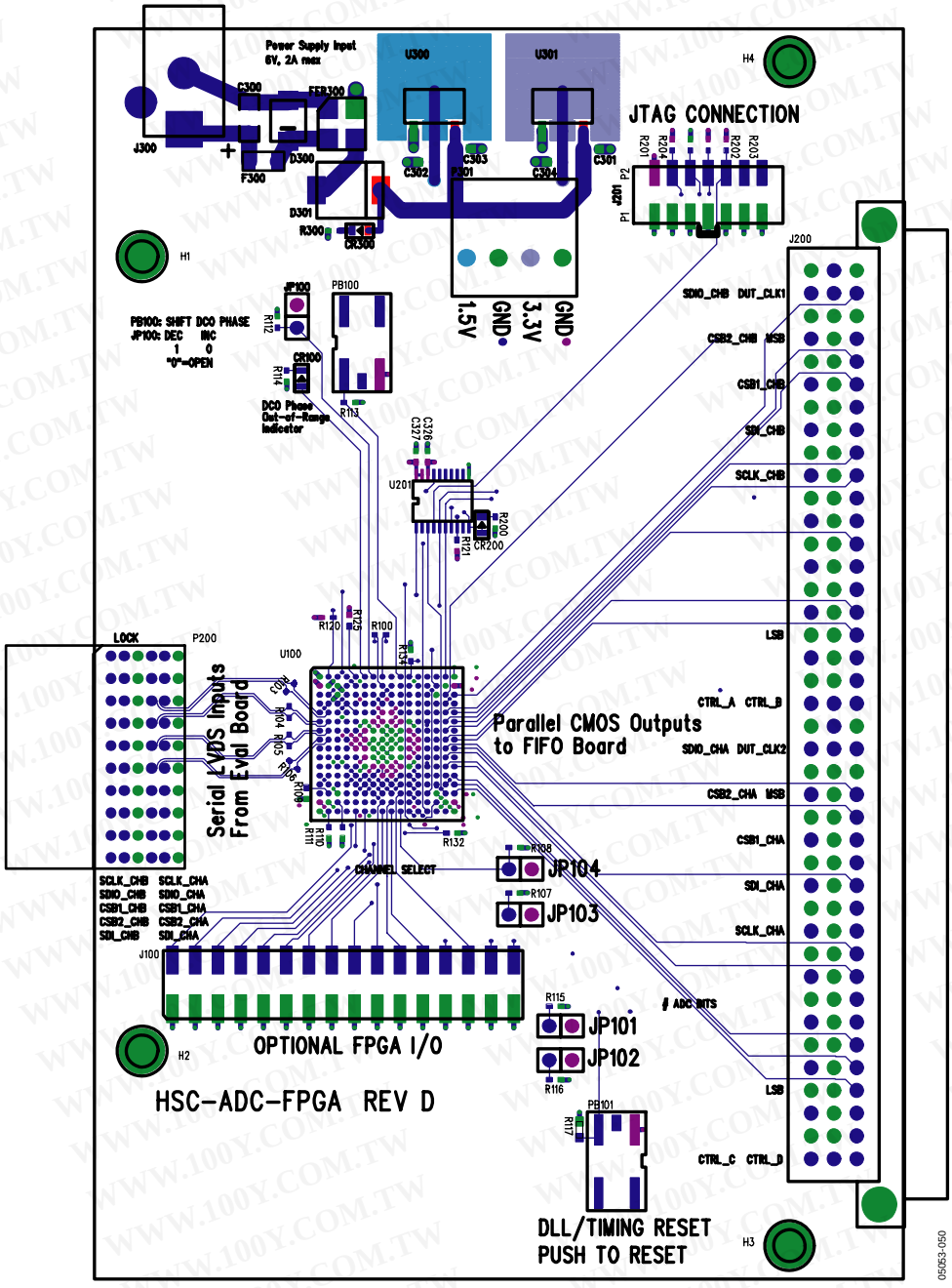

Figure 9. Layer 1—Primary Side (Top)

LAYER 2—GROUND PLANE

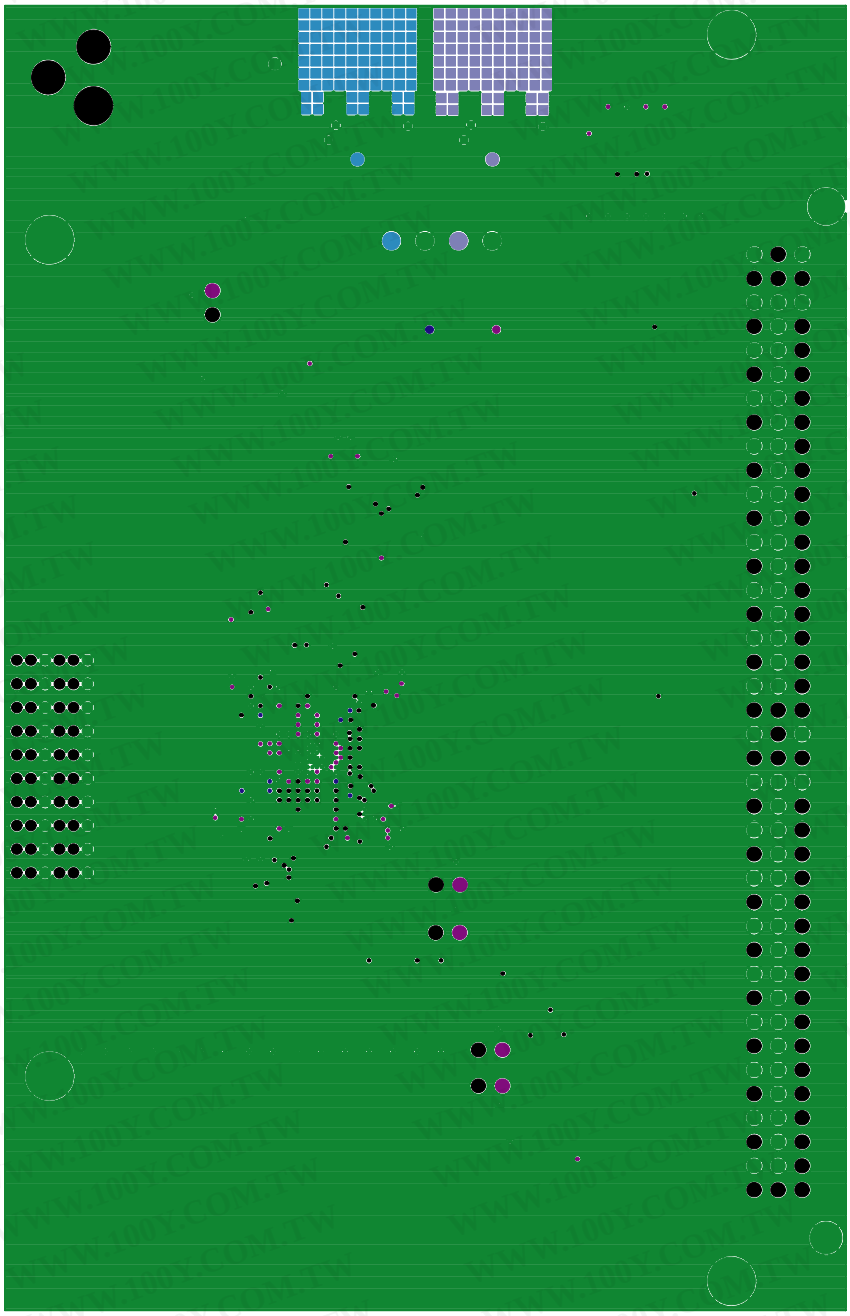

Figure 10. Layer 2—Ground Plane

LAYER 3—POWER PLANE

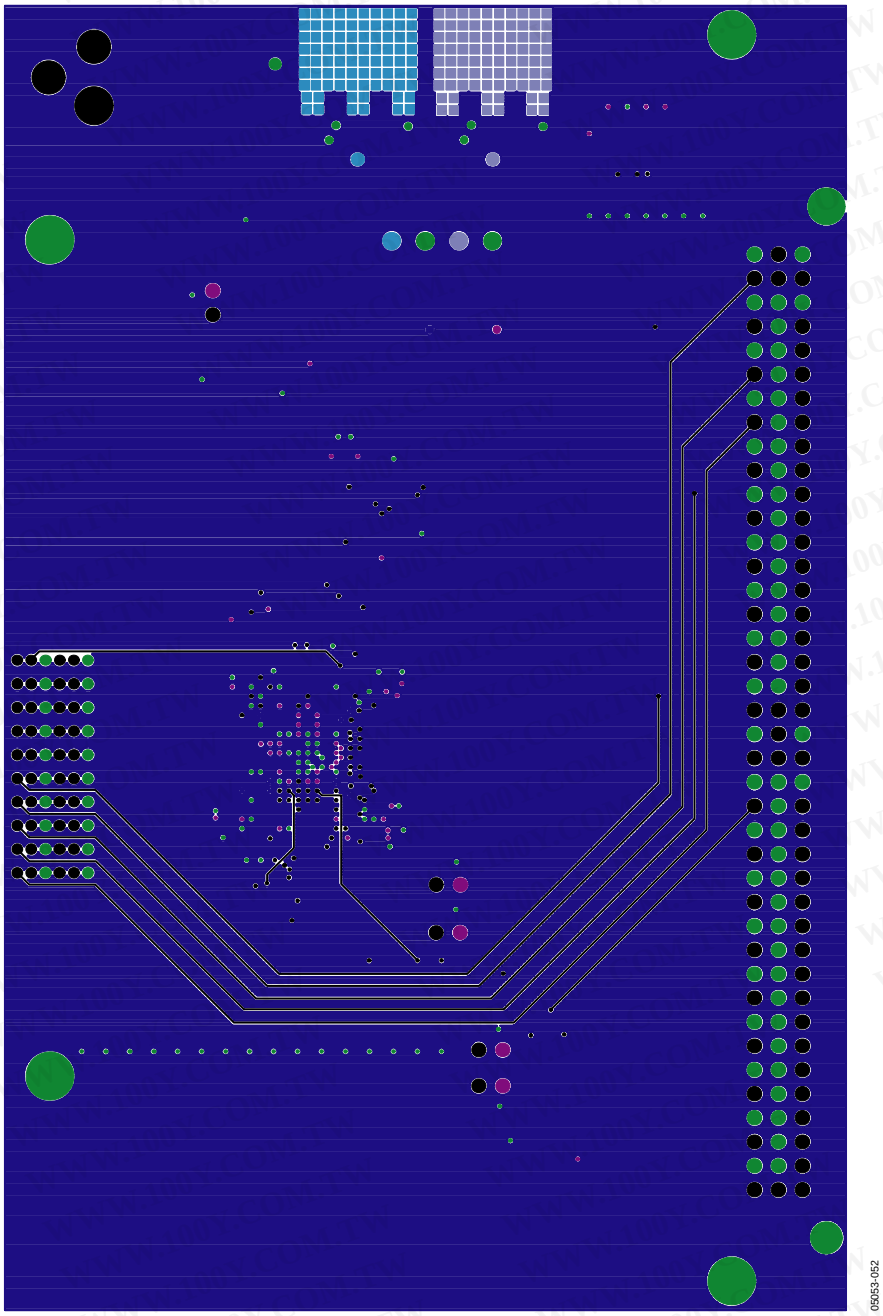

Figure 11. Layer 3—+1.5 V Power Plane and Signal

LAYER 4—SECONDARY SIDE

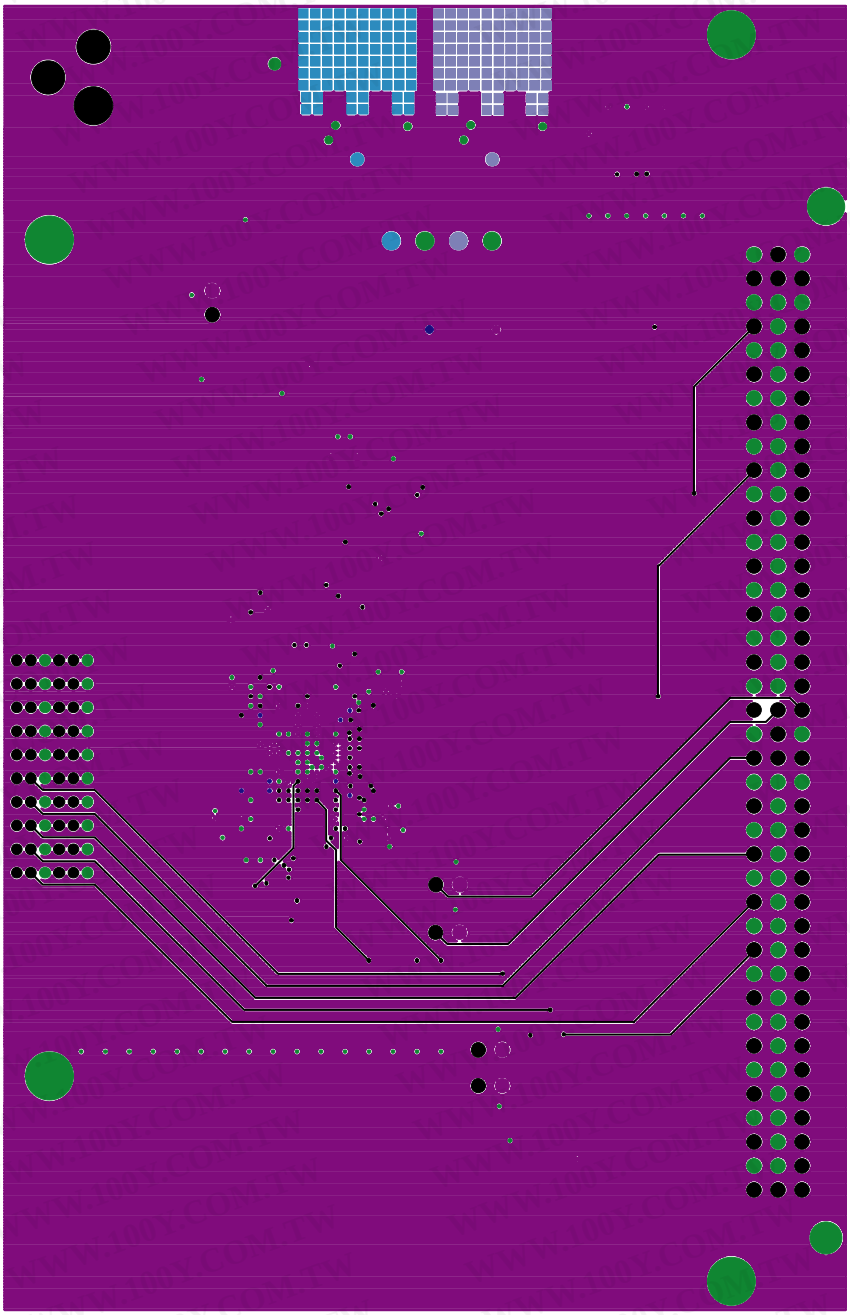

Figure 12. Layer 4—+3.3V Power Plane and Signal

LAYER 5—GROUND PLANE

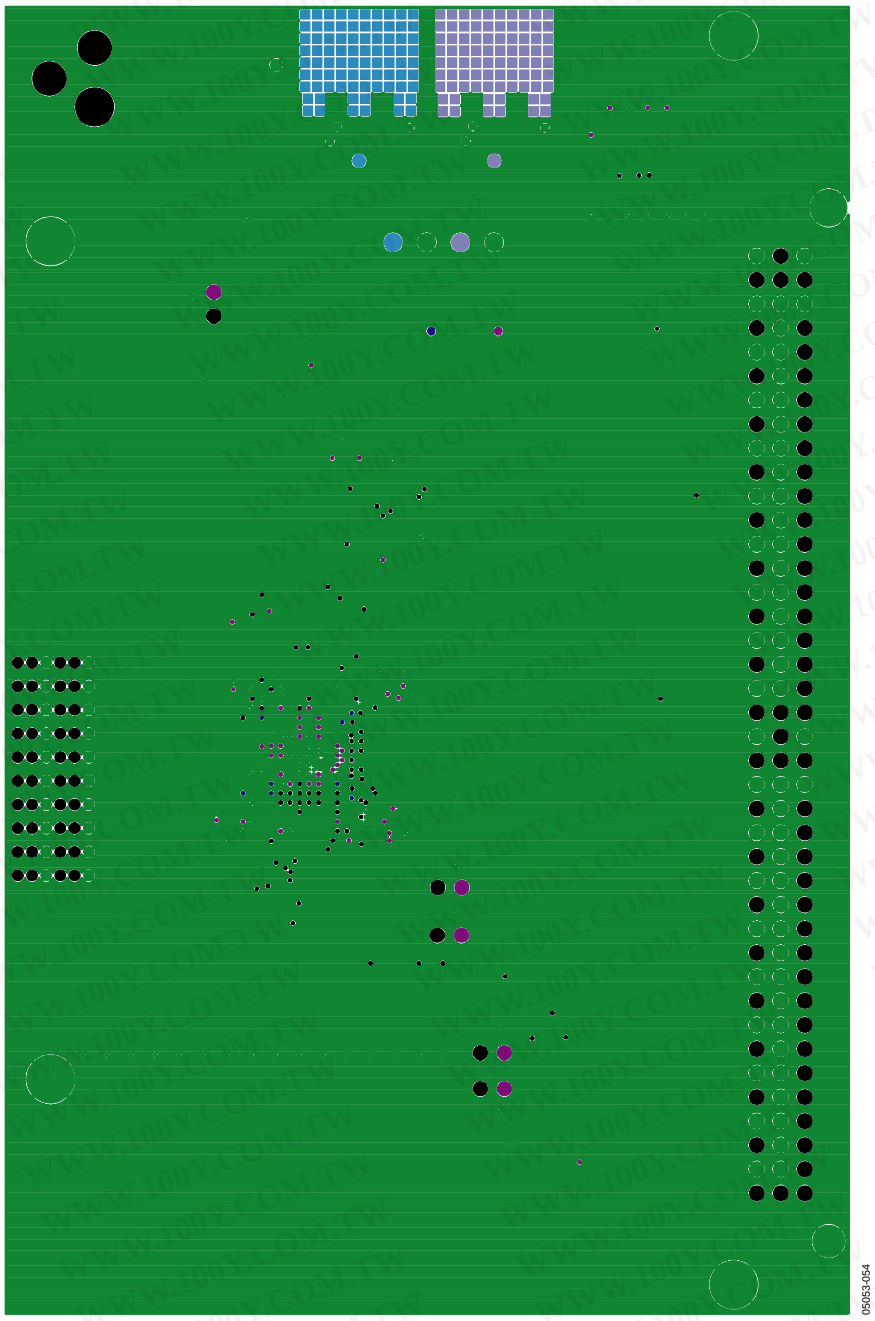

Figure 13. Layer 5—Ground Plane

LAYER 6—SECONDARY SIDE

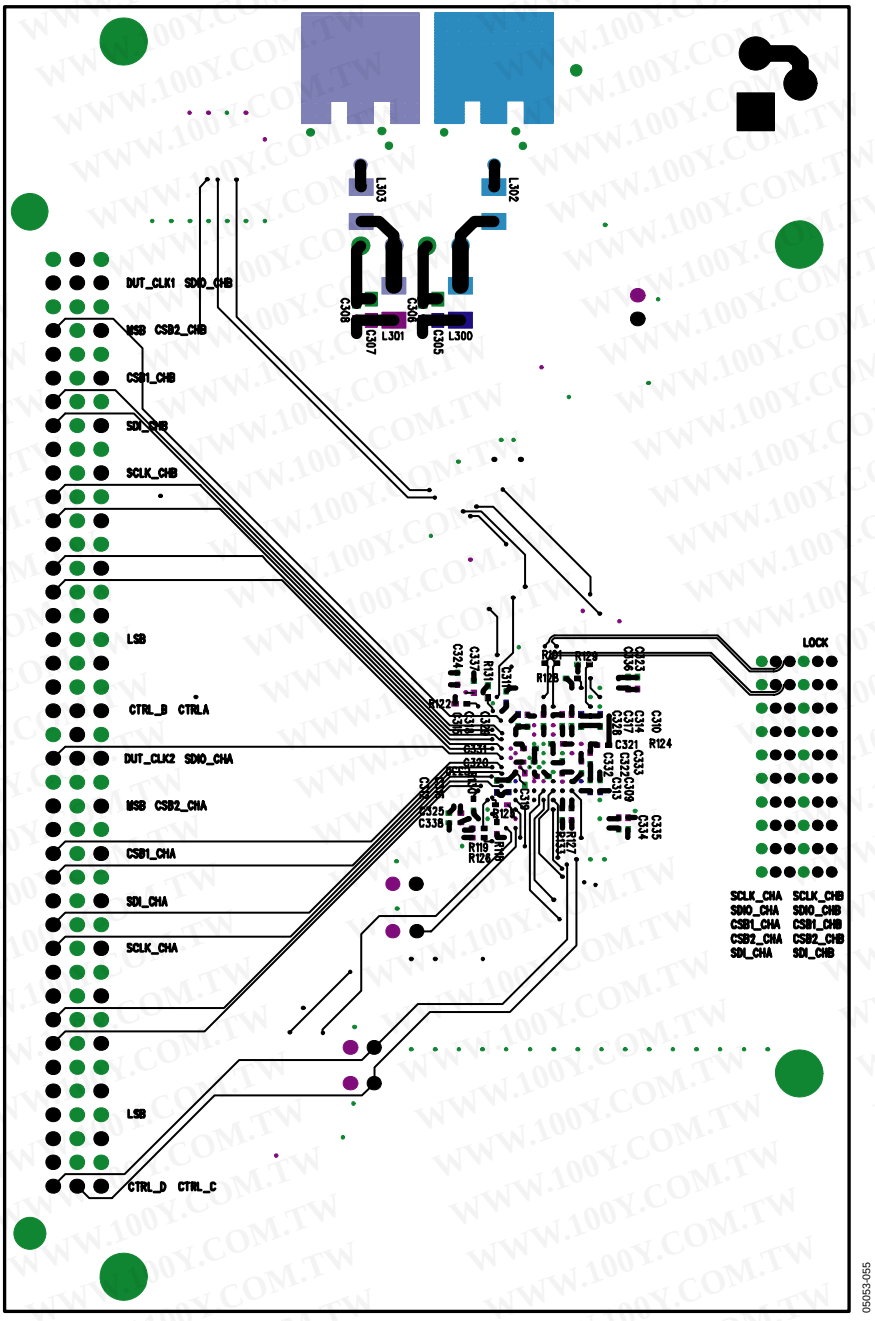

Figure 14. Layer 6—Secondary Side (Bottom)

ORDERING INFORMATION

BILL OF MATERIALS

Table 6.

Item	QTY	REFDES	Device	Package	Value	Manufacturer and Part No.
1	1	HSC-ADC-FPGA	PCB	PCB	REV D	
2	15	C309, C310, C311,C312, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327	Capacitor	402	0.1 µF, ceramic, X5R, 10 V, 10% tolerance	Panasonic, ECJ-0EB1A104K
3	2	C305, C307	Capacitor	805	10 µF, 6.3 V ±10%, ceramic, X5R	AVX, 08056D106KAT2A
4	2	C306, C308	Capacitor	603	0.1 µF, ceramic, X7R, 16 V, 10% tolerance	Kemet, C0603C104K4RACTU
5	15	C313, C314, C315, C316, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338	Capacitor	402	1 nF, ceramic, X7R, 25 V, 10% tolerance	Kemet, C0402C102K3RACTU
6	1	C300	Capacitor	1206	10 µF, tantalum, 16 V, 10% tolerance	Kemet, T491B106K016AS
7	4	C301, C302, C303, C304	Capacitor	603	1 µF, ceramic, X5R, 6.3 V, 10% tolerance	Panasonic, ECJ-1VB0J105K
8	3	CR100, CR200, CR300	LED	SMT	Green, 4 V, 5 m candela	Panasonic, LNJ314G8TRA
9	1	D301	Diode	DO-214AB	30 V, 3 A, SMC	Micro Commercial Co., SK33MSCT
10	1	D300	Diode	DO-214AA	50 V, 2 A, SMC	Micro Commercial Co., S2A
11	1	F300	Fuse	1210	6.0 V, 2.2 A trip current resettable fuse	Tyco/Raychem, NANOSMDC110F-2
12	1	FER300	Ferrite bead	2020	10 µH, 5 A, 50 V, 190 Ω @ 100 MHz	Murata, DLW5BSN191SQ2L
13	1	J200	Connector	HEADER	TSW-140-08-G-T-RA, 120-pin header assembly	Samtec, TSW-140-08-G-T-RA
14	1	J201	Connector	HEADER	87832-1420, 14-pin dual ROM shrouded header	Molex, 87832-1420
15	1	J300	Connector	0.1", PCMT	RAPC722, power supply connector	Switchcraft, SC1153
16	5	JP100, JP101, JP102, JP103, JP104	Connector	JMPR_OPEN	87267-0850	Samtec, TSW-102-07-G-S
17	4	L300, L301, L302, L303	Ferrite bead	1210	10 µH, BEAD CORE 3.2X2.5X1.6 SMD, 2 A	Panasonic, EXC-CL3225U1
18	1	P200	Connector	HEADER	1469028-1, right angle 2 pair, 25 mm, header assembly	Tyco, 1469028-1
19	2	PB100, PB101	Switch	SMT	SPST, 20 mA, push-button switch	Panasonic, EVQ-PHP03T
20	6	R100, R101, R103, R104, R105, R106	Resistor	402	100 Ω, 1/16 W, 5% tolerance	Panasonic, ERJ-2GEJ101X
21	1	R117	Resistor	603	1 kΩ, 1/10 W, 5% tolerance	Panasonic, ERJ-3GEYJ102V
22	18	R107, R108, R109, R110, R111, R112, R113, R115, R116, R122, R123, R124, R125, R126, R127, R201, R203, R204	Resistor	402	1 kΩ, 1/16 W, 1% tolerance	Panasonic, ERJ-2RKF1001X
23	3	R114, R200, R300	Resistor	402	261 Ω, 1/16 W, 1% tolerance	Panasonic, ERJ-2RKF2610X
24	10	R118, R119, R120, R121, R128, R129, R130, R131, R132, R133	Resistor	402	49.9 Ω, 1/16 W, 1% tolerance	Panasonic, ERJ-2RKF49R9X
25	1	R134	Resistor	402	10 kΩ, 1/16 W, 5% tolerance	Yageo America, 9C04021A1002JLHF3

Item	QTY	REFDES	Device	Package	Value	Manufacturer and Part No.
26	1	U301	IC	SOT-223	ADP33339AKC-3.3, 1.5 A, 3.3 V LDO regulator	ADI, ADP33339AKC-3.3
27	1	U300	IC	SOT-223	ADP33339AKC-1.5, 1.5 A, 1.5 V LDO regulator	ADI, ADP33339AKC-1.5
28	1	U100	IC	BGA	XC2V250-5FG256C, FPGA	Xilinx, XC2V250-5FG256C
29	1	U201	IC	SSOT	XCF02SV020, EPROM	Xilinx, XCF02SV020
30	4	MP101-104	Part of assembly		CBSB-14-01A-RT, 7/8" height, standoffs for circuit board support	Richco, CBSB-14-01A-RT
31	5	MP105-108	Part of assembly		SNT-100-BK-G-H, 100 mil jumpers	Samtec, SNT-100-BK-G-H

ORDERING GUIDE

Model	Package Description
HSC-ADC-FPGA-9289	Quad-Channel High Speed Serial LVDS to Parallel CMOS Converter for the AD9289 only
HSC-ADC-FPGA-4	Quad-Channel High Speed Serial LVDS to Parallel CMOS Converter for the AD9287, AD9219, AD9228, AD9229, AD9259

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

EB05053-0-11/05(B)