Differential Input, 1 MSPS 12-Bit ADC in µSOIC-8 and SO-8

AD7450

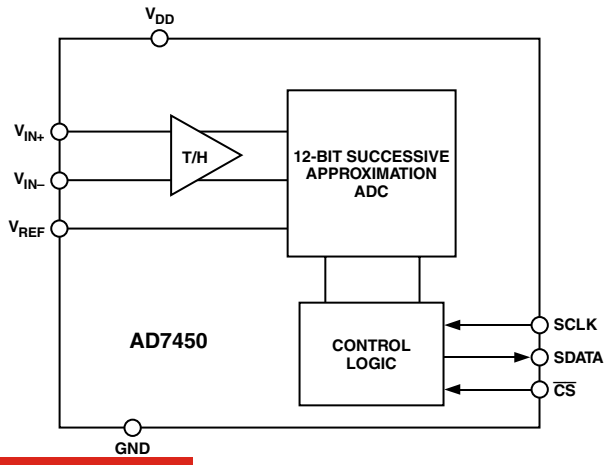
FEATURES

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 3 V and 5 V
- Low Power at Max Throughput Rate:
  - 3.75 mW Max at 833 kSPS with 3 V Supplies
  - 9 mW Max at 1 MSPS with 5 V Supplies
- Fully Differential Analog Input
- Wide Input Bandwidth:
  - 70 dB SINAD at 300 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High-Speed Serial Interface—SPI™/QSPI™
  - MICROWIRE™/DSP Compatible
- Power-Down Mode: 1 µA Max
- 8-Lead µSOIC and SOIC Packages

APPLICATIONS

- Transducer Interface
- Battery-Powered Systems
- Data Acquisition Systems
- Portable Instrumentation
- Motor Control
- Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7450 is a 12-bit, high-speed, low power, successive approximation (SAR) analog-to-digital converter that features a fully differential analog input. It operates from a single 3 V or 5 V power supply and features throughput rates up to 833 kSPS or 1 MSPS, respectively.

This part contains a low noise, wide bandwidth, differential track-and-hold amplifier (T/H) that can handle input frequencies in excess of 1 MHz with the –3 dB point typically being 20 MHz. The reference voltage for the AD7450 is applied externally to the V_{REF} pin and can be varied from 100 mV to 3.5 V, depending on the power supply and what suits the application. The value of the reference voltage determines the common-mode voltage range of the part. With this truly differential input structure and variable reference input, the user can select a variety of input ranges and bias points.

The conversion and data acquisition processes are controlled using $\overline{CS}$ and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signals are sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point.

The SAR architecture of this part ensures that there are no pipeline delays.

The AD7450 uses advanced design techniques to achieve low power dissipation at high throughput rates.

PRODUCT HIGHLIGHTS

1. Operation with either 3 V or 5 V power supplies.
2. High throughput with low power consumption. With a 3 V supply, the AD7450 offers 3.75 mW max power consumption for 833 kSPS throughput.
3. Fully differential analog input.
4. Flexible power/serial clock speed management. The conversion rate is determined by the serial clock, allowing the power to be reduced as the conversion time is reduced through the serial clock speed increase. This part also features a shutdown mode to maximize power efficiency at lower throughput rates.
5. Variable voltage reference input.
6. No pipeline delay.
7. Accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.
8. ENOB > 8 bits typically with 100 mV reference.

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Rev. A

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AD7450–SPECIFICATIONS[1] (V_{DD} = 2.7 V to 3.3 V, f_{SCLK} = 15 MHz, f_S = 833 kSPS, V_{REF} = 1.25 V, F_{IN} = 200 kHz; V_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 18 MHz, f_S = 1 MSPS, V_{REF} = 2.5 V, F_{IN} = 300 kHz; V_{CM}[2] = V_{REF}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Conditions/Comments	A Version	B Version	Unit
DYNAMIC PERFORMANCE				
Signal-to-(Noise + Distortion) Ratio (SINAD)[3]	V_{DD} = 5 V	70	70	dB min
	V_{DD} = 3 V	68	68	dB min
Total Harmonic Distortion (THD)[3]	V_{DD} = 5 V, –80 dB typ	–75	–75	dB max
	V_{DD} = 3 V, –78 dB typ	–73	–73	dB max
Peak Harmonic or Spurious Noise[3]	V_{DD} = 5 V, –82 dB typ	–75	–75	dB max
	V_{DD} = 3 V, –80 dB typ	–73	–73	dB max
Intermodulation Distortion (IMD)[3]				
Second Order Terms		–85	–85	dB typ
Third Order Terms		–85	–85	dB typ
Aperture Delay[3]		10	10	ns typ
Aperture Jitter[3]		50	50	ps typ
Full Power Bandwidth[3]	@ –3 dB	20	20	MHz typ
	@ –0.1 dB	2.5	2.5	MHz typ
Power Supply Rejection Ratio (PSRR)[3, 4]		–87	–87	dB typ
DC ACCURACY				
Resolution		12	12	Bits
Integral Nonlinearity (INL)[3]		±2	±1	LSB max
Differential Nonlinearity (DNL)[3]	Guaranteed No Missed Codes to 12 Bits	–1/+2	±1	LSB max
Zero Code Error[3]	V_{DD} = 5 V	±3	±3	LSB max
	V_{DD} = 3 V	±6	±6	LSB max
Positive Gain Error[3]	V_{DD} = 5 V	±3	±3	LSB max
	V_{DD} = 3 V	±6	±6	LSB max
Negative Gain Error[3]	V_{DD} = 5 V	±3	±3	LSB max
	V_{DD} = 3 V	±6	±6	LSB max
ANALOG INPUT				
Full-Scale Input Span	2 × V_{REF}[5]	$V_{IN+} - V_{IN-}$	$V_{IN+} - V_{IN-}$	V
Absolute Input Voltage				
V_{IN+}	V_{CM}[2] = V_{REF}	$V_{CM} \pm V_{REF}/2$	$V_{CM} \pm V_{REF}/2$	V
V_{IN-}	V_{CM}[2] = V_{REF}	$V_{CM} \pm V_{REF}/2$	$V_{CM} \pm V_{REF}/2$	V
DC Leakage Current		±1	±1	µA max
Input Capacitance	When in Track	20	20	pF typ
	When in Hold	6	6	pF typ
REFERENCE INPUT				
V_{REF} Input Voltage	5 V supply (±1% tolerance for specified performance)	2.5[6]	2.5[6]	V
	3 V supply (±1% tolerance for specified performance)	1.25[7]	1.25[7]	V
DC Leakage Current		±1	±1	µA max
V_{REF} Input Capacitance		15	15	pF typ
LOGIC INPUTS				
Input High Voltage, V_{INH}		2.4	2.4	V min
Input Low Voltage, V_{INL}		0.8	0.8	V max
Input Current, I_{IN}	Typically 10 nA, V_{IN} = 0 V or V_{DD}	±1	±1	µA max
Input Capacitance, C_{IN}[8]		10	10	pF max
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} = 5 V, I_{SOURCE} = 200 µA	2.8	2.8	V min
	V_{DD} = 3 V, I_{SOURCE} = 200 µA	2.4	2.4	V min
Output Low Voltage, V_{OL}	I_{SINK} = 200 µA	0.4	0.4	V max
Floating-State Leakage Current		±1	±1	µA max
Floating-State Output Capacitance[8]		10	10	pF max
Output Coding		Two's Complement	Two's Complement	

Parameter	Conditions/Comments	A Version	B Version	Unit
CONVERSION RATE				
Conversion Time	888 ns with an 18 MHz SCLK 1.07 µs with a 15 MHz SCLK	16	16	SCLK Cycles
Track-and-Hold Acquisition Time[3, 8]	Sine Wave Input	200	200	ns max
Throughput Rate[9]	V_{DD} = 5 V	1	1	MSPS max
	V_{DD} = 3 V	833	833	kSPS max
POWER REQUIREMENTS				
V_{DD}	Range: 3 V ± 10%; 5 V ± 5%	3/5	3/5	V min/max
I_{DD}[10, 11]				
Normal Mode (Static)	V_{DD} = 3 V/5 V SCLK; ON or OFF	0.5	0.5	mA typ
Normal Mode (Operational)	V_{DD} = 5 V; f_{SAMPLE} = 1 MSPS	1.8	1.8	mA max
	V_{DD} = 3 V; f_{SAMPLE} = 833 kSPS	1.25	1.25	mA max
Full Power-Down Mode	SCLK ON or OFF	1	1	µA max
Power Dissipation				
Normal Mode (Operational)	V_{DD} = 5 V; f_{SAMPLE} = 1 MSPS; 1.38 mW typ for 100 KSPS[10]	9	9	mW max
	V_{DD} = 3 V; f_{SAMPLE} = 833 kSPS; 0.53 mW typ for 100 KSPS[10]	3.75	3.75	mW max
Full Power-Down Mode	V_{DD} = 5 V; SCLK ON or OFF	5	5	µW max
	V_{DD} = 3 V; SCLK ON or OFF	3	3	µW max

NOTES
[1]Temperature range is as follows: A and B Versions: –40°C to +85°C.
[2]Common-mode voltage. The input signal can be centered on any choice of dc common-mode voltage as long as this value is in the range specified in Figures 8 and 9.
[3]See Terminology section.
[4]A 200 mV p-p sine wave, varying in frequency from 1 kHz to 200 kHz is coupled onto V_{DD}. A 2.2 nF capacitor is used to decouple V_{DD} to GND.
[5]If the input spans of V_{IN+} and V_{IN-} are both V_{REF}, and they are 180° out of phase, the differential voltage is $2 \times V_{REF}$.
[6]The AD7450 is functional with a reference input from 100 mV and for V_{DD} = 5 V, the reference can range up to 3.5 V (see References section).
[7]The AD7450 is functional with a reference input from 100 mV and for V_{DD} = 3 V, the reference can range up to 2.2 V (see References section).
[8]Sample tested @ 25°C to ensure compliance.
[9]See Serial Interface section.
[10]See Power Versus Throughput Rate section.
[11]Measured with a midscale dc input.

TIMING SPECIFICATIONS[1, 2] (V_{DD} = 2.7 V to 3.3 V, f_{SCLK} = 15 MHz, f_S = 833 kSPS, V_{REF} = 1.25 V; V_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 18 MHz, f_S = 1 MSPS, V_{REF} = 2.5 V; V_{CM}[3] = V_{REF}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} 3 V	5 V	Unit	Description
f_{SCLK}[4]	50	50	kHz min	
	15	18	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		t_{SCLK} = 1/f_{SCLK}
	1.07	0.88	µs max	SCLK = 15 MHz, 18 MHz
t_{QUIET}	25	25	ns min	Minimum Quiet Time between the End of a Serial Read and the Next Falling Edge of $\overline{CS}$
t_1	10	10	ns min	Minimum $\overline{CS}$ Pulsewidth
t_2	10	10	ns min	$\overline{CS}$ Falling Edge to SCLK Falling Edge Setup Time
t_3[5]	20	20	ns max	Delay from $\overline{CS}$ Falling Edge until SDATA Three-State Disabled
t_4[5]	40	40	ns max	Data Access Time after SCLK Falling Edge
t_5	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK High Pulsewidth
t_6	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK Low Pulsewidth
t_7	10	10	ns min	SCLK Edge to Data Valid Hold Time
t_8[6]	10	10	ns min	SCLK Falling Edge to SDATA Three-State Enabled
	35	35	ns max	SCLK Falling Edge to SDATA Three-State Enabled
$t_{POWER-UP}$[7]	1	1	µs max	Power-Up Time from Full Power-Down

NOTES
[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2]See Figure 1 and the Serial Interface section.
[3]Common-mode voltage.
[4]Mark/space ratio for the SCLK input is 40/60 to 60/40.
[5]Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V with V_{DD} = 5 V, and the time for an output to cross 0.4 V or 2.0 V for V_{DD} = 3 V.
[6]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[7]See Power-Up Time section.

Specifications subject to change without notice.

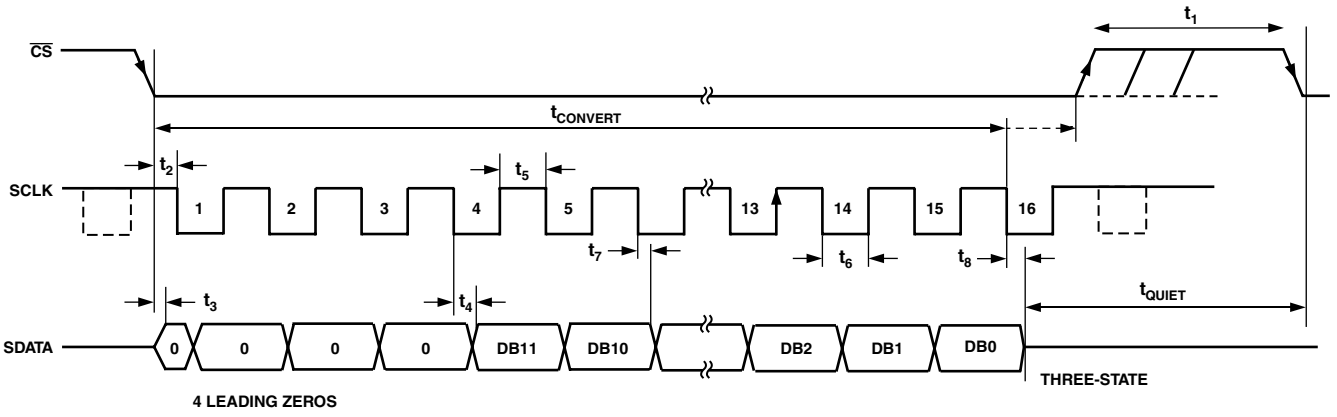


Figure 1. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +7 V
V_{IN+} to GND . . . . . –0.3 V to V_{DD} + 0.3 V
$V_{IN–}$ to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
V_{REF} to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial (A and B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
SOIC, µSOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 157°C/W (SOIC)
. . . . . 205.9°C/W (µSOIC)
θ_{JC} Thermal Impedance . . . . . 56°C/W (SOIC)
. . . . . 43.74°C/W (µSOIC)
Lead Temperature, Soldering
Vapor Phase (60 secs) . . . . . 215°C
Infrared (15 secs) . . . . . 220°C
ESD . . . . . 3.5 kV

NOTES
[1]Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

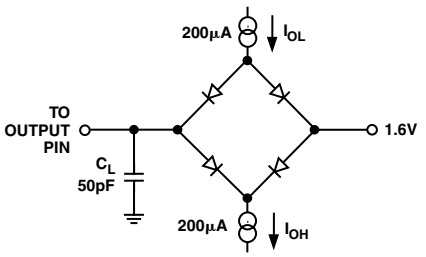
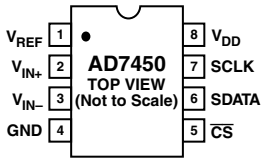


Figure 2. Load Circuit for Digital Output Timing Specifications

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7450 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Function
1	V_{REF}	Reference Input for the AD7450. An external reference must be applied to this input. For a 5 V power supply, the reference is 2.5 V (±1%), and for a 3 V power supply, the reference is 1.25 V (±1%) for specified performance. This pin should be decoupled to GND with a capacitor of at least 0.1 μF. See the References section for more details.
2	V_{IN+}	Positive Terminal for Differential Analog Input
3	V_{IN-}	Negative Terminal for Differential Analog Input
4	GND	Analog Ground. Ground reference point for all circuitry on the AD7450. All analog input signals and any external reference signal should be referred to this GND voltage.
5	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating a conversion on the AD7450 and framing the serial data transfer.
6	SDATA	Serial Data. Logic output. The conversion result from the AD7450 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data that is provided MSB first. The output coding is two's complement.
7	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7450's conversion process.
8	V_{DD}	Power Supply Input. V_{DD} is 3 V (±10%) or 5 V (±5%). This supply should be decoupled to GND with a 0.1 μF capacitor and a 10 μF tantalum capacitor.

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\text{–}to\text{–}(Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7450, it is defined as:

$$THD\ (dB) = 20\ log\ \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m and n = 0, 1, 2, or 3. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa –2fb).

The AD7450 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay
This is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter
This is the sample-to-sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth
The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

Common-Mode Rejection Ratio (CMRR)
The common-mode rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} of frequency fs:

$$CMRR(dB) = 10\ \log\ (Pf/Pfs)$$

Pf is the power at the frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

Integral Nonlinearity (INL)
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Code Error
This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal $V_{IN+} - V_{IN-}$ (i.e., 0 LSB).

Positive Gain Error
This is the deviation of the last code transition (011...110 to 011...111) from the ideal $V_{IN+} - V_{IN-}$ (i.e., $+V_{REF} - 1$ LSB), after the zero code error has been adjusted out.

Negative Gain Error
This is the deviation of the first code transition (100...000 to 100...001) from the ideal $V_{IN+} - V_{IN-}$ (i.e., $-V_{REF} + 1$ LSB), after the zero code error has been adjusted out.

Track and Hold Acquisition Time
The track and hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

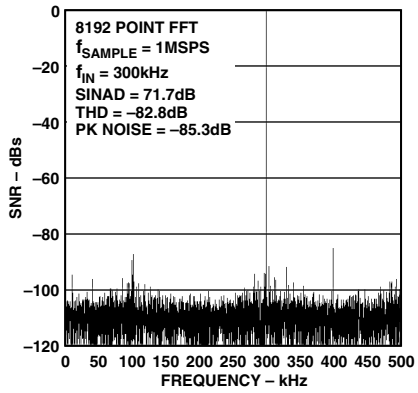
Power Supply Rejection Ratio (PSRR)
The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_S.

$$PSRR\ (dB) = 10\ log\ (Pf/Pfs)$$

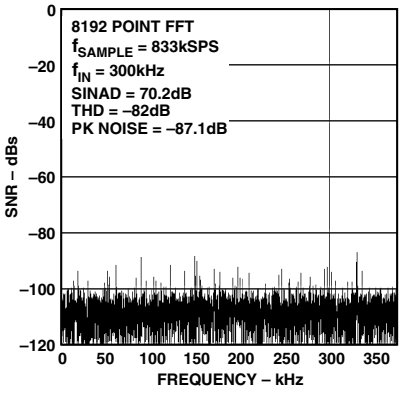
Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

AD7450–Typical Performance Characteristics

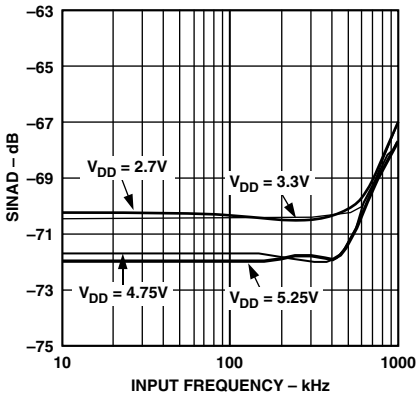
(Default Conditions: T_A = 25°C)



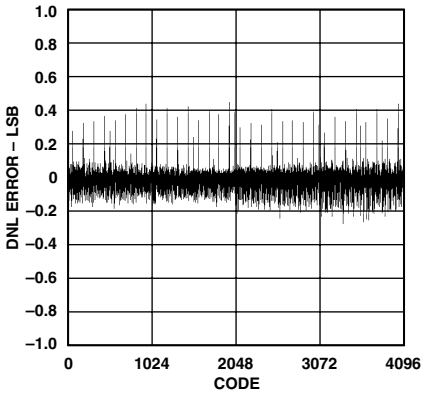
TPC 1. Dynamic Performance at 1 MSPS with V_{DD} = 5 V



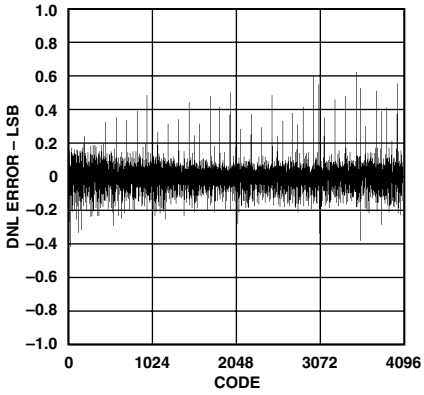
TPC 2. Dynamic Performance at 833 kSPS with V_{DD} = 3 V



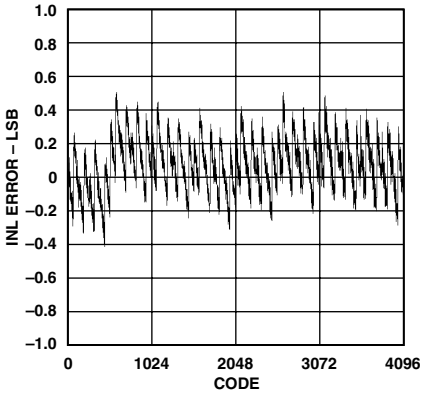
TPC 3. SINAD vs. Analog Frequency for Various Supply Voltages



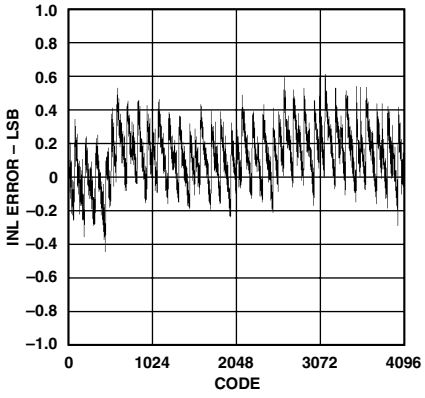
TPC 4. Typical Differential Nonlinearity (DNL) V_{DD} = 5 V



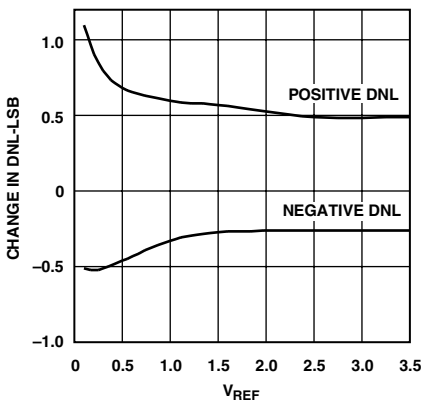
TPC 5. Typical Differential Nonlinearity (DNL) V_{DD} = 3 V



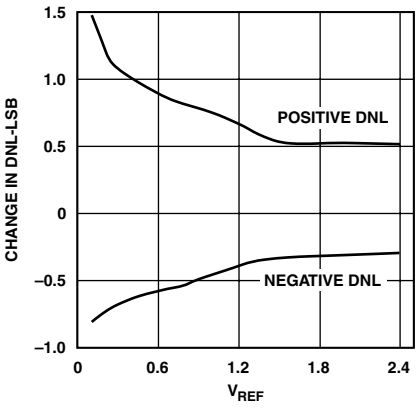
TPC 6. Typical Integral Nonlinearity (INL) V_{DD} = 5 V



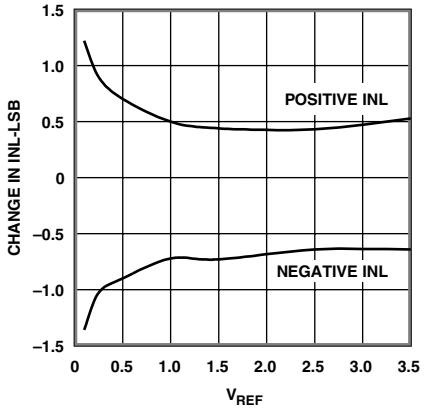
TPC 7. Typical Integral Nonlinearity (INL) V_{DD} = 3 V



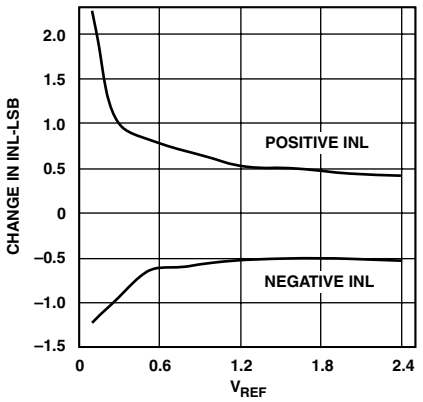
TPC 8. Change in DNL vs. Reference Voltage V_{DD} = 5 V



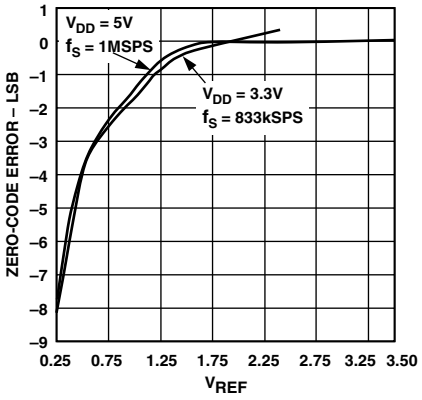
*TPC 9. Change in DNL vs. Reference Voltage V_{DD} = 3.3 V**



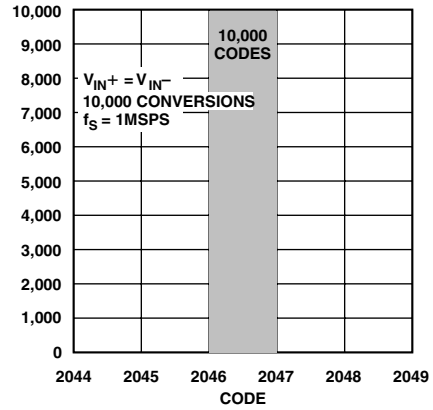
TPC 10. Change in INL vs. Reference Voltage V_{DD} = 5 V



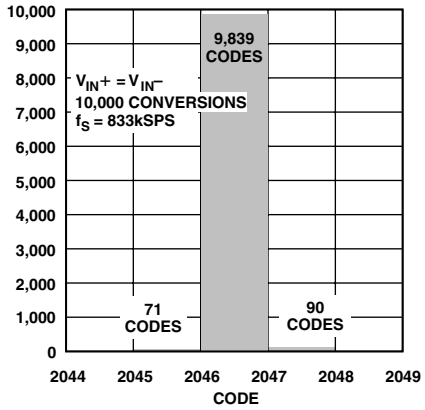
*TPC 11. Change in INL vs. Reference Voltage V_{DD} = 3.3 V**



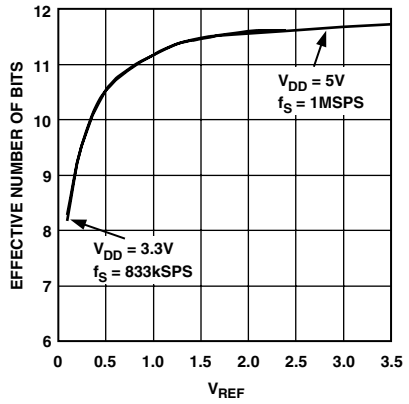
*TPC 12. Change in Zero-Code Error vs. Reference Voltage V_{DD} = 5 V and 3.3 V**



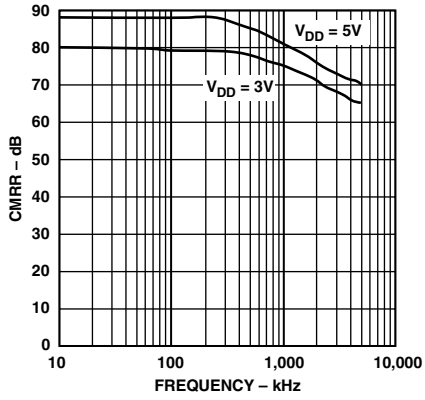
TPC 13. Histogram of the Output Codes with a DC Input for V_{DD} = 5 V



TPC 14. Histogram of the Output Codes with a DC Input for V_{DD} = 3 V



*TPC 15. Change in ENOB vs. Reference Voltage V_{DD} = 5 V and 3.3 V**



TPC 16. CMRR vs. Input Frequency for V_{DD} = 5 V and 3 V

*See References section.

CIRCUIT INFORMATION

The AD7450 is a fast, low power, single-supply, 12-bit successive approximation analog-to-digital converter (ADC). It can operate with a 5 V and 3 V power supply and is capable of throughput rates up to 1 MSPS and 833 kSPS when supplied with an 18 MHz or 15 MHz clock, respectively. This part requires an external reference to be applied to the V_{REF} pin, with the value of the reference chosen depending on the power supply and what suits the application.

When operated with a 5 V supply, the maximum reference that can be applied to the part is 3.5 V, and when operated with a 3 V supply, the maximum reference that can be applied to the part is 2.2 V. (See the References section.)

The AD7450 has an on-chip differential track-and-hold amplifier, a successive approximation (SAR) ADC, and a serial interface that is housed in either an 8-lead SOIC or µSOIC package. The serial clock input accesses data from the part and also provides the clock source for the successive approximation ADC. The AD7450 features a power-down option for reduced power consumption between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7450 is a successive approximation ADC based on two capacitive DACs. Figures 3 and 4 show simplified schematics of the ADC in acquisition and conversion phase, respectively. The ADC is comprised of control logic, a SAR, and two capacitive DACs. In Figure 3 (the acquisition phase), SW3 is closed and SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

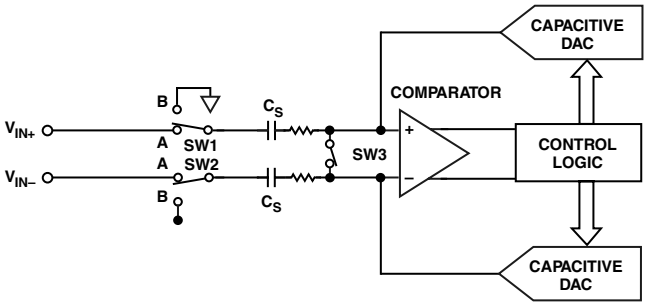


Figure 3. ADC Acquisition Phase

When the ADC starts a conversion (Figure 4), SW3 will open and SW1 and SW2 will move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC's output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.

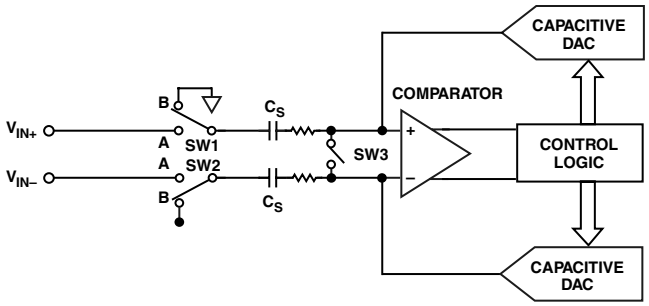


Figure 4. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7450 is two's complement. The designed code transitions occur at successive LSB values (i.e., 1 LSB, 2 LSB, and so on), and the LSB size is $2 \times V_{REF} / 4096$. The ideal transfer characteristic of the AD7450 is shown in Figure 5.

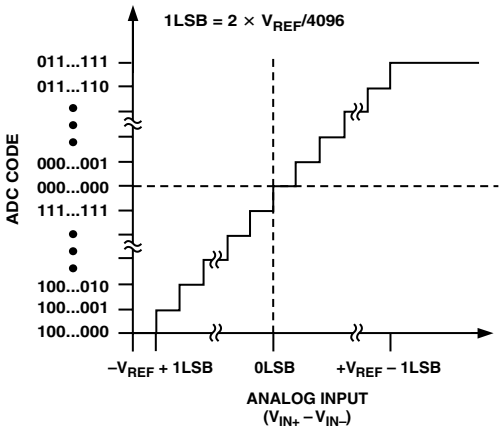


Figure 5. Ideal Transfer Characteristics

TYPICAL CONNECTION DIAGRAM

Figure 6 shows a typical connection diagram for the AD7450 for both 5 V and 3 V supplies. In this setup, the GND pin is connected to the analog ground plane of the system. The V_{REF} pin is connected to either a 2.5 V or a 1.25 V decoupled reference source, depending on the power supply, to set up the analog input range. The common-mode voltage has to be set up externally and is the value that the two inputs are centered on. For more details on driving the differential inputs and setting up the common mode, see the Driving Differential Inputs section. The conversion result for the ADC is output in a 16-bit word consisting of four leading zeros followed by the MSB of the 12-bit result. For applications where power consumption is of concern, the power-down mode should be used between conversions, or bursts of several conversions, to improve power performance. See Modes of Operation section.

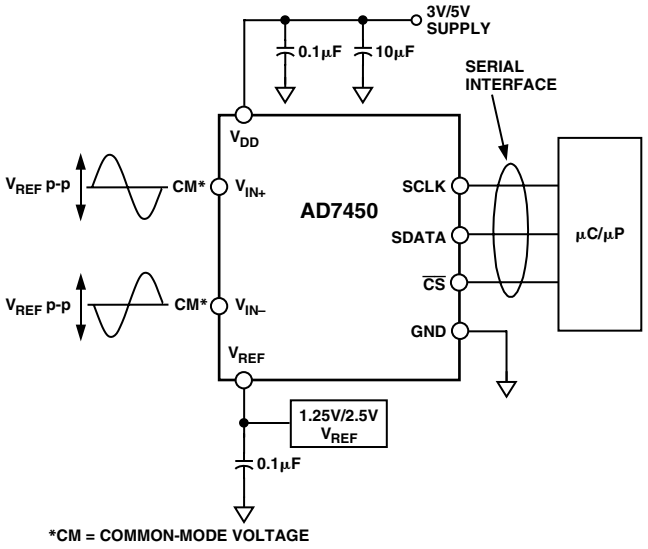


Figure 6. Typical Connection Diagram

THE ANALOG INPUT

The analog input of the AD7450 is fully differential. Differential signals have a number of benefits over single-ended signals, including noise immunity based on the device's common-mode rejection, improvements in distortion performance, doubling of the device's available dynamic range, and flexibility in input ranges and bias points.

Figure 7 defines the fully differential analog input of the AD7450.

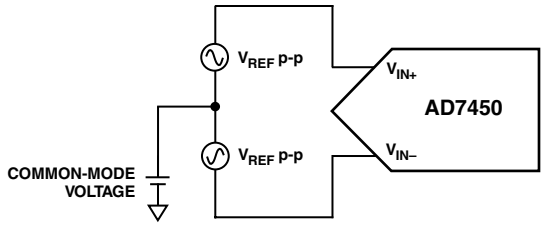


Figure 7. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins (i.e., $V_{IN+} - V_{IN-}$). V_{IN+} and V_{IN-} are simultaneously driven by two signals each of amplitude V_{REF} that are 180° out of phase. The amplitude of the differential signal is therefore $-V_{REF}$ to $+V_{REF}$ p-p (i.e., $2 \times V_{REF}$). This is regardless of the common mode (CM). The common mode is the average of the two signals, i.e., $(V_{IN+} + V_{IN-})/2$, and is therefore the voltage that the two inputs are centered on. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally and its range varies with V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range will be determined by the amplifier's output voltage swing.

Figures 8 and 9 show how the common-mode range typically varies with V_{REF} for both a 5 V and a 3 V power supply. The common mode must be in this range to guarantee the functionality of the AD7450.

For ease of use, the common mode can be set up to be equal to V_{REF}, resulting in the differential signal being ±V_{REF} centered on V_{REF}. When a conversion takes place, the common mode is rejected resulting in a virtually noise free signal of amplitude $-V_{REF}$ to $+V_{REF}$ corresponding to the digital codes of 0 to 4095.

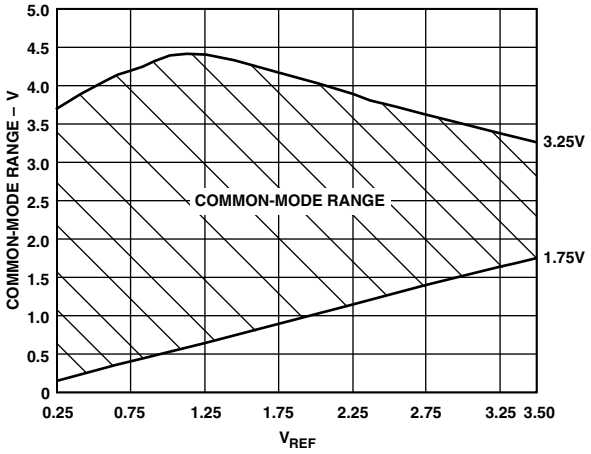


Figure 8. Input Common-Mode Range vs. V_{REF} (V_{DD} = 5 V and V_{REF} (Max) = 3.5 V)

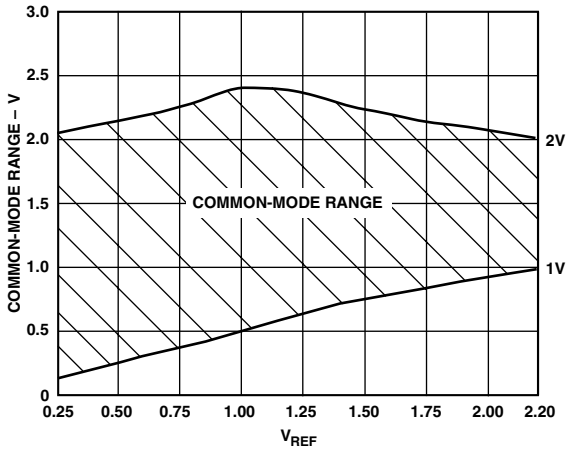


Figure 9. Input Common-Mode Range vs. V_{REF} (V_{DD} = 3 V and V_{REF} (Max) = 2.2 V)

Figure 10 shows examples of the inputs to V_{IN+} and V_{IN-} for different values of V_{REF} for V_{DD} = 5 V. It also gives the maximum and minimum common-mode voltages for each reference value according to Figure 8.

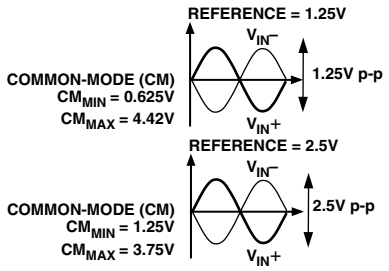


Figure 10. Examples of the Analog Inputs to V_{IN+} and V_{IN-} for Different Values of V_{REF} for V_{DD} = 5 V

Analog Input Structure

Figure 11 shows the equivalent circuit of the analog input structure of the AD7450. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This will cause these diodes to become forward biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The capacitors, C1, in Figure 11 are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the ON resistance of the switches. The value of these resistors is typically about 100 Ω. The capacitors, C2, are the ADC's sampling capacitors and have a capacitance of 16 pF typically.

For ac applications, removing high-frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

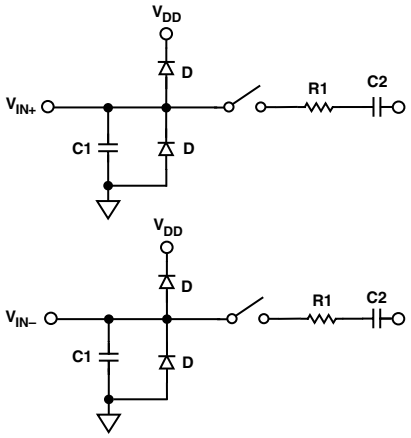


Figure 11. Equivalent Analog Input Circuit Conversion Phase—Switches Open Track Phase—Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and the performance will degrade. Figure 12 shows a graph of the THD versus the analog input signal frequency for different source impedances.

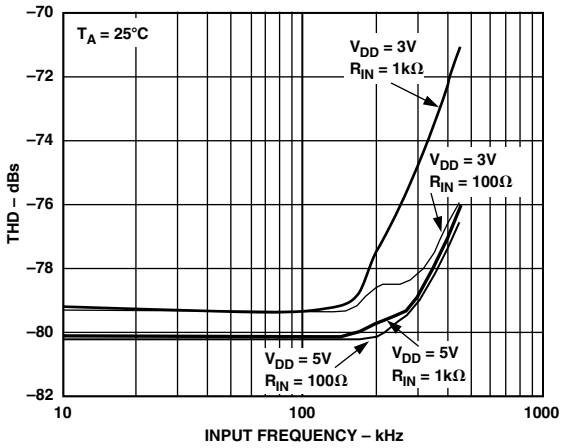


Figure 12. THD vs. Analog Input Frequency for Various Source Impedances for V_{DD} = 5 V and 3 V

Figure 13 shows a graph of the THD versus the analog input frequency for V_{DD} of 5 V ± 5% and 3 V ± 10%, while sampling at 1 MSPS and 833 kSPS with a SCLK of 18 MHz and 15 MHz, respectively. In this case, the source impedance is 10 Ω.

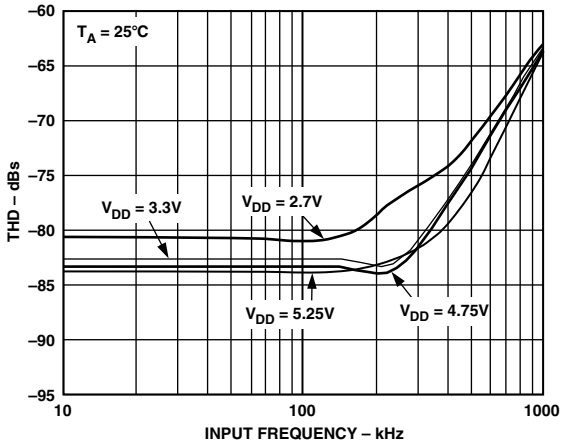


Figure 13. THD vs. Analog Input Frequency for 3 V ± 10% and 5 V ± 5% Supply Voltages

DRIVING DIFFERENTIAL INPUTS

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally and has a range that is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs (see Figures 8 and 9). Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

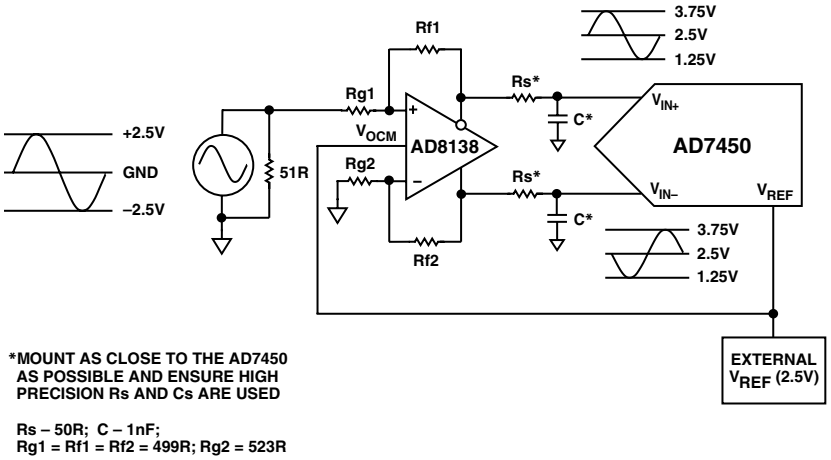


Figure 14. Using the AD8138 as a Single-Ended-to-Differential Amplifier

Differential Amplifier

An ideal method of applying differential drive to the AD7450 is to use a differential amplifier, such as the AD8138. This part can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. In both cases, the analog input needs to be bipolar. It also provides common-mode level shifting and buffering of the bipolar input signal. Figure 14 shows how the AD8138 can be used as a single-ended-to-differential amplifier. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC via a pair of series resistors to minimize the effects of switched capacitance on the front end of the ADC. The RC low-pass filter on each analog input is recommended in ac applications to remove the high-frequency components of the analog input. The architecture of the AD8138 results in outputs that are highly balanced over a wide frequency range without requiring tightly matched external components.

If the analog input source being used has zero impedance then all four resistors (Rg1, Rg2, Rf1, and Rf2) should be the same. If the source has a 50 Ω impedance and a 50 Ω termination, for example, the value of Rg2 should be increased by 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain (see Figure 14). The outputs of the amplifier are perfectly matched, balanced differential outputs of identical amplitude and exactly 180° out of phase.

The AD8138 is specified with 3 V, 5 V, and ±5 V power supplies, but the best results are obtained when it is supplied by ±5 V. A lower cost device that could also be used in this configuration with slight differences in characteristics to the AD8138, but with similar performance and operation, is the AD8132.

Op Amp Pair

An op amp pair can be used to directly couple a differential signal to the AD7450. The circuit configurations shown in Figures 15a and 15b show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and a unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. Examples of suitable dual op amps that could be used in this configuration to provide differential drive to the AD7450 are the AD8042, AD8056, and AD8022.

Care must be taken when choosing the op amp, since the selection will depend on the required power supply and the system performance objectives. The driver circuits in Figure 15a and Figure 15b are optimized for dc coupling applications requiring optimum distortion performance.

The differential op amp driver circuit in Figure 15a is configured to convert and level shift a single-ended, ground referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

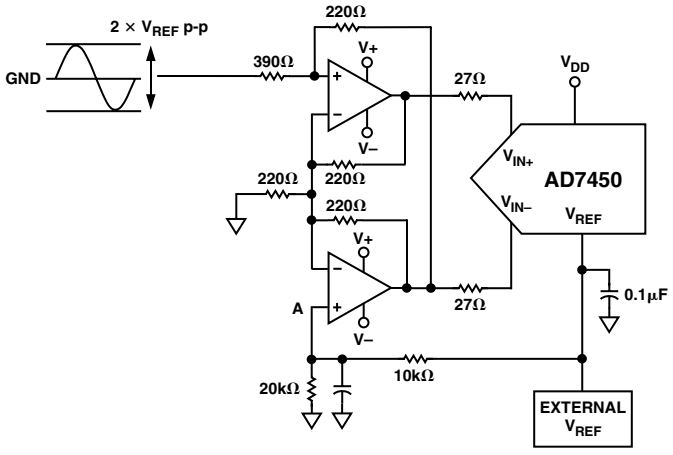


Figure 15a. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Input into a Differential Input

The circuit configuration shown in Figure 15b converts a unipolar, single-ended signal into a differential signal.

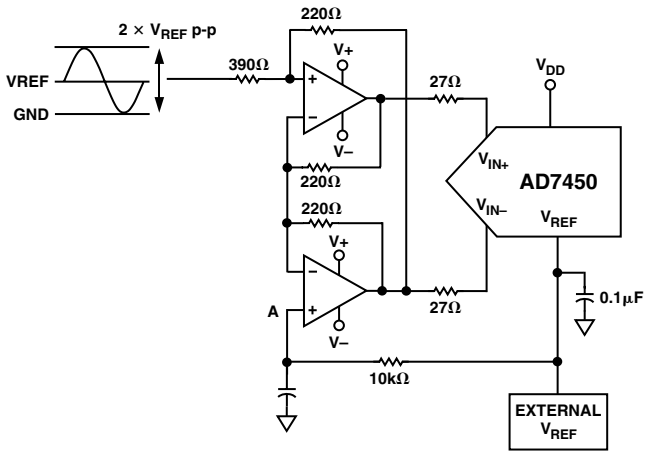


Figure 15b. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Input into a Differential Input

RF Transformer

In systems that do not need to be dc-coupled, an RF transformer with a center tap offers a good solution for generating differential inputs. Figure 16 shows how a transformer is used for single-ended-to-differential conversion. It provides the benefits of operating the ADC in the differential mode without contributing additional noise and distortion. An RF transformer also has the benefit of providing electrical isolation between the signal source and the ADC. A transformer can be used for most ac applications. The center tap is used to shift the differential signal to the common-mode level required. In this case, it is connected to the reference so the common-mode level is the value of the reference.

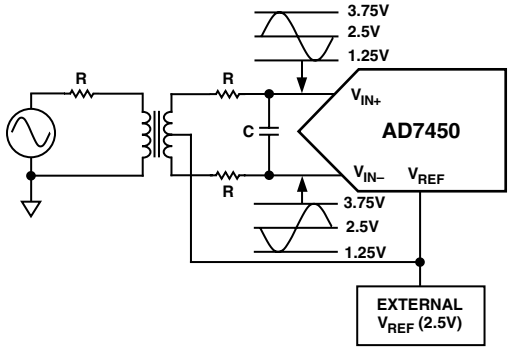


Figure 16. Using an RF Transformer to Generate Differential Inputs

REFERENCES SECTION

An external reference source is required to supply the reference to the AD7450. This reference input can range from 100 mV to 3.5 V. With a 5 V power supply, the specified reference is 2.5 V and the maximum reference is 3.5 V. With a 3.3 V power supply, the specified reference is 1.25 V and the maximum reference is 2.4 V. In both cases, the reference is functional from 100 mV. It is important to ensure that, when choosing the reference value for a particular application, the maximum analog input range (V_{IN} max) is never greater than V_{DD} + 0.3 V to comply with the maximum ratings of the part. The following two examples calculate the maximum V_{REF} input that can be used when operating the AD7450 at V_{DD} of 5 V and 3.3 V, respectively.

Example 1:

$$V_{IN}\ max = V_{DD} + 0.3$$

$$V_{IN}\ max = V_{REF} + V_{REF}/2$$

$$If\ V_{DD} = 5\,V$$

$$Then\ V_{IN}\ max = 5.3\,V$$

$$Therefore\ 3 \times V_{REF}/2 = 5.3\,V$$

$$V_{REF}\ max = 3.5\,V$$

Therefore, when operating at V_{DD} = 5 V, the value of V_{REF} can range from 100 mV to a maximum value of 3.5 V. When V_{DD} = 4.75 V, V_{REF} max = 3.37 V.

Example 2:

$$V_{IN}\ max = V_{DD} + 0.3$$

$$V_{IN}\ max = V_{REF} + V_{REF}/2$$

$$If\ V_{DD} = 3.3\,V$$

$$Then\ V_{IN}\ max = 3.6\,V$$

$$Therefore\ 3 \times V_{REF}/2 = 3.6\,V$$

$$V_{REF}\ max = 2.4\,V$$

Therefore, when operating at V_{DD} = 3.3 V, the value of V_{REF} can range from 100 mV to a maximum value of 2.4 V. When V_{DD} = 2.7 V, V_{REF} max = 2 V.

These examples show that the maximum reference applied to the AD7450 is directly dependant on the value of V_{DD}.

The performance of the part at different reference values is shown in TPC 8 to TPC 12 and in TPC 15. The value of the reference sets the analog input span and the common-mode voltage range. Errors in the reference source will result in gain errors in the AD7450 transfer function and will add to specified full-scale errors on the part. A capacitor of 0.1 µF should be used to decouple the V_{REF} pin to GND. Table I lists examples of suitable voltage references to be used that are available from Analog Devices, and Figure 17 shows a typical connection diagram for the V_{REF} pin.

Table I. Examples of Suitable Voltage References

Reference	Output Voltage	Initial Accuracy (% Max)	Operating Current (µA)
AD589	1.235	1.2–2.8	50
AD1580	1.225	0.08–0.8	50
REF192	2.5	0.08–0.4	45
REF43	2.5	0.06–0.1	600
AD780	2.5	0.04–0.2	1000

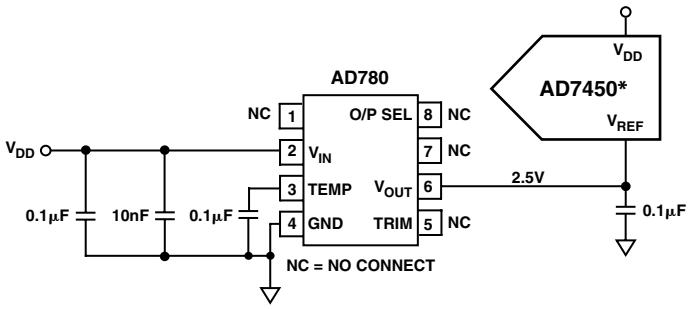


Figure 17. Typical V_{REF} Connection Diagram for V_{DD} = 5 V

SINGLE-ENDED OPERATION

When supplied with a 5 V power supply, the AD7450 can handle a single-ended input. The design of this part is optimized for differential operation, so with a single-ended input, performance will degrade. Linearity will typically degrade by 0.2 LSBs, zero code and full-scale errors will typically degrade by 2 LSBs, and ac performance is not guaranteed.

To operate the AD7450 in single-ended mode, the V_{IN+} input is coupled to the signal source, while the V_{IN-} input is biased to the appropriate voltage corresponding to the midscale code transition. This voltage is the common mode, which is a fixed dc voltage (usually the reference). The V_{IN+} input swings around this value and should have voltage span of $2 \times V_{REF}$ to make use of the full dynamic range of the part. Therefore, the input signal will have peak-to-peak values of common mode ± V_{REF}. If the analog input is unipolar then an op amp in a noninverting unity gain configuration can be used to drive the V_{IN+} pin. Because the ADC operates from a single supply, it is necessary to level shift ground based bipolar signals to comply with the input requirements. An op amp can be configured to rescale and level shift the ground based bipolar signal so it is compatible with the selected input range of the AD7450 (see Figure 18).

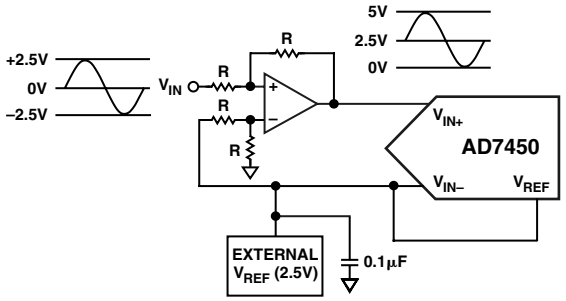


Figure 18. Applying a Bipolar Single-Ended Input to the AD7450

SERIAL INTERFACE

Figure 19 shows a detailed timing diagram for the serial interface of the AD7450. The serial clock provides the conversion clock and also controls the transfer of data from the AD7450 during conversion. $\overline{CS}$ initiates the conversion process and frames the data transfer. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion initiated at this point. The conversion will require 16 SCLK cycles to complete.

Once 13 SCLK falling edges have occurred, the track-and-hold will go back into track on the next SCLK rising edge as shown at Point B in Figure 19. On the 16th SCLK falling edge, the SDATA line will go back into three-state.

If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated, and the SDATA line will go back into three-state. Sixteen serial clock cycles are required to perform a conversion and to access data from the AD7450. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out on the subsequent SCLK falling edges beginning with the second leading zero. Thus, the first falling clock edge on the serial clock provides the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge. Once the conversion is complete and the data has been accessed after the 16 clock cycles, it is important to ensure that before the next conversion is initiated, enough time is left to meet the acquisition and quiet time specifications (see timing examples). To achieve 1 MSPS with an 18 MHz clock for V_{DD} = 5 V, an 18 clock burst will perform the conversion and leave enough time before the next conversion for the acquisition and quiet time. This is the same for achieving 833 kSPS with a 15 MHz clock for V_{DD} = 3 V.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge, i.e., the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the leading zero provided and the 15th SCLK edge would have DB0 provided.

Timing Example 1

Having f_{SCLK} = 18 MHz and a throughput rate of 1 MSPS gives a cycle time of:

$$1/Throughput = 1/1{,}000{,}000 = 1\ \mu s$$

A cycle consists of:

$$t_2 + 12.5\left(1/f_{SCLK}\right) + t_{ACQ} = 1\ \mu s$$

Therefore, if t_2 = 10 ns then:

$$10\ ns + 12.5\left(1/18\ MHz\right) + t_{ACQ} = 1\ \mu s$$

$$t_{ACQ} = 296\ ns$$

This 296 ns satisfies the requirement of 200 ns for t_{ACQ}. From Figure 20, t_{ACQ} is comprised of:

$$2.5\left(1/f_{SCLK}\right) + t_8 + t_{QUIET}$$

where t_8 = 35 ns. This allows a value of 122 ns for t_{QUIET}, satisfying the minimum requirement of 25 ns.

Timing Example 2

Having f_{SCLK} = 5 MHz and a throughput rate of 315 kSPS gives a cycle time of:

$$1/Throughput = 1/315{,}000 = 3.174\ \mu s$$

A cycle consists of:

$$t_2 + 12.5\left(1/f_{SCLK}\right) + t_{ACQ} = 3.174\ \mu s$$

Therefore if t_2 is 10 ns then:

$$10\ ns + 12.5\left(1/5\ MHz\right) + t_{ACQ} = 3.174\ \mu s$$

$$t_{ACQ} = 664\ ns$$

This 664 ns satisfies the requirement of 200 ns for t_{ACQ}. From Figure 20, t_{ACQ} is comprised of:

$$2.5\left(1/f_{SCLK}\right) + t_8 + t_{QUIET}$$

where t_8 = 35 ns. This allows a value of 129 ns for t_{QUIET}, satisfying the minimum requirement of 25 ns.

As in this example and with other slower clock values, the signal may already be acquired before the conversion is complete, but it is still necessary to leave 25 ns minimum t_{QUIET} between conversions. In Timing Example 2, the signal should be fully acquired at approximately Point C in Figure 20.

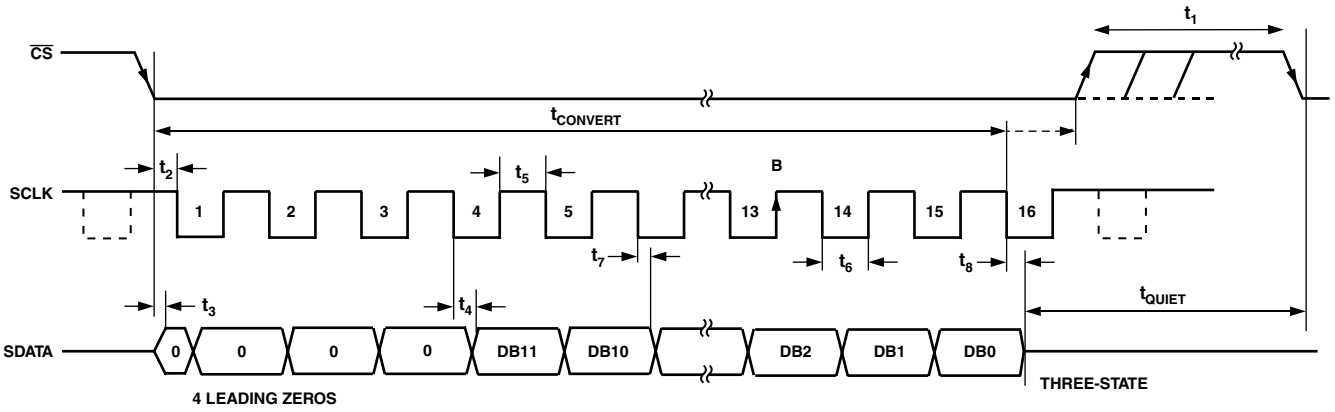


Figure 19. Serial Interface Timing Diagram

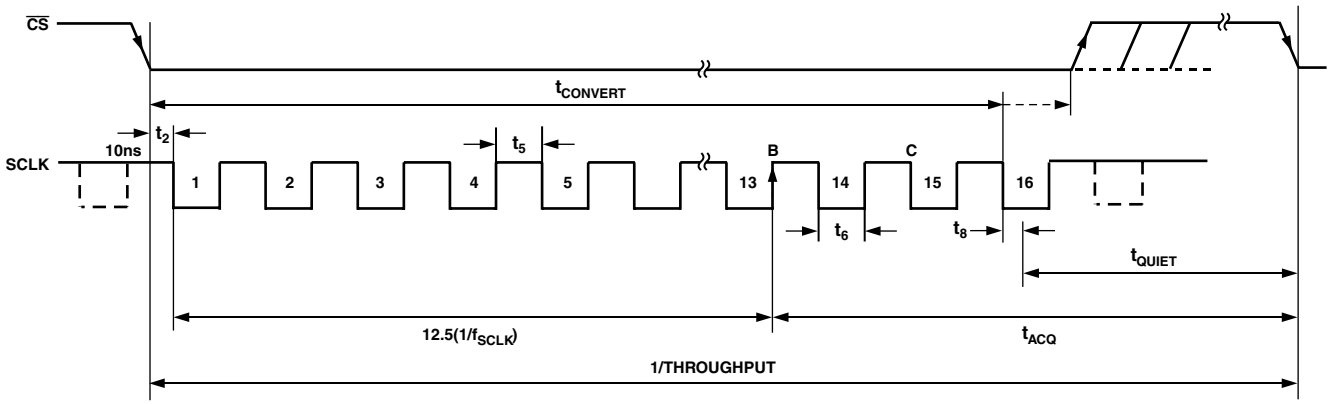


Figure 20. Serial Interface Timing Example

MODES OF OPERATION

The mode of operation of the AD7450 is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, normal mode and power-down mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether or not the AD7450 will enter the power-down mode. Similarly, if already in power-down, $\overline{CS}$ controls whether the device will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for the fastest throughput rate performance. The user does not have to worry about any power-up times since the AD7450 is kept fully powered up. Figure 21 shows the general diagram of the operation of the AD7450 in this mode. The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$.

If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part will remain powered up, but the conversion will be terminated and SDATA will go back into three-state.

Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or idle low until sometime prior to the next conversion. Once a data transfer is complete, i.e., when SDATA has returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by again bringing $\overline{CS}$ low.

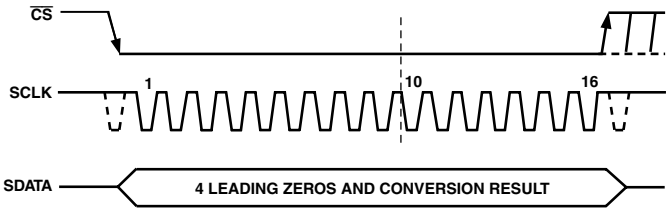


Figure 21. Normal Mode Operation

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion or a series of conversions may be performed at a high throughput rate, during which the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7450 is in the power-down mode, all analog circuitry is powered down. To enter power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK as shown in Figure 22.

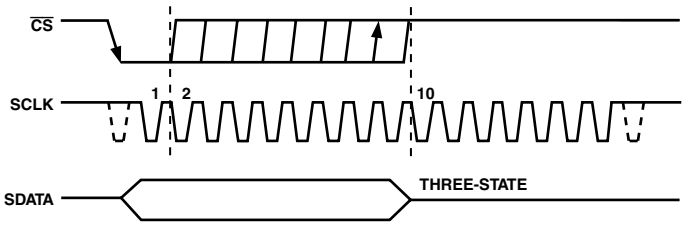


Figure 22. Entering Power-Down Mode

Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will enter power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ will be terminated, and SDATA will go back into three-state. The time from the rising edge of $\overline{CS}$ to SDATA three-state enabled will never be greater than t_8 (see Timing Specifications). If $\overline{CS}$ is brought high before the second SCLK falling edge, the part will remain in normal mode and will not power down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

To exit this mode of operation and power the AD7450 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device will begin to power up and continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up after 1 μs has elapsed and, as shown in Figure 23, valid data will result from the next conversion.

If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the AD7450 will again go back into power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will again power down on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

Power-Up Time

The power-up time of the AD7450 is typically 1 μs, which means that with any frequency of SCLK up to 18 MHz, one dummy cycle will always be sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. The quiet time, t_{QUIET}, must still be allowed from the point at which the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$.

When running at the maximum throughput rate of 1 MSPS, the AD7450 will power up and acquire a signal within ±0.5 LSB in one dummy cycle, i.e., 1 μs. When powering up from the power-down mode with a dummy cycle, as in Figure 23, the track-and-hold, which was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as Point A in Figure 23.

Although at any SCLK frequency one dummy cycle is sufficient to power the device up and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; 1 μs will be sufficient to power the device up and acquire the input signal.

For example, if a 5 MHz SCLK frequency was applied to the ADC, the cycle time would be 3.2 μs (i.e., 1/(5 MHz) × 16). In one dummy cycle, 3.2 μs, the part would be powered up and V_{IN} acquired fully. However, after 1 μs with a 5 MHz SCLK, only 5 SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case, the $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time, t_{QUIET}, to initiate the conversion.

When power supplies are first applied to the AD7450, the ADC may either power up in the power-down mode or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if the user wishes the part to power up in power-down mode, then the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as that shown in Figure 22.

Once supplies are applied to the AD7450, the power-up time is the same as that when powering up from the power-down mode. It takes approximately 1 μs to power up fully if the part powers up in normal mode. It is not necessary to wait 1 μs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed.

As mentioned earlier, when powering up from the power-down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track-and-hold will already be in track. This means if (assuming one has the facility to monitor the ADC supply current) the ADC powers up in the desired mode of operation, and thus a dummy cycle is not required to change the mode, then a dummy cycle is not required to place the track-and-hold into track.

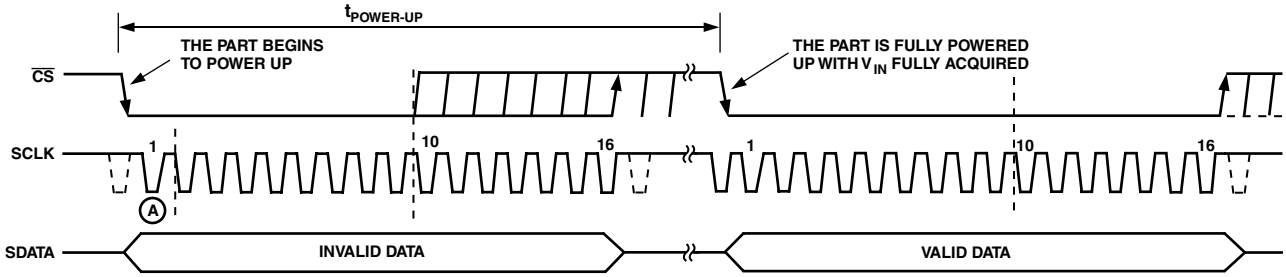


Figure 23. Exiting Power-Down Mode

POWER VERSUS THROUGHPUT RATE

By using the power-down mode on the AD7450 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 24 shows how, as the throughput rate is reduced, the device remains in its power-down state longer, and the average power consumption reduces accordingly. It shows this for both 5 V and 3 V power supplies.

For example, if the AD7450 is operated in continuous sampling mode with a throughput rate of 100 kSPS and an SCLK of 18 MHz, and the device is placed in the power-down mode between conversions, then the power consumption is calculated as follows:

Power dissipation during normal operation = 9 mW max for V_{DD} = 5 V.

If the power-up time is one dummy cycle, i.e., 1 µs, and the remaining conversion time is another cycle, i.e., 1 µs, then the AD7450 can be said to dissipate 9 mW for 2 µs* during each conversion cycle.

If the throughput rate = 100 kSPS, then the cycle time = 10 µs, and the average power dissipated during each cycle is:

$$(2/10) \times 9\ mW = 1.8\ mW$$

For the same scenario, if V_{DD} = 3 V, the power dissipation during normal operation is 3.75 mW max.

The AD7450 can now be said to dissipate 3.75 mW for 2 µs* during each conversion cycle.

The average power dissipated during each cycle with a throughput rate of 100 kSPS is therefore:

$$(2/10) \times 3.75\ mW = 0.75\ mW$$

This is how the power numbers in Figure 24 are calculated.

For throughput rates above 320 kSPS, it is recommended that the serial clock frequency is reduced for optimum power performance.

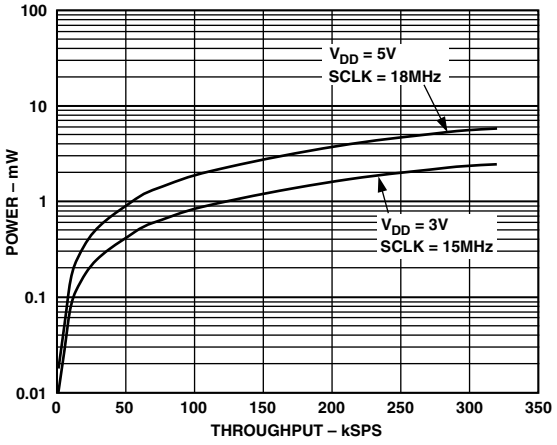


Figure 24. Power vs. Throughput Rate for Power-Down Mode

MICROPROCESSOR AND DSP INTERFACING

The serial interface on the AD7450 allows the part to be directly connected to a range of different microprocessors. This section explains how to interface the AD7450 with some of the more common microcontroller and DSP serial interface protocols.

*This figure assumes a very small time to enter power-down mode. This will increase as the burst of clocks used to enter the power-down mode is increased.

AD7450 to ADSP-21xx

The ADSP-21xx DSPs are interfaced directly to the AD7450 without any glue logic required.

The SPORT control register should be set up as follows:
TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data-Words
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0
ITFS = 1

To implement the power-down mode, SLEN should be set to 1001 to issue an 8-bit SCLK burst.

The connection diagram is shown in Figure 25. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

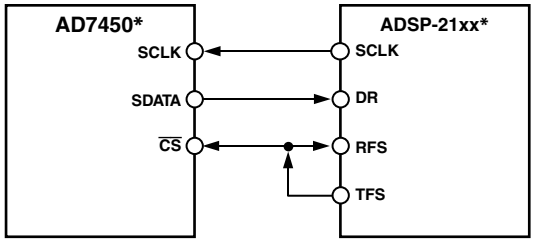


Figure 25. Interfacing to the ADSP-21xx

The timer registers are loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, (i.e., AX0 = TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low, and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted, or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, then a SCLK of 2 MHz is obtained and eight master clock periods will elapse for every 1 SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in nonequidistant sampling as the transmit instruction is occurring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, then equidistant sampling will be implemented by the DSP.

AD7450 to TMS320C5x/C54x

The serial interface on the TMS320C5x/C54x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices, such as the AD7450. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x/C54x and the AD7450 with no glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (Tx serial clock) and FSX (Tx frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The format bit, FO, may be set to 1 to set the word length to 8 bits in order to implement the power-down mode on the AD7450. The connection diagram is shown in Figure 26. For signal processing applications, it is imperative that the frame synchronization signal from the TMS320C5x/C54x provide equidistant sampling.

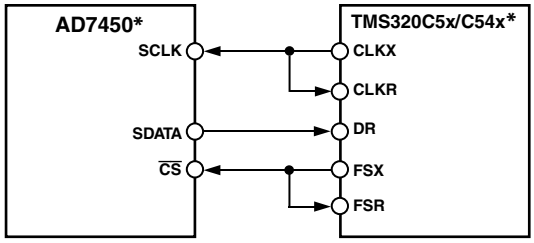


Figure 26. Interfacing to the TMS320C5x/C54x

AD7450 to MC68HC16

The serial peripheral interface (SPI) on the MC68HC16 is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 1, and clock phase bit (CPHA) = 0. The SPI is configured by writing to the SPI control register (SPCR)—see the 68HC16 user manual. The serial transfer will take place as a 16-bit operation when the SIZE bit in the SPCR register is set to SIZE = 1. To implement the power-down modes with an 8-bit transfer set SIZE = 0. A connection diagram is shown in Figure 27.

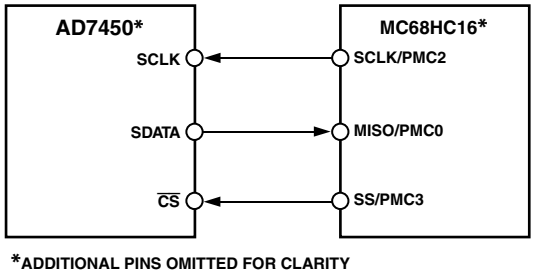


Figure 27. Interfacing to the MC68HC16

AD7450 to DSP56xxx

The connection diagram in Figure 28 shows how the AD7450 can be connected to the SSI (synchronous serial interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in synchronous mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both Tx and Rx (Bits FSL1 = 1 and FSL0 = 0 in CRB). Set the word length to 16 by setting Bits WL1 = 1 and WL0 = 0 in CRA. To implement the power-down mode on the AD7450, the word length can be changed to 8 bits by setting its WL1 = 0 and WL0 = 0 in CRA. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP56xxx will provide equidistant sampling.

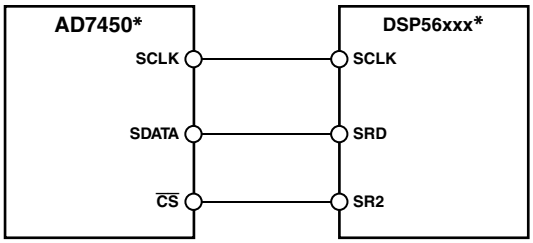


Figure 28. Interfacing to the DSP56xxx

APPLICATION HINTS

Grounding and Layout

The printed circuit board that houses the AD7450 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes since it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the GND pin on the AD7450 as possible. Avoid running digital lines under the device, as this will couple noise onto the die. The analog ground plane should be allowed to run under the AD7450 to avoid noise coupling. The power supply lines to the AD7450 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

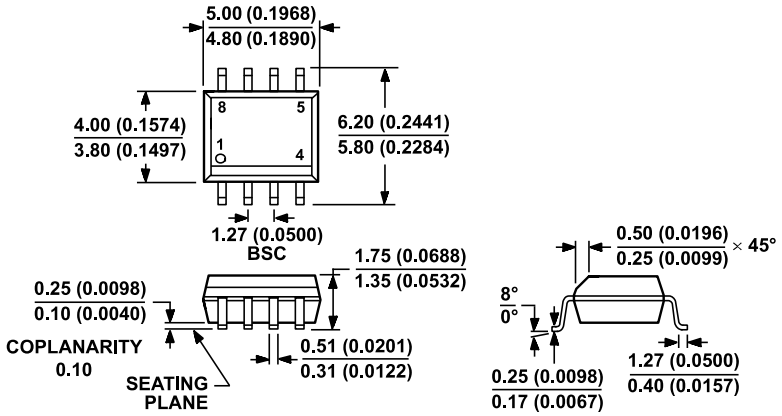
Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum capacitors in parallel with 0.1 μF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

EVALUATING THE AD7450 PERFORMANCE

The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Evaluation Board Controller. The Evaluation Board Controller can be used in conjunction with the AD7450 evaluation board, as well as many other Analog Devices evaluation boards ending with the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7450.

The software allows the user to perform ac (fast Fourier Transform) and dc (Histogram of codes) tests on the AD7450. See the evaluation board technical note for more information.

OUTLINE DIMENSIONS

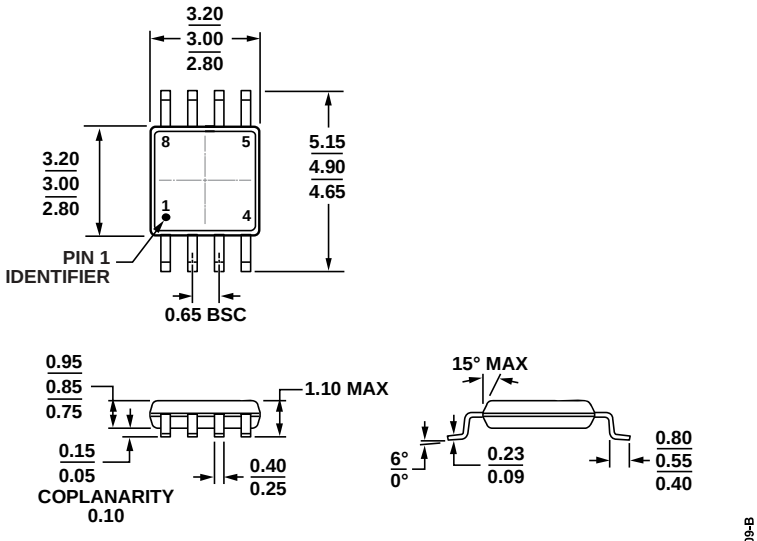


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 29. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

100709-B

Figure 30. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding Information
AD7450ARZ	40°C to +85°C	8-Lead Mini Small Outline Package [SOIC_N]	R-8	
AD7450ARZ-REEL	40°C to +85°C	8-Lead Mini Small Outline Package [SOIC_N]	R-8	
AD7450ARZ-REEL7	40°C to +85°C	8-Lead Mini Small Outline Package [SOIC_N]	R-8	
AD7450ARMZ	40°C to +85°C	8-Lead Standard Small Outline Package [MSOP]	RM-8	C3S
AD7450ARMZ-REEL7	40°C to +85°C	8-Lead Standard Small Outline Package [MSOP]	RM-8	C3S
AD7450BRZ	40°C to +85°C	8-Lead Mini Small Outline Package [SOIC_N]	R-8	
AD7450BRMZ	40°C to +85°C	8-Lead Standard Small Outline Package [MSOP]	RM-8	C3R

[1] Z = RoHS Compliant Part.

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REVISION HISTORY

9/10—Rev 0 to Rev. A