4 ADC with PLL, 192 kHz, 24-Bit ADC

AD1974

FEATURES

Phase-locked loop generated or direct master clock
Low EMI design
107 dB dynamic range and SNR
−94 dB THD + N
Single 3.3 V supply
Tolerance for 5 V logic inputs
Supports 24 bits and 8 kHz to 192 kHz sample rates
Differential ADC input
SPI®-controllable for flexibility
Software-controllable clickless mute
Software power-down
Right justified, left justified, I²S, and TDM modes
Master and slave modes up to 16-channel input/output
Available in a 48-lead LQFP

APPLICATIONS

Automotive audio systems
Home Theater Systems
Set-top boxes
Digital audio effects processors

GENERAL DESCRIPTION

The AD1974 is a high performance, single-chip ADC that provides four analog-to-digital converters (ADCs) with differential inputs using the Analog Devices, Inc. patented multibit sigma-delta (Σ-Δ) architecture. An SPI port is included, allowing a microcontroller to enable mutes and adjust many other parameters. The AD1974 operates from 3.3 V digital and analog supplies. The AD1974 is available in a single-ended output 48-lead LQFP.

The AD1974 is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board phase-locked loop (PLL) to derive the master clock from the LR clock or from an external crystal, the AD1974 eliminates the need for a separate high frequency master clock and can also be used with a suppressed bit clock. The ADCs are designed using the latest continuous time architectures from Analog Devices to further minimize EMI. By using 3.3 V supplies, power consumption is minimized, further reducing emissions.

FUNCTIONAL BLOCK DIAGRAM

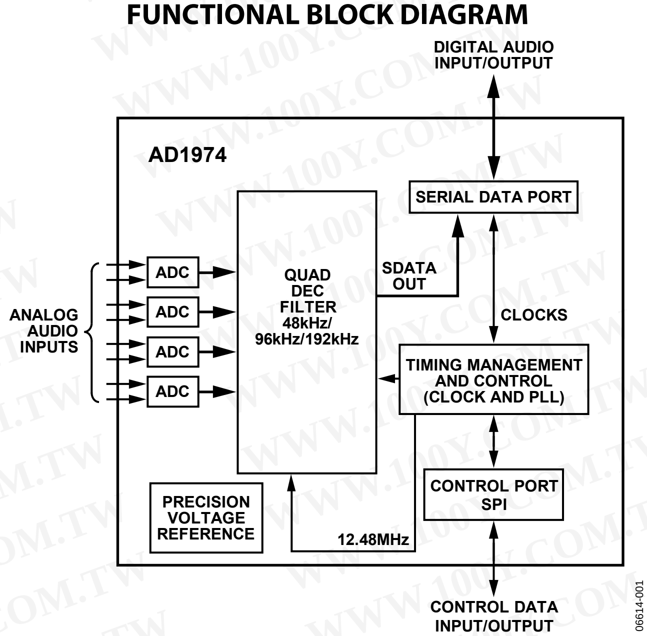

Figure 1.

Rev. B

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REVISION HISTORY

6/10—Rev. A to Rev. B

Changed 130°C to 125°C Throughout ... 4
Changed T_A to T_C Throughout ... 4
Changes to Endnote 2 in Ordering Guide ... 24

11/09—Rev. 0 to Rev. A

Changed Codec to ADC ... Throughout
Changes to Features and General Description Sections ... 1
Changes to Clock Signals Section ... 11
Changes to Figure 12 and Figure 13 ... 16
Changes to Control Registers Section ... 18

4/07—Revision 0: Initial Version

SPECIFICATIONS

TEST CONDITIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications.

Supply Voltages (AVDD, DVDD)	3.3 V
Temperature Range[1]	As specified in Table 1 and Table 2
Master Clock	12.288 MHz (48 kHz f_S, 256 × f_S mode)
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 bits
Load Capacitance (Digital Output)	20 pF
Load Current (Digital Output)	±1 mA or 1.5 kΩ to ½ DVDD supply
Input Voltage High	2.0 V
Input Voltage Low	0.8 V

[1] Functionally guaranteed at −40°C to +125°C case temperature.

ANALOG PERFORMANCE SPECIFICATIONS

Specifications guaranteed at 25°C (ambient).

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS					
ADC Resolution	All ADCs		24		Bits
Full-Scale Input Voltage (Differential)			1.9		V rms
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
No Filter (RMS)		98	102		dB
With A-Weighted Filter (RMS)		100	105		dB
Total Harmonic Distortion + Noise (THD + N)	−1 dBFS		−96	−87	dB
Gain Error		−10		+10	%
Interchannel Gain Mismatch		−0.25		+0.25	dB
Offset Error		−10	0	+10	mV
Gain Drift			100		ppm/°C
Interchannel Isolation			−110		dB
CMRR	100 mV rms, 1 kHz		55		dB
	100 mV rms, 20 kHz		55		dB
Input Resistance			14		kΩ
Input Capacitance			10		pF
Input Common-Mode Bias Voltage			1.5		V
REFERENCE					
Internal Reference Voltage	FILTR pin		1.50		V
External Reference Voltage	FILTR pin	1.32	1.50	1.68	V
Common-Mode Reference Output	CM pin		1.50		V

Specifications measured at 125°C (case).

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS					
ADC Resolution	All ADCs		24		Bits
Full-Scale Input Voltage (Differential)			1.9		V rms
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
No Filter (RMS)		95	102		dB
With A-Weighted Filter (RMS)		97	105		dB
Total Harmonic Distortion + Noise (THD + N)	−1 dBFS		−96	−87	dB
Gain Error		−10		+10	%
Interchannel Gain Mismatch		−0.25		+0.25	dB
Offset Error		−10	0	+10	mV
REFERENCE					
Internal Reference Voltage	FILTR pin		1.50		V
External Reference Voltage	FILTR pin	1.32	1.50	1.68	V
Common-Mode Reference Output	CM pin		1.50		V

CRYSTAL OSCILLATOR SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit
Transconductance		3.5		Mmhos

DIGITAL INPUT/OUTPUT SPECIFICATIONS

−40°C < T_C < +125°C, DVDD = 3.3 V ± 10%.

Table 4.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
Input Voltage High (V_{IH})		2.0			V
Input Voltage High (V_{IH})	MCLKI pin	2.2			V
Input Voltage Low (V_{IL})				0.8	V
Input Leakage	I_{IH} @ V_{IH} = 2.4 V			10	µA
	I_{IL} @ V_{IL} = 0.8 V			10	µA
High Level Output Voltage (V_{OH})	I_{OH} = 1 mA	DVDD − 0.60			V
Low Level Output Voltage (V_{OL})	I_{OL} = 1 mA			0.4	V
Input Capacitance				5	pF

POWER SUPPLY SPECIFICATIONS

Table 5.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
SUPPLIES					
Voltage					
	DVDD	3.0	3.3	3.6	V
	AVDD	3.0	3.3	3.6	V
Digital Current	MCLK = 256 f_S				
Normal Operation	f_S = 48 kHz		56		mA
	f_S = 96 kHz		65		mA
	f_S = 192 kHz		95		mA
Power-Down	f_S = 48 kHz to 192 kHz		2.0		mA
Analog Current					
Normal Operation			74		mA
Power-Down			23		mA
DISSIPATION					
Operation	MCLK = 256 f_S, 48 kHz				
All Supplies			429		mW
Digital Supply			185		mW
Analog Supply			244		mW
Power-Down, All Supplies			83		mW
POWER SUPPLY REJECTION RATIO					
Signal at Analog Supply Pins	1 kHz, 200 mV p-p		50		dB
	20 kHz, 200 mV p-p		50		dB

DIGITAL FILTERS

Table 6.

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes @ 48 kHz					
Pass Band		0.4375 f_S		21		kHz
Pass-Band Ripple				±0.015		dB
Transition Band		0.5 f_S		24		kHz
Stop Band		0.5625 f_S		27		kHz
Stop-Band Attenuation			79			dB
Group Delay		22.9844 f_S		479		μs

TIMING SPECIFICATIONS

−40°C < T_C < +125°C, DVDD = 3.3 V ± 10%.

Table 7.

Parameter	Condition	Comments	Min	Max	Unit
INPUT MASTER CLOCK (MCLK) AND RESET					
t_{MH}	MCLK duty cycle	ADC clock source = PLL clock @ 256 f_S, 384 f_S, 512 f_S, 768 f_S	40	60	%
t_{MH}		ADC clock source = direct MCLK @ 512 f_S (bypass on-chip PLL)	40	60	%
f_{MCLK}	MCLK frequency	PLL mode, 256 f_S reference	6.9	13.8	MHz
f_{MCLK}		Direct 512 f_S mode		27.6	MHz
t_{PDR}	Low		15		ns
t_{PDRR}	Recovery	Reset to active output	4096		t_{MCLK}

Parameter	Condition	Comments	Min	Max	Unit
PLL					
Lock Time	MCLK and LRCLK input			10	ms
256 f_S VCO Clock Output Duty Cycle MCLK_O Pin			40	60	%
SPI PORT		See Figure 5			
t_{CCH}	CCLK high		35		ns
t_{CCL}	CCLK low		35		ns
f_{CCLK}	CCLK frequency	$f_{CCLK} = 1/t_{CCP}$; only t_{CCP} shown in Figure 5		10	MHz
t_{CDS}	CDATA setup	To CCLK rising	10		ns
t_{CDH}	CDATA hold	From CCLK rising	10		ns
t_{CLS}	Setup	To CCLK rising	10		ns
t_{CLH}	Hold	From CCLK falling	10		ns
t_{CLHIGH}	High	Not shown in Figure 5	10		ns
t_{COE}	COUT enable	From CCLK falling		30	ns
t_{COD}	COUT delay	From CCLK falling		30	ns
t_{COH}	COUT hold	From CCLK falling, not shown in Figure 5	30		ns
t_{COTS}	COUT tristate	From CCLK falling		30	ns
ADC SERIAL PORT		See Figure 13			
t_{ABH}	ABCLK high	Slave mode	10		ns
t_{ABL}	ABCLK low	Slave mode	10		ns
t_{ALS}	ALRCLK setup	To ABCLK rising, slave mode	10		ns
t_{ALH}	ALRCLK hold	From ABCLK rising, slave mode	5		ns
t_{ALS}	ALRCLK skew	From ABCLK falling, master mode	−8	+8	ns
t_{ABDD}	ASDATA delay	From ABCLK falling		18	ns
AUXILIARY INTERFACE		See Figure 12			
t_{XDS}	AAUXDATA setup	To AUXBCLK rising	10		ns
t_{XDH}	AAUXDATA hold	From AUXBCLK rising	5		ns
t_{XBH}	AUXBCLK high		10		ns
t_{XBL}	AUXBCLK low		10		ns
t_{XLS}	AUXLRCLK setup	To AUXBCLK rising	10		ns
t_{XLH}	AUXLRCLK hold	From AUXBCLK rising	5		ns

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Analog (AVDD)	−0.3 V to +3.6 V
Digital (DVDD)	−0.3 V to +3.6 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 V to DVDD + 0.3 V
Operating Temperature Range (Case)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

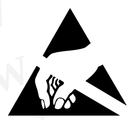
THERMAL RESISTANCE

θ_{JA} represents thermal resistance, junction-to-ambient; θ_{JC} represents the thermal resistance, junction-to-case. All characteristics are for a 4-layer board.

Table 9.

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LQFP	50.1	17	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

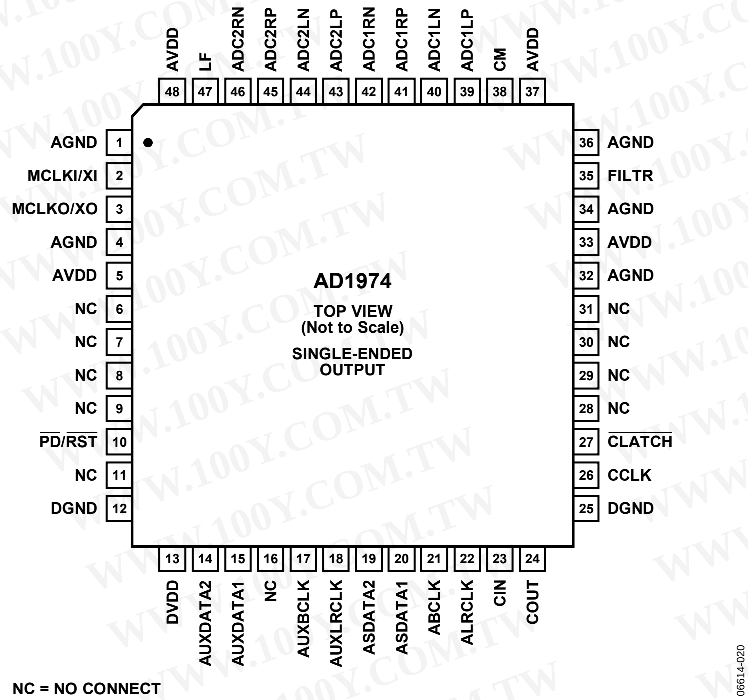


Figure 2. AD1974 Single-Ended Output, 48-Lead LQFP Pin Configuration

Table 10. Pin Function Description

Pin No.	Type[1]	Mnemonic	Description
1, 4, 32, 34, 36	I	AGND	Analog Ground.
2	I	MCLKI/XI	Master Clock Input/Crystal Oscillator Input.
3	O	MCLKO/XO	Master Clock Output/Crystal Oscillator Output.
5, 33, 37, 48	I	AVDD	Analog Power Supply. Connect to analog 3.3 V supply.
6 to 9, 11, 16, 28 to 31		NC	No Connect.
10	I	PD/RST	Power-Down/Reset (Active Low).
12, 25	I	DGND	Digital Ground.
13	I	DVDD	Digital Power Supply. Connect to digital 3.3 V supply.
14	I/O	AUXDATA2	Auxiliary Data Input 2 (From External ADC 2).
15	I/O	AUXDATA1	Auxiliary Data Input 1 (From External ADC 1).
17	I/O	AUXBCLK	Auxiliary Bit Clock.
18	I/O	AUXLRCLK	Auxiliary Left-Right Framing Clock.
19	I/O	ASDATA2	ADC Serial Data Output 2 (ADC 2 Left and ADC 2 Right)/ADC TDM Data Input.
20	O	ASDATA1	ADC Serial Data Output 1 (ADC 1 Left and ADC 1 Right)/ADC TDM Data Output.
21	I/O	ABCLK	Serial Bit Clock for ADCs.
22	I/O	ALRCLK	Left-Right Framing Clock for ADCs.
23	I	CIN	Control Data Input (SPI).
24	I/O	COUT	Control Data Output (SPI).
26	I	CCLK	Control Clock Input (SPI).
27	I	CLATCH	Latch Input for Control Data (SPI).
35	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass with 10 μF‖100 nF to AGND.
38	O	CM	Common-Mode Reference Filter Capacitor Connection. Bypass with 47 μF‖100 nF to AGND.
39	I	ADC1LP	ADC1 Left Positive Input.
40	I	ADC1LN	ADC1 Left Negative Input.
41	I	ADC1RP	ADC1 Right Positive Input.
42	I	ADC1RN	ADC1 Right Negative Input.
43	I	ADC2LP	ADC2 Left Positive Input.

Pin No.	Type[1]	Mnemonic	Description
44	I	ADC2LN	ADC2 Left Negative Input.
45	I	ADC2RP	ADC2 Right Positive Input.
46	I	ADC2RN	ADC2 Right Negative Input.
47	O	LF	PLL Loop Filter, Return to AVDD.

[1] I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

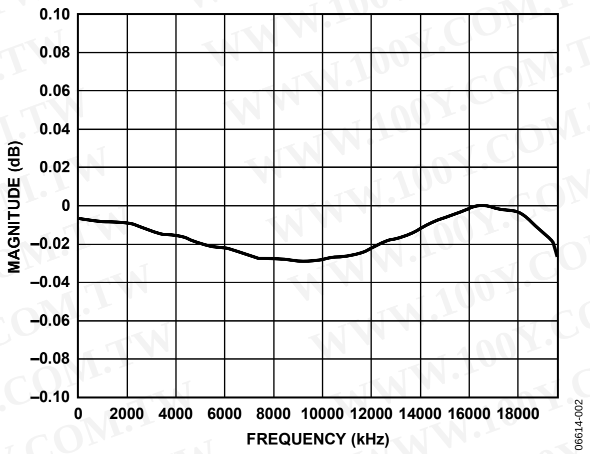


Figure 3. ADC Pass-Band Filter Response, 48 kHz

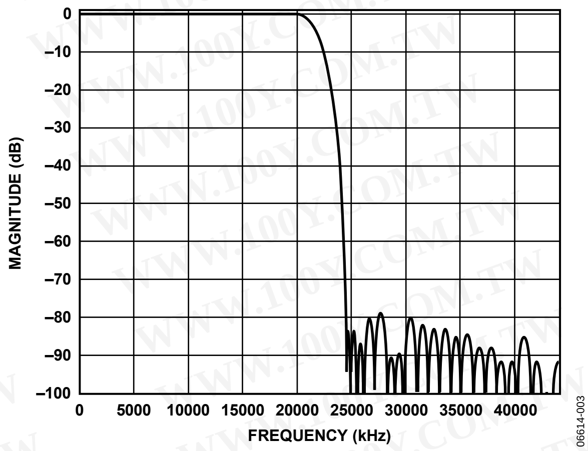


Figure 4. ADC Stop-Band Filter Response, 48 kHz

THEORY OF OPERATION

ANALOG-TO-DIGITAL CONVERTERS (ADCS)

There are four ADC channels in the AD1974 configured as two stereo pairs with differential inputs. The ADCs can operate at a nominal sample rate of 48 kHz, 96 kHz, or 192 kHz. The ADCs include on-board digital antialiasing filters with a 79 dB stop-band attenuation and a linear phase response, operating at an oversampling ratio of 128 (48 kHz, 96 kHz, and 192 kHz modes). Digital outputs are supplied through two serial data output pins (one for each stereo pair) as well as a common frame (ALRCLK) and bit clock (ABCLK). Alternatively, one of the time division multiplexed (TDM) modes can be used to access up to 16 channels on a single TDM data line.

The ADCs must be driven from a differential signal source for best performance. The input pins of the ADCs connect to internal switched capacitors. To isolate the external driving op amp from the glitches caused by the internal switched capacitors, each input pin should be isolated by using a series connected, external, 100 Ω resistor together with a 1 nF capacitor connected from each input to ground. This capacitor must be of high quality, for instance, a ceramic NPO capacitor or a polypropylene film capacitor.

The differential inputs have a nominal common-mode voltage of 1.5 V. The voltage at the common-mode reference pin (CM) can be used to bias external op amps to buffer the input signals (see the Power Supply and Voltage Reference section). The inputs can also be ac-coupled and do not need an external dc bias to CM.

A digital high-pass filter can be switched in line with the ADCs under serial control to remove residual dc offsets. It has a 1.4 Hz, 6 dB per octave cutoff at a 48 kHz sample rate. The cutoff frequency scales directly with sample frequency.

The voltage at CM can be used to bias the external op amps that buffer the output signals (see the Power Supply and Voltage Reference section).

CLOCK SIGNALS

The on-chip PLL can be selected to reference the input sample rate from either the LRCLK or AUXLRCK pins or 256, 384, 512, or 768 times the sample rate, referenced to the 48 kHz mode from the MCLKI/XI pin. The default at power-up is $256 \times f_S$ from MCLKI. In 96 kHz mode, the master clock frequency stays at the same absolute frequency; therefore, the actual multiplication rate is divided by 2. In 192 kHz mode, the actual multiplication rate is divided by 4. For example, if the AD1974 is programmed in $256 \times f_S$ mode, the frequency of the master clock input is 256×48 kHz = 12.288 MHz. If the AD1974 is then switched to 96 kHz operation (by writing to the SPI port), the frequency of the master clock should remain at 12.288 MHz ($128 \times f_S$). In 192 kHz mode, this becomes $64 \times f_S$.

The internal clock for the ADCs is $256 \times f_S$ for all clock modes. By default, the on-board PLL generates this internal master clock from an external clock. A direct $512 \times f_S$ (referenced to 48 kHz mode) master clock can be used for the ADCs if selected in the PLL and Clock Control 1 register.

Note that it is not possible to use a direct clock for the ADCs set to the 192 kHz mode. It is required that the on-chip PLL be used in this mode.

The PLL can be powered down in the PLL and Clock Control 0 register. To ensure reliable locking when changing PLL modes, or if the reference clock is unstable at power-on, power down the PLL and then power it back up when the reference clock has stabilized.

The internal MCLK can be disabled in the PLL and Clock Control 0 register to reduce power dissipation when the AD1974 is idle. The clock should be stable before it is enabled. Unless a standalone mode is selected (see the Serial Control Port section), the clock is disabled by reset and must be enabled by writing to the SPI port for normal operation.

To maintain the highest performance possible, it is recommended that the clock jitter of the internal master clock signal be limited to less than 300 ps rms time interval error (TIE). Even at these levels, extra noise or tones can appear in the outputs if the jitter spectrum contains large spectral peaks. If the internal PLL is not being used, it is highly recommended that an independent crystal oscillator generate the master clock. In addition, it is especially important that the clock signal should not be passed through an FPGA, CPLD, DSP, or other large digital chip before being applied to the AD1974. In most cases, this induces clock jitter due to the sharing of common power and ground connections with other unrelated digital output signals. When the PLL is used, jitter in the reference clock is attenuated above a certain frequency depending on the loop filter.

RESET AND POWER-DOWN

The reset pin sets all the control registers to their default settings. To avoid pops, reset does not power down the analog outputs. After reset is deasserted, and the PLL acquires a lock condition, an initialization routine runs inside the AD1974. This initialization lasts for approximately 256 master clock cycles.

The PLL and Clock Control 0 register and the ADC Control 1 register power down their respective sections using power down bits. All other register settings are retained. The $\overline{\text{PD}}$/RST pin should be pulled low by an external resistor to guarantee proper startup.

Table 11. Standalone Mode Selection

ADC Clocks	CIN	COUT	CCLK	$\overline{\text{CLATCH}}$
Slave	0	0	0	0
Master	0	1	0	0

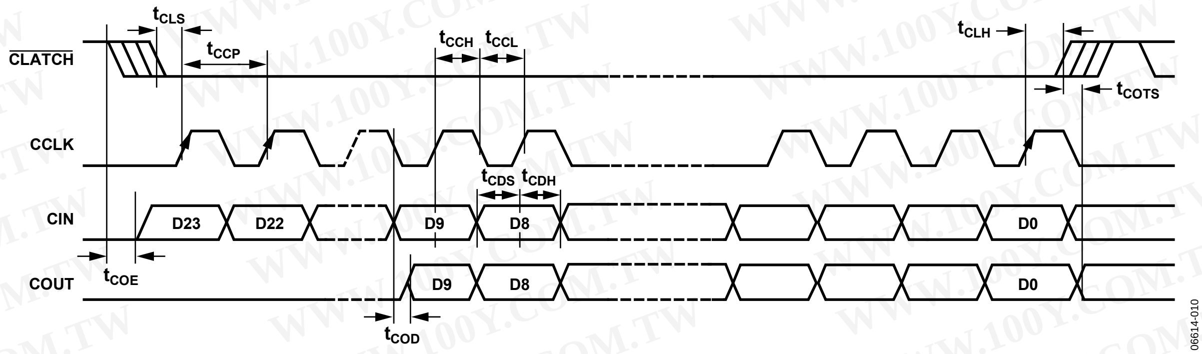


Figure 5. Format of the SPI Signal

SERIAL CONTROL PORT

The AD1974 has an SPI control port that permits the programming and reading back of the internal control registers for the ADCs and the clock system. There is also a standalone mode available for operation without serial control that is configured at reset using the serial control pins. All registers are set to default, except the internal MCLK enable, which is set to 1; ADC BCLK and LRCLK master/slave, which are set by COUT. Standalone mode only supports stereo mode with an I²S data format and 256 f_S MCLK rate (see Table 11 for details). Using a weak pull-up resistor in applications that have a microcontroller is highly recommended. This pull-up resistor ensures that the AD1974 recognizes the presence of a microcontroller.

The SPI control port of the AD1974 is a 4-wire serial control port. The format is similar to that of the Motorola SPI® format except that the input data-word is 24 bits wide. The serial bit clock and latch can be completely asynchronous to the sample rate of the ADCs. Figure 5 shows the format of the SPI signal. The first byte is a global address with a read/write bit. For the AD1974, the address is 0x04, shifted left one bit due to the R/$\overline{\text{W}}$ bit. The second byte is the AD1974 register address and the third byte is the data.

POWER SUPPLY AND VOLTAGE REFERENCE

The AD1974 is designed for 3.3 V supplies. Separate power supply pins (Pin 5, Pin 13, Pin 33, Pin 37, and Pin 38) are provided for the analog and digital sections. These pins should be bypassed with 100 nF ceramic chip capacitors, as close to the pins as possible, to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 22 μF should also be placed on the same PC board as the ADC. For critical applications, improved performance is obtained with separate supplies for the analog and digital sections. If this is not possible, it is recommended that the analog and digital supplies be isolated by means of a ferrite bead in series with each supply. It is important that the analog supply be as clean as possible.

All digital inputs are compatible with TTL and CMOS levels. All outputs are driven from the 3.3 V DVDD supply and are compatible with TTL and 3.3 V CMOS levels.

The ADC internal voltage reference (VREF) is brought out on FILTR and should be bypassed as close as possible to the AD1974 with a parallel combination of 10 μF and 100 nF. Any external current drawn should be limited to less than 50 μA.

VREF can be disabled in the PLL and Clock Control 1 register and FILTR can be driven from an external source. The ADC input gain varies by the inverse ratio.

CM is the internal common-mode reference. It should be bypassed as close as possible to the AD1974, with a parallel combination of 47 μF and 100 nF. This voltage can be used to bias external op amps to the common-mode voltage of the input and output signal pins. The output current should be limited to less than 0.5 mA source and 2 mA sink.

SERIAL DATA PORTS—DATA FORMAT

The four ADC channels use a common serial bit clock (ABCLK) and a left-right framing clock (ALRCLK) in the serial data port. The clock signals are all synchronous with the sample rate. The normal stereo serial modes are shown in Figure 11.

The ADC serial data modes default to I²S. The ports can also be programmed for left justified, right justified, and TDM modes. The word width is 24 bits by default and can be programmed for 16 or 20 bits. The ADC serial formats and serial clock polarity are programmable according to the ADC Control 1 register. The ADC serial ports are programmable to become the bus masters according to the ADC Control 2 register. By default, both ADC serial ports are in the slave mode.

TDM MODES

The AD1974 serial ports also have several different TDM serial data modes. The first and most commonly used configuration is shown in Figure 6 where the ADC serial port outputs one data stream consisting of four on-chip ADCs followed by four unused slots. In this mode, ABCLK is set to 256 f_S (8-channel TDM mode).

The I/O pins of the serial ports are defined according to the serial mode selected. For a detailed description of the function of each pin in TDM and AUX Modes, see Table 12.

The AD1974 allows system configurations with more than four ADC channels (see Figure 7 and Figure 8) that use 8 ADCs and 16 ADCs. In this mode, four AUX channel slots in the TDM output stream follow four on-chip ADC channel slots. It should be noted that due to the high ABCLK frequency, this mode is available only in the 48 kHz/44.1 kHz/32 kHz sample rate.

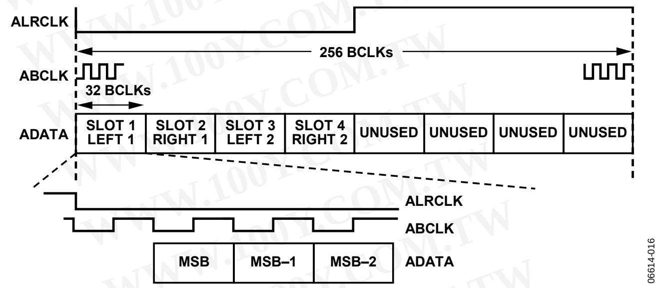


Figure 6. ADC TDM (8-Channel I²S Mode)

Table 12. Pin Function Changes in TDM and AUX Modes

Pin Name	Stereo Mode	TDM Mode	AUX Mode
ASDATA1	ADC1 data output	ADC TDM data output	ADCTDM data output
ASDATA2	ADC2 data output	ADC TDM data input	Not used (float)
AUXDATA1	Not used (ground)	Not used (ground)	AUXDATA in 1 (from external ADC1)
AUXDATA2	Not used (ground)	Not used (ground)	AUXDATA in 2 (from external ADC2)
ALRCLK	ADC LRCLK input/output	ADC TDM frame sync input/output	ADCTDM frame sync input/output
ABCLK	ADC BCLK input/output	ADC TDM BCLK input/output	ADCTDM BCLK input/output
AUXLRCLK	Not used (ground)	Not used (ground)	AUXLRCLK input/output
AUXBCLK	Not used (ground)	Not used (ground)	AUXBCLK input/output

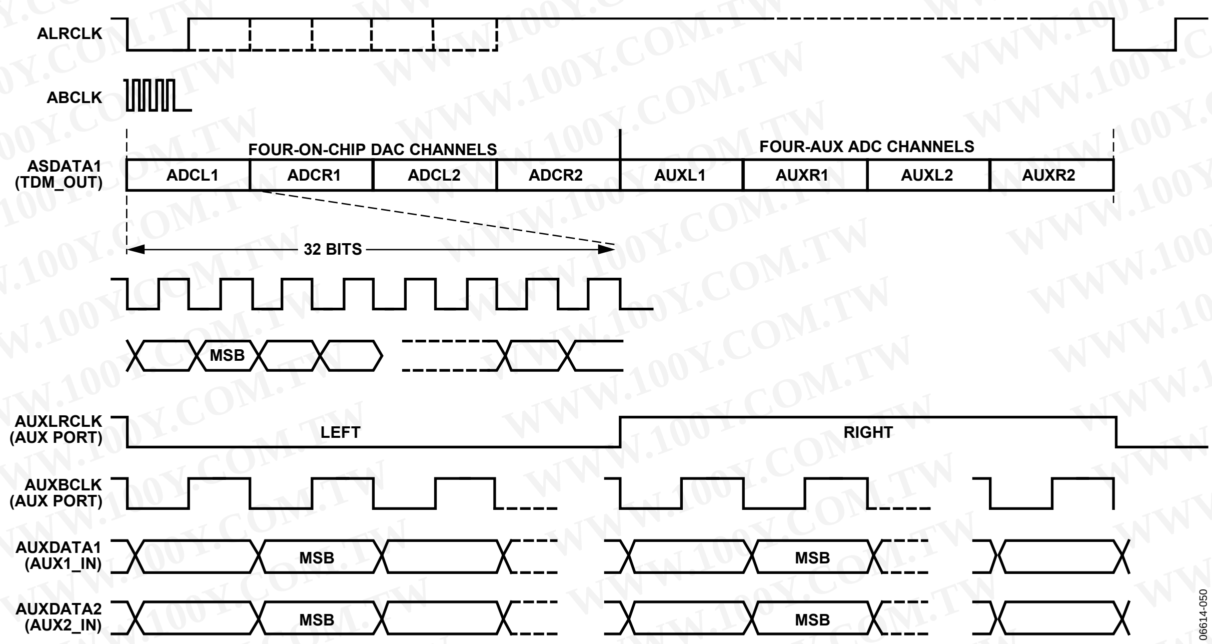


Figure 7. 8-Channel AUX ADC Mode

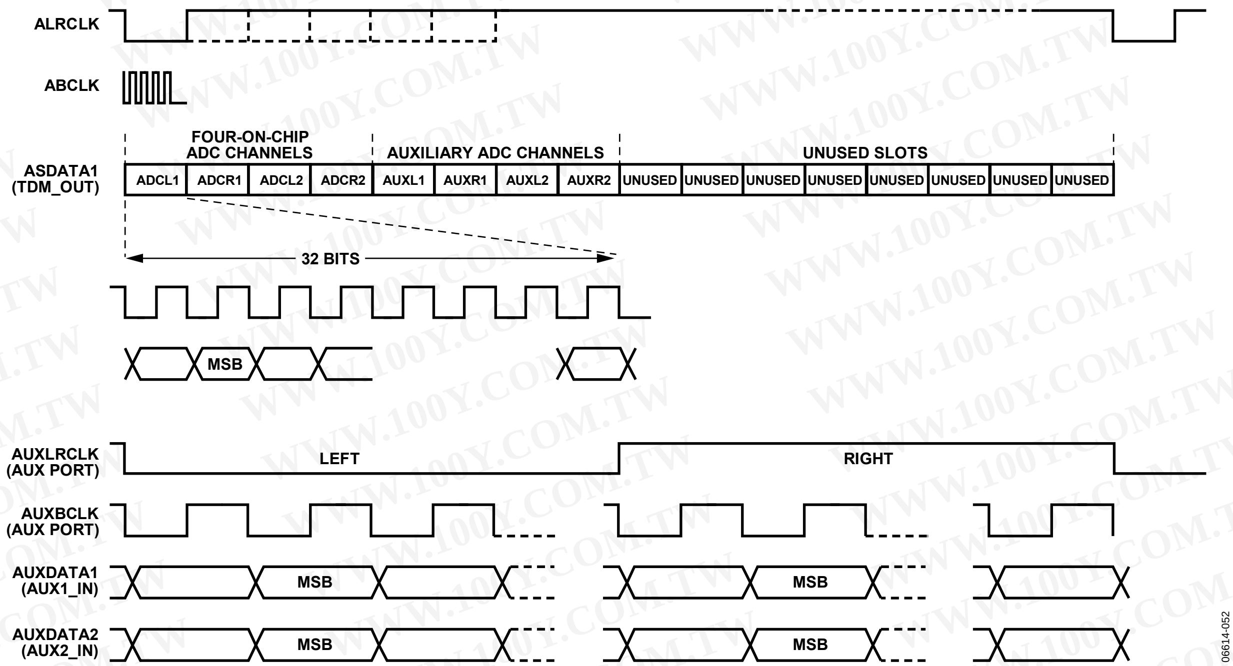


Figure 8. 16-Channel AUX ADC Mode

DAISY-CHAIN MODE

The AD1974 also allows a daisy-chain configuration to expand the system to 8 ADCs and 16 ADCs (see Figure 9 and Figure 10). There are two configurations for the ADC port to work in daisy-chain mode. The first one is with an ABCLK at 256 f_S shown in Figure 9. The second configuration is with an ABCLK at 512 f_S shown in Figure 10. Note that in the 512 f_S ABCLK mode, the ADC channels occupy the first eight slots, the second eight slots are empty. The TDM_IN of the first AD1974 must be grounded in all modes of operation. The second AD1974 is the device attached to the DSP TDM port.

The I/O pins of the serial ports are defined according to the serial mode selected. See Table 13 for a detailed description of the function of each pin. See Figure 14 for a typical AD1974 configuration with two external stereo ADCs.

Figure 11 through Figure 13 show the serial mode formats. For maximum flexibility, the polarity of LRCLK and BCLK are programmable. All of the clocks are shown with their normal polarity. The default mode is I^2S.

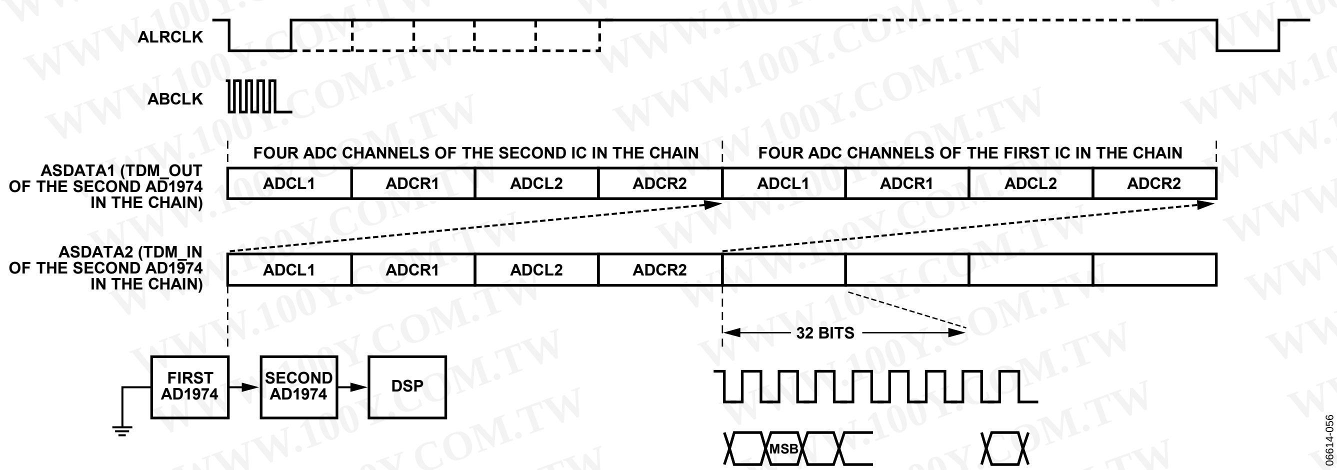


Figure 9. ADC TDM Daisy-Chain Mode (256 f_S ABCLK, Two AD1974 Daisy Chains)

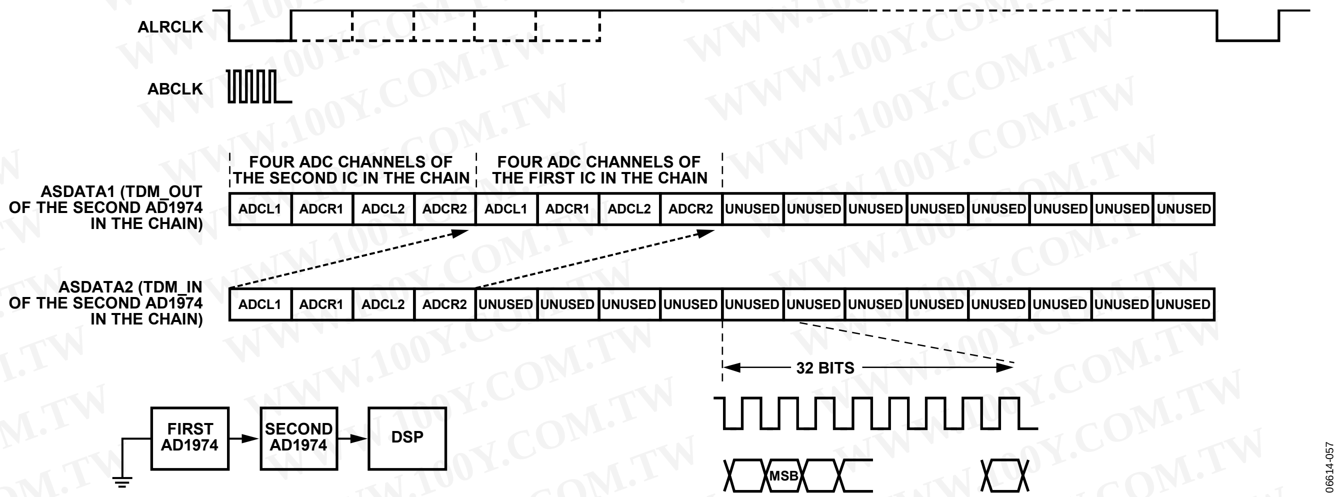


Figure 10. ADC TDM Daisy-Chain Mode (512 f_S ABCLK, Two AD1974 Daisy Chains)

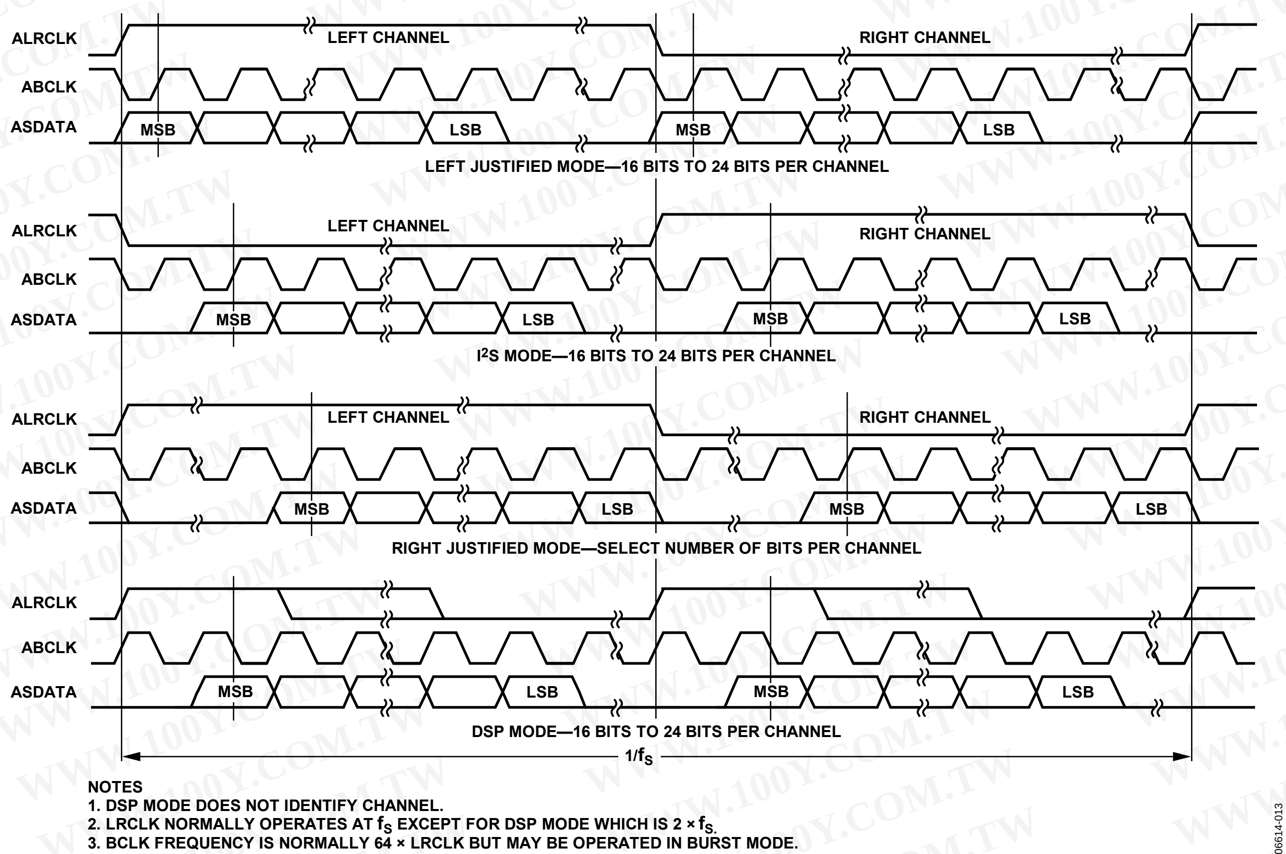


Figure 11. Stereo Serial Modes

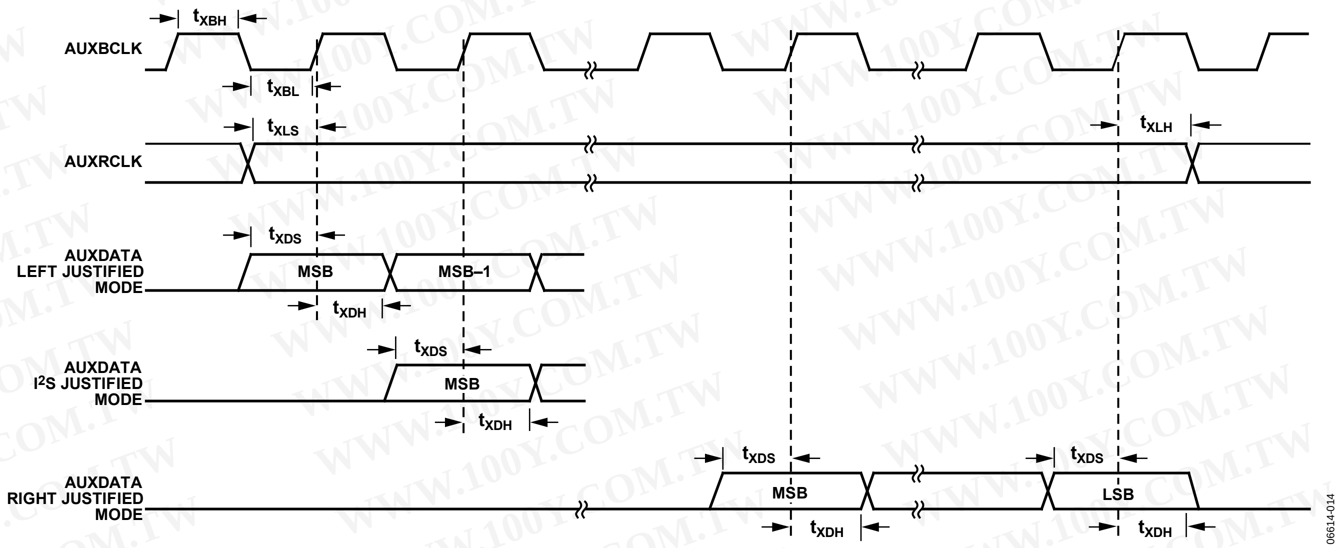


Figure 12. Auxiliary Serial Timing

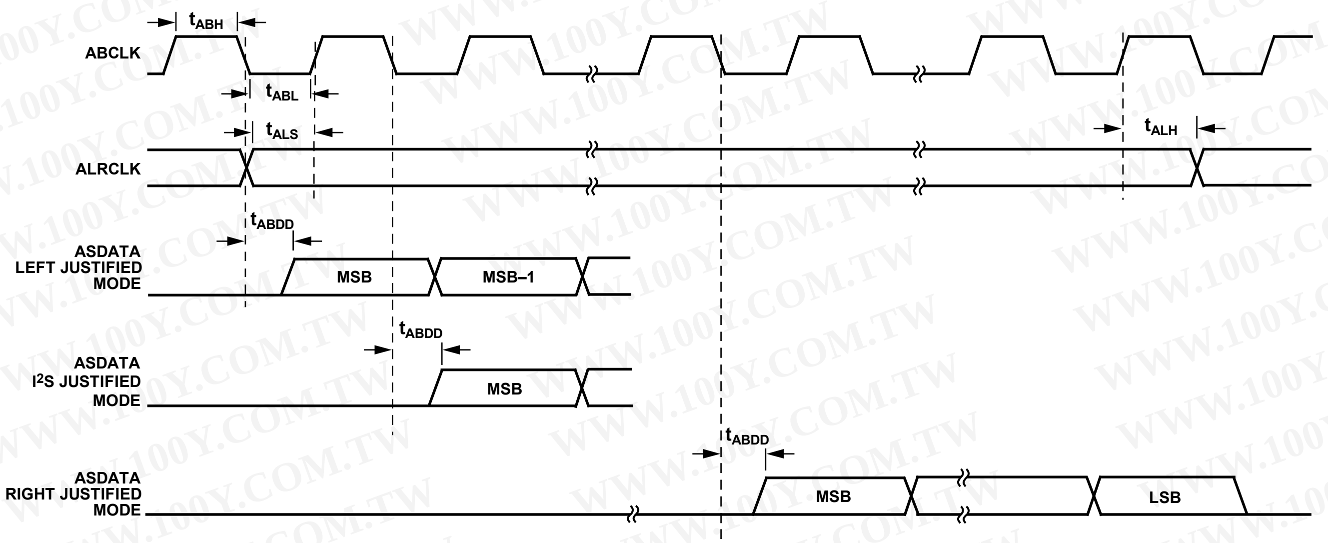


Figure 13. ADC Serial Timing

Table 13. Pin Function Changes in TDM and AUX Modes (Replication of Table 12)

Pin Name	Stereo Mode	TDM Mode	AUX Mode
ASDATA1	ADC1 data output	ADC TDM data output	ADCTDM data output
ASDATA2	ADC2 data output	ADC TDM data input	Not used (float)
AUXDATA1	Not used (ground)	Not used (ground)	AUXDATA in 1 (from external ADC1)
AUXDATA2	Not used (ground)	Not used (ground)	AUXDATA in 2 (from external ADC2)
ALRCLK	ADC LRCLK input/output	ADC TDM Frame Sync input/output	ADCTDM frame sync input/output
ABCLK	ADC BCLK input/output	ADC TDM BCLK input/output	ADCTDM BCLK input/output
AUXLRCLK	Not used (ground)	Not used (ground)	AUXLRCLK input/output
AUXBCLK	Not used (ground)	Not used (ground)	AUXBCLK input/output

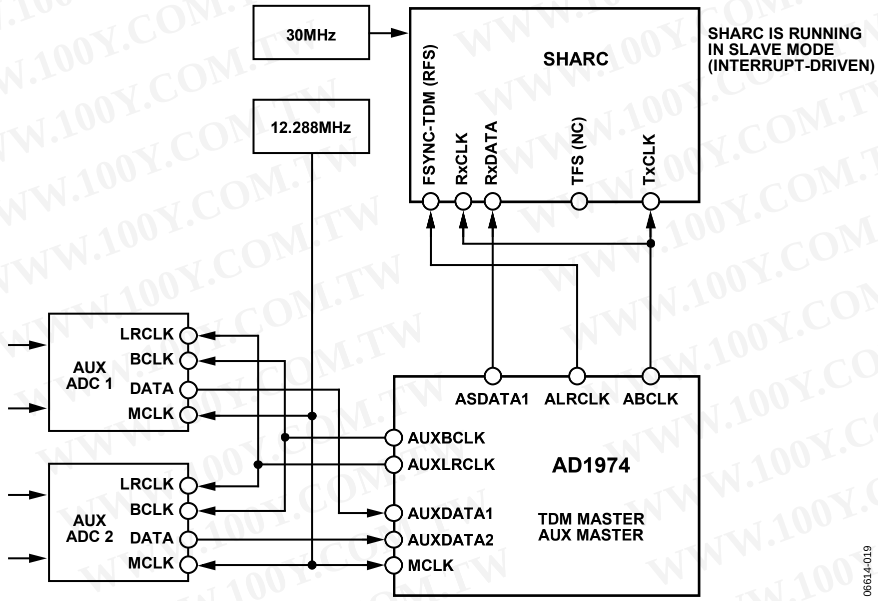


Figure 14. Example of AUX Mode Connection to SHARC® (AD1974 as TDM Master/AUX Master Shown)

CONTROL REGISTERS

The global address for the AD1974 is 0x04, shifted left one bit due to the R/$\overline{W}$ bit. All registers are reset to 0.

Note that the first setting in each control register parameter is the default setting.

Table 14. Register Format

	Global Address	R/$\overline{W}$	Register Address	Data
Bit	23:17	16	15:8	7:0

Table 15. Register Addresses Description

Address	Function
0	PLL and Clock Control 0
1	PLL and Clock Control 1
2	AUXPORT Control 0
3	AUXPORT Control 1
4	AUXPORT Control 2
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	ADC Control 0
15	ADC Control 1
16	ADC Control 2

PLL AND CLOCK CONTROL REGISTERS

Table 16. PLL and Clock Control 0

Bit	Value	Function	Description
0	0	Normal operation	PLL power-down
	1	Power-down	
2:1	00	INPUT 256 (×44.1 kHz or 48 kHz)	MCLKI/XI pin functionality (PLL active), master clock rate setting
	01	INPUT 384 (×44.1 kHz or 48 kHz)	
	10	INPUT 512 (×44.1 kHz or 48 kHz)	
	11	INPUT 768 (×44.1 kHz or 48 kHz)	
4:3	00	XTAL oscillator enabled	MCLKO/XO pin, master clock rate setting
	01	256 × f_S VCO output	
	10	512 × f_S VCO output	
	11	Off	
6:5	00	MCLKI/XI	PLL input
	01	AUXLRCLK	
	10	ALRCLK	
	11	Reserved	
7	0	Disable: ADC idle	Internal MCLK enable
	1	Enable: ADC active	

Table 17. PLL and Clock Control 1

Bit	Value	Function	Description
0	0 1	PLL clock MCLK	AUXPORT clock source select
1	0 1	PLL clock MCLK	ADC clock source select
2	0 1	Enabled Disabled	On-chip voltage reference
3	0 1	Not locked Locked	PLL lock indicator (read only)
7:4	0000	Reserved	

AUXPORT CONTROL REGISTERS

Table 18. AUXPORT Control 0

Bit	Value	Function	Description
0	0 1	Reserved Reserved	Reserved
2:1	00 01 10 11	32 kHz/44.1 kHz/48 kHz 64 kHz/88.2 kHz/96 kHz 128 kHz/176.4 kHz/192 kHz Reserved	Sample rate
5:3	000 001 010 011 100 101 110 111	1 0 8 12 16 Reserved Reserved Reserved	AUXDATA delay (AUXBCLK periods)
7:6	00 01 10 11	Stereo (normal) Reserved ADC AUX mode (ADC-, TDM-coupled) Reserved	Serial format

Table 19. AUXPORT Control 1

Bit	Value	Function	Description
0	0 1	Reserved Reserved	
2:1	00 01 10 11	64 (two channels) Reserved Reserved Reserved	AUXBCLKs per frame
3	0 1	Left low Left high	AUXLRCLK polarity
4	0 1	Slave Master	AUXLRCLK master/slave
5	0 1	Slave Master	AUXBCLK master/slave
6	0 1	AUXBCLK pin Internally generated	AUXBCLK source
7	0 1	Normal Inverted	AUXBCLK polarity

Table 20. AUXPORT Control 2

Bit	Value	Function	Description
0	0	Reserved	
	1	Reserved	
2:1	00	Reserved	
	01	Reserved	
	10	Reserved	
	11	Reserved	
4:3	00	24	Word width
	01	20	
	10	Reserved	
	11	16	
5	0	Reserved	
	1	Reserved	
7:6	00	Reserved	

ADC CONTROL REGISTERS

Table 21. ADC Control 0

Bit	Value	Function	Description
0	0	Normal	Power-down
	1	Power down	
1	0	Off	High-pass filter
	1	On	
2	0	Unmute	ADC1L mute
	1	Mute	
3	0	Unmute	ADC1R mute
	1	Mute	
4	0	Unmute	ADC2L mute
	1	Mute	
5	0	Unmute	ADC2R mute
	1	Mute	
7:6	00	32 kHz/44.1 kHz/48 kHz	Output sample rate
	01	64 kHz/88.2 kHz/96 kHz	
	10	128 kHz/176.4 kHz/192 kHz	
	11	Reserved	

Table 22. ADC Control 1

Bit	Value	Function	Description
1:0	00	24	Word width
	01	20	
	10	Reserved	
	11	16	
4:2	000	1	SDATA delay (BCLK periods)
	001	0	
	010	8	
	011	12	
	100	16	
	101	Reserved	
	110	Reserved	
	111	Reserved	

Bit	Value	Function	Description
6:5	00	Stereo	Serial format
	01	TDM (daisy chain)	
	10	ADC AUX mode (TDM-coupled)	
	11	Reserved	
7	0	Latch in midcycle (normal)	BCLK active edge (TDM_IN)
	1	Latch in at end of cycle (pipeline)	

Table 23. ADC Control 2

Bit	Value	Function	Description
0	0	50/50 (allows 32-/24-/20-/16-BCLK per channel)	LRCLK format
	1	Pulse (32-BCLK/channel)	
1	0	Drive out on falling edge (DEF)	BCLK polarity
	1	Drive out on rising edge	
2	0	Left low	LRCLK polarity
	1	Left high	
3	0	Slave	LRCLK master/slave
	1	Master	
5:4	00	64	BCLKs per frame
	01	128	
	10	256	
	11	512	
6	0	Slave	BCLK master/slave
	1	Master	
7	0	ABCLK pin	BCLK source
	1	Internally generated	

ADDITIONAL MODES

The AD1974 offers several additional modes for board level design enhancements. To reduce the EMI in board level design, serial data can be transmitted without an explicit BCLK. See Figure 15 for an example of an ADC TDM data transmission mode that does not require high speed ABCLK. This configuration is applicable when the AD1974 master clock is generated by the PLL with the ALRCLK as the PLL reference frequency.

To relax the requirement for the setup time of the AD1974 in cases of high speed TDM data transmission, the AD1974 can latch in the data using the falling edge of ABCLK. This effectively dedicates the entire BCLK period to the setup time. This mode is useful in cases where the source has a large delay time in the serial data driver. Figure 16 shows this pipeline mode of data transmission.

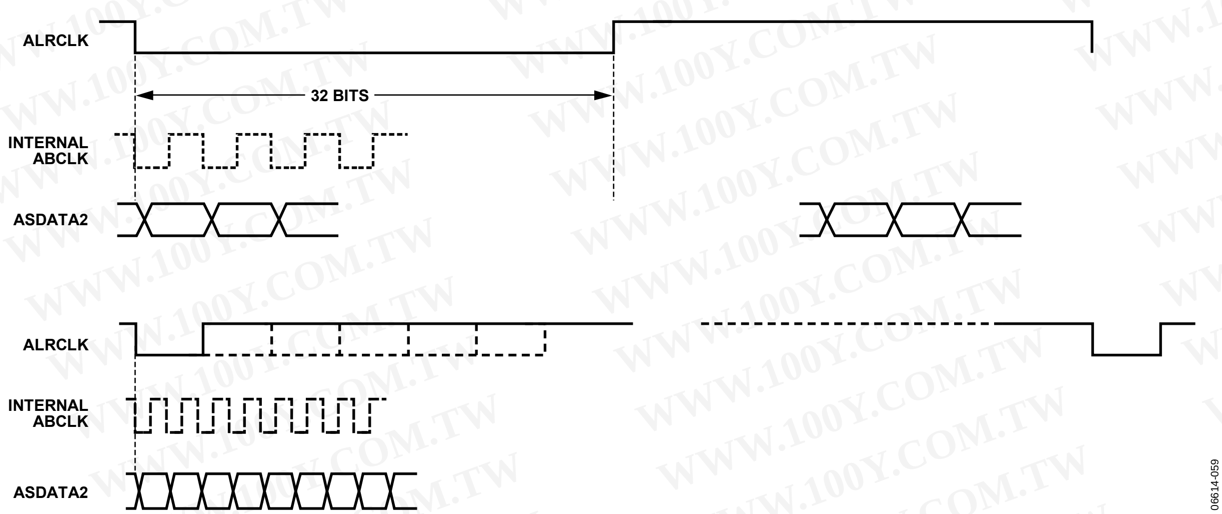


Figure 15. Serial ADC Data Transmission in TDM Format Without ABCLK (Applicable Only If PLL Locks to ALRCLK)

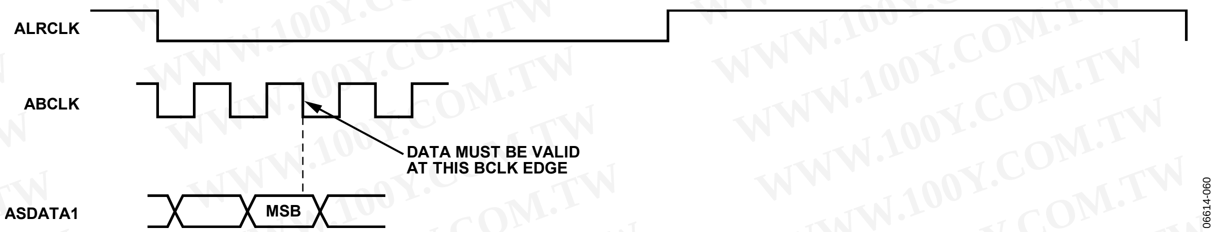


Figure 16. I²S Pipeline Mode in ADC Serial Data Transmission
(Applicable in Stereo and TDM Useful for High Frequency TDM Transmission)

APPLICATION CIRCUITS

Typical applications circuits are shown in Figure 17 and Figure 18. Figure 17 shows a typical ADC input filter circuit. Recommended loop filters for LR clock and master clock as the PLL reference are shown in Figure 18.

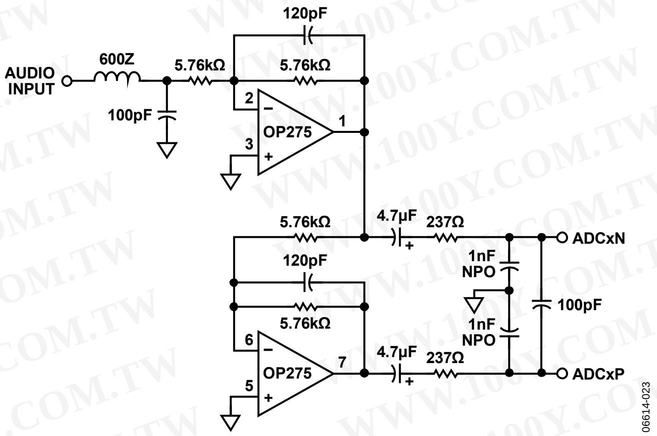


Figure 17. Typical ADC Input Filter Circuit

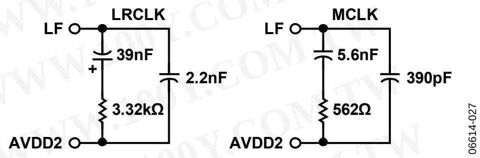
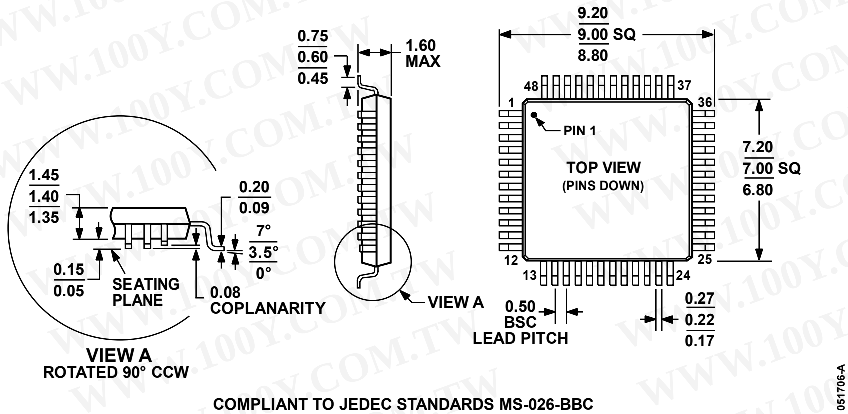


Figure 18. Recommended Loop Filters for LRCLK or MCLK PLL Reference

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 19. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option
AD1974YSTZ	2	−40°C to +105°C	48-Lead LQFP	ST-48
AD1974YSTZ-RL	2	−40°C to +105°C	48-Lead LQFP, 13" Tape and Reel	ST-48
EVAL-AD1974AZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] SPI control port.

D06614-0-6/10(B)