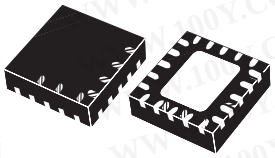
STS1TX

Low data-rate, low power sub-1GHz transmitter

Datasheet - production data



QFN20

Features

- Frequency bands: 150-174 MHz, 300-348 MHz, 387-470 MHz, 779-956 MHz
- Modulation schemes: 2-FSK, GFSK, MSK, GMSK, OOK, and ASK
- Air data rate from 1 to 500 kbps
- Very low power consumption (21 mA TX at +11 dBm)
- Programmable channel spacing (12.5 kHz min.)
- Programmable output power up to +16 dBm
- Fast startup and frequency synthesizer settling time (6 µs)
- Integrated temperature sensor
- Battery indicator and low battery detector
- TX FIFO buffer (96 bytes each)
- Configurability via SPI interface
- AES 128-bit encryption co-processor
- Fully integrated ultra low power RC oscillator
- Wakeup on internal timer and on external event
- Flexible packet length with dynamic payload length
- Automatic CRC handling
- FEC with interleaving
- Whitening of data
- Wireless M-BUS, EN 300 220, FCC CFR47 15 (15.205, 15.209, 15.231, 15.247, 15.249), and ARIB STD T-67, T93, T-108 compliant
- QFN20 4x4 mm RoHS package
- Operating temperature range from -40 °C to 85 °C

Applications

- AMR (automatic meter reading)
- Home and building automation
- WSN (wireless sensors network)
- Industrial monitoring and control
- Wireless fire and security alarm systems
- Point-to-point wireless link

Table 1. Device summary

Order code	Package	Packing
STS1TXQTR	QFN20	Tape and reel

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1 Description

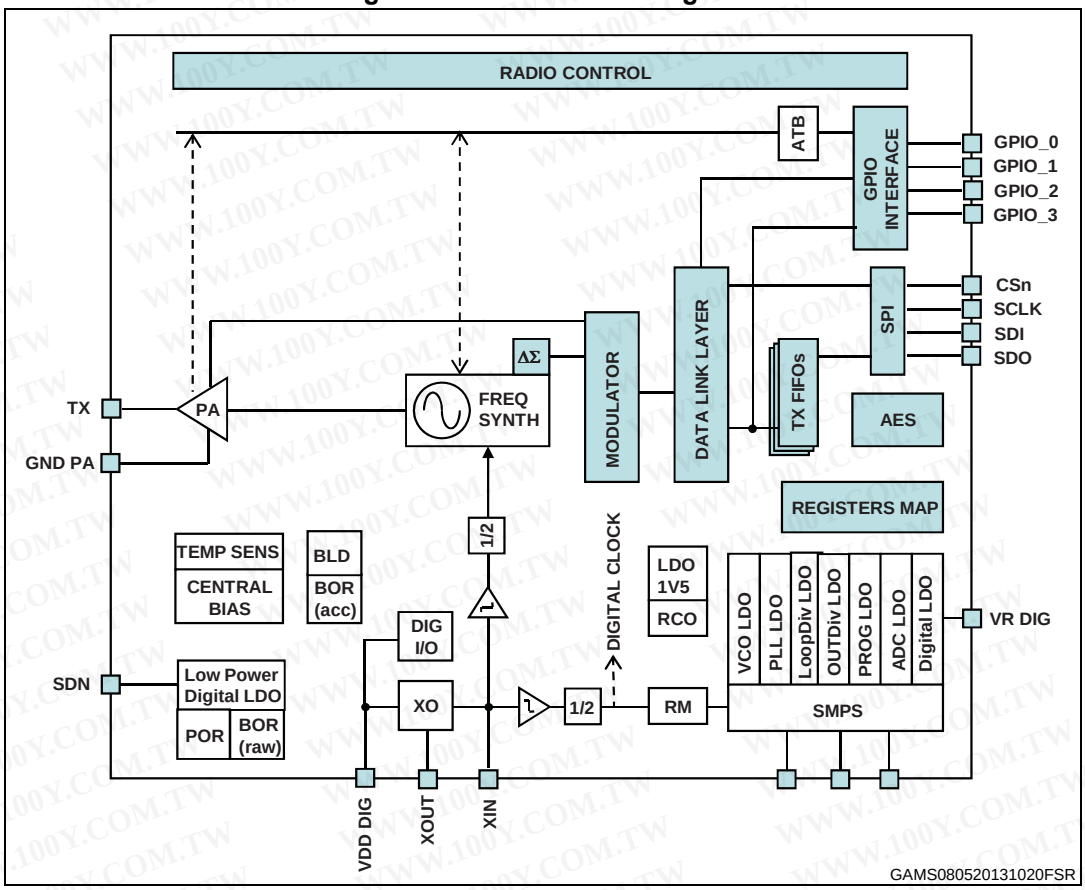
The STS1TX is a very low-power RF transmitter intended for RF wireless applications in the sub-1 GHz band. It is designed to operate both in the license-free ISM and SRD frequency bands at 169, 315, 433, 868, and 915 MHz, but can also be programmed to operate at other frequencies in the 300-348, 387-470, and 779-956 MHz bands. The air data rate is programmable from 1 to 500 kbps, and the STS1TX can be used in systems with channel spacing of 12.5/25 kHz, complying with the EN 300 220 standard. It uses very few discrete external components and integrates a configurable baseband modem, which supports data management and modulation. The data management handles the data in the proprietary fully-programmable packet format, and also allows the M-Bus standard compliance format (all performance classes).

An AES 128-bit encryption co-processor is available for secure data transfer. The STS1TX supports different modulation schemes: 2-FSK, GFSK, OOK, ASK, and MSK. Transmitted data bytes are buffered in FIFO (TX FIFO), accessible via the SPI interface for host processing.

2 Introduction

A simplified block diagram of the STS1TX is shown in *Figure 1*.

Figure 1. STS1TX block diagram



The transmitter part of the STS1TX is based on direct synthesis of the RF frequency. The power amplifier (PA) input is the LO generated by the RF synthesizer, while the output level can be configured between -30 dBm and +11 dBm in 0.5 dB steps. The data to be transmitted can be provided by an external MCU either through the 96-byte TX FIFO writable via SPI, or directly using a programmable GPIO pin. The STS1TX supports frequency hopping, extending the link range and improving performance.

The STS1TX has a very efficient power management (PM) system.

An integrated switched mode power supply (SMPS) regulator allows operation from a battery voltage ranging from +1.8 V to +3.6 V, and with power conversion efficiency of at least 80%.

A crystal must be connected between XIN and XOUT. It is digitally configurable to operate with different crystals. As an alternative, an external clock signal can be used to feed XIN for proper operation. The STS1TX also has an integrated low-power RC oscillator, generating the 34.7 kHz signal used as a clock for the slowest timeouts (i.e. sleeping and backoff).

A standard 4-pin SPI bus is used to communicate with the external MCU. Four configurable general purpose I/Os are available.

3 Typical application diagram and pin description

3.1 Typical application diagram

This section describes different application diagrams for the STS1TX that can be used based on customer requirements. In particular, *Figure 2* shows the default configuration and *Figure 3* shows the TX boost mode configuration. The default configuration provides the best power consumption figures. The TX boost mode configuration is used to increase TX output power.

Figure 2. Suggested application diagram

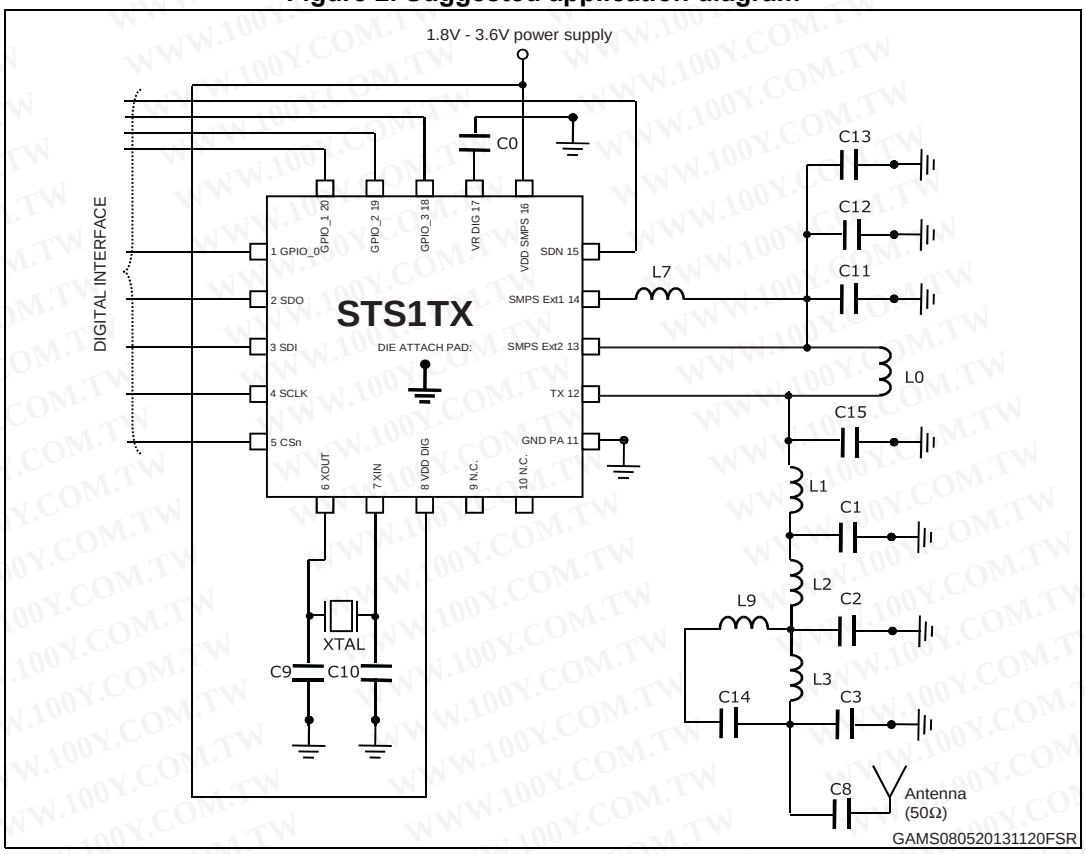


Figure 3. Application diagram for TX boost mode

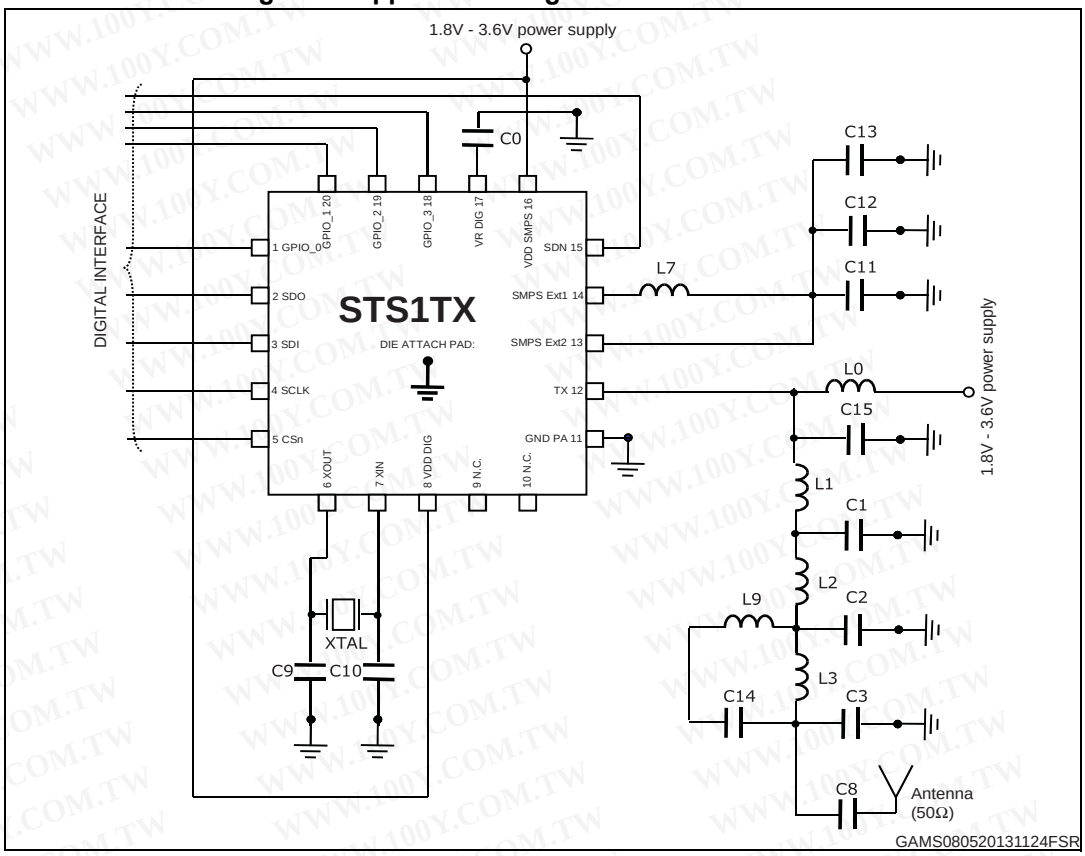


Table 2. Description of the external components of the typical application diagram

Components	Description
C0	Decoupling capacitor for on-chip voltage regulator to digital part
C1, C2, C3, C14, C15	RF LC filter/matching capacitors
C8	Matching DC blocking capacitors
C9, C10	Crystal loading capacitors
C11, C12, C13	SMPS LC filter capacitor
L0	RF choke inductor
L1, L2, L3, L9	RF LC filter/matching inductors
XTAL	24, 26, 48, 52 MHz

Table 2 covers all the frequency bands using a set of different external components as shown in *Table 3: BOM for different bands*.

Table 3. BOM for different bands

Ref design (1)	170 MHz band		315 MHz band		433 MHz band		868 MHz band		915/922 MHz band	
	STEVAL-IKRV001V1		STEVAL-IKRV001V2		STEVAL-IKRV001V3		STEVAL-IKRV001V4		STEVAL-IKRV001V5	
Comp.	Supplier	Value	Supplier	Value	Supplier	Value	Supplier	Value	Supplier	Value
C0	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF
C1	Murata	18pF	Murata	12pF	Murata	8.2pF		NE	Murata	7pF
C2	Murata	27pF	Murata	27pF	Murata	18pF	Murata	8.2pF	Murata	2.4pF
C3	Murata	4.3pF	Murata	15pF	Murata	10pF	Murata	5.6pF	Murata	3.6pF
C8	Murata	390pF	Murata	220pF	Murata	220pF	Murata	220pF	Murata	220pF
C9	Murata	12pF	Murata	12pF	Murata	12pF	Murata	12pF	Murata	12pF
C10	Murata	10pF	Murata	10pF	Murata	10pF	Murata	10pF	Murata	10pF
C11	Murata	1µF	Murata	1µF	Murata	1µF	Murata	470nF	Murata	1µF
C12	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF
C13	Murata	560pF	Murata	330pF	Murata	330pF	Murata	330pF	Murata	330pF
C14	Murata	220pF	Murata	1.8pF	Murata	1.8pF	Murata	1.2pF		NE
C15	Murata	6.2pF	Murata	1.2pF		NE		NE		NE
L0	Murata	200nH	Murata	220nH	Murata	150nH	Murata	100nH	Murata	100nH
L1	Coilcraft	39nH	Murata	12nH	Murata	8.2nH	Murata	3nH	Murata	3.6nH
L2	Coilcraft	56nH	Murata	12nH	Murata	10nH		0R0 (resistor)	Murata	5.1nH
L3	Murata	3.6pF (cap.)	Murata	15nH	Murata	10nH	Murata	4.3nH	Tyco Electronics	0R0
L9	Coilcraft	51nH	Murata	15nH	Murata	6.2nH	Murata	2.7nH		NE
XTAL	NDK	25 MHz	NDK	50 MHz	NDK	50 or 52 MHz	NDK	50 or 52 MHz	NDK	50 or 52 MHz

1. For complete BOM including part numbers, please check the corresponding reference design.

4 Pinout

Table 4. Pinout description

Pin	Name	I/O	Description
1	GPIO_0	I/O	See description of GPIOs below
2	MISO	O	SPI data output pin
3	MOSI	I	SPI data input pin
4	SCLK	I	SPI clock input pin
5	CSn	I	SPI chip select
6	XOUT	O	Crystal oscillator output. Connect to an external 26 MHz crystal or leave floating if driving the XIN pin with an external signal source
7	XIN	I	Crystal oscillator input. Connect to an external 26 MHz crystal or to an external source. If using an external clock source with no crystal, DC coupling with a nominal 0.2 VDC level is recommended with minimum AC amplitude of 400 mVpp. The instantaneous level at input cannot exceed the 0 - 1.4 V range.
8	VBAT	VDD	+1.8 V to +3.6 V input supply voltage
9	NC	-	
10	NC	-	
11	GND_PA	GND	Ground for PA. To be carefully decoupled from other grounds.
12	TX	O	RF output signal
13	SMPS Ext2	I	Regulated DC-DC voltage input
14	SMPS Ext1	O	DC-DC output pin
15	SDN	I	Shutdown input pin. 0-VDD V digital input. SDN should be = ‘0’ in all modes except shutdown mode. When SDN =’1’ the STS1TX is completely shut down and the contents of the registers are lost.
16	VBAT	VDD	+1.8 V to +3.6 V input supply voltage
17	VREG(1)	VDD	Regulated output voltage. A 100 nF decoupling capacitor is required
18	GPIO3	I/O	General purpose I/O that may be configured through the SPI registers to perform various functions, including: – MCU clock output – FIFO status flags – Wakeup input – Battery level detector – Temperature sensor output
19	GPIO2	I/O	
20	GPIO1	I/O	
21	GND	GND	Exposed pad ground pin

1. This pin is intended for use with the STS1TX only. It cannot be used to provide supply voltage to other devices.

5 Absolute maximum ratings and thermal data

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.

Table 5. Absolute maximum ratings

Pin	Parameter	Value	Unit
8,14,16	Supply voltage and SMPS output	-0.3 to +3.9	V
17	DC voltage on VREG	-0.3 to +1.4	V
1,3,4,5,15,18,19,20	DC voltage on digital input pins	-0.3 to +3.9	V
2	DC voltage on digital output pins	-0.3 to +3.9	V
11	DC voltage on analog pins	-0.3 to +3.9	V
6,7	DC voltage on XTAL pins	-0.3 to +1.4	V
13	DC voltage on SMPS Ext2 pin	-0.3 to +1.8	V
12	DC voltage on TX pin	-0.3 to +3.9	V
T_{STG}	Storage temperature range	-40 to +125	°C
$V_{ESD-HBM}$	Electrostatic discharge voltage	±1.0	KV

Table 6. Thermal data

Symbol	Parameter	QFN20	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient	45	°C/W

Table 7. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BAT}	Operating battery supply voltage	1.8	3	3.6	V
T_A	Operating ambient temperature range	-40		85	°C

6 Characteristics

6.1 General characteristics

Table 8. General characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
FREQ	Frequency range	150	-	174	MHz
		300		348	MHz
		387		470	MHz
		779		956	MHz
DR	Air data rate for each modulation scheme. Note that if “Manchester”, “3-out-of-6” and/or FEC encoding/decoding options are selected, the effective bit rate will be lower.				
	2-FSK	1	-	500	kBaud
	GMSK (BT=1, BT=0.5)	1		500	kBaud
	GFSK (BT=1, BT=0.5)	1		500	kBaud
	MSK	1		500	kBaud
	OOK/ASK	1		250	kBaud

6.2 Electrical specifications

6.2.1 Electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance is referred to a 50 Ohm antenna connector, via the reference design using the application diagram as in *Figure 2*, unless otherwise noted.

Table 9. Power consumption static modes

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IBAT	Supply current	Shutdown (1)	-	2.5	-	nA
		Standby (1)		600		
		Sleep (1)		850		
		Ready (default mode)(1)		400		µA
		Lock(1)		4.4		mA

1. See *Table 18*.

Table 10. Power consumption

Symbol	Parameter	Test conditions	SMPS ON	SMPS OFF	Unit
IBAT	Supply current	TX (1)(2) +16 dBm 169 MHz	54		mA
		TX (1)(2) +16 dBm 315 MHz	52		
		TX (1)(2) +16 dBm 433 MHz	49.3		
		TX (1)(2) +15.5 dBm 868 MHz	44		
		TX (1)(2) +16 dBm 920 MHz	45.2		
		TX (1) +11 dBm 169 MHz	18	33	
		TX (1) +11 dBm 315 MHz	22	37	
		TX (1) +11 dBm 433 MHz	19.5	33	
		TX (1) +11 dBm 868 MHz	21	41	
		TX (1) +11 dBm 920 MHz	20	39	
		TX (1) -8 dBm 169 MHz	6		
		TX (1) -8 dBm 315 MHz	6.5		
		TX (1) -7 dBm 433 MHz	7		
		TX (1) -7 dBm 868 MHz	7		

1. See table *Table 18*.
2. TX boost mode configuration V_{BAT} = 3.6 V.

6.2.2 Digital SPI

Table 11. Digital SPI input and output (SDO, SDI, SCLK, CSn, and SDN) and GPIO specification (GPIO_1-4)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency				10	MHz
C_{IN}	Port I/O capacitance			1.4		pF
T_{RISE}	Rise time	0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		6.0		ns
		0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
T_{FALL}	Fall time	0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		7.0		ns
		0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
V_{IH}	Logic high level input voltage		VDD/2 +0.3			V

Table 11. Digital SPI input and output (SDO, SDI, SCLK, CSn, and SDN) and GPIO specification (GPIO_1-4) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Logic low level input voltage				VDD/8 +0.3	V
V_{OH}	High level output voltage	IOH = -2.4 mA (-4.2 mA if high output current capability is programmed).	(5/8)* VDD+ 0.1			V
V_{OL}	Low level output voltage	IOL = +2.4 mA (+4 mA if high output current capability is programmed).			0.5	V

6.2.3 RF transmitter

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance is referred to a 50 Ohm antenna connector, via the reference design.

Table 12. RF transmitter characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{MAX\_TX\_BOOST}$	Maximum output power(1)	Delivered to a 50 Ohm single-ended load via reference design using TX boost mode configuration	-	16		dBm
P_{MAX}	Maximum output power(1)	Delivered to a 50 Ohm single-ended load via reference design	-	11		dBm
P_{MIN}	Minimum output power	Delivered to a 50 Ohm single-ended load via reference design	-	-30		dBm
P_{STEP}	Output power step		-	0.5		dB

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{SPUR,ETSI}$	Unwanted emissions according to ETSI EN300 220-1(harmonic included, using reference design)	RF = 170 MHz, frequencies below 1 GHz	-		-36	dBm
		RF = 170 MHz, Frequencies above 1 GHz	-		< -60	dBm
		RF = 170 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-55	dBm
		RF = 434 MHz, frequencies below 1 GHz	-		-42	dBm
		RF = 434 MHz, Frequencies above 1 GHz	-		-46	dBm
		RF = 434 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-61	dBm
		RF = 868 MHz, frequencies below 1 GHz	-		-51	dBm
		RF = 868 MHz, Frequencies above 1 GHz	-		-40	dBm
		RF = 868 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-54	dBm

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{SPUR,FCC}$	Unwanted emissions according to FCC part 15(harmonic included, using reference design)	RF = 310-320 MHz, harmonics (measured with max output power)	-		-37	dBm
		RF = 310-320 MHz, 1.705 MHz <f< 30 MHz	-		<-60	dBm
		RF = 310-320 MHz, 30 MHz <f< 88 MHz	-		<-60	dBm
		RF = 310-320 MHz, 88 MHz <f< 216 MHz	-		<-60	dBm
		RF = 310-320 MHz, 216 MHz <f< 960 MHz	-		<-60	dBm
		RF = 310-320 MHz, 960 MHz <f	-		<-60	dBm
		RF = 902-928 MHz, 1.705 MHz <f< 30 MHz (@ max output power)	-		<-70	dBm
		RF = 902-928 MHz, 30 MHz <f< 88 MHz (@ max output power)	-		<-70	dBm
		RF = 902-928 MHz, 88 MHz <f< 216 MHz (@ max output power)	-		<-70	dBm
		RF = 902-928 MHz, 216 MHz <f< 960 MHz (@ max output power)	-		-52	dBm
		RF = 902-928 MHz, 960 MHz <f (@ max output power)	-		-41	dBm
		2^{nd} and 7^{th} harmonics	-		-25	dBc

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{SPUR,ARIB}$	Unwanted emissions according to ARIB	RF = 312-315 MHz, frequency below 1 GHz (@ max output power, according to ARIB STD-T93)	-		-41	dBm
		RF = 312-315 MHz, frequency above 1 GHz (@ max output power, according to ARIB STD-T93)	-		-48	dBm
		RF = 426-470 MHz (@ max output power, according to ARIB STD-T67)	-		<-40	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, f< 710 MHz (@ max output power, according to ARIB STD-T108)	-		<-55	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 710 MHz <f< 915 MHz (@ max output power, according to ARIB STD-T108)	-		-55	dBm
		RF = 915-917 MHz and RF = 924-930 MHz, 915 MHz <f< 930 MHz (@ max output power, according to ARIB STD-T108)	-		-36	dBm
		RF = 920-924 MHz, 915 MHz <f< 920.3 MHz (@ max output power, according to ARIB STD-T108)	-		<-36	dBm
		RF = 920-924 MHz, 920.3 MHz <f< 924.3 MHz (@ max output power, according to ARIB STD-T108)	-		-55	dBm
		RF = 920-924 MHz, 924.3 MHz <f< 930 MHz (@ max output power, according to ARIB STD-T108)	-		-36	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 930 MHz <f< 1000 MHz (@ max output power, according to ARIB STD-T108)	-		-55	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 1000 MHz <f< 1215 MHz (@ max output power, according to ARIB STD-T108)	-		<-60	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 1215 MHz <f (@ max output power, according to ARIB STD-T108)	-		-38	dBm

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{HARM}	Harmonics level	RF = 170 MHz, 2nd harmonic (max power level)	-		-36	dBm
		RF = 170 MHz, 3rd harmonic (max power level)	-		-55	
		RF = 315 MHz, 2nd harmonic (max power level)	-		-52	dBc
		RF = 315 MHz, 3rd harmonic (max power level)	-		-52	
		RF = 433 MHz, 2nd harmonic (max power level)	-		-43	dBm
		RF = 433 MHz, 3rd harmonic (max power level)	-		-46	
		RF = 868 MHz, 2nd harmonic (max power level)	-		-40	
		RF = 868 MHz, 3rd harmonic (max power level)	-		-42	
		RF = 915 MHz, 2nd harmonic (max power level)	-		-28	dBc
		RF = 915 MHz, 3rd harmonic (max power level)	-		-42	dBm
		RF = 922 MHz, 2nd harmonic (max power level)	-		-39	
		RF = 922 MHz, 3rd harmonic (max power level)	-		-60	
PA_{LOAD}	Optimum load impedance (simulated values)	170 MHz, using reference design	-	46 + j36		Ohm
		315 MHz, using reference design	-	25 + j27		Ohm
		433 MHz, using reference design	-	29 + j19		Ohm
		868 MHz, using reference design	-	34 - j7		Ohm
		915 MHz, using reference design	-	15 + j28		Ohm
		922 MHz, using reference design	-	42 - j15		Ohm

1. In ASK/OOK modulation, indicated value represents peak power.

6.2.4 Crystal oscillator

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. Frequency synthesizer characteristics are referred to 915 MHz band.

Table 13. Crystal oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$XTAL_F$	Crystal frequency	Range 1 Range 2	24 48		26 52	MHz
F_{TOL}	Frequency tolerance(1)			± 40		ppm
PN_{XTAL}	Minimum requirement on external reference phase noise mask (Fxo=26 MHz), to avoid degradation on synthesizer phase/noise	100 Hz			-90	dBc/Hz
		1 kHz			-120	dBc/Hz
		10 kHz			-135	dBc/Hz
		100 kHz			-140	dBc/Hz
		1 MHz			-140	dBc/Hz
T_{START}	Startup time(2)	V_{BAT}=1.8 V, Fxo= 52 MHz	60	120	220	µs

1. Including initial tolerance, crystal loading, aging, and temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.
2. Startup times are crystal dependent. The crystal oscillator transconductance can be tuned to compensate the variation of crystal oscillator series resistance.

Table 14. Ultra low power RC oscillator

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RC_F	Calibrated frequency	Calibrated RC oscillator frequency is derived from crystal oscillator frequency. Digital clock domain 26 MHz	-	34.7		kHz
RC_{TOL}	Frequency accuracy after calibration				±1	%

Table 15. N-Fractional ΣΔ frequency synthesizer characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{RES}	Frequency resolution	Fxo = 26 MHz high band	-	33		Hz
PN_{SYNTH}	RF carrier phase noise (915 MHz band)	10 kHz	-100	-97	-94	dBc/Hz
		100 kHz	-104	-101	-99	dBc/Hz
		200 kHz	-105	-102	-100	dBc/Hz
		500 kHz	-112	-110	-107	dBc/Hz
		1 MHz	-120	-118	-116	dBc/Hz
		2 MHz	-123	-121	-119	dBc/Hz
TO_{TIME}	PLL turn-on/hop time			60	80	µs
CAL_{TIME}	PLL calibration time			54		µs

6.2.5 Sensors

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V.

Table 16. Analog temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{ERR}	Error in temperature	Across the temperature range	-	±2.5	-	°C
T_{SLOPE}	Temperature coefficient			2.5		mV/ °C
V_{TS-OUT}	Output voltage level			0.92		V
T_{ICC}	Current consumption	Buffered output (low output impedance; about 400 Ohm)		600		µA
		Not buffered output (high output impedance; about 100 kΩ)		10		µA

Table 17. Battery indicator and low battery detector(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BLT}	Battery level thresholds		2.1		2.7	V
V_{BOT}	Brownout threshold	Measured in slow battery variation (static) conditions (inaccurate)		1.535		V
		Measured in slow battery variation (static) conditions (accurate)		1.684		V
BOT_{hyst}	Brownout threshold hysteresis			70		mV

1. For battery powered equipment, the TX does not transmit at incorrect frequencies under low battery voltage conditions. It either remains on channel or stops transmitting. The latter can of course be implemented by using a lock detect and/or by switching off the PA under control of the battery monitor. For testing purposes this control is enabled/disabled by SPI.

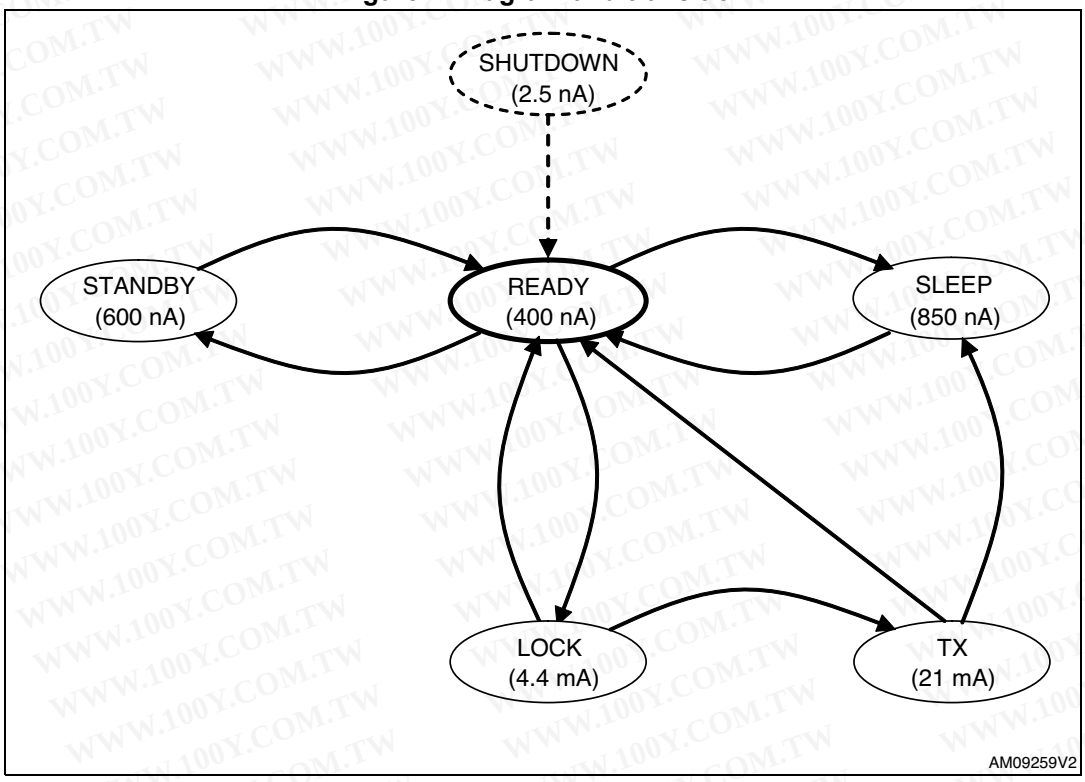
7 Operating modes

The STS1TX is equipped with a built-in main controller which controls the switching between the two main operating modes: transmit (TX).

In shutdown condition (the STS1TX can be switched on/off with the external pin SDN, all other functions/registers/commands are available through the SPI interface and GPIOs), no internal supply is generated (in order to minimize battery leakage), and hence, all stored data and configurations are lost. The GPIO and SPI ports during SHUTDOWN are in HiZ. From shutdown, the STS1TX can be switched on from the SDN pin and goes into READY state, which is the default, where the reference signal from XO is available.

From READY state, the STS1TX can be moved to LOCK state to generate the high precision LO signal and/or TX mode. At the end of the operations above, the STS1TX can return to its default state (READY) and can then be put into a sleep condition (SLEEP state), with very low power consumption. If no timeout is required, the STS1TX can be moved from READY to STANDBY state, which has the lowest possible current consumption while retaining FIFO, status and configuration registers. To manage the transitions towards and between these operating modes, the controller works as a state-machine, whose state switching is driven by SPI commands. See *Figure 4* for state diagram and transition time between states.

Figure 4. Diagram and transition



The STS1TX radio control has three stable states (READY, STANDBY, LOCK) which may be defined stable, and they are accessed by the specific commands (respectively READY, STANDBY, and LOCKTX), which can be left only if any other command is used. All other states are transient, which means that in a typical configuration, the controller remains in

those states, at most for any time-out timer duration. Also the READY and LOCK states behave as transients when they are not directly accessed with the specific commands (for example, when LOCK is temporarily used before reaching the TX state).

Table 18. States

STATE[6:0](1)	State/mode	Digital LDO	SPI	Xtal	RF Synth.	Wakeup timer	Response time to(2)
							TX
-	SHUTDOWN	OFF (register contents lost)	Off	Off	Off	Off	NA
0x40	STANDBY	ON (FIFO and register contents retained)	On	Off	Off	Off	125 µs
0x36	SLEEP		On	Off	Off	On	125 µs
0x03	READY (Default)		On	On	Off	Don't care	50 µs
0x0F	LOCK		On	On	On	Don't care	NA
0x5f	TX		On	On	On	Don't care	NA

1. All others values of STATE[6:0] are invalid and are an indication of an error condition due to bad registers configuration and/or hardware issue in the application board hosting STS1TX.
2. These values are crystal dependent. The values are referred to 52 MHz.

Note: Response time SHUTDOWN to READY is ~650 µs.

READY state is the default state after the power-on reset event. In the steady condition, the XO is settled and usable as the time reference for RCO calibration, for frequency synthesis, and as the system clock for the digital circuits.

The TX mode can be activated directly by the MCU using the TX command, or automatically if the state machine wakes up from SLEEP mode and some previous TX is pending. The values are intend to a VCO manual calibration.

In LOCK state the synthesizer is in a locking condition(a). If LOCK state is reached using specific command LOCKTX, the state machine remains in LOCK state and waits for the next command. This feature can be used by the MCU to perform preliminary calibrations, as the MCU can read the calibration word in the RCO_VCO_CALIBR_OUT register and store it in a non-volatile memory, and after that it requires a further tuning cycle.

When TX is activated by the TX command, the state machine goes into TX state and remains there until the current packet is fully transmitted or, in the case of direct mode TX, TXFIFO underflow condition is reached or the SABORT command is applied.

a. LOCK state is reached when one of the following events occurs first: lock detector assertion or locking timeout expiration.

After TX completion, the possible destinations are:

- TX, if the persistent-TX option is enabled in the PROTOCOL configuration registers
- PROTOCOL, if some protocol option (e.g. automatic re-transmission) is enabled
- READY, if TX is completed and no protocol option is in progress.

The SABORT command can always be used in TX state to break any deadlock condition and the subsequent destination depends on STS1TX programming according to the description above.

Commands are used in the STS1TX to change the operating mode, to enable/disable functions, and so on. A command is sent on the SPI interface and may be followed by any other SPI access without pulling CSn high.

The complete list of commands is reported in *Table 19*. Note that the command code is the second byte to be sent on the MOSI pin (the first byte must be 0x80).

Table 19. Commands list

Command code	Command name	Execution state	Description
0x60	TX	READY	Start to transmit
0x62	READY	STANDBY, SLEEP, LOCK	Go to READY
0x63	STANDBY	READY	Go to STANDBY
0x64	SLEEP	READY	Go to SLEEP
0x66	LOCKTX	READY	Go to LOCK state by using the TX configuration of the synthesizer
0x67	SABORT	TX	Exit from TX state and go to READY state
0x68	LDC_RELOAD	All	Reload the LDC timer with the value stored in the LDC_PRESCALER/COUNTER registers
0x69	SEQUENCE_UPDATE	All	Reload the packet sequence counter with the value stored in the PROTOCOL[2] register.
0x6A	AES Enc	All	Start the encryption routine
0x6B	AES Key	All	Start the procedure to compute the key for decryption
0x6C	AES Dec	All	Start decryption using the current key
0x6D	AES KeyDec	All	Compute the key and start decryption
0x70	SRES	All	Reset
0x72	FLUSHTXFIFO	All	Clean the TX FIFO

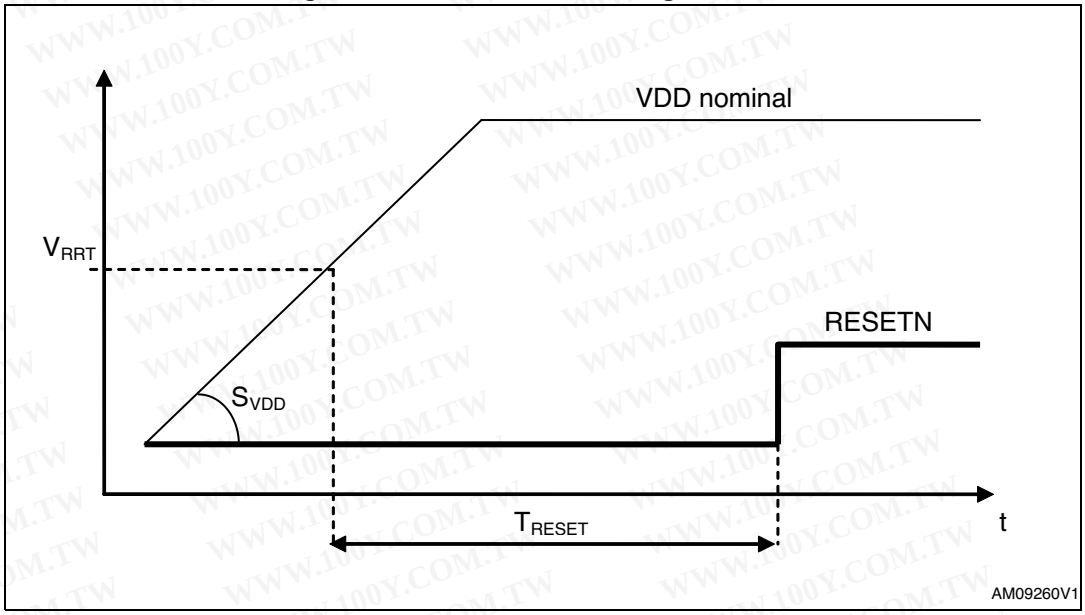
The commands are immediately valid after SPI transfer completion (i.e. no need for any CSn positive edge).

7.1 Reset sequence

The STS1TX includes an automatic power-on reset (POR) circuit which generates an internal RESETN active (low) level for a time T_{RESET} after the VDD reaches the reset

release threshold voltage V_{RRT} (provided that SDN is low), as shown below. The same reset pulse is generated after a step-down on the input pin SDN (provided that VDD>V_{RRT}).

Figure 5. Power-on reset timing and limits



The parameters V_{RRT} and T_{RESET} are fixed by design. At RESET, all the registers are initialized to their default values. Typical and extreme values are reported in the following table.

Table 20. POR parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{RRT}	Reset startup threshold voltage		0.5		V
T_{RESET}	Reset pulse width	0.24	0.65	1.0	ms

Note: An SRES command is also available, which generates an internal RESET of the STS1TX.

7.2 Timer usage

Most of the timers are programmable via R/W registers. All timer registers are made up of two bytes: the first byte is a multiplier factor (prescaler); the second byte is a counter value.

Timer period= PRESCALER x COUNTER x Tclk

Note: If the counter register value (prescaler register value) is 0, the related timer never stops (infinite timeout), despite the value written in the prescaler register (counter register).

The available timers and their features are listed in the following table.

Table 21. STS1TX timers description and duration

No.	Register name	Description	Source	Time step	Max. time
3	LDCR_PRESCALER	Wakeup period	RCO	~29µs	~2s
4	LDCR_COUNTER				

Note: It is not allowed to set LDC_PRESCALER or LDC_COUNTER to 0

For LDCR_COUNTER and LDCR_PRESCALER only, the effective number of cycles counted is given by the value + 1 (e.g. counter=1 and prescaler=1 produces 2 x 2=4 counts, counter=1 and prescaler=2 produces 2 x 3=6 counts, etc.).

8 Block description

8.1 Power management

The STS1TX integrates a high efficiency step-down converter cascaded with LDOs meant to supply both analog and digital parts. However, an LDO directly fed by the external battery provides a controlled voltage to the data interface block.

8.1.1 Switching frequency

The SMPS switching frequency can be provided either by a divider by four or by a programmable rate multiplier. The divider by four or the rate multiplier is activated when the EN_RM bit is set to both 0 and 1 in the PM_CONFIG[2:0] register bank. When the rate multiplier is activated, the divider ratio can be programmed by KRM[14:0] word in the PM_CONFIG[2:0] register bank. In this case, the SMPS switching frequency is given by the following formula:

$$F_{sw} = \frac{KRM \cdot f_{CLK}}{2^{15}}$$

The SMPS runs properly when the bits SET_SMPS_VTUNE and SET_SMPS_PLLBW (see PM_CONFIG[2:0] register bank) are set according to the programmed switching frequency.

Table 22. SMPS configuration settings

SET_SMPS_PLLBW	SET_SMPS_VTUNE	Switching frequency range
0	0	2.0 MHz - 4.5 MHz
0	1	3.5 MHz - 7.0 MHz
1	0	4.5 MHz - 7.5 MHz
1	1	4.5 MHz - 10 MHz

8.2 Power-on-reset (POR)

The power-on-reset circuit generates a reset pulse upon power-up which is used to initialize the entire digital logic. Power-on-reset senses V_{BAT} voltage.

8.3 Low battery indicator

The battery indicator can provide the user with an indication of the battery voltage level.

There are two blocks to detect battery level:

- Brownout with a fixed threshold as defined in *Table 17: Battery indicator and low battery detector*
- Battery level detector with a programmable threshold as defined in *Table 17: Battery indicator and low battery detector*.

Both blocks can be optionally activated to provide the MCU with an early warning of impending power failure. It does not reset the system, but gives the MCU time to prepare for an orderly power-down and provides hardware protection of data stored in the program memory, by preventing write instructions being executed.

The low battery indicator function is available in any of the STS1TX operating modes. As this function requires the internal bias circuit operation, the overall current consumption in STANDBY, SLEEP, and READY modes is increased by 400 µA.

8.4 Voltage reference

This block provides the precise reference voltage needed by the internal circuit.

8.5 Oscillator and RF synthesizer

A crystal connected to XIN and XOUT is used to provide a clock signal to the frequency synthesizer. The allowed clock signal frequency is either 24, 26, 48, or 52 MHz. As an alternative, an external clock signal can be used to feed XIN for proper operation. In this option, XOUT can be left either floating or tied to ground.

Since the digital macro cannot be clocked at that double frequency (48 MHz or 52 MHz), a divided clock is used in this case.

The digital clock divider is enabled by default and must be kept enabled if the crystal is in the (48 - 52) MHz range; if the crystal is in the (24 - 26) MHz range, then the divider must be disabled before starting any TX operation. The safest procedure to disable the divider without any risk of glitches in the digital clock is to switch into STANDBY mode, thereby resetting the bit-field PD_CLKDIV in the XO_RCO_TEST register, and then return to the READY state. Also, the synthesizer reference signal can be divided by 2, setting the bit-field REFDIV in the SYNTH_CONFIG register.

The integrated phase locked loop (PLL) is capable of synthesizing a wide band of frequencies, in particular the bands from 150 to 174 MHz, from 300 to 348 MHz, from 387 to 470 MHz, or from 779 to 956 MHz, the input signal for the PA in the TX chain.

Frequency tolerance and startup times depend on the crystal used, although some tuning of the latter parameter is possible through the GM_CONF field of the ANA_FUNC_CONF registers.

Table 23. Programmability of trans-conductance at startup

GM_CONF[2:0]	Gm at startup [mS]
000	13.2
001	18.2
010	21.5
011	25.6
100	28.8
101	33.9

Table 23. Programmability of trans-conductance at startup (continued)

GM_CONF[2:0]	Gm at startup [mS]
110	38.5
111	43.0

Depending on the RF frequency and channel spacing, a very high accurate crystal or TCXO may be required.

The RF synthesizer implements fractional sigma delta architecture to allow fast settling and narrow channel spacing. It is fully integrated and uses a multi-band VCO to cover the whole frequency range. All internal calibrations are performed automatically.

The PLL output frequency can be configured by programming the SYNT field of the SYNT3, SYNT2, SYNT1, and SYNT0 registers and BS field of the SYNT0 register. The user must configure these registers according to the effective reference frequency in use (24 MHz, 26 MHz, 48 MHz, or 52 MHz). In the latter two cases, the user must enable the frequency divider by 2 for the digital clock, in order to run the digital macro at a lower frequency. The configuration bit for the digital clock divider is inside the XO_RCO_TEST register (default case is divider enabled). In addition, the user can also enable a divider by 2 applied to the reference clock. The configuration bit for the reference clock divider is inside the SYNTH_CONFIG[1] register. The user must select a 3-bit word in order to set the charge pump current according to the LO frequency variations, in order to have a constant loop bandwidth. This can be done by writing the WCP field of the SYNT3 register, according to the following table:

Table 24. CP word look-up

Channel frequency		WCP [2:0]
145.1	147.1	000
147.1	149.1	001
149.1	151.1	010
151.1	153.2	011
153.2	155.2	100
155.2	157.2	101
157.2	159.2	110
159.2	161.1	111
161.3	163.5	000
163.5	165.7	001
165.7	168.0	010
168.0	170.3	011
170.3	172.5	100
172.5	174.8	101
174.8	177.0	110
177.0	179.3	111

Table 24. CP word look-up (continued)

Channel frequency		WCP [2:0]
290.3	294	000
294.3	298.3	001
298.3	302.3	010
302.4	306.4	011
306.4	310.4	100
310.4	314.4	101
314.4	318.4	110
318.4	322.6	111
322.6	327.0	000
327.0	331.4	001
331.4	335.9	010
335.9	340.5	011
340.5	344.9	100
344.9	349.5	101
349.5	353.9	110
353.9	358.5	111
387.0	392.3	000
392.3	397.7	001
397.7	403.0	010
403.0	408.5	011
413.8	419.2	101
419.2	424.6	110
424.6	430.1	111
430.1	436.0	000
436.0	441.9	001
441.9	447.9	010
447.9	454.0	011
454.0	459.9	100
459.9	466.0	101
466.0	471.9	110
471.9	478.0	111
774.0	784.7	000
784.7	795.3	001
795.3	806.0	010
806.0	817.0	011

Table 24. CP word look-up (continued)

Channel frequency		WCP [2:0]
817.0	827.7	100
827.7	838.3	101
838.3	849.2	110
849.2	860.2	111
860.2	872.0	000
872.0	883.8	001
883.8	895.8	010
908.0	919.8	100
919.8	932.0	101
932.0	943.8	110
943.8	956.0	111

The STS1TX is provided with an automatic and very fast calibration procedure for the frequency synthesizer. If not disabled, it is performed each time the SYNTH is required to lock to the programmed RF channel frequency (i.e. from READY to LOCK/TX). Calibration time is 54 µs.

After completion, the calibration word is used automatically by the STS1TX and is stored in the RCO_VCO_CALIBR_OUT[1:0] registers.

In order to get the synthesizer locked when the calibration procedure is not enabled, the correct calibration words to be used must be previously stored in the RCO_VCO_CALIBR_IN[2:0] registers using VCO_CALIBR_TX field.

The advantage of performing an offline calibration is that the LOCK/setting time is roughly 20 µs (using proper VCO_CALIBR_TX register values).

It is recommended to set the T split time to the longest value (3.47 ns) to facilitate the calibrator operation, SEL_TSPLIT field of the register SYNTH_CONFIG[0] (register address 0x9F) at 1.

If calibration is enabled, the LOCK/setting time is approximately 80 µs.

8.6 RCO: features and calibration

The STS1TX contains an ultra low-power RC oscillator capable of generating 34.7 kHz with both 24 MHz and 26 MHz; the RC oscillator frequency is calibrated comparing it to the digital domain clock fCLK divided by 692 or 750, respectively. The configuration bit, called 24_26MHz_SELECT in the ANA_FUNC_CONF register, contains the information of the calibrator regarding the frequency of the crystal under operation. If the digital domain clock is 25 MHz, the setting of the configuration bit 24_26MHz_SELECT will calibrate the low power RC oscillator according to the following table:

Table 25. RC calibrated speed

Digital domain clock	24_26MHz_SELECT	RC calibrated speed
24 MHz	0	34.7 kHz
26 MHz	1	34.7 kHz
25 MHz	0	36.1 kHz
25 MHz	1	33.3 kHz

By default, the calibration is disabled at reset to avoid using an out-of-range reference frequency (for instance, when the XTAL is 26 MHz and the digital divider is active, in fact, by default). After the internal clock divider is correctly configured, the user can enable the RCO calibration in the PROTOCOL[2] register.

The user can replace the internal 34 kHz-signal source with an external one (provided through a GPIO, *Section 10.3*). To enable the usage of the external signal, the user must set the EXT_RCOSC bit in the XO_RCO_CONFIG register. However, the internal calibrator is not automatically disabled from the EXT_RCOSC bit (the user must reset the RCO_CALIBRATION bit in the PROTOCOL[2] register, if previously set).

8.6.1 RC oscillator calibration

RC oscillator calibration is enabled when bit RCO_CALIBRATION is set in the PROTOCOL[2] register (by default the calibration is disabled). The calibration words found by the calibration algorithm are accessible in the RCO_VCO_CALIBR_OUT[1:0] registers (fields RWT_OUT[3:0] and RFB_OUT[4:0],).

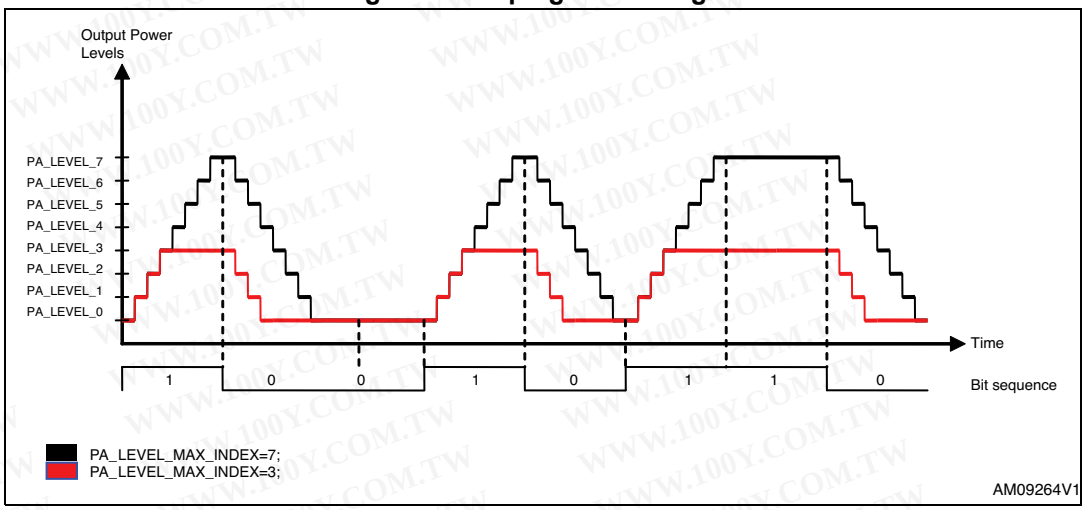
When the calibration is disabled, the frequency of the RC oscillator is set by a couple of configuration words, namely RWT_IN[3:0] and RFB_IN[4:0], in the RCO_VCO_CALIBR_IN[2:0] registers (fields RWT_IN[3:0] and RFB_IN[4:0]). RWT_IN[3:0] can range from 0 up to 13 (decimal value) affecting the raw value of the frequency, while the more accurate and fine control is up to RFB_IN[4:0] (ranging from 1 up to 31).

8.7 Transmitter

The STS1TX contains an integrated PA capable of transmitting at output levels between -30 dBm to +11 dBm. The PA is single-ended and has a dedicated pin (TXOUT). The PA output is ramped up and down to prevent unwanted spectral splatter. In TX mode the PA drives the signal generated by the frequency synthesizer out to the antenna terminal. The output power of the PA is programmable via SPI. Delivered power, as well as harmonic content, depends on the external impedance seen by the PA. To obtain approval on ETSI EN 300 220, it is possible to program TX to send an unmodulated carrier.

The output stage is supplied from the SMPS through an external choke and is loaded with a LC-type network which has the function of transforming the impedance of the antenna and filter out the harmonics.

Figure 6. Shaping of ASK signal



8.8 Temperature sensors (TS)

The STS1TX can provide an analog temperature indication as a voltage level, which is available at the GPIO_0 pin. The voltage level V0 at room temperature (or any other useful reference temperature) should be acquired and stored by the MCU in order to compensate for the offset. The relationship between temperature and voltage is the following:

Equation 1

$$T = 400 \cdot (V_{temp} - V_0) + (T_0 + 3.75) \qquad (°C)$$

where V_0 is the voltage at temperature T_0.

Two output modes are available: buffered or not buffered (high output impedance, about 100 kΩ). The latter mode is the default.

The TS function is available in every operating mode. When enabled, the internal logic allows the switching on of all the necessary circuitry.

To enable the TS function, the user must perform the following operations:

- Set to 1 the TS bit in the ANA_FUNC_CONF[0] register
- Program as “Analog” (00) the GPIO_MODE field in the GPIO0_CONF register (other fields are neglected)
- Optionally, enable the buffered mode (the EN_TS_BUFFER bit in the PM_CONFIG[2] register).

As the TS function requires the internal bias circuit operation, the overall current consumption in STANDBY, SLEEP, and READY modes is increased by 400 µA.

8.9 AES encryption co-processor

The STS1TX provides data security support as it embeds an advanced encryption standard (AES) core which implements a cryptographic algorithm in compliance with NIST FIPS 197.

Three registers are available to use the AES engine of STS1TX:

- AES_KEY_IN [15:0]: R/W type register (128-bit), used to provide the key to use
- AES_DATA_IN [15:0]: R/W type register (128-bit), used to provide the input to the AES engine
- AES_DATA_OUT [15:0]: R type register (128-bit), used to retrieve the output of the AES operation.

The core processes 128-bit data blocks using 128-bit keys.

The AES can be accessed in any of the STS1TX operation modes.

To turn on the AES engine, the AES_ON bit in the ANA_FUNC_CONF[0] register must be set.

Once the AES engine is on, it processes the operations according to the commands sent.

The STS1TX engine provides 4 different operations:

1. Encryption using a given encryption key (AES Enc command). In this operation, the MCU puts the encryption key into the AES_KEY_IN[15:0] register and the data to encrypt into the AES_DATA_IN[15:0]. The MCU sends the AES Enc command and when the AES_EOP (end of operation) is issued, the MCU can retrieve the data encrypted from AES_DATA_OUT[15:0]
2. Decryption key derivation starting from an encryption key (AES Key command). In this operation, the MCU puts the encryption key into AES_DATA_IN[15:0]. The MCU sends the AES Key command and when the AES_EOP (end of operation) is issued, the MCU can retrieve the decryption key from AES_DATA_OUT[15:0]
3. Data decryption using a decryption key (AES Dec command). In this operation, the MCU puts the decryption key into the AES_KEY_IN[15:0] register and the data to decrypt into AES_DATA_IN[15:0]. The MCU sends the AES Dec command and when the AES_EOP (end of operation) is issued, the MCU can retrieve the data decrypted from AES_DATA_OUT[15:0].
4. Data decryption using a decryption key (AES KeyDec command). In this operation, the MCU puts the encryption key into the AES_KEY_IN[15:0] register and the data to decrypt into AES_DATA_IN[15:0]. The MCU sends the AES KeyDec command and when the AES_EOP (end of operation) is issued, the MCU can retrieve the data decrypted from AES_DATA_OUT[15:0].

9 Transmission and reception

9.1 PA configuration

The PA output power level can be configured by programming the PA_POWER[8:0] register bank. The user can store up to eight output levels to provide flexible PA power ramp-up and ramp-down at the start and end of a frequency modulation transmission as well as ASK modulation shaping.

The power levels of the ramp are controlled by 7-bit words (PA_LEVEL_x, x=0 – 7), according to the following table:

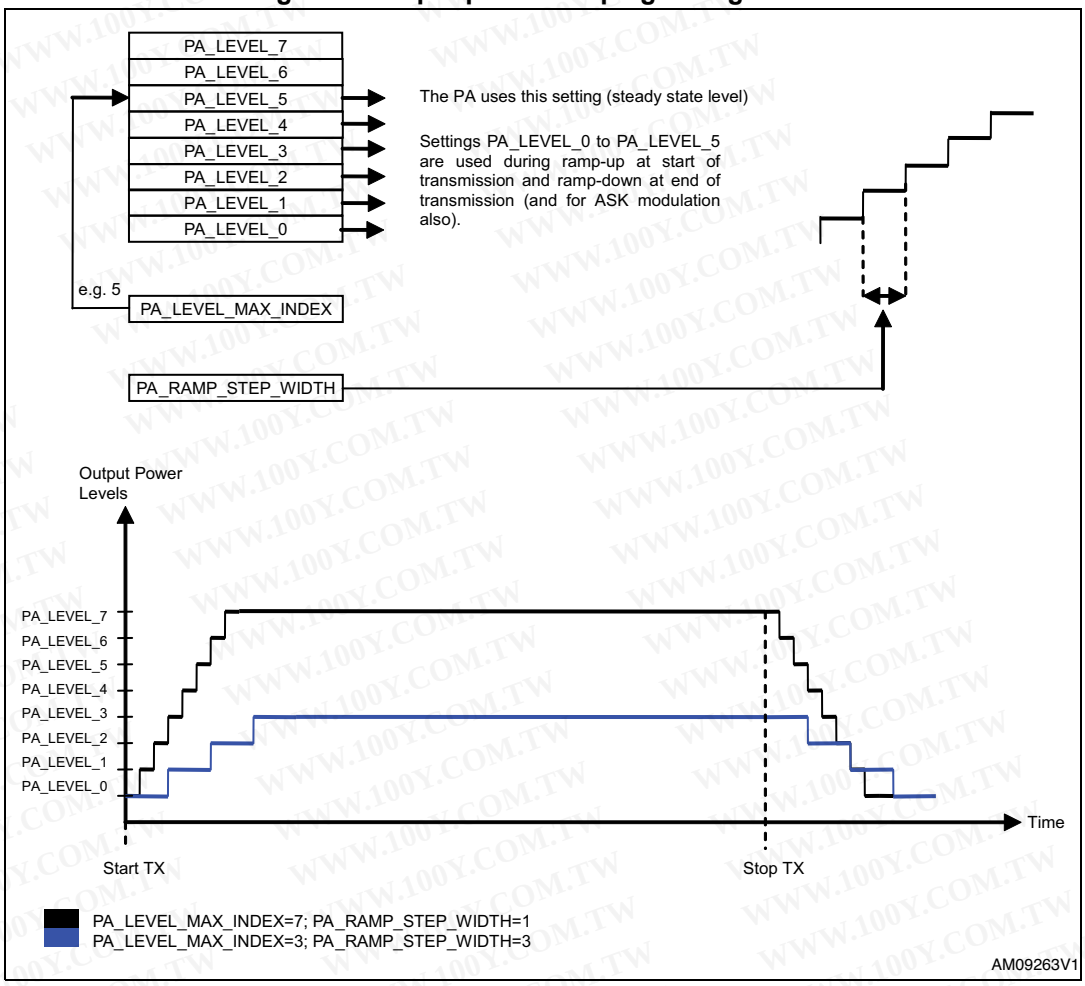
Table 26. PA_level

PA_LEVEL_x	Comment	P_{OUT} [dBm] (170MHz)
0	No output power: output stage in high impedance mode and all circuits switched off.	-
1	Maximum output power	11
…		
30		0
…		
42		-6
…		
90	Minimum level	-34
91-127	Reserved	N/A

The power ramping is enabled by the PA_RAMP_ENABLE bit. If enabled, the ramp starts from the level defined by the word PA_LEVEL_0 and stops at the level defined by the word PA_LEVEL_x, where x is the value of the 3-bit field PA_LEVEL_MAX_INDEX. So, a maximum of 8 steps can be set up. *Figure 7* describes the levels table and shows some examples.

Each step is held for a time interval defined by the 2-bit field PA_RAMP_STEP_WIDTH. The step width is expressed in terms of bit period units ($T_b/8$), maximum value is 3 (which means $4 \times T_b/8 = T_b/2$). Therefore the PA ramp may last up to 4 T_b (about 3.3 ms if the bit rate is 1.2 kbit/s).

Figure 7. Output power ramping configuration



The set of 8 levels is used to shape the ASK signal. In this case, the modulator works as a counter that counts up when transmitting a one and down when transmitting a zero. The counter counts at a rate equal to 8 times the symbol rate (in this case, the field PA_RAMP_STEP_WIDTH is not used). This counter value is used as an index for the lookup in the levels table in *Figure 7* to associate the relevant POUT value. Therefore, in order to utilize the whole table, PA_LEVEL_MAX_INDEX should be 7 when ASK is active. The real shaping of the ASK signal is dependent on the configuration of the PA_LEVEL_x registers. *Figure 7* shows some examples of ASK shaping.

Using the a frequency modulation, the output power is configured by PA_LEVEL_x, with x=PA_LEVEL_MAX_INDEX.

For OOK modulation, the signal is abruptly switched between two levels only, these are PA_LEVEL_0 and PA_LEVEL_x, with x=PA_LEVEL_MAX_INDEX.

The 2-bit CWC field in the PA_POWER register bank can be used to tune the internal capacitive load of the PA (up to 3.6 pF in steps of 1.2 pF) in order to optimize the performance at different frequencies.

The output power are reported in *Table 26: PA_level*.

9.2 RF channel frequency settings

RF channels can be defined using the CHSPACE and CHNUM registers.

The channel center frequency can be programmed as:

Equation 2

$$f_c = f_{base} + f_{offset} + \left(\frac{f_{XO}}{2^{15}} \cdot CHSPACE\right) \cdot CHNUM$$

This allows the setting of up to 256 channels with a programmable raster. The raster granularity is about 793 Hz at 26 MHz and becomes about 1587 Hz at 52 MHz.

The actual channel spacing is from 793 Hz to 202342 Hz in 793 Hz steps for the 26 MHz configuration and from 1587 to 404685 Hz in 1587 Hz steps for the 52 MHz configuration.

The base carrier frequency, i.e. the carrier frequency of channel #0, is controlled by the SYNT0, SYNT1, SYNT2, and SYNT3 registers according to the following formula:

Equation 3

$$f_{base} = \frac{f_{XO}}{\frac{(B * D)}{2}} \cdot \frac{SYNT}{2^{18}}$$

where:

- f_{XO} is the frequency of the XTAL oscillator (typically 24 MHz, 26 MHz, 48 MHz, or 52 MHz)
- SYNT is a programmable 26-bit integer.

Equation 4

$$B = \begin{cases} 6 \text{ for the high band (from 779MHz to 956MHz, BS} = 1) \\ 12 \text{ for the middle band (387MHz to 470MHz, BS} = 3) \\ 16 \text{ for the low band (300MHz to 348MHz, BS} = 4) \\ 32 \text{ for the very low band (169 MHz, BS} = 5) \end{cases}$$

Equation 5

$$D = \begin{cases} 1 \text{ if REFDIV 0 (internal reference divider is disabled)} \\ 2 \text{ if REFDIV 1 (internal reference divider is enabled)} \end{cases}$$

The offset frequency is a correction term which can be set to compensate the crystal inaccuracy after e.g. lab calibration.

Equation 6

$$f_{offset} = \frac{f_{XO}}{2^{18}} \cdot FC\_OFFSET$$

where:

- FC_OFFSET is a 12-bit integer (expressed as 2's complement number) set by the FC_OFFSET[1:0] registers

Furthermore, the selection between VCOH (“high”) and VCOL (“low”) in the frequency synthesizer according to the band selected and the VCO threshold is required.

If the center frequency is below the frequency threshold for that frequency band, the VCO_L must be selected by setting the bit 2 VCO_L_SEL field in the SYNTH_CONFIG register.

If the center frequency is above the frequency threshold for that frequency band, VCO_H must be selected by setting the bit 1 VCO_ H _SEL field in the SYNTH_CONFIG register.

Table 27. Frequency threshold

Frequency threshold for each band (MHz)(1)			
Very low band	Low band	Middle band	High band
161281250	322562500	430083334	860166667

1. By default, the VCO_H is selected.

The user must make sure that actual frequency programming is inside the specified frequency range. The accuracy of the offset is about 99 Hz for the 26 MHz reference and about 198 Hz for the 52 MHz reference.

9.3 Modulation scheme

The following modulation formats are supported: 2-FSK, GFSK, MSK, OOK, and ASK. The actual modulation format used is controlled by the MOD_TYPE field of the MOD0 register:

- MOD_TYPE =
  - 0 (00): 2-FSK
  - 1 (01): GFSK
  - 2 (10): ASK/OOK
  - 3 (11): MSK

In 2-FSK and GFSK modes, the frequency deviation is controlled by the FDEV register according to the following formula:

Equation 7

$$f_{dev} = f_{xo}\frac{\text{floor}((8 + \text{FDEV\_M}) \cdot 2^{\text{FDEV\_E}-1})}{2^{18}}$$

where:

- f_{XO} is the XTAL oscillator frequency (typically 26 MHz or 52 MHz).
- FDEV_M is a 3-bit integer ranging from 0 to 7
- FDEV_E is a 4-bit integer ranging from 0 to 9.

The f_{dev} values obtainable are then:

For f_{XO} = 52 MHz

E/M	0	1	2	3	4	5	6	7
0	793.5	793.5	991.8	991.8	1190.2	1190.2	1388.5	1388.5
1	1586.9	1785.3	1983.6	2182.0	2380.4	2578.7	2777.1	2975.5
2	3173.8	3570.6	3967.3	4364.0	4760.7	5157.5	5554.2	5950.9
3	6347.7	7141.1	7934.6	8728.0	9521.5	10314.9	11108.4	11901.9
4	12695.3	14282.2	15869.1	17456.1	19043.0	20629.9	22216.8	23803.7
5	25390.6	28564.5	31738.3	34912.1	38085.9	41259.8	44433.6	47607.4
6	50781.3	57128.9	63476.6	69824.2	76171.9	82519.5	88867.2	95214.8
7	101562.5	114257.8	126953.1	139648.4	152343.8	165039.1	177734.4	190429.7
8	203125.0	228515.6	253906.3	279296.9	304687.5	330078.1	355468.8	380859.4
9	406250.0	457031.3	507812.5	558593.8	609375.0	660156.3	710937.5	761718.8

For f_{XO} = 26 MHz

E/M	0	1	2	3	4	5	6	7
0	396.7	396.7	495.9	495.9	595.1	595.1	694.3	694.3
1	793.5	892.6	991.8	1091.0	1190.2	1289.4	1388.5	1487.7
2	1586.9	1785.3	1983.6	2182.0	2380.4	2578.7	2777.1	2975.5
3	3173.8	3570.6	3967.3	4364.0	4760.7	5157.5	5554.2	5950.9
4	6347.7	7141.1	7934.6	8728.0	9521.5	10314.9	11108.4	11901.9
5	12695.3	14282.2	15869.1	17456.1	19043.0	20629.9	22216.8	23803.7
6	25390.6	28564.5	31738.3	34912.1	38085.9	41259.8	44433.6	47607.4
7	50781.3	57128.9	63476.6	69824.2	76171.9	82519.5	88867.2	95214.8
8	101562.5	114257.8	126953.1	139648.4	152343.8	165039.1	177734.4	190429.7
9	203125.0	228515.6	253906.3	279296.9	304687.5	330078.1	355468.8	380859.4

With this solution the maximum deviation for the 26 MHz case is limited to about 355 kHz, but this is still acceptable since the maximum useful deviation is about 125 kHz (MSK @ 500 kbps).

In GFSK mode the Gaussian filter BT product can be set to 1 or 0.5 by the field BT_SEL of the MOD0 register.

In MSK mode, the frequency deviation is automatically set to ¼ of the data rate and the content of the FDEV register is ignored.

The calculation done within the modem assumes that the digital clock is equal to the synthesizer reference. Hence, in the 52-MHz case the MSK can actually be configured by setting the frequency deviation to ¼ of the data rate through the FDEV registers as for normal 2-FSK. The same is true for GMSK mode, which can be configured by setting the frequency deviation to ¼ of the data rate through the FDEV registers as for normal GFSK with Gaussian filter BT equal to 1 or 0.5.

OOK and ASK

If MOD_TYPE = 2 and power ramping is enabled, then ASK is used; otherwise, if MOD_TYPE = 2 and power ramping is disabled, then OOK is used.

When OOK is selected, a bit '1' is transmitted with the power specified by PA_POWER[PA_LEVEL_MAX_INDEX], a bit '0' is transmitted with the power specified by PA_POWER[0](normally set to PA off).

When ASK is selected, a bit '1' is transmitted with a power ramp increasing from PA_POWER[0] to PA_POWER[PA_LEVEL_MAX_INDEX], a bit '0' is transmitted with a power ramp decreasing from PA_POWER[PA_LEVEL_MAX_INDEX] to PA_POWER[0]. The duration of each power step is 1/8 of the symbol time.

If more '1's are transmitted consecutively, the PA power remains at PA_POWER[PA_LEVEL_MAX_INDEX] for all '1's following the first one; If more '0's are transmitted consecutively, the PA power remains at PA_POWER[0] for all '0's following the first one.

CW mode

For test and measurement purposes the device can be programmed to generate a continuous wave carrier without any modulation by setting the CW field of the MOD0 register. In transmission, a TXSOURCE like PN9 should be configured to keep the transmitter in TX state for an undefined period of time.

9.3.1 Data rate

The data rate is controlled by the MOD0 and MOD1 registers according to the following formula:

Equation 8

$$DataRate = f_{clk} \cdot \frac{(256 + DATA\_RATE\_M) \cdot 2^{DATARATE\_E}}{2^{28}}$$

where:

- DATARATE_M is an 8-bit integer ranging from 0 to 255
- DATARATE_E is a 4-bit integer ranging from 0 to 15
- f_{clk} is the digital clock frequency (typically 26 MHz).

The minimum data rate at f_{clk} = 26 MHz is about 25 Hz; the maximum data rate is about 1.6 MHz. Be advised that performance for such values is not guaranteed.

9.4 Data coding and integrity check process

9.4.1 FEC

The device provides hardware support for error correction and detection.

Error correction can be either enabled or disabled according to link reliability and power consumption needs. Convolutional coding with a rate=½ and k=4 is applied on the payload and CRC before transmission (poly [13,17]).

To further improve error correction performance, a data interleaver is used when convolutional coding is enabled. Data interleaving/de-interleaving is performed using a 4x4-bit matrix interleaver.

To fill the entire matrix, at least 2 bytes of data payload are required (16 cells). In the interleaver matrix, the encoded data bits are written along the rows and the sequence to send to the modulator is obtained by reading the matrix elements along the columns of the matrix. Due to the size of the matrix, the overall data transmitted must be an exact integer multiple of two, to fill the rows and columns of the matrix. If necessary, the framer is able to add automatically extra bytes at the end of the packet, so the number of bytes is an number.

FEC and interleaving are enabled/disabled together.

To enable FEC/INTERL, the field FEC_EN of PCKTCTRL1 must be set to ‘1’. When FEC/INTERL is enabled, the number of transmitted bits is roughly doubled, hence the on-air packet duration in time is roughly doubled as well. The data rate specified in *Section 9.3.1* always applies to the on-air transmitted data.

A termination byte is automatically appended to set the encoder to the 0-state at the end of the packet.

9.4.2 CRC

Error detection is implemented by means of cyclic redundancy check codes.

The length of the checksum is programmable to 8, 16, or 24 bits.

The CRC can be added at the end of the packet by the field CRC_MODE of the register PCKCTRL1.

The following standard CRC polynomials can be selected:

- CRC mode = 1, 8 bits: the poly is (0x07) X^8+X^2+X+1
- CRC mode = 2, 16 bits: the poly is (0x8005) $X^{16}+X^{15}+X^2+1$
- CRC mode = 3, 16 bits: the poly is (0x1021) $X^{16}+X^{12}+X^5+1$
- CRC mode = 4, 24 bits: the poly is (0x864CFB) $X^{24}+X^{23}+X^{18}+X^{17}+X^{14}+X^{11}+X^{10}+X^7+X^6+X^5+X^4+X^3+X+1$
- CRC is calculated over all fields excluding preamble and SYNC word.

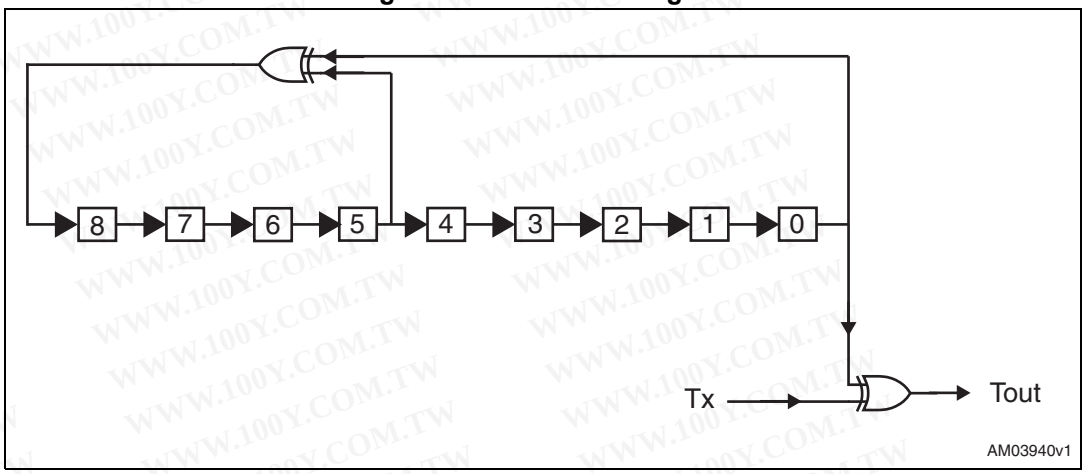
9.4.3 Data whitening

To prevent short repeating sequences (e.g., runs of 0’s or 1’s) that create spectral lines, which may complicate symbol tracking at the receiver or interfere with other transmissions, the device implements a data whitening feature. Data whitening can be optionally enabled by setting the filed WHIT_EN of the PCKTCTRL1 register to '1'. Data whitening is implemented by a maximum length LFSR generating a pseudo-random binary sequence used to XOR data before entering the encoding chain. The length of the LSFR is set to 9 bits. The pseudo-random sequence is initialized to all 1's.

Data whitening, if enabled, is applied on all fields excluding the preamble and the SYNC words.

Whitening is applied according to the following LFSR implementation:

Figure 8. LFSR block diagram



It is recommended to always enable data whitening.

9.4.4 Data padding

If FEC is enabled then the total length of payload and CRC must be an even number (in order to completely fill up the interleaver). If not, a proper filling byte is automatically inserted in transmission and removed by the receiver. The total packet length is affected, and it is configured automatically enabling the FEC.

9.5 Packet handler engine

Before on-the-air transmission, raw data is properly cast into a packet structure. The STS1TX offers a highly flexible and fully programmable packet; the structure of the packet, the number, the type, and the dimension of the fields inside the packet depend on one of the possible configuration settings. Through a suitable register the user can choose the packet configuration from three options: STack, WM-Bus, and Basic.

The current packet format is set by the PCK_FRMT field of the PCKTCTRL3 register. In particular:

- 0 Basic packet format
- 2 MBUS packet format
- 3 STack packet format.

The general packet parameters which can be set by the user are listed and described hereafter. Some particular restrictions are possible depending on the selected packet format.

9.5.1 STack packet

1-32	1-4	0-16 bit	1	1	0-4	2 bit	1 bit	0-65535	0-3
Preamble	Sync	Length	Dest. address	Source address	Control	Seq. No.	NO_ACK	Payload	CRC

Preamble (programmable field): the length of the preamble is programmable from 1 to 32 bytes by the PREAMBLE_LENGTH field of the PCKTCTRL2 register. Each preamble byte is a '10101010' binary sequence.

Sync (programmable field): the length of the synchronization field is programmable (from 1 to 4 bytes) through dedicated registers. The SYNC word is programmable through registers SYNC1, SYNC2, SYNC3, and SYNC4. If the programmed sync length is 1 then only the SYNC1 word is transmitted; if the programmed sync length is 2 then only SYNC1 and SYNC2 words are transmitted and so on.

Length (programmable/optional field): the packet length field is an optional field that is defined as the cumulative length of Address (2 bytes always), Control, and Payload fields. It is possible to support fixed and variable packet length. In fixed mode, the field length is not used.

Destination address (programmable/optional field): is filled with the value of register TX_DEST_ADDR.

Source address (programmable field): is filled with the value of register TX_SOURCE_ADDR. The field ADDRESS_LEN of the PCKTCTRL4 register must be set always to 2.

Control (programmable/optional field): is programmable from 0 to 4 bytes through the CONTROL_LEN field of the PCKTCTRL4 register. Control fields of the packet can be set using the TX_CTRL_FIELD[3:0] register.

Sequence number (programmable field): is a 2-bit field and contains the sequence number of the transmitted packet. It is incremented automatically every time a new packet is transmitted. It can be re-loaded with the value in the TX_SEQ_NUM_RELOAD[1:0] field of the PROTOCOL[2] register, by using the SEQUENCE_UPDATE command.

NO_ACK (programmable field): It is programmed by the bit field NACK_TX of the register PROTOCOL[0]. It is important set to 0 the bit field in the others packet formats.

Payload (programmable/optional field): the device supports both fixed and variable payload length transmission from 0 to 65535 bytes.

On the transmitter, the payload length is always set as: PCKTLEN1 × 256 + PCKTLEN0.

In variable length mode, the width of the binary field transmitted, where the actual length of payload is written, can be configured through the field LEN_WIDTH of the PCKTCTRL3 register according to the maximum length expected in the specific application.

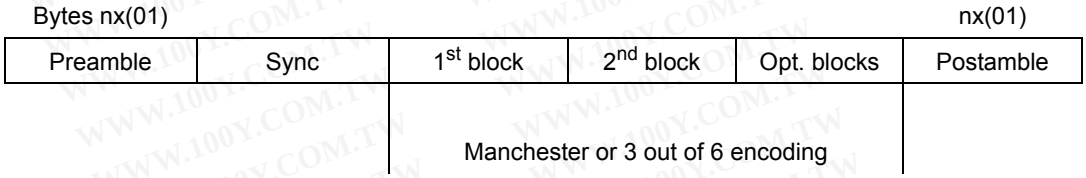
Example 1

- If the variable payload length is from 0 to 31 bytes, then LEN_WIDTH = 5
- If the variable payload length is from 0 to 255 bytes, then LEN_WIDTH = 8
- If the variable payload length is from 0 to 65535 bytes, then LEN_WIDTH = 16.

CRC (programmable/optional field): There are different polynomials CRC: 8 bits, 16 bits (2 polynomials are available) and 24 bits.

9.5.2 Wireless M-Bus packet (W M-BUS, EN13757-4)

The WM-BUS packet structure is shown in the figure below (refer to EN13757 for details about sub-mode specific radio setting).



The preamble consists of a number of chip sequences '01' whose length depends on the chosen sub-mode according to EN13757-4. The length can be programmed using the MBUS_PRMBL_CTRL, from a minimum to a maximum dictated from the standard specification.

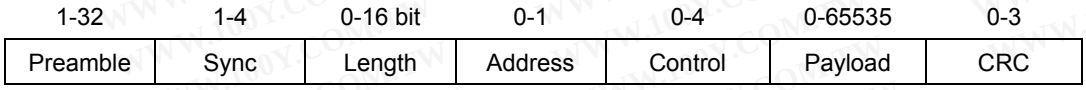
1st block, 2nd block, and optional blocks: can be defined by the user. The packet handler engine uses the Manchester or the “3 out of 6” encoding for all the blocks according to the defined sub-mode.

The postamble consists of a number of chip sequences '01' whose length depends on the chosen sub-mode according to EN13757-4. The length can be programmed using the MBUS_PSTMBL_CTRL, from a minimum to a maximum dictated from the standard specification.

The sub-mode can be chosen setting the MBUS_SUBMODE[2:0] field of the MBUS_CTRL register. There are 5 possible cases:

- Submode S1, S2 (long header) (MBUS_SUBMODE=0):
  - Header length = MBUS_PRMBL_CTRL + 279 (in '01' bit pairs)
  - Sync word = 0x7696 (length 18 bits)
- Submode S1-m, S2, T2 (other to meter) (MBUS_SUBMODE =1):
  - Header length = MBUS_PRMBL_CTRL + 15 (in '01' bit pairs)
  - Sync word = 0x7696 (length 18 bits)
- Submode T1, T2 (meter to other) (MBUS_SUBMODE =3):
  - Header length = MBUS_PRMBL_CTRL + 19 (in '01' bit pairs)
  - Sync word = 0x3D (length 10 bits)
- Submode R2, short header (MBUS_SUBMODE =5):
  - Header length = MBUS_PRMBL_CTRL + 39 (in '01' bit pairs)
  - Sync word = 0x7696 (length 18 bits).
- Submode N1, N2, short header:
  - Header length = 8 (in '01' bit pairs)
  - Sync word = 0xF68D (length 18 bits).

9.5.3 Basic packet



Preamble (programmable field): the length of the preamble is programmable from 1 to 32 bytes by the PREAMBLE_LENGTH field of the PCKTCTRL2 register. Each preamble byte is a '10101010' binary sequence.

Sync (programmable field): the length of the synchronization field is programmable (from 1 to 4 bytes) through dedicated registers. The SYNC word is programmable through registers SYNC1, SYNC2, SYNC3, and SYNC4. If the programmed sync length is 1, then only SYNC word is transmitted; if the programmed sync length is 2 then only SYNC1 and SYNC2 words are transmitted and so on.

Length (programmable/optional field): the packet length field is an optional field that is defined as the cumulative length of Address, Control, and Payload fields. It is possible to support fixed and variable packet length. In fixed mode, the field length is not used.

Destination address (programmable/optional field): is filled with the value of register TX_DEST_ADDR.

Control (programmable/optional field): is programmable from 0 to 4 bytes through the CONTROL_LEN field of the PCKTCTRL4 register. Control fields of the packet can be set using the TX_CTRL_FIELD[3:0] register.

Payload (programmable/optional field): the device supports both fixed and variable payload length transmission from 0 to 65535 bytes.

On the transmitter, the payload length is always set as: PCKTLEN1 × 256 + PCKTLEN0.

On the receiver, if the field FIX_VAR_LEN of PCKTCTRL2 register is set to 1, the payload length is directly extracted from the received packet itself; if FIX_VAR_LEN is set to 0, the payload length is controlled by the PCKTLEN0 and PCKTLEN1 registers as the transmitter.

Furthermore, in variable length mode, the width of the binary field transmitted, where the actual length of payload is written, must be configured through the field LEN_WIDTH of the PCKTCTRL3 register according to the maximum length expected in the specific application.

Example 1

- If the variable payload length is from 0 to 31 bytes, then LEN_WIDTH = 5
- If the variable payload length is from 0 to 255 bytes, then LEN_WIDTH = 8
- If the variable payload length is from 0 to 65535 bytes, then LEN_WIDTH = 16.

CRC (programmable/optional field): There are different polynomials CRC: 8 bits, 16 bits (2 polynomials are available) and 24 bits.

9.6 Data modes

Direct modes are primarily intended to completely bypass all the framer/deframer operations, in order to give the user maximum flexibility in the choice of frame formats, controlled by the field TXSOURCE of the PCKTCTRL1 register. In particular:

TXSOURCE =

- 0 - normal modes
- 1 - direct through FIFO: the packet is written in TX FIFO. The user build the packet according to his need including preamble, payload and soon on. The data are transmitted without any processing.
- 2 - direct through GPIO: the packet bits are continuously read from one of the GPIO pins, properly configured, and transmitted without any processing. To allow the

synchronization of an external data source, a data clock signal is also provided on one of the GPIO pins. Data are sampled by the device on the rising edge of such clock signal; it is the responsibility of the external data source to provide a stable input at this edge.

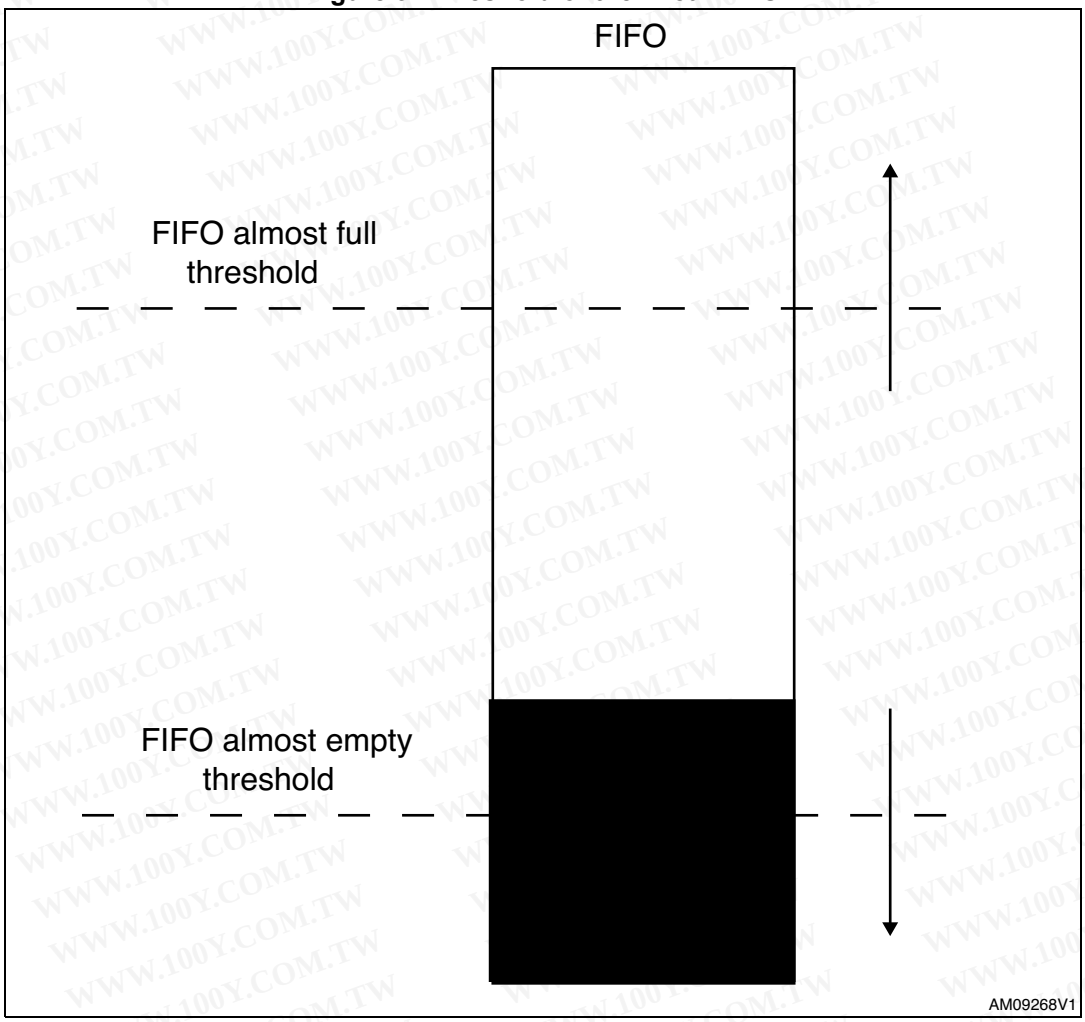
- 3 - PN9 mode: a pseudo-random binary sequence is generated internally. This mode is provided for test purposes only.

9.7 Data FIFO

In the STS1TX there is a TX FIFO for data to be transmitted, which is 96 bytes in length.

The SPI interface is used to write to the TX FIFO (see *Figure 9*) starting from the address 0xFF.

Figure 9. Threshold of the linear FIFO



The FIFO has two programmable thresholds: FIFO almost full and FIFO almost empty.

The FIFO almost full event occurs when the data crosses the threshold from below to above. The TX FIFO almost empty threshold can be configured using the field TXAETHR in the FIFO_CONFIG[0] register.

The FIFO almost empty event occurs when the data crosses the threshold from above to below. The TX FIFO almost full threshold can be configured using the field TXAFTHR in the FIFO_CONFIG[1] register.

Another event occurs when the FIFO goes into overflow or underflow.

The overflow happens when the data in the FIFO are more than 96 bytes. The underflow happens when the STS1TX accesses the FIFO locations to read data, but there is no data present.

For example:

- If it sends more data than the actual number of bytes in the TX FIFO, the TX FIFO underflow/overflow error occurs for an underflow event.
- If it writes more than 96 bytes in the TX FIFO, a TX FIFO underflow/overflow error occurs for an overflow event.

An easy way to clean the FIFOs is to use the flush command: FLUSHTXFIFO

The write TX FIFO operation needs an extra SPI transaction to write correctly the last byte into the TX FIFO. Usually, this last SPI transaction is generated from the TX command sent to transmit the data, otherwise a dummy SPI transaction must be done.

Using the auto-retransmission feature of the STS1TX (packet format STack), if the packet is more than 96 bytes, the packet must be reloaded into the TX FIFO by the MCU. However, if the payload is 96 bytes or less, the STS1TX handles the payload and it is not necessary to reload the data into the TX FIFO at each retransmission.

9.8 Frequency hopping

In order to ensure good link reliability in an interference corrupted scenario, the device supports frequency hopping, managed by the MCU; in particular, the STS1TX supports slow frequency hopping, meaning that the systems change frequency at a rate slower than the information rate.

Depending on the desired blanking interval (the time during a hop), frequency hopping can be done by performing the complete PLL calibration for each channel hop, or reading in the suitable register calibration data calculated at startup and stored in the non-volatile memory of the MCU. The former solution gives a long blanking interval but is more robust compared with supply voltage and temperature variation. The latter provides a shorter blanking time but is sensitive to voltage and temperature variation and requires memory space to store calibration data for each channel involved in hopping.

10 MCU interface

Communication with the MCU goes through a standard 4-wire SPI interface and 4 GPIOs. The device is able to provide a system clock signal to the MCU.

MCU performs the following operations:

- Program the STS1TX in different operating modes by sending commands
- Read and write buffered data, and status information from the SPI
- Get interrupt requests from the GPIO pins
- Apply external signals to the GPIO pins

10.1 Serial peripheral interface

The STS1TX is configured by a 4-wire SPI-compatible interface (CSn, SCLK, MOSI, and MISO). More specifically:

- CSn: chip select, active low
- SCLK: bit clock
- MOSI: data from MCU to STS1TX (STS1TX is the slave)
- MISO: data from STS1TX to MCU (MCU is the master).

As the MCU is the master, it always drives the CSn and SCLK. According to the active SCLK polarity and phase, the STS1TX SPI can be classified as mode 1 (CPOL=0, CPHA=0), which means that the base value of SCLK is zero, data are read on the clock's rising edge and data are changed on the clock's falling edge. The MISO is in tri-state mode when CSn is high. All transfers are done most significant bit first.

The SPI can be used to perform the following operations:

- Write data (to registers or FIFO queue)
- Read data (from registers or FIFO queue)
- Write commands.

The SPI communication is supported in all the active states, and also during the low power state: STANDBY and SLEEP (see *Table 18: States*).

When accessing the SPI interface, the two status bytes of the MC_STATE[1:0] registers are sent to the MISO pin. The timing diagrams of the three operations above are reported below.

Figure 10. SPI “write” operation

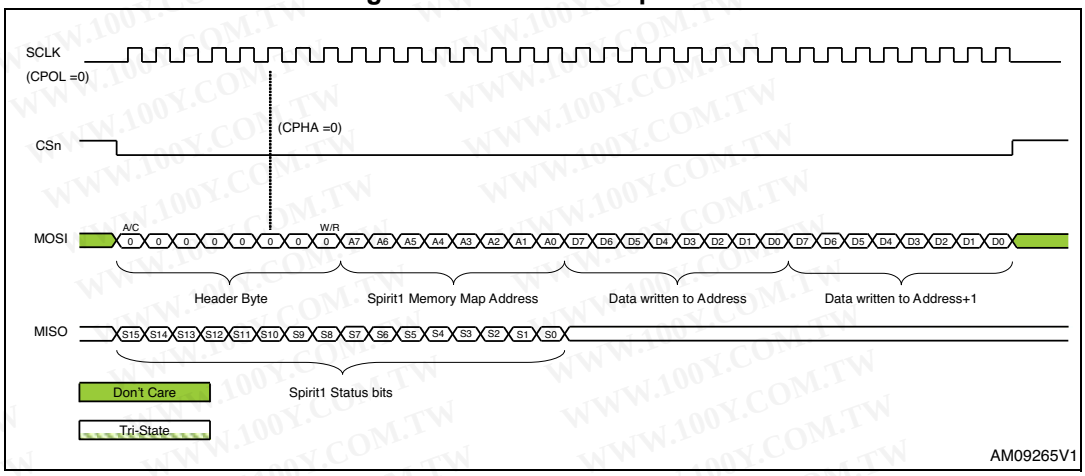


Figure 11. SPI “read” operation

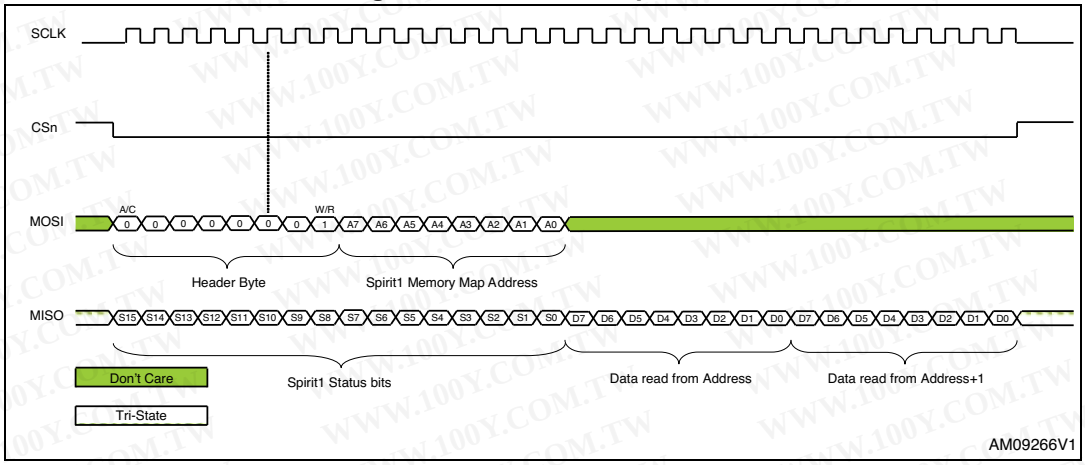
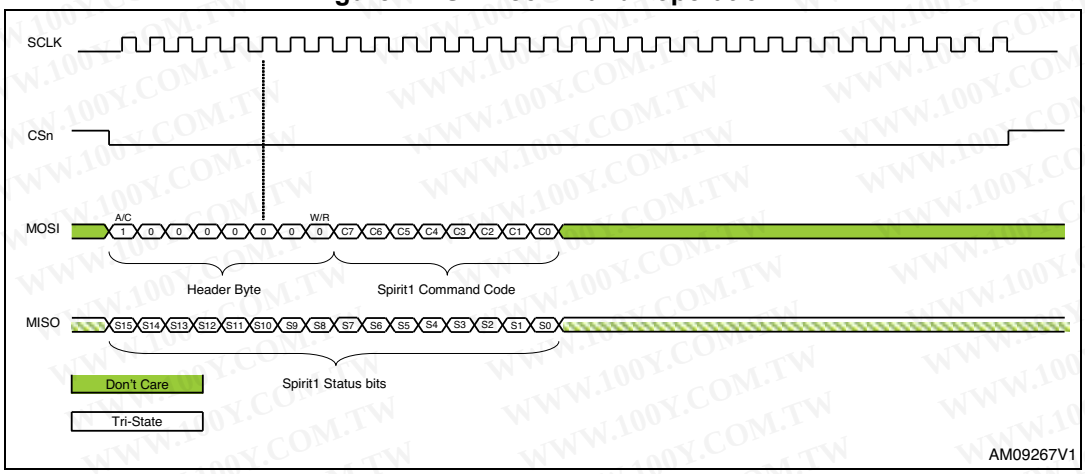


Figure 12. SPI “command” operation



Concerning the first byte, the MSB is an A/C bit (Address/Commands: 0 indicates that the following byte is an address, 1 indicates that the following byte is a command code), while the LSB is a W/R bit (Write/Read: 1 indicates a read operation). All other bits must be zero.

Read and write operations are persistently executed while CSn is kept active (low), the address being automatically incremented (burst mode).

Accessing the FIFO is done as usual with the read and write commands, by putting, as the address, the code 0xFF. Burst mode is available to access the sequence of bytes in the FIFO. Clearly, TX-FIFO with a write operation.

Details of the SPI parameters are reported below.

Table 28. SPI interface timing requirements

Symbol	Parameter	Min.	Max.	Unit
f_{SCLK}	SCLK frequency		10	MHz
t_{sp}	CSn low to positive edge on SCLK	2		µs

10.2 Interrupts

In order to notify the MCU of a certain number of events an interrupt signal is generated on a selectable GPIO. The following events trigger an interrupt to the MCU:

Table 29. Interrupts

Bit	Events group	Interrupt event
0	Packet oriented	Not used
1		Not used
2		TX data sent
3		Not used
4		Not used
5		TX FIFO underflow/overflow error
6		Not used
7		TX FIFO almost full
8		TX FIFO almost empty
9		Not used
10		Not used
11		Not used
12	Signal quality related	Not used
13		Not used
14		Not used

Table 29. Interrupts (continued)

Bit	Events group	Interrupt event
15	Device status related	Not used
16		READY(1)
17		STANDBY state switching in progress
18		Low battery level
19		Power-on reset
20		Brownout event
21		LOCK
29	Others	Not used
30		AES end–of–operation

1. The interrupt flag n.16 is set each time the STS1TX goes to READY state and the XO has completed its setting transient (XO ready condition detected).

All interrupts are reported on a set of interrupt status registers and are individually maskable. The interrupt status register must be cleared upon a read event from the MCU.

The status of all the interrupts is reported on the IRQ_STATUS[3:0] registers: bits are high for the events that have generated any interrupts. The interrupts are individually maskable using the IRQ_MASK[3:0] registers: if the mask bit related to a particular event is programmed at 0, that event does not generate any interrupt request.

10.3 GPIOs

The total number of GPIO pins is 4. Each pin is individually configurable.

Digital outputs can be selected from the following (see GPIOx_CONF register):

Table 30. Digital outputs

I/O selection	Output signal
0	nIRQ (interrupt request, active low)
1	POR inverted (active low)
2	Wakeup timer expiration: ‘1’ when WUT has expired
3	Low battery detection: ‘1’ when battery is below threshold setting
4	TX data internal clock output (TX data are sampled on the rising edge of it)
5	TX state indication: ‘1’ when the STS1TX is transiting in the TX state
6	TX FIFO almost empty flag
7	TX FIFO almost full flag
8	Not used
9	Not used
10	Not used

Table 30. Digital outputs (continued)

I/O selection	Output signal
11	Not used
12	Not used
13	Not used
14	Not used
15	Not used
16	Not used
17	Not used
18	TX mode indicator (to enable an external range extender)
19	VDD (to emulate an additional GPIO of the MCU, programmable by SPI)
20	GND (to emulate an additional GPIO of the MCU, programmable by SPI)
21	External SMPS enable signal (active high)
22	Device in SLEEP or STANDBY states
23	Device in READY state
24	Device in LOCK state
25	Device waiting for a high level of the lock-detector output signal
26	Device waiting for timer expiration before starting to sample the lock-detector output signal
27	Device waiting for a high level of the READY2 signal from XO
28	Device waiting for timer expiration to allow PM block settling
29	Device waiting for end of VCO calibration
30	Device enables the full circuitry of the SYNTH block
31	Device waiting for a high level of the RCCAL_OK signal from the RCO calibrator

All interrupts are reported on a set of interrupt status registers and are individually maskable. The interrupt status register must be cleared upon a read event from the MCU.

The status of all the interrupts is reported on the IRQ_STATUS[3:0] registers: bits are high for the events that have generated any interrupts. The interrupts are individually maskable using the IRQ_MASK[3:0] registers: if the mask bit related to a particular event is programmed at 0, that event does not generate any interrupt request.

Digital inputs can be selected from the following (see GPIOx_CONF register):

Table 31. Digital inputs

I/O selection	Input signal
0	1 >> TX command
1	Not used
2	TX data input for direct modulation

Table 31. Digital inputs (continued)

I/O selection	Input signal
3	Wakeup from external input (sensor output)
4	External clock @ 34.7 kHz (used for LDC modes timing)
From 5 to 31	Not used

The only available analog output is the temperature sensor, see *Section 8.8*.

10.4 MCU clock

The STS1TX can directly provide the system clock to the MCU in order to avoid the need for an additional crystal. The clock signals for the MCU can be available on the GPIO pins. The source oscillator can be the internal RCO or the XO depending on the active state. When XO is active, it is the source clock (the RCO is not available in this condition).

In addition, different ratios are available and programmable through the MCU_CK_CONF configuration register, as described in *Table 32*.

Table 32. MCU_CK_CONF configuration register

MCU_CK_CONF[4:0]		Clock source	Division ratio
XO_RATIO	RCO_RATIO		
Don’t care	0	RCO	1
	1		1/128
0	Don’t care	XO	1
1			2/3
2			1/2
3			1/3
4			1/4
5			1/6
6			1/8
7			1/12
8			1/16
9			1/24
10			1/36
11			1/48
12			1/64
13			1/96
14			1/128
15			1/192

In STANDBY state, no oscillator is available as the clock source. In order to allow the MCU to better handle this event, and avoid a potential dead state situation, a dedicated procedure is forecast when the STS1TX enters STANDBY state. A few extra clock cycles can be provided to the MCU before actually stopping the clock (an interrupt is generated to notify the MCU of this event).

The number of extra cycles can be programmed through the MCU_CK_CONF configuration register to 0, 64, 256, or 512. The MCU can make use of these cycles to prepare to standby or to switch on any auxiliary clock generator. The maximum transition time from READY to STANDBY is then:

Equation 9

$$\Delta T_{READY\ STANDBY} = \frac{1}{f_{clk}} \cdot \frac{512}{1/192} = \frac{98304}{f_{clk}}$$

where f_{clk} is the digital clock frequency (typically 26 MHz).

The transition to SLEEP state causes the MCU clock source to change from XO to RCO. Similarly, when the STS1TX exits SLEEP to any active state, the source is the XO. Both these transitions are implemented in order to be glitch-free. This is guaranteed by synchronizing both transitions, switching on the rising or falling edge of the RCO clock.

The clock provided to the MCU depends on the current state:

Table 33. MCU clock vs. state

State	Source oscillator	MCU clock
SHUTDOWN	N/A	N/A
STANDBY	N/A	Tail
SLEEP	RC Osc	RC/1 or RC/128
READY TUNING TX	XTAL	XTAL/N

11 Register table

This section describes all the registers used to configure the STS1TX. The description is structured in sections according to the register usage.

STS1TX has three types of registers:

- Read and write (R/W), which can be completely managed by SPI using READ and WRITE operations
- Read-only (R)
- Read-and-reset (RR), is automatically cleared after a READ operation.

A further category of special registers collects the ones which cannot be categorized in any of the three mentioned above R/W, R, or RR.

The fields named as “Reserved” must not be overridden by the user. Otherwise, behavior is not guaranteed.

The memory map is shown in the following table:

Table 34. General configuration registers

Register	Address	Bit	Field name	Reset	R/W	Description
ANA_FUNC_CONF[1]	0x00	7:5	Reserved	000	R/W	
		4:2	GM_CONF[2:0]	011		Sets the driver gm of the XO at startup
		1:0	SET_BLD_LVL[1:0]	00		Sets the BLD threshold 00: 2.7 V 01: 2.5 V 10: 2.3 V 11: 2.1 V

Table 34. General configuration registers (continued)

Register	Address	Bit	Field name	Reset	R/W	Description
ANA_FUNC_CONF[0]	0x01	7	Reserved	1	R/W	
		6	24_26MHz_SELECT	1		1: 26 MHz configuration 0: 24 MHz configuration (impact only RCO calibration reference and loop filter tuning)
		5	AES_ON	0		1: AES engine enabled
		4	EXT_REF	0		0: reference signal from XO circuit 1: reference signal from XIN pin
		3	Reserved	0		
		2	BROWN_OUT	0		1: enables accurate brownout detection
		1	BATTERY_LEVEL	0		1: enables battery level detector circuit
		0	TS	0		1: enables the “temperature sensor” function
GPIO3_CONF	0x02	7:3	GPIO_SELECT[4:0]	10100	R/W	GPIO3 configuration (default: digital GND)
		2	Reserved	0		
		1:0	GPIO_MODE[1:0]	10		GPIO3 mode: 01b: digital input 10b: digital output low power 11b: digital output high power (default: digital output low power)
GPIO2_CONF	0x03	7:3	GPIO_SELECT[4:0]	10100	R/W	GPIO2 configuration (default: digital GND)
		2	Reserved	0		
		1:0	GPIO_MODE	10		GPIO2 mode: 01b: digital input 10b: digital output low power 11b: digital output high power (default: digital output low power)

Table 34. General configuration registers (continued)

Register	Address	Bit	Field name	Reset	R/W	Description
GPIO1_CONF	0x04	7:3	GPIO_SELECT[4:0]	10100	R/W	GPIO1 configuration (default: digital GND)
		2	Reserved	0		
		1:0	GPIO_MODE	10		GPIO1 mode: 01b: digital input 10b: digital output low power 11b: digital output high power (default: digital output low power)
GPIO0_CONF	0x05	7:3	GPIO_SELECT[4:0]	00001	R/W	GPIO0 configuration (default: power-on reset signal)
		2	Reserved	0		
		1:0	GPIO_MODE	10		GPIO0 mode: 00b: analog 01b: digital input 10b: digital output low power 11b: digital output high power (default: digital output low power)
MCU_CK_CONF	0x06	7	EN_MCU_CLK	0	R/W	1: The internal divider logic is running, so the MCU clock is available (but proper GPIO configuration is needed)
		6:5	CLOCK_TAIL[1:0]	0		Number of extra clock cycles provided to the MCU before switching to STANDBY state: 00: 0 extra clock cycle 01: 64 extra clock cycles 10: 256 extra clock cycles 11: 512 extra clock cycles
		4:1	XO_RATIO[3:0]	0		Divider for the XO clock output
		0	RCO_RATIO	0		Divider for the RCO clock output 0: 1 1: 1/128
XO_RCO_TEST	0xB4	7:4	Reserved	0010		
		3	PD_CLKDIV	0		1: disable both dividers of the digital clock (and reference clock for the SMPS) and IF-ADC clock.
		2:0	Reserved	001		

Table 34. General configuration registers (continued)

Register	Address	Bit	Field name	Reset	R/W	Description
SYNTH_CONFIG[0]	0x9F	7	SEL_TSPLIT	0	R/W	0: split time: 1.75 ns 1: split time: 3.47 ns
		6:0	Reserved	0100000		
SYNTH_CONFIG[1]	0x9E	7	REFDIV	0	R/W	Enable division by 2 on the reference clock: 0: $f_{REF} = f_{XO}$ frequency 1: $f_{REF} = f_{XO}$ frequency / 2
		6:3	Reserved	1011		
		2	VCO_L_SEL	0		1: enable VCO_L
		1	VCO_H_SEL	1		1: enable VCO_H
		0	Reserved	1		

Table 35. Radio configuration registers (analog blocks)

Register name	Address	Bit	Field Name	Reset	R/W	Description
SYNT3	0x08	7:5	WCP[2:0]	000	R/W	Set the charge pump current according to the VCO frequency. See *Table 24*.
		4:0	SYNT[25:21]	01100		SYNT[25:21], highest 5 bits of the PLL programmable divider The valid range depends on f_{XO} and REFDIV settings; for f_{XO}=26MHz. See *Equation 2*
SYNT2	0x09	7:0	SYNT[20:13]	0x84	R/W	SYNT[20:13], intermediate bits of the PLL programmable divider. See *Equation 2*
SYNT1	0x0A	7:0	SYNT[12:5]	0xEC	R/W	SYNT[12:5], intermediate bits of the PLL programmable divider. See *Equation 2*
SYNT0	0x0B	7:3	SYNT[4:0]	01010	R/W	SYNT[4:0], lowest bits of the PLL programmable divider. See *Equation 2*
		2:0	BS	001	R/W	Synthesizer band select. This parameter selects the out-of-loop divide factor of the synthesizer (B in *Equation 2*). 1: 6 Band select factor for high band 3: 12 Band select factor for middle band 4: 16 Band select factor for low band 5: 32 Band select factor for very low band

Table 35. Radio configuration registers (analog blocks) (continued)

Register name	Address	Bit	Field Name	Reset	R/W	Description
CHSPACE	0x0C	7:0	CH_SPACING	0xFC	R/W	Channel spacing in steps of $f_{XO}/2^{15}$ (~793 for f_{XO} = 26 MHz, ~732 for f_{XO} = 24 MHz).
FC_OFFSET[1]	0x0E	7:4	Reserved	0	R/W	Carrier offset in steps of $f_{XO}/2^{18}$ and represented as 12 bits 2-complement integer. It is added / subtracted to the carrier frequency set by the SYNTx register. This register can be used to set a fixed correction value obtained e.g. from crystal measurements.
		3:0	FC_OFFSET[11:8]	0		
FC_OFFSET[0]	0x0F	7:0	FC_OFFSET[7:0]	0	R/W	
PA_POWER[8]	0x10	7	Reserved	0	R/W	Output power level for 8th slot (+12 dBm)
		6:0	PA_LEVEL_7	0000011		
PA_POWER[7]	0x11	7	Reserved	0	R/W	Output power level for 7th slot (+6 dBm)
		6:0	PA_LEVEL_6	0001110		
PA_POWER[6]	0x12	7	Reserved	0	R/W	Output power level for 6th slot (0 dBm)
		6:0	PA_LEVEL_5	0011010		
PA_POWER[5]	0x13	7	Reserved	0	R/W	Output power level for 5th slot (-6 dBm)
		6:0	PA_LEVEL_4	0100101		
PA_POWER[4]	0x14	7	Reserved	0	R/W	Output power level for 4th slot (-12 dBm)
		6:0	PA_LEVEL_3	0110101		
PA_POWER[3]	0x15	7	Reserved	0	R/W	Output power level for 3rd slot (-18 dBm)
		6:0	PA_LEVEL_2	1000000		
PA_POWER[2]	0x16	7	Reserved	0	R/W	Output power level for 2nd slot (-24 dBm)
		6:0	PA_LEVEL_1	1001110		
PA_POWER[1]	0x17	7	Reserved	0	R/W	Output power level for first slot (-30 dBm)
		6:0	PA_LEVEL_0	0000000		

Table 35. Radio configuration registers (analog blocks) (continued)

Register name	Address	Bit	Field Name	Reset	R/W	Description
PA_POWER[0]	0x18	7:6	CWC[1:0]	00	R/W	Output stage additional load capacitors bank (to be used to optimize the PA for different sub-bands): 00: 0 pF 01: 1.2 pF 10: 2.4 pF 11: 3.6 pF
		5	PA_RAMP_ENABLE	0		1: enable the power ramping
		4:3	PA_RAMP_STEP_WIDTH[1:0]	00		Step width (unit: 1/8 of bit period)
		2:0	PA_LEVEL_MAX_INDEX	111		Final level for power ramping or selected output power index.

Table 36. Radio configuration registers (digital blocks)

Register name	Address	Bit	Field Name	Reset	R/W	Description
MOD1	0x1A	7:0	DATARATE_M	0x83	R/W	The mantissa value of the data rate equation (see *Equation 8*)
MOD0	0x1B	7	CW	0	R/W	1: enable the CW transmit mode
		6	BT_SEL	0		Select BT value for GFSK 0: BT = 1 1: BT = 0.5
		5:4	MOD_TYPE[1:0]	01		Modulation type 0: 2-FSK 1: GFSK 2: ASK/OOK 3: MSK
		3:0	DATARATE_E	1010		The exponent value of the data rate equation (see *Equation 8*)
FDEV0	0x1C	7:4	FDEV_E[3:0]	0100	R/W	The exponent value of the frequency deviation equation (see *Equation 7*)
		3	CLOCK_REC_ALGO_SEL	0		Select PLL or DLL mode for symbol timing recovery
		2:0	FDEV_M	101		The mantissa value of the frequency deviation equation (see *Equation 7*)

Table 37. Packet/protocol configuration registers

Register name	Address	Bit	Field Name	Reset	R/W	Description
PCKTCTRL4	0x30	7:5	Reserved	000	R/W	
		4:3	ADDRESS_LEN[1:0]	00		Length of address field in bytes: 0 or 1: Basic 2: STack
		2:0	CONTROL_LEN	000		Length of control field in bytes
PCKTCTRL3	0x31	7:6	PCKT_FRMT[1:0]	00	R/W	Format of packet. 0: basic, 2: WM-Bus, 3: STack (see *Section 9.5*)
		5:4	Reserved	00		
		3:0	LEN_WID	0111		Size in number of binary digit of length field
PCKTCTRL2	0x32	7:3	PREAMBLE_LENGTH[4:0]	00011	R/W	Length of preamble field in bytes (from 1 to 32)
		2:1	SYNC_LENGTH[1:0]	11		Length of sync field in bytes (from 1 to 4)
		0	FIX_VAR_LEN	0		Packet length mode. 0: fixed, 1: variable (in variable mode the field LEN_WID of PCKTCTRL3 register must be configured)
PCKTCTRL1	0x33	7:5	CRC_MODE[2:0]	001	R/W	CRC: 0: No CRC, 1: 0x07, 2: 0x8005, 3: 0x1021, 4: 0x864CBF
		4	WHIT_EN[0]	0		1: enable the whitening mode on the data (see *Section 9.4.3*)
		3:2	TXSOURCE[1:0]	00		TX source data: 0: normal mode, 1: direct through FIFO, 2: direct through GPIO, 3: PN9
		1	Reserved	0		
		0	FEC_EN	0		1: enable the FEC encoding in TX. (see *Section 9.4.1*)

Table 37. Packet/protocol configuration registers (continued)

Register name	Address	Bit	Field Name	Reset	R/W	Description
PCKTLEN1	0x34	7:0	PCKTLEN1	0	R/W	Length of packet in bytes (MSB)
PCKTLEN0	0x35	7:0	PCKTLEN0	0x14	R/W	Length of packet in bytes (LSB)
SYNC4	0x36	7:0	SYNC4	0x88	R/W	Sync word 4
SYNC3	0x37	7:0	SYNC3	0x88	R/W	Sync word 3
SYNC2	0x38	7:0	SYNC2	0x88	R/W	Sync word 2
SYNC1	0x39	7:0	SYNC1	0x88	R/W	Sync word 1
MBUS_PRMBL	0x3B	7:0	MBUS_PRMBL[7:0]	0x20	R/W	MBUS preamble length in chip sequence ‘01’
MBUS_PSTMBL	0x3C	7:0	MBUS_PSTMBL[7:0]	0x20	R/W	MBUS postamble length in chip sequence ‘01’
MBUS_CTRL	0x3D	7:4	Reserved	00000	R/W	
		3:1	MBUS_SUBMODE[2:0]	000		MBUS sub mode: allowed values are 0, 1, 3 and 5 WM-BUS sub mode: 0: S1 S2 long header, 1: S1m S2 T2 other to meter, 3: T1 T2 meter to other, 5: R2 short header
		0	Reserved	0		
FIFO_CONFIG[1]	0x40	7	Reserved	0	R/W	
		6:0	TXAFTHR [6:0]	110000	R/W	FIFO almost full threshold for TX FIFO
FIFO_CONFIG[0]	0x41	7	Reserved	0	R/W	
		6:0	TXAETHR [6:0]	110000	R/W	FIFO almost empty threshold for TX FIFO
PCKT_FLT_GOALS[3]	0x4B	7:0	TX_DEST_ADDR	0	R/W	TX packet destination fields
PCKT_FLT_GOALS[0]	0x4E	7:0	TX_SOURCE_ADDR	0	R/W	TX packet source
PROTOCOL[2]	0x50	23:21	Reserved	0	R/W	1: CS value contributes to timeout disabling
		20:19	TX_SEQ_NUM_RELOAD[1:0]	0		TX sequence number to be used when counting reset is required using the related command.
		18	RCO_CALIBRATION	0		1: enable the automatic RCO calibration
		17	VCO_CALIBRATION	1		1: enable the automatic VCO calibration
		16	LDC_MODE	0		1: LDC mode on

Table 37. Packet/protocol configuration registers (continued)

Register name	Address	Bit	Field Name	Reset	R/W	Description
PROTOCOL[1]	0x51	15:12	Reserved	0000	R/W	
		11	SEED_RELOAD	0		1: reload the back-off random generator seed using the value written in the BU_COUNTER_SEED_MSBYTE / LSBYTE registers
		10	CSMA_ON	0		1: CSMA channel access mode enabled
		9	CSMA_PERS_ON	0		1: CSMA persistent (no back-off) enabled
		8	Reserved	0		
PROTOCOL[0]	0x52	7:4	Reserved	0	R/W	
		3	NACK_TX	1		1: field NO_ACK=1 on transmitted packet
		2:0	Reserved	0		
TIMERS[3]	0x55	31:24	LDC_PRESCALER[7:0]	1	R/W	Prescaler value of the LDC wakeup timer. When this timer expires the STS1TX exits SLEEP state.
TIMERS[2]	0x56	23:16	LDC_COUNTER[7:0]	0	R/W	Counter value of the LDC wakeup timer. When this timer expires the STS1TX exits SLEEP state.
TX_CTRL_FIELD[3]	0x68	7:0	TX_CTRL3	0	R/W	Control field value to be used in TX packet as byte n.3
TX_CTRL_FIELD[2]	0x69	7:0	TX_CTRL2	0	R/W	Control field value to be used in TX packet as byte n.2
TX_CTRL_FIELD[1]	0x6A	7:0	TX_CTRL1	0	R/W	Control field value to be used in TX packet as byte n.1
TX_CTRL_FIELD[0]	0x6B	7:0	TX_CTRL0	0	R/W	Control field value to be used in TX packet as byte n.0
PM_CONFIG[2]	0xA4	7	Reserved	0	R/W	
		6	EN_TS_BUFFER	0		1: temperature sensor output is buffered
		5	DISABLE_SMPS	0		0: enable internal SMPS 1: disable internal SMPS
		4	Reserved	0		
		3	SET_SMPS_VTUNE	1		Sets the SMPS Vtune voltage
		2	SET_SMPS_PLLBW	1		Sets the SMPS bandwidth
		1:0	Reserved	00		

Table 37. Packet/protocol configuration registers (continued)

Register name	Address	Bit	Field Name	Reset	R/W	Description
PM_CONFIG[1]	0xA5	7	EN_RM	0	R/W	0: divider by 4 enabled (SMPS' switching frequency is F_{SW}=FOSC/4) 1: rate multiplier enabled (SMPS' switching frequency is F_{SW}=KRM*FOSC/(2^15)
		6:0	KRM[14:8]	0100000		Sets the divider ration of the rate multiplier.
PM_CONFIG[0]	0xA6	7:0	KRM[7:0]	0	R/W	
XO_RCO_CONFIG	0xA7	7:4	Reserved	1110	R/W	
		3	EXT_RCOSC	0		1:the 34.7kHz signal must be supplied from a GPIO pin
		2:0	Reserved	001		
TEST_SELECT	0xA8	7:0	Reserved	0x00	R/W	
PM_TEST	0xB2	7:0	Reserved	0x42		

Table 38. Frequently used registers

Register name	Address	Bit	Field Name	Reset	R/W	Description
CHNUM	0x6C	7:0	CH_NUM	0	R/W	Channel number. This value is multiplied by the channel spacing and added to the synthesizer base frequency to generate the actual RF carrier frequency. See *Equation 2*
VCO_CONFIG	0xA1	7:6	Reserved	00	R/W	
		5:0	VCO_GEN_CURR	010001		Set the VCO current
RCO_VCO_CALIBR_IN[2]	0x6D	7:4	RWT_IN[3:0]	0111	R/W	RWT word value for the RCO
		3:0	RFB_IN[4:1]	0000		RFB word value for the RCO
RCO_VCO_CALIBR_IN[1]	0x6E	7	RFB_IN[0]	0	R/W	
		6:0	VCO_CALIBR_TX[6:0]	1001000		Word value for the VCO to be used in TX mode
AES_KEY_IN[15]	0x70	7:0	AES_KEY15	0	R/W	AES engine key input (128 bits)
AES_KEY_IN[14]	0x71	7:0	AES_ KEY14	0	R/W	AES engine key input (128 bits)
	…	7:0	…	…	…	…
AES_KEY_IN[1]	0x7E	7:0	AES_ KEY1	0	R/W	AES engine key input (128 bits)
AES_KEY_IN[0]	0x7F	7:0	AES_ KEY0	0	R/W	AES engine key input (128 bits)

Table 38. Frequently used registers (continued)

Register name	Address	Bit	Field Name	Reset	R/W	Description
AES_DATA_IN[15]	0x80	7:0	AES_IN15	0	R/W	AES engine data input (128 bits)
AES_DATA_IN[14]	0x81	7:0	AES_IN14	0	R/W	AES engine data input (128 bits)
	…	…	…	…	…	…
AES_DATA_IN[1]	0x8E	7:0	AES_IN1	0	R/W	AES engine data input (128 bits)
AES_DATA_IN[0]	0x8F	7:0	AES_IN0	0	R/W	AES engine data input (128 bits)
IRQ_MASK[3]	0x90	7:0	INT_MASKT[31:24]	0	R/W	The IRQ mask register to route the IRQ information to a GPIO. See *Table 29*.
IRQ_MASK[2]	0x91	7:0	INT_MASK [23:16]	0	R/W	The IRQ mask register to route the IRQ information to a GPIO. See *Table 29*.
IRQ_MASK[1]	0x92	7:0	INT_MASK[15:8]	0	R/W	The IRQ mask register to route the IRQ information to a GPIO. See *Table 29*.
IRQ_MASK[0]	0x93	7:0	INT_MASK [7:0]	0	R/W	The IRQ mask register to route the IRQ information to a GPIO. See *Table 29*.
DEM_CONFIG	0xA3	7:2	Reserved	001101	R/W	Reserved do not modify
		1	DEM_ORDER	1		Set it to 0 during radio initialization
		0	Reserved	1		Reserved do not modify
PM_CONFIG	0xA4	7	Reserved	0	R/W	
		6	EN_TS_BUFFER	0		1: temperature sensor output is buffered
		5	DISABLE_SMPS	0		0: enable internal SMPS 1: disable internal SMPS
MC_STATE[1]	0xC0	7:3	Reserved	0101	R	
		2	TX_FIFO_FULL	0		1: TX FIFO is full
		1	Reserved	0		
		0	ERROR_LOCK	0		1: RCO calibrator error
MC_STATE[0]	0xC1	7:1	STATE[6:0]	0	R	Current MC state. See *Table 18*.
		0	XO_ON	0		1: XO is operating
TX_PCKT_INFO	0xC2	7:6	Reserved	0	R	
		5:4	TX_SEQ_NUM	0		Current TX packet sequence number
		3:0	Reserved	0		

Table 38. Frequently used registers (continued)

Register name	Address	Bit	Field Name	Reset	R/W	Description
AES_ DATA_OUT[15]	0xD4	7:0	AES_OUT15	0	R	AES engine data output (128 bits)
AES_ DATA_OUT[14]	0xD5	7:0	AES_OUT14	0	R	AES engine data output (128 bits)
	…	…	…	…	…	…
AES_ DATA_OUT[1]	0xE2	7:0	AES_OUT1	0	R	AES engine data output (128 bits)
AES_ DATA_OUT[0]	0xE3	7:0	AES_OUT0	0	R	AES engine data output (128 bits)
RCO_VCO_CALIBR_OUT[1]	0xE4	7:4	RWT_OUT[3:0]	0	R	RWT word from internal RCO calibrator
		3:0	RFB_OUT[4:1]	0		RFB word from internal RCO calibrator
RCO_VCO_CALIBR_OUT[0]	0xE5	7	RFB_OUT[0]	0	R	
		6:0	VCO_CALIBR_DATA	0		Output word from internal VCO calibrator
LINEAR_FIFO_STATUS[1]	0xE6	7	Reserved	0	R	
		6:0	ELEM_TXFIFO	0		Number of elements in the linear TX FIFO (from 0 to 96 bytes)
IRQ_STATUS[3]	0xFA	7:0	INT_EVENT[31:24]	0	RR	The IRQ status register. See *Table 29*.
IRQ_STATUS[2]	0xFB	7:0	INT_EVENT[23:16]	0	RR	The IRQ status register. See *Table 29*.
IRQ_STATUS[1]	0xFC	7:0	INT_EVENT[15:8]	0	RR	The IRQ status register. See *Table 29*.
IRQ_STATUS[0]	0xFD	7:0	INT_EVENT[7:0]	0	RR	The IRQ status register. See *Table 29*.

Table 39. General information

Register	Address	Bit	Field name	Reset	R/W	Description
DEVICE_INFO[1:0]	0xF0	7:0	PARTNUM[7:0]	0x01	R	Device part number
	0xF1	7:0	VERSION[7:0]	0x30	R	Device version number

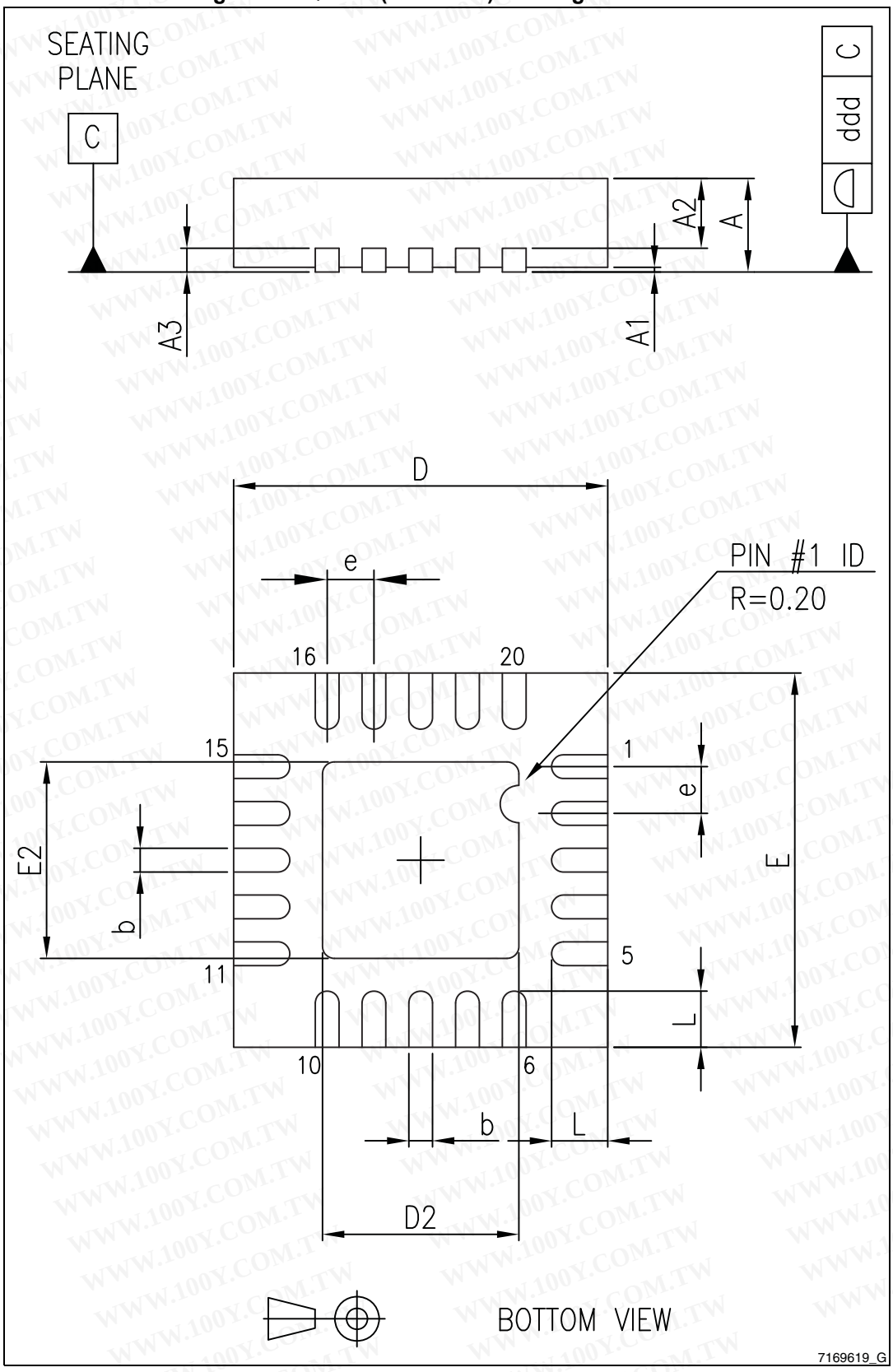
12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 40. QFN20 (4 x 4 mm.) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	3.85	4.00	4.15
D2	2.55	2.60	2.65
E	3.85	4.00	4.15
E2	2.55	2.60	2.65
e	0.45	0.50	0.55
L	0.35	0.55	0.75
ddd			0.08

Figure 13. QFN20 (4 x 4 mm.) drawing dimension



13 Revision history

Table 41. Document revision history

Date	Revision	Changes
07-Aug-2013	1	Initial release.

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