

Conversion from SST49LF020 to SST49LF020A



Application Note
October 2002

INTRODUCTION

This document describes the differences between the SST49LF020 and the SST49LF020A products. Please refer to the SST49LF020 datasheet (S71175-02-000) and the SST49LF020A datasheet (S71206-02-000) for detail specification description. There are no AC or DC parametric differences between the SST49LF020 and SST49LF020A. Functional differences are described below.

PARALLEL PROGRAMMING (PP) MODE

Parallel programming mode supports fast In-System or PROM programming for manufacturing. Pin assignments are the same for the SST49LF020 and SST49LF020A in PP mode. Software algorithms written for SST49LF020 will also work for SST49LF020A. Note that the Device ID Read will return 61H for SST49LF020 and 52H for SST49LF020A.

LOW PIN COUNT (LPC) MODE

Pin Assignments

The SST49LF020A has four ID pins, ID[3:0], to support multiple LPC flash devices to be strapped on to the same LPC bus to increase memory density in a system. The ID pins are only applicable when the device is in LPC mode. The SST49LF020 does not support multiple device selection and the pins on this device are reserved and should be left unconnected in LPC mode. Refer to Table 1 and Table 2 on pin signal differences for each package offered.

TABLE 3: ADDRESS BITS DEFINITION

Part Number	A31:A23	A22	A21:A18	A17:A0
SST49LF020	XXXX XXXX Xb	X=Memory Access FFBC 0100H =GPI Register Access	XXXXb	Device Memory address
SST49LF020A	1111 1111 1b	1=Memory Access 0=Register Access	ID[3:0] ¹	Device Memory address

1. Strapping values for Hardware ID pins, ID[3:0], allow multiple devices to be attached to the same bus to increase memory densities in a system

TABLE 1: 32-PLCC PIN SIGNAL DIFFERENCES

Pin #	Mode ¹	SST49LF020	SST49LF020A
9	LPC	Reserved ²	ID3
10	LPC	Reserved ²	ID2
11	LPC	Reserved ²	ID1
12	LPC	Reserved ²	ID0

T1.0 2045

1. PP mode or LPC mode, indicates which mode is affected
2. Reserved pins must be left unconnected

TABLE 2: 32-TSOP PIN SIGNAL DIFFERENCES

Pin #	Mode ¹	SST49LF020	SST49LF020A
17	LPC	Reserved ²	ID3
18	LPC	Reserved ²	ID2
19	LPC	Reserved ²	ID1
20	LPC	Reserved ²	ID0

T2.0 2045

1. PP mode or LPC mode, indicates which mode is affected
2. Reserved pins must be left unconnected

System Compatibility

System Memory Mapping

The LPC interface protocol has address length of 32-bit or 4 GByte. The SST49LF020 only decodes address bits A17:A0 for memory access, and General Purpose Inputs Register (GPI_REG) location FFBC0100H. The SST49LF020A will only respond to memory address range FFFF FFFFH: FFC0 0000H and register address range FFBF FFFFH: FF80 0000H. See Table 3 for Address Bits Definition. The SST49LF020A will ignore any LPC cycles outside these address ranges.

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Multiple Device Selection

The SST49LF020A supports four ID pins, ID[3:0], allowing up to 16 devices to be attached to the same bus by using different ID strapping values in a system. The boot device has hardware ID value of 0000; all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011, etc.), the SST49LF020A compares the address bits [A21:A18] in every LPC address memory cycle and if [A21:A18] are not the inverse of the hardware strapping state of ID[3:0], the device will ignore the remainder of the cycle. The SST49LF020 does not support this feature.

Registers

The SST49LF020A supports two JEDEC ID registers where the manufacturer and device ID may be read in LPC mode in addition to the General Purpose Inputs Registers (GPI_REG). For the boot device, the manufacturer and device ID may be read from register memory location FFBC000H and FFBC001H respectively. Refer to SST49LF020A datasheet for register memory locations for different ID strapping values when multiple LPC flash devices are used in a system. The SST49LF020 does not support JEDEC ID registers in LPC. The manufacturer and device IDs may be read in PP mode for the SST49LF020.

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