seeq

000701

52B13/52B23/52B33
52B13H/52B23H/52B33H
Electrically Erasable ROM

PRELIMINARY DATA SHEET

March 1983

Features

- **Input Latches**
- **Single 5V Supply**
- **Specified over V_{CC} ±10% Range**
- **TTL Byte Erase/Byte Write/Chip Clear**
- **1 ms or 10 ms Byte Erase/Byte Write**
- **10,000 Erase/Write Cycles per Byte**
- **Silicon Signature™ and DiTrace™**
- **Fast Read Access Time — 250 ns**
- **JEDEC Approved Byte Wide Memory Pinout**

Description

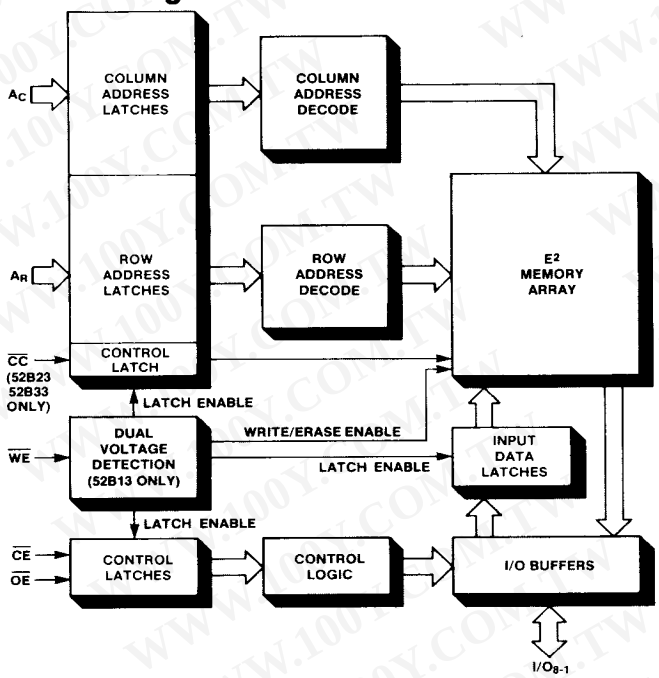
SEEQ's family of 5 volt, electrically erasable read only memories, E²ROMs, include three densities. The 52B13 and 52B13H are 2048 x 8 bit, the 52B23 and 52B23H are 4096 x 8 bit, and the 52B33 and 52B33H are 8192 x 8 bit E²ROM. Each device operates on 5 volt TTL levels in the read, write and erase modes. In addition, high voltage (14-22 volts) may be used with the 52B13 for erase and write. All devices have a chip clear mode in which the entire memory is erased in a single erase cycle. The 52B13 performs chip clear with a high voltage signal while the other devices in the family require only a TTL level signal on $\overline{OE}$. The erasure time for both chip clear and byte erase is under 10 ms for all device types. Where faster erase/write times are required, the "H" product may be used to achieve erase or write in under 1 ms.

Data, addresses, $\overline{CE}$, $\overline{CC}$ and $\overline{OE}$ are latched on the leading edge of $\overline{WE}$. The system controller needs only to maintain the $\overline{WE}$ signal during the erase/write cycle after the latches are activated. Once written, which requires under 10 ms, there is no limit to the number of times that the data may be read. Each byte may be erased and written at least 10,000 times.

This family of E²ROMs include Silicon Signature™ and DiTrace™, SEEQ's on-chip traceability feature. This feature provides the ability to trace the history of any packaged device back to the wafer level. Silicon Signature™ contains device revisions and programming information. The process lot numbers and data is written into DiTrace™.

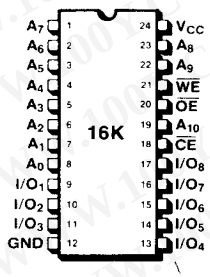
The members of SEEQ's family of latched E²ROMs are each available in the military (-55° C to +125° C) and the extended (-40° C to +85° C) temperature ranges.

Block Diagram

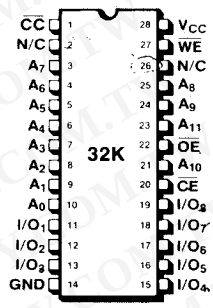


Pin Configurations

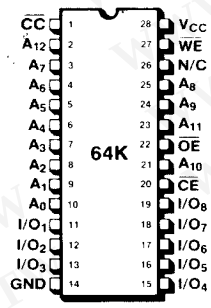
52B13/52B13H



52B23/52B23H



52B33/52B33H



Pin Names

A_C	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_R	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

Device Operation

Each member of SEEQ's family of latched E²ROM's has six modes of operation (refer to Table 1). The control signals that determine these modes are TTL compatible with the exception of two operations for the 52B13. The 52B13 has a dual voltage detection circuit that allows the use of either a TTL or a high voltage, 21-volt pulse. For byte erase and write, a 5- or 21-volt signal may be applied to $\overline{WE}$. For chip clear, a 21-volt signal is applied to $\overline{OE}$. This dual voltage capability makes the 52B13 compatible with previous generations of E²ROM's.

The "H" members of the family operate in the same manner as the other devices except for a faster $\overline{WE}$ pulse width (TTL voltage only) during byte erase and byte write. The "H" product types permit byte write and erase times of 1 ms compared to 10 ms for the standard product. The chip clear time is 10 ms.

Read

A read is accomplished by presenting the address of the desired byte to the Column and Row Address inputs with A_0 as the LSB. Once the address is stable, $\overline{CE}$ is brought LOW in order to enable the chip ($\overline{WE}$ must be at a TTL HIGH during the entire read cycle). The output drivers are made active by bringing $\overline{OE}$ to a TTL LOW. Data is valid t_{CE} after $\overline{CE}$ or t_{OE} after $\overline{OE}$ is LOW. The power dissipation of the chip may be reduced by taking $\overline{CE}$ to a TTL HIGH between operations. This lowers P_D by over 60%. The latches are transparent in the read mode.

Byte Erase/Write

Each byte of the memory may be individually erased or written with TTL level pulses. The two operations have the same timing and specifications since the byte erase is performed by writing all HIGHs (HEX FF) to the selected byte. This restores the byte to its "virgin" state of logical one. The byte erase is performed by presenting the device with $\overline{CE}$ at a logical LOW and $\overline{OE}$ at a logical HIGH after the address is stable. These controls must be stable for t_S before $\overline{WE}$ is taken active. The data must be stable for t_{DS}. All of these control inputs together with the address and data lines are latched on the falling edge of $\overline{WE}$. After t_H they may be removed and the next condition established while the byte is being erased or written. This effectively increases the write speed. After t_{WP}, $\overline{WE}$ may be returned to the TTL HIGH level and the next operation begun t_{WR} after the rising edge of the pulse.

Chip Clear

The chip clear is performed by taking $\overline{CC}$ and $\overline{CE}$ to a TTL LOW level and $\overline{OE}$ to a HIGH level. For the 52B13, this requires a high voltage level but all other family members operate on TTL levels. The order in which the controls are set does not matter, only that they are stable for t_S before $\overline{WE}$ goes low. The I/O and the Address inputs are Don't Care's. After the control and data inputs are stable, take $\overline{WE}$ low. This latches all control and data inputs and, after t_H all inputs with the exception of $\overline{WE}$ become Don't Care's. $\overline{WE}$ must be maintained at a LOW level for the duration of the chip clear cycle and then return it to a HIGH level. Another mode of operation may be started t_{WR} after $\overline{WE}$ is stable. The memory has now been returned to its "virgin" state and contains all 1's.

Power Up/Down Considerations

Internal circuitry on all devices guard against inadvertent programming of bits during times when V_{CC} is below the normal operating voltage. The device outputs will remain in high impedance and the write/erase circuitry disabled as long as $\overline{WE}$ is kept at V_{IL}. Normal operation, as outlined in Table 1, can begin only after $\overline{WE}$ has been taken to V_{IH}.

Table 1. Mode Selection (V_{CC} = 5V ± 10%)

Mode \ Function	$\overline{CE}$	$\overline{CC}$[3]	$\overline{OE}$	$\overline{WE}$	I/O
Read[1]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby[1]	V_{IH}	Don't Care	Don't Care	Don't Care	High Z
Byte Erase[2]	V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write[2]	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Erase[2]	V_{IL}	V_{IL}	V_{OE}/V_{IH}[4]	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	Don't Care	High Z

Notes:
1. $\overline{WE}$ may be from V_{IH} to 6V in the read and standby mode.
2. $\overline{WE}$ may be at V_{IL} (TTL W/E Mode) or from 15V to 22V (High Voltage W/E Mode) in the byte erase, byte write, or chip erase mode of the 52B13. $\overline{WE}$ must be used in the TTL W/E mode only for all "H" products.
3. $\overline{CC}$ available only on 52B23/52B23H and 52B33/52B33H.
4. The 52B13/52B13H require V_{OE}. All other devices require V_{IH}.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +100° C
Under Bias ..... -10° C to +80° C
All Inputs or Outputs with Respect to Ground ..... +6V to -0.3V

52B13 Only
$\overline{WE}$ During Writing/Erasing with Respect to Ground ..... +22.5V to -0.3V
Duration of $\overline{WE}$ Supply at 22V During W/E Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions (All Operating Modes — Reference Table 1)

	52BXX-3	52BXX-200/-250/-350
V_{CC} Supply Voltage	5V ± 5%	5V ± 10%
Temperature Range	0 to 70° C	0 to 70° C

D.C. Operating Characteristics During Read or Write/Erase

(Over the Operating V_{CC} and Temperature Range)

Symbol	Parameter	Min.	Nom.[1]	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	µA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode			10	µA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	µA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	µA	$\overline{WE} = V_{IL}$
	Chip Erase — High Voltage Mode[2]			1.5	mA	$\overline{WE}$ = 22V
I_{CC1}	V_{CC} Standby Current 52B13/H		15	30	mA	$\overline{CE} = V_{IH}$
	52B23/H, 52B33/H		18	40	mA	
I_{CC2}	V_{CC} Active Current 52B13/H		50	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$
	52B23/H, 52B33/H		60	110	mA	
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.1		0.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	-0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{WE}	$\overline{WE}$ Read Voltage	2		V_{CC} + 1	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode[2]	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 µA
V_{OE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	I_{OE} = 10 µA

Notes:
1. Nominal values are for T_A = 25° C and V_{CC} = 5.0V.
2. Applies to 52B13 only.

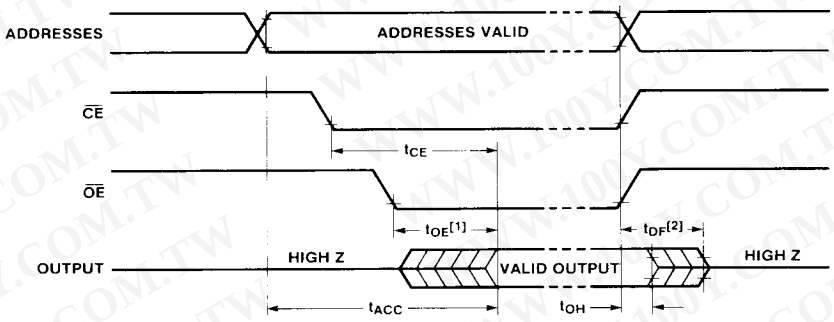
A.C. Operating Characteristics During Read (Over Operating V_{CC} and Temperature Range)

Symbol	Parameter	Device Number Extension	52BXX/52BXXH Min.	Nom.	Max.	Units	Conditions
t_{ACC}	Address to Data Valid	-200			200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		-250			250	ns	
		-350/-3			350	ns	
t_{CE}	Chip Enable to Data Valid	-200			200	ns	$\overline{OE} = V_{IL}$
		-250			250	ns	
		-350/-3			350	ns	
t_{OE}[1]	Output Enable to Data Valid	-200	10		80	ns	$\overline{CE} = V_{IL}$
		-250	10		90	ns	
		-350/-3	10		100	ns	
t_{DF}[2]	Output Enable to High Impedance	-200	0		60	ns	$\overline{CE} = V_{IL}$
		-250	0		70	ns	
		-350/-3	0		80	ns	
t_{OH}	Output Hold				0	ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/ C_{OUT}[3]	Input/Output Capacitance				10	pF	$V_{IN}=0/V_{OUT}=0$, $T_A = 25°C$

A.C. Operating Characteristics During Write/Erase (Over Operating V_{CC} and Temperature Range)

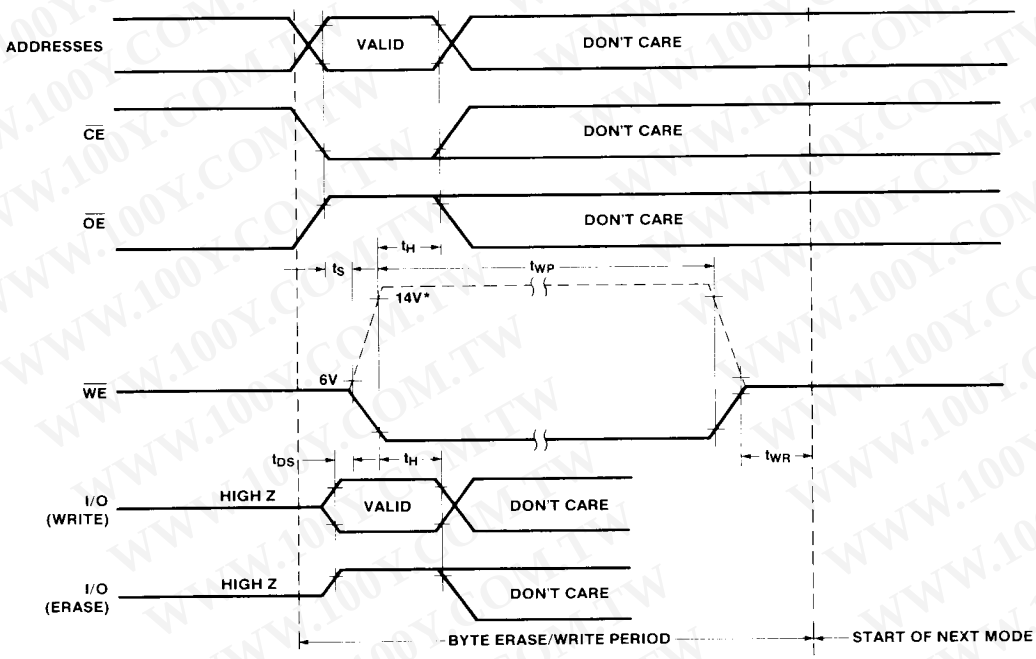
Symbol	Parameter		Min.	Max.	Units
Q[4]	Maximum Endurance		10,000		Cycles/Byte
t_S	$\overline{CC}$, $\overline{CE}$, $\overline{OE}$ or A_N Setup to $\overline{WE}$		50		ns
t_{DS}	Data Setup to $\overline{WE}$		0		ns
t_H[5]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, A_N or Data Change		50		ns
t_{WP}	Write Enable, $\overline{WE}$, Pulse Width	Chip Clear — All Devices	9	70	ms
		Byte Modes — 52BXX	9	70	ms
		Byte Modes — 52BXXH	1	20	ms
t_{WR}[6]	$\overline{WE}$ to Mode Change		50		ns

READ TIMING

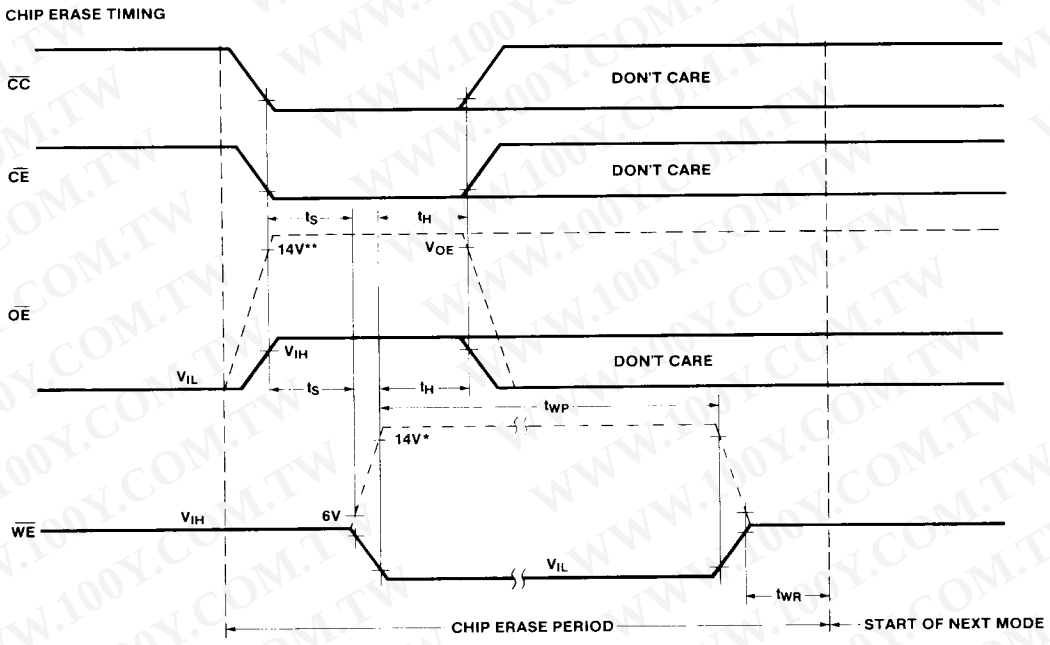


Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.
4. Maximum endurance, Q, is the number of write and erase cycles/byte.
5. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
6. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

BYTE ERASE OR BYTE WRITE TIMING



CHIP ERASE TIMING

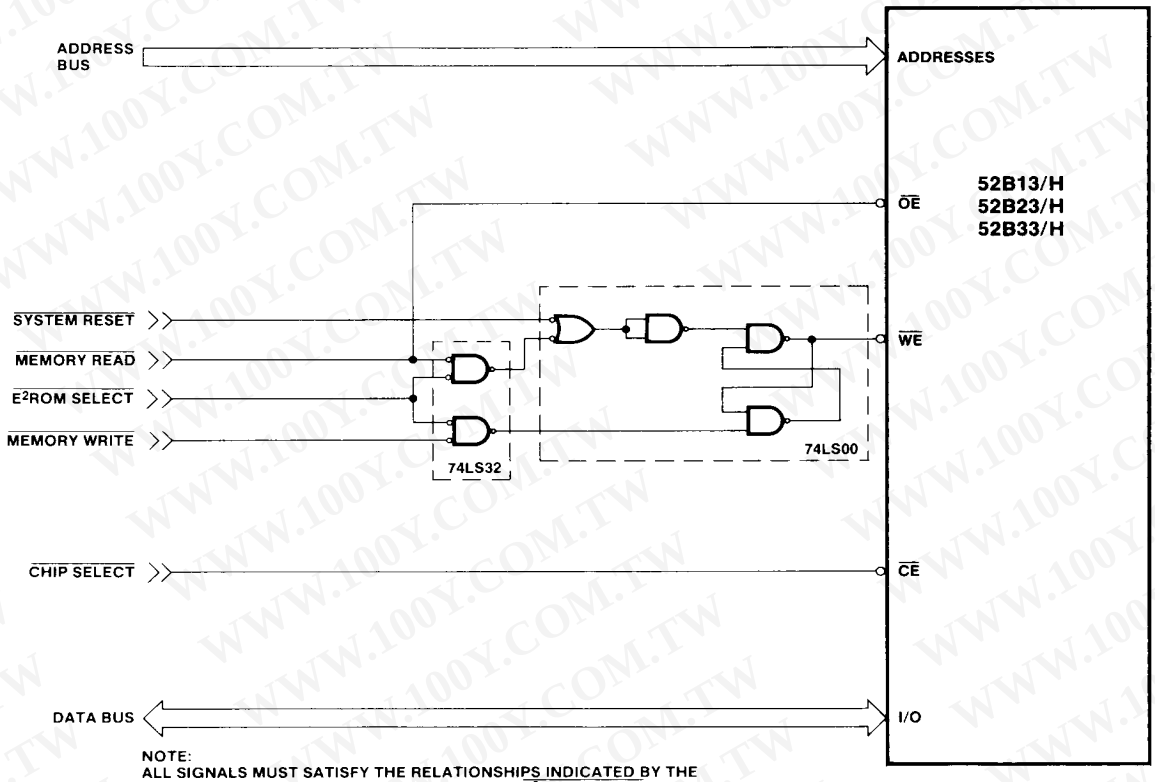


ADDRESS AND I/O PINS ARE "DON'T CARE".

*IN THE BYTE ERASE/WRITE OR CHIP ERASE MODE, $\overline{WE}$ FOR THE 52B13 MAY BE EITHER A HIGH OR TTL VOLTAGE. $\overline{WE}$ FOR THE 52XXH IS TTL ONLY.

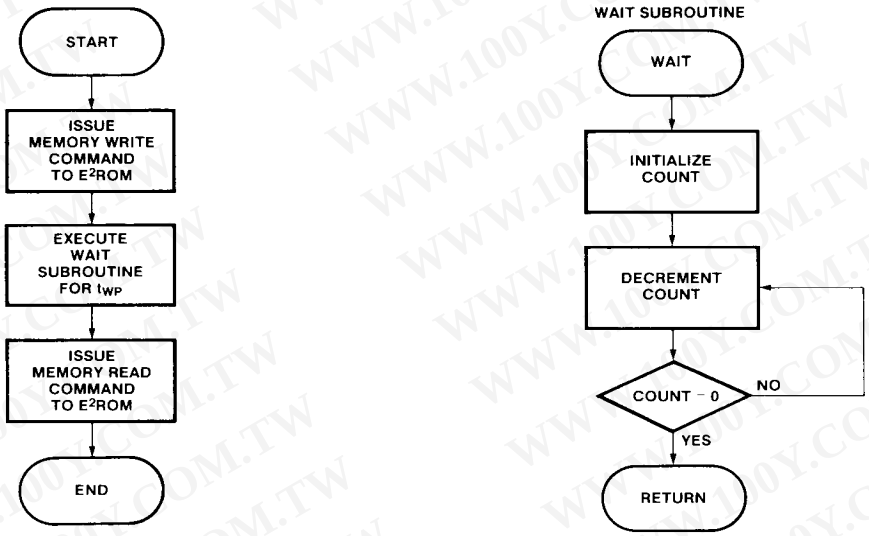
**IN THE CHIP ERASE MODE, $\overline{OE}$ IS A HIGH VOLTAGE FOR THE 52B13/52B13H ONLY.

Microprocessor Interface Circuit Example for Byte Write/Erase



NOTE:
ALL SIGNALS MUST SATISFY THE RELATIONSHIPS INDICATED BY THE TIMING DIAGRAMS SHOWN ON PAGES 4 AND 5. E^2ROM SELECT IS DERIVED FROM THE CHIP SELECT SIGNALS OF ALL DEVICES FOR WHICH THIS CIRCUIT GATES WE. THIS MAY ENTAIL A SIMPLE OR FUNCTION. IN CASE OF A SINGLE E^2ROM, THE TWO SIGNALS WOULD BE COMMON.

Typical E^2ROM Write/Erase Routine



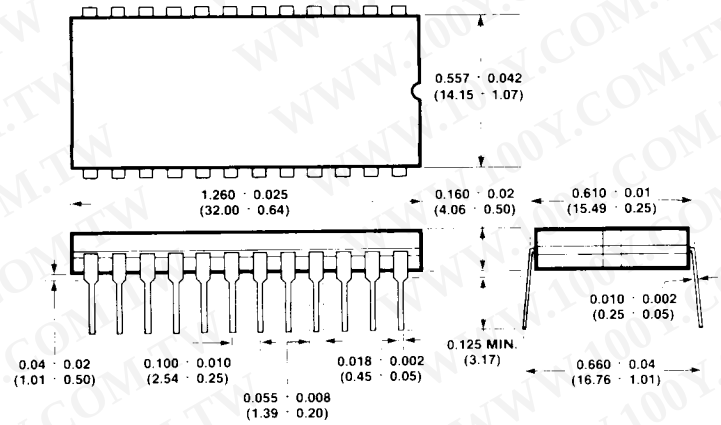
Ordering Information

PART NUMBER **D Q 5 2 B 1 3 H — 250**

PACKAGE TYPE	OPERATING TEMPERATURE RANGE	DEVICE TYPE	WRITE TIME	ACCESS TIME
D = CERDIP	Q = 0°C TO 70°C	52B13 = 2K x 8 E^2ROM	(BLANK) = 10 ms	200 = 200 ns
		52B23 = 4K x 8 E^2ROM	H = 1 ms, 5 Volt	250 = 250 ns
		52B33 = 8K x 8 E^2ROM		350 = 350 ns
				3 = 350 ns

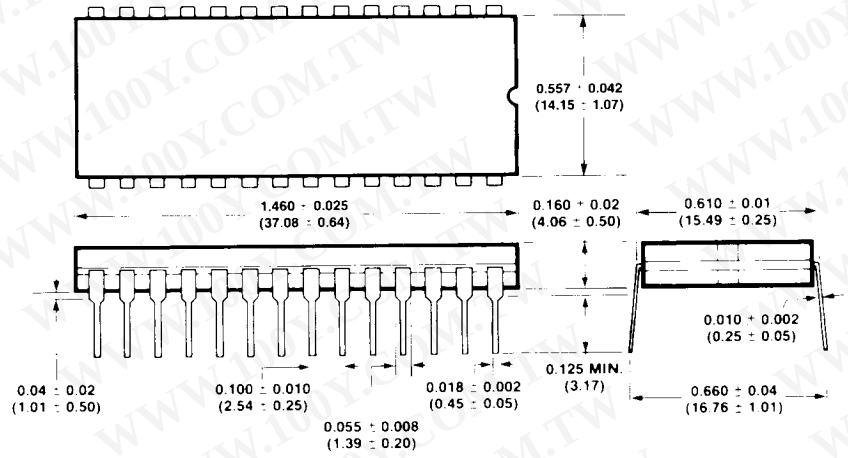
Packaging Information

24-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



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U.S. SALES OFFICES

Corporate Sales and Marketing Headquarters
SEEQ Technology, Inc.
San Jose, California 95131
(408) 942-1990
TWX: 910-338-2313
Telex: 296609

Western Area Sales Office
SEEQ Technology, Inc.
Irvine, California 92714
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