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Status	Product Specification
Memory Products	

82S23

82S123

256-bit TTL bipolar PROM

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S23 and 82S123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

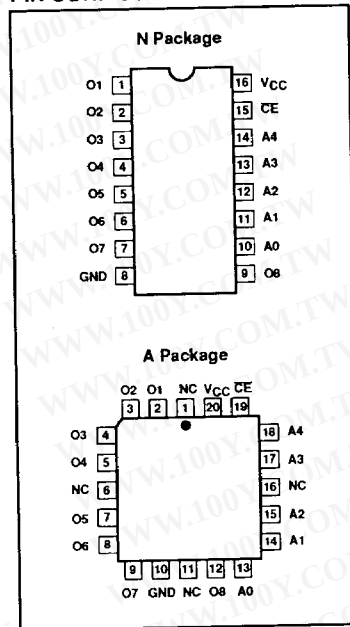
FEATURES

- Address access time: 50ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- One Chip Enable input
- Output options:
 - N82S23: Open Collector
 - N82S123: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

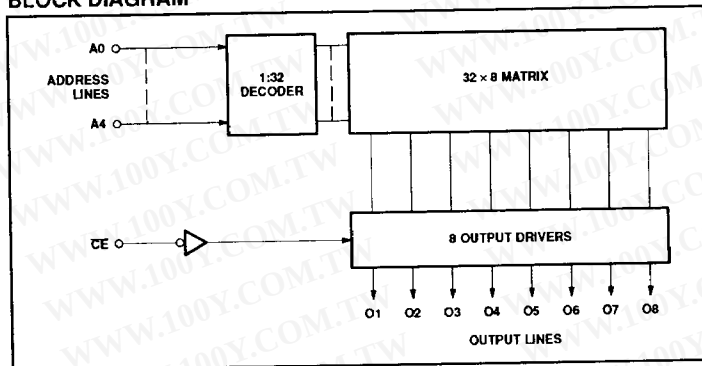
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

PIN CONFIGURATIONS



BLOCK DIAGRAM



勝特力材料 886-3-5753170
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[Http://www.100y.com.tw](http://www.100y.com.tw)

256-bit TTL bipolar PROM (32 × 8)**82S23 / 82S123****ORDERING INFORMATION**

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N82S23 N, N82S123 N
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82S23 A, N82S123 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High (82S23)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S123)	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
			MIN	TYP ³	MAX	
Input voltage						
V _{IL}	Low	V _{CC} = 4.75V	2.0		0.8	V
V _{IH}	High	V _{CC} = 5.25V			V	
V _{IC}	Clamp	I _{IN} = -12mA			-1.2	V
Output voltage						
V _{OL}	Low	CE = Low I _{OUT} = 16mA	2.4		0.45	V
V _{OH}	High	I _{OUT} = -2.0mA			V	
Input current						
I _{IL}	Low	V _{IN} = 0.45V			-100	μA
I _{IH}	High	V _{IN} = 5.5V			50	μA
Output current						
I _{OLK}	Leakage (82S23)	CE = High, V _{OUT} = 5.5V	-15		40	μA
I _{OZ}	Hi-Z state (82S123)	CE = High, V _{OUT} = 5.5V			40	μA
		CE = High, V _{OUT} = 0.5V			-40	μA
I _{OS}	Short circuit (82S123) ⁴	CE = Low, V _{OUT} = 0V, High stored			-90	mA
Supply current ⁵						
I _{CC}		V _{CC} = 5.25V			96	mA
Capacitance						
C _{IN}	Input	CE = High, V _{CC} = 5.0V V _{IN} = 2.0V		5		pF
C _{OUT}	Output	V _{OUT} = 2.0V		8		pF

NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground terminal.
3. Typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
4. Duration of short circuit should not exceed 1 second.
5. Measured with all inputs grounded and all outputs open.

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82S23 / 82S123

$$R_1 = 270\Omega, R_2 = 600\Omega, C_1 = 30\text{pF}, 0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}, 4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$$

NOTES:

1. Typical values are $V_{CC} = 5V$, $T_{amb} = +25^{\circ}C$.
2. Tested at an address cycle time of $1\mu s$.
3. Measured at a delta of $0.5V$ from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

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The timing diagram illustrates the relationship between the ADDRESS, CE (Chip Enable), and data bus signals for the 82S23 decoder. The ADDRESS signal is a square wave between 0V and +3.0V. The CE signal is a square wave between 0V and +3.0V. The data bus signal is shown for two cases: D1 - O8 82S123 and D1 - O8 82S23. The data bus signal is high-impedance (Hi-Z) when CE is high and transitions to a valid output level (V_{OH} or V_{OL}) when CE is low. The timing parameters shown are t_{CE} (CE pulse width), t_{CD} (CE to data delay), t_{AA} (address-to-data delay), and V_{OH} (output high voltage).