16,384 (2K X 8) BIT UV ERASABLE PROM

DESCRIPTION

The μPD2716 is a 16,384 bit (2048 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5 volt supply, making it ideal for microprocessor applications. It offers a standby mode with an attendant 75% savings in power consumption, and is compatible with the μPD2316E as a ROM. This allows for economical change-over to a masked ROM for production quantities, where desired.

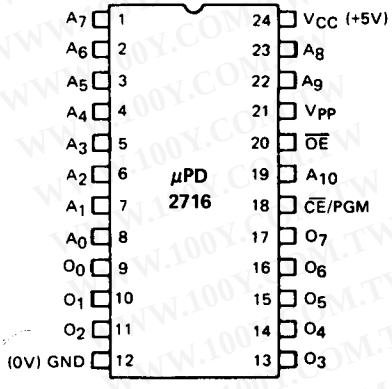
The μPD2716 features fast, simple one pulse programming controlled by TTL level signals. Total programming time for all 16,384 bits is only 100 seconds.

FEATURES

- Ultraviolet Erasable and Electrically Programmable
- Access Time – 390 ns Max
- Single Location Programming
- Programmable with Single Pulse
- Low Power Dissipation Standby Mode
- Input/Output TTL Compatible for Reading and Programming
- Pin Compatible to μPD2316E, μPD446 and μPD4016.
- Single +5V Power Supply
- 24 Pin Ceramic DIP
- Three-State Outputs

4

PIN CONFIGURATION



PIN NAMES

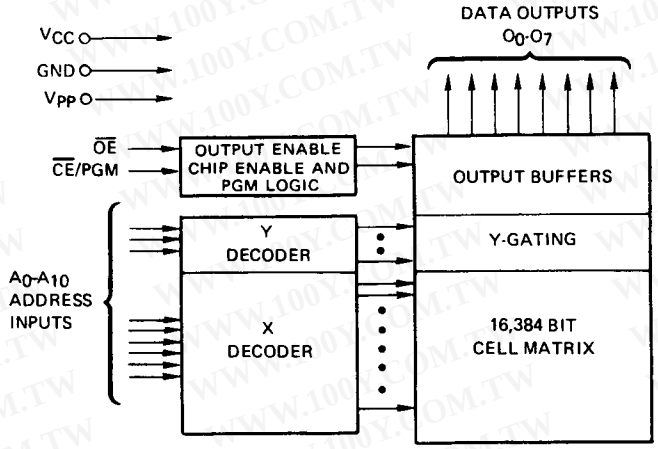
A_0-A_{10}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$/PGM	Chip Enable/Program

TABLE 1. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM	$\overline{OE}$	VPP	VCC	OUTPUTS
Read	V_{IL}	V_{IL}	+5	+5	DOUT
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	DIN
Program Verify	V_{IL}	V_{IL}	+25	+5	DOUT
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

V_{IH} and V_{IL} are TTL high level ("1") and TTL low level ("0") respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +125°C
Output Voltage	-0.3 to +6 Volts
Input Voltage	-0.3 to +6 Volts
Supply Voltage V_{CC}	-0.3 to +6 Volts
Supply Voltage Vpp	-0.3 to +26.5 Volts

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

DC CHARACTERISTICS

READ MODE AND STANDBY MODE

T_a = 0°C ~ 70°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage	V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage	V_{IL}	-0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current	I_{IL}			10	μA	V_{IN} = 5.25V
V_{PP} Current	I_{PP1}			5	mA	V_{PP} = 5.85V
V_{CC} Current ②	I_{CC1}		10	25	mA	$\overline{CE}/PGM$ = V_{IH} $\overline{OE}$ = V_{IL} Standby Mode
	I_{CC2}		57	100	mA	$\overline{CE}/PGM$ = V_{IL} $\overline{OE}$ = V_{IL} Read Mode

Notes: ① V_{CC} must be applied simultaneously or before Vpp and removed after Vpp.

② Vpp may be connected directly to V_{CC} (+5V) at read mode and standby mode. The supply current would then be the sum of I_{PP1} and I_{CC} (I_{CC1} or I_{CC2}).

③ The tolerance of 0.6V allows the use of a driver circuit for switching the Vpp supply pin from +25V to +5V.

DC CHARACTERISTICS (CONT.)

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①④ = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Low Voltage	V_{IL}	-0.1		0,8	V	
Input Leakage Current	I_{IL}			10	μA	V_{IN} = 5.25V/0.45V
V_{PP} Current	I_{PP1}			5	mA	$\overline{CE}/PGM = V_{IL}$ Program Verify / Program Inhibit
	I_{PP2}			30	mA	$\overline{CE}/PGM = V_{IH}$ Program Mode
V_{CC} Current	I_{CC}			100	mA	

AC CHARACTERISTICS

READ MODE AND STANDBY MODE

T_a = 0°C to +70°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay	t_{ACC}				ns	$\overline{CE}/PGM = \overline{OE} = V_{IL}$
$\overline{CE}/PGM$ to Output Delay	t_{CE}				ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		100	ns	$\overline{CE}/PGM = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE}/PGM = \overline{OE} = V_{IL}$

Test Conditions
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2V

Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①④ = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

Test Conditions:

Input Pulse Levels . . . . . 0.8V to 2.2V
Input Timing Reference Level. . . . . 1V and 2V
Output Timing Reference Level . .0.8V and 2V

Notes: ① V_{CC} must be applied simultaneously or before V_{PP} and removed after V_{PP}.

② V_{PP} may be connected directly to V_{CC} (+5V) at read mode and standby mode. The supply current would then be the sum of I_{PP1} and I_{CC} (I_{CC1} or I_{CC2}).

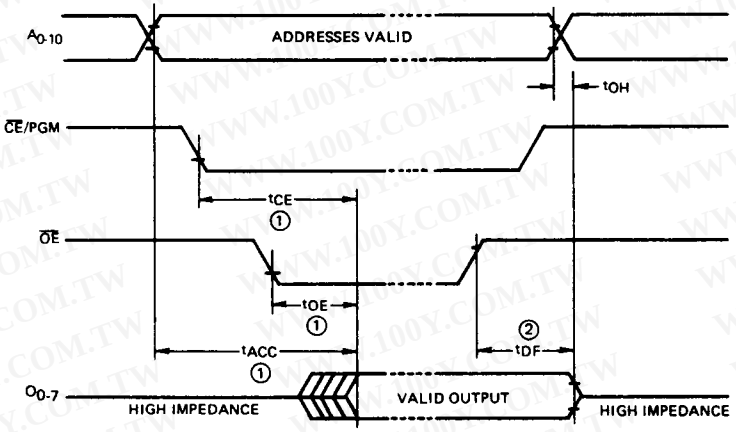
③ The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from +25V to +5V.

④ During programming, program inhibit, and program verify, a maximum of +26V should be applied to the V_{PP} pin. Overshoot voltages to be generated by the V_{PP} [illegible] uld be limited to less than +26V.

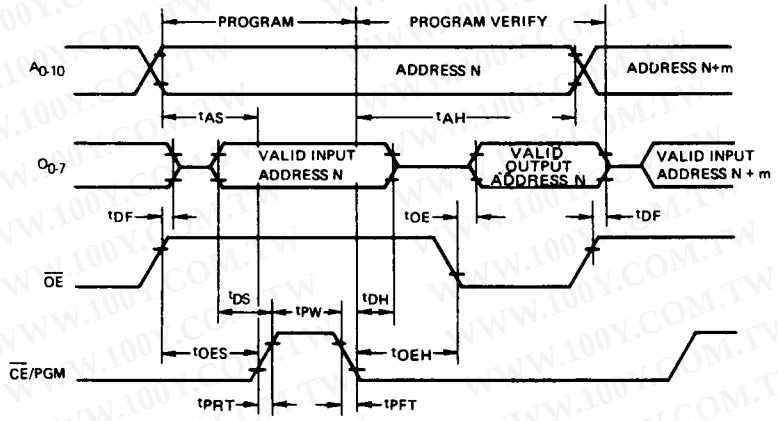
4

TIMING WAVEFORMS

READ MODE



PROGRAM MODE



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$/PGM for read mode without impact on t_{ACC}

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$/PGM, whichever occurs first.

FUNCTIONAL DESCRIPTION

The μPD2716 operates from a single +5V power supply and, accordingly, is ideal for use with +5V microprocessors such as μPD8085 and μPD8048/8748.

Programming of the μPD2716 is achieved with a single 50 ms TTL pulse. Total programming time for all 16,384 bits is only 100 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be programmed easily and without any special programmer.

The μPD2716 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 525 mW to a maximum standby power dissipation of 132 mW. This results in a 75% savings with no increase in access time.

Erasure of the μPD2716 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2716. Consequently, if the μPD2716 is to be exposed to these types of lighting conditions for long periods of time, the μPD2716 window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2716 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm^2 power rating.

During erasure, the μPD2716 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

OPERATION

The five operation modes of the μPD2716 are listed in Table 1. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply should be at +25V during programming, program verification and program inhibit, and it should be at +5V during read and standby. $\overline{CE}$/PGM, $\overline{OE}$ and V_{PP} select the operation mode as shown in Table 1.

READ MODE

When $\overline{CE}$/PGM and $\overline{OE}$ are at low (0) level with V_{PP} at +5V, the READ MODE is set and the data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

STANDBY MODE

The μPD2716 is placed in the standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$/PGM and a V_{PP} of +5V. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced by 75% from 525 mW to 132 mW.

PROGRAMMING MODE

Programming of the μPD2716 is commenced by erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2716 is placed in the programming mode by applying a high (1) level TTL signal to the $\overline{OE}$ with V_{PP} at +25V. The data to be programmed is applied to the output pins 8 bits in parallel at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple μPD2716s are connected in parallel, except for $\overline{CE}$/PGM, individual μPD2716s can be programmed by applying a high (1) level TTL pulse to the $\overline{CE}$/PGM input of the desired μPD2716 to be programmed.

Programming of multiple μPD2716s in parallel with the same data is easily accomplished. All the alike inputs are tied together and are programmed by applying a high (1) level TTL pulse to the $\overline{CE}$/PGM inputs.

PROGRAMMING INHIBIT MODE

Programming of multiple μPD2716s in parallel with different data is rendered more easily by the program inhibit mode. Except for $\overline{CE}$/PGM, all alike inputs (including $\overline{OE}$) of the parallel μPD2716s may be common. Programming is accomplished by applying a TTL level program pulse to the μPD2716 $\overline{CE}$/PGM input with V_{PP} at +25V. A low level applied to the $\overline{CE}$/PGM of the other μPD2716 will inhibit it from being programmed.

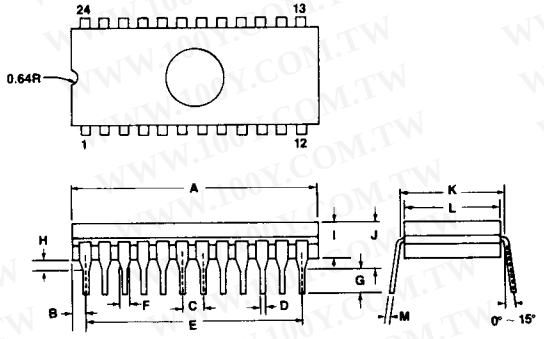
PROGRAM VERIFY MODE

A verify should be performed on the programmed bits to determine that the data was correctly programmed on all bits of the μPD2716. The program verify can be performed with V_{PP} at +25V and $\overline{CE}$/PGM and $\overline{OE}$ at low (0) levels.

OUTPUT DESELECTION

The data outputs of two or more μPD2716s may be wire-ored together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2716s should be deselected by raising the $\overline{OE}$ input to a TTL high.

PACKAGE OUTLINE μPD2716D (CERDIP)

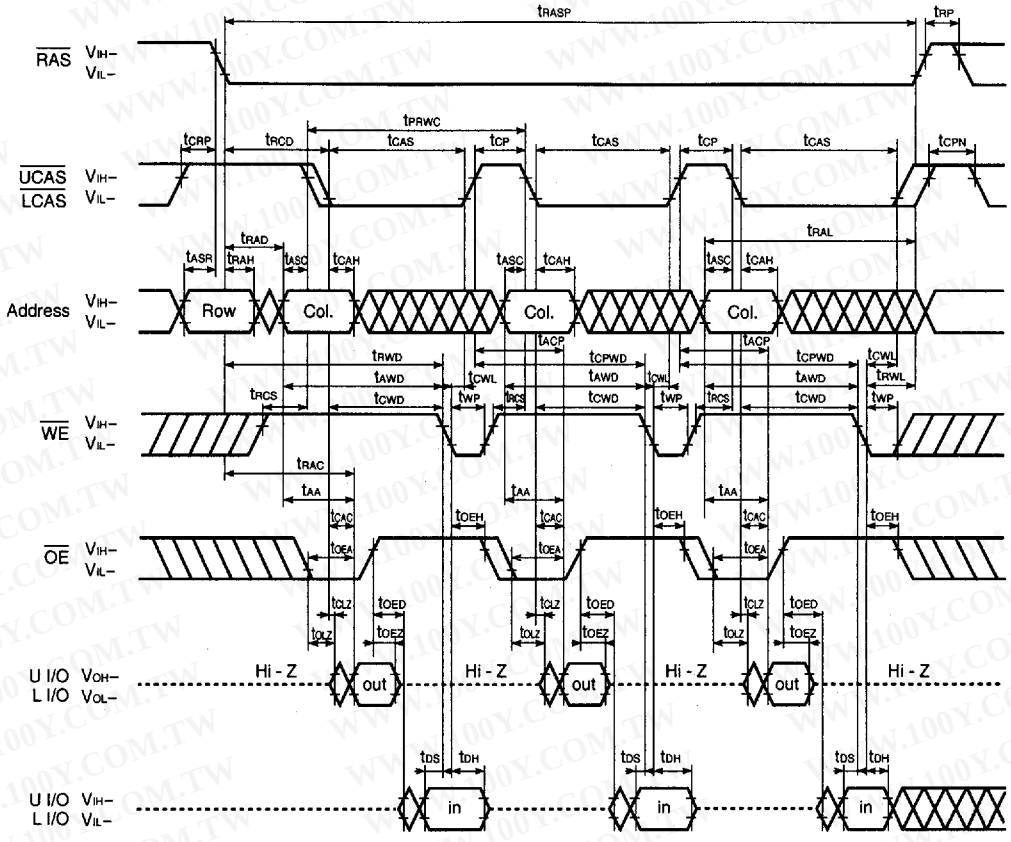


Item	Millimeters	Inches
A	33.5 MAX.	1.32 MAX.
B	2.78	1.1
C	2.54	0.1
D	0.46 ± 0.10	0.018 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.020
I	5.0 MAX.	0.20
J	5.5 MAX.	0.216
K	15.24	0.60
L	14.66	0.58
M	0.25 ± 0.05	0.010 ± 0.002

Window Label

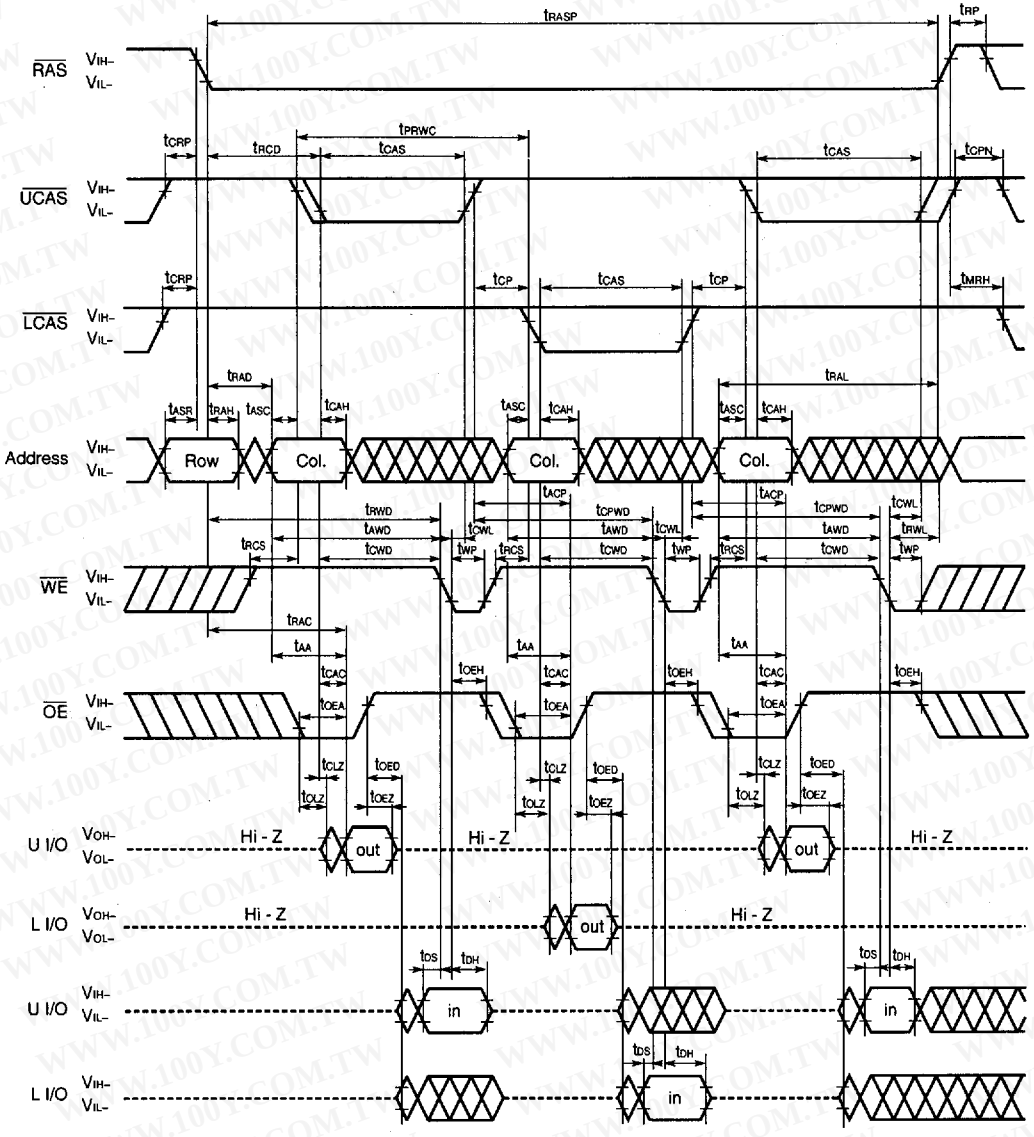
An amber-colored window label is provided unattached for the convenience of the user. The window label filters ultra-violet light frequencies, thus preventing accidental erasure or long-term degradation caused by ambient light or sunlight.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

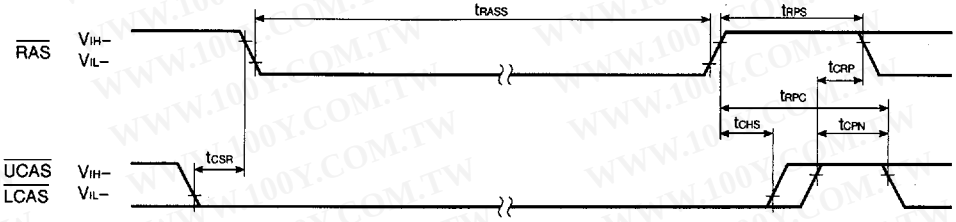
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

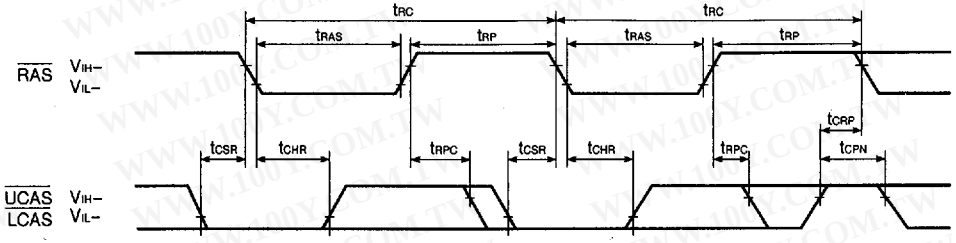
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles (t_{RAS} < 100 μs), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

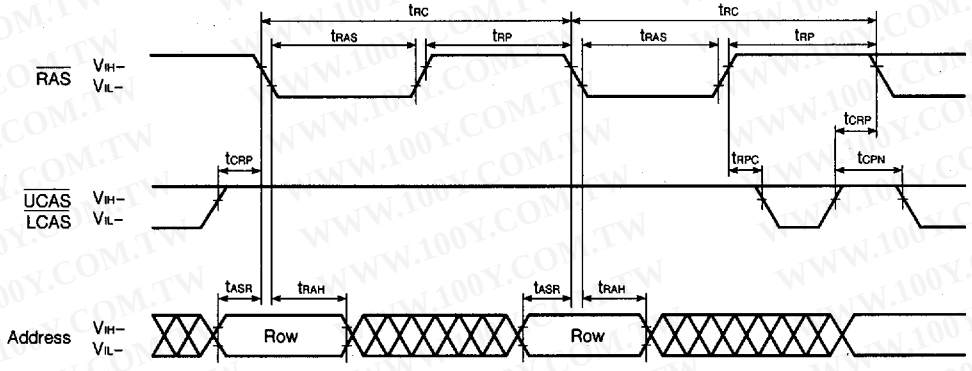
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)