

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4049BP,TC4049BF,TC4049BFN, TC4050BP,TC4050BF,TC4050BFN

TC4049B Hex Buffer/Converter (inverting type)

TC4050B Hex Buffer/Converter (non-inverting type)

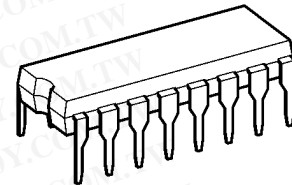
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC4049B, TC4050B contain six circuits of buffers. TC4049B is inverter type and TC4050B is non-inverter type.

Since one TTL or DTL can be directly driven having large output current, these are useful for interfacing from CMOS to TTL or DTL. As voltage up to $V_{SS} + 18$ volts can be applied to the input regardless of V_{DD} , these can be also used as the level converter IC's which converts CMOS logical circuits of 15 volts or 10 volts system to CMOS/TTL logical circuits of 5 volts system.

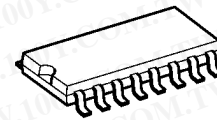
Ideal switching characteristic has been obtained by the circuit diagram of three stage inverters for TC4049B and two stage inverters for TC4050B.

TC4049BP, TC4050BP



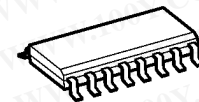
DIP16-P-300-2.54A

TC4049BF, TC4050BF



SOP16-P-300-1.27A

TC4049BFN, TC4050BFN



SOL16-P-150-1.27

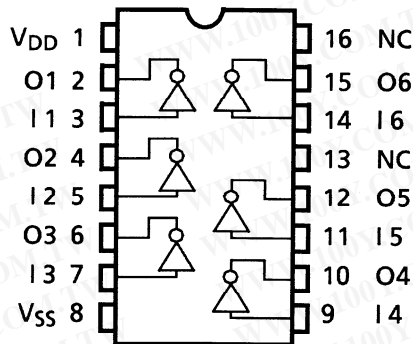
Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

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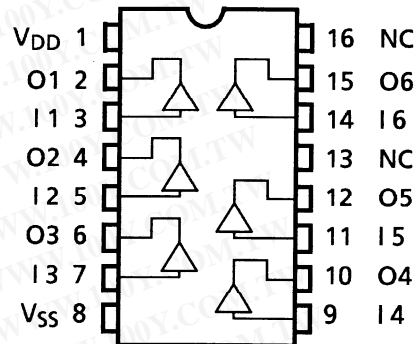
Pin Assignment

TC4049B



(TOP VIEW)

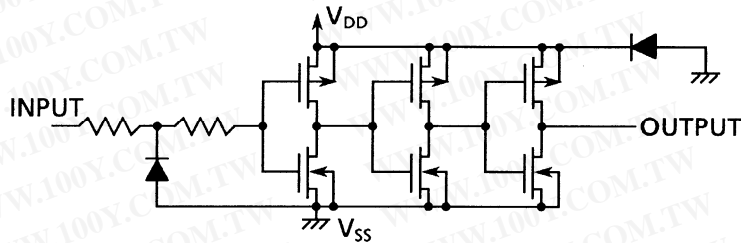
TC4050B



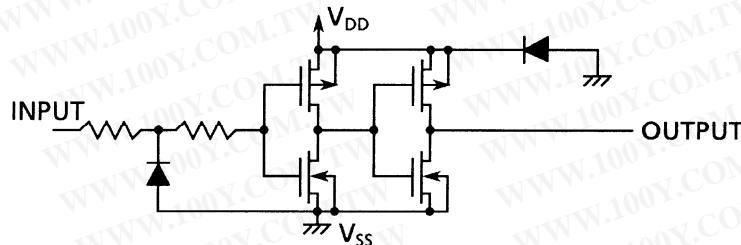
(TOP VIEW)

Circuit Diagram

1/6 TC4049B



1/6 TC4050B



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Output voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC input current	I_{IN}	± 10	mA
Power dissipation	P_D	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T_{opr}	-40~85	°C
Storage temperature range	T_{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges ($V_{SS} = 0\text{ V}$) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	18	V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{DD} or V_{SS} .

Static Electrical Characteristics ($V_{SS} = 0\text{ V}$)

Characteristics	Sym- bol	Test Condition	V_{DD} (V)	-40°C		25°C			85°C		Unit	
				Min	Max	Min	Typ.	Max	Min	Max		
High-level output voltage	V_{OH}	$ I_{OUT} < 1\ \mu\text{A}$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V	
			10	9.95	—	9.95	10.00	—	9.95	—		
			15	14.95	—	14.95	15.00	—	14.95	—		
Low-level output voltage	V_{OL}	$ I_{OUT} < 1\ \mu\text{A}$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V	
			10	—	0.05	—	0.00	0.05	—	0.05		
			15	—	0.05	—	0.00	0.05	—	0.05		
Output high current	I_{OH}	$V_{OH} = 4.6\text{ V}$ $V_{OH} = 2.5\text{ V}$ $V_{OH} = 9.5\text{ V}$ $V_{OH} = 13.5\text{ V}$ $V_{IN} = V_{SS}, V_{DD}$	5	-0.73	—	-0.65	-1.2	—	-0.58	—	mA	
			5	-2.40	—	-2.10	-3.9	—	-1.90	—		
			10	-1.80	—	-1.65	-2.5	—	-1.35	—		
			15	-4.80	—	-4.30	-8.0	—	-3.50	—		
Output low current	I_{OL}	$V_{OL} = 0.4\text{ V}$ $V_{OL} = 0.5\text{ V}$ $V_{OL} = 1.5\text{ V}$ $V_{IN} = V_{SS}, V_{DD}$	5	3.8	—	3.2	6.4	—	2.9	—	mA	
			10	9.6	—	8.0	16.0	—	6.6	—		
			15	28.0	—	24.0	48.0	—	20.0	—		
Input high voltage	V_{IH}	$V_{OUT} = 0.5\text{ V}, 4.5\text{ V}$ $V_{OUT} = 1.0\text{ V}, 9.0\text{ V}$ $V_{OUT} = 1.5\text{ V}, 13.5\text{ V}$ $ I_{OUT} < 1\ \mu\text{A}$	5	3.5	—	3.5	2.75	—	3.5	—	V	
			10	7.0	—	7.0	5.50	—	7.0	—		
			15	11.0	—	11.0	8.25	—	11.0	—		
Input low voltage	V_{IL}	$V_{OUT} = 0.5\text{ V}, 4.5\text{ V}$ $V_{OUT} = 1.0\text{ V}, 9.0\text{ V}$ $V_{OUT} = 1.5\text{ V}, 13.5\text{ V}$ $ I_{OUT} < 1\ \mu\text{A}$	5	—	1.5	—	2.25	1.5	—	1.5	V	
			10	—	3.0	—	4.50	3.0	—	3.0		
			15	—	4.0	—	6.75	4.0	—	4.0		
Input current	"H" level	I_{IH}	$V_{IH} = 18\text{ V}$	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
	"L" level	I_{IL}	$V_{IL} = 0\text{ V}$	18	—	-0.1	—	-10^{-5}	-0.1	—	-1.0	
Quiescent supply current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ (Note)	5	—	1	—	0.002	1	—	30	μA	
			10	—	2	—	0.004	2	—	60		
			15	—	4	—	0.008	4	—	120		

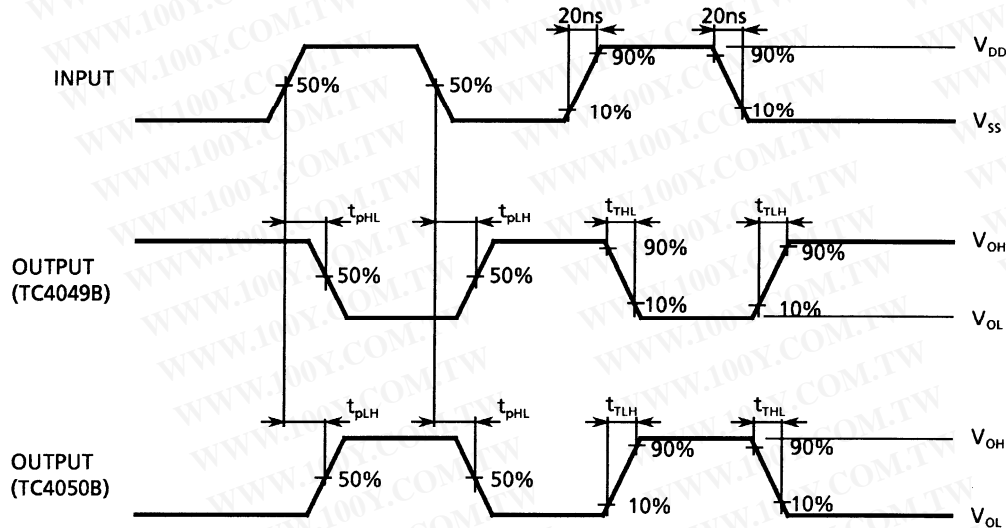
Note: All valid input combinations.

Dynamic Electrical Characteristics (Ta = 25°C, VSS = 0 V, CL = 50 pF)

Characteristics		Symbol	Test Condition	VDD (V)	Min	Typ.	Max	Unit
Output transition time (low to high)		t _{TLH}	—	5	—	60	160	ns
				10	—	30	80	
				15	—	25	60	
Output transition time (high to low)		t _{THL}	—	5	—	120	60	ns
				10	—	10	40	
				15	—	8	30	
TC4049B	Propagation delay time (low to high)	t _{pLH}	—	5	—	60	120	ns
				10	—	35	65	
				15	—	30	50	
	Propagation delay time (high to low)	t _{pHL}	—	5	—	40	60	ns
				10	—	20	30	
				15	—	15	20	
TC4050B	Propagation delay time (low to high)	t _{pLH}	—	5	—	50	130	ns
				10	—	30	70	
				15	—	25	55	
	Propagation delay time (high to low)	t _{pHL}	—	5	—	30	70	ns
				10	—	17	35	
				15	—	14	25	
Input capacitance		C _{IN}	—	—	5	7.5	pF	

Waveform for Measurement of Dynamic Characteristics

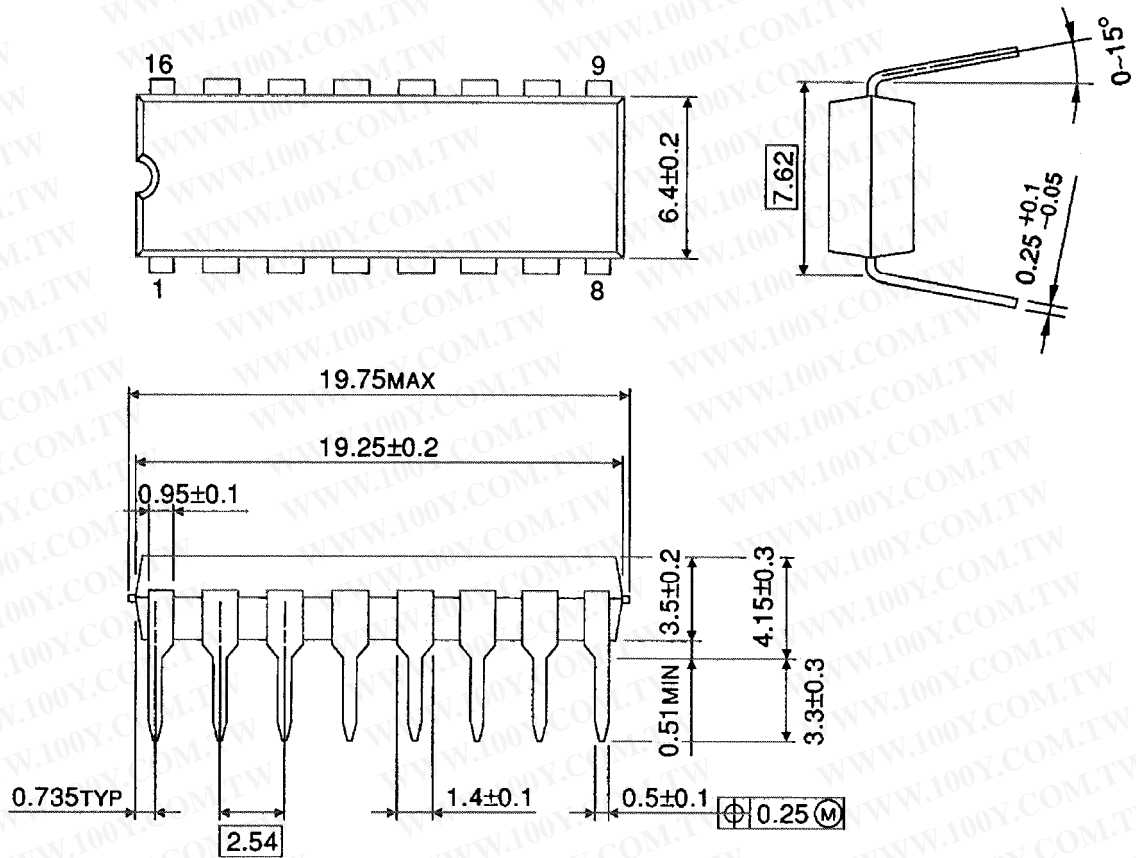
Waveform



Package Dimensions

DIP16-P-300-2.54A

Unit : mm

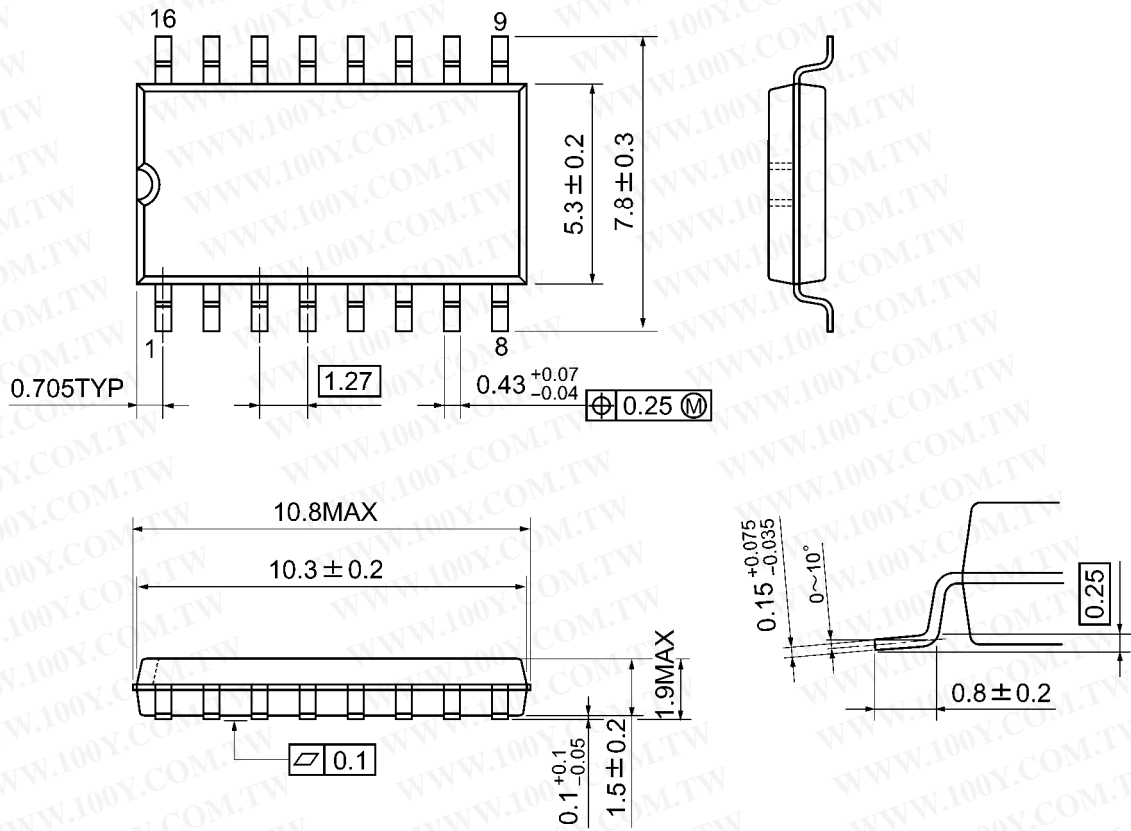


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm

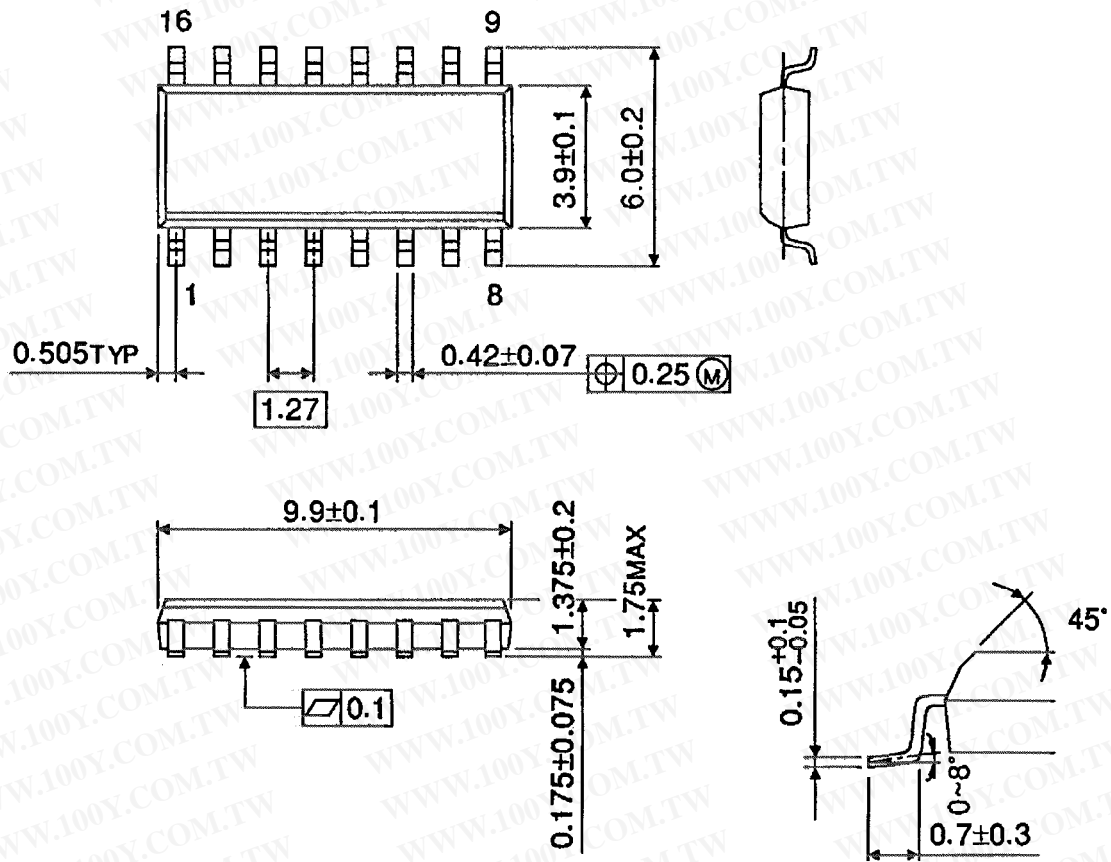


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Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)