

# SN54LVT16245A, SN74LVT16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143E – MAY 1992 – REVISED JANUARY 1996

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus™* Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16245A . . . WD PACKAGE  
SN74LVT16245A . . . DGG OR DL PACKAGE  
(TOP VIEW)

1DIR	1	48	$\overline{1OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
$V_{CC}$	7	42	$V_{CC}$
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
$V_{CC}$	18	31	$V_{CC}$
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	$\overline{2OE}$

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## description

The 'LVT16245A are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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 **TEXAS  
INSTRUMENTS**

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## description (continued)

The SN74LVT16245A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

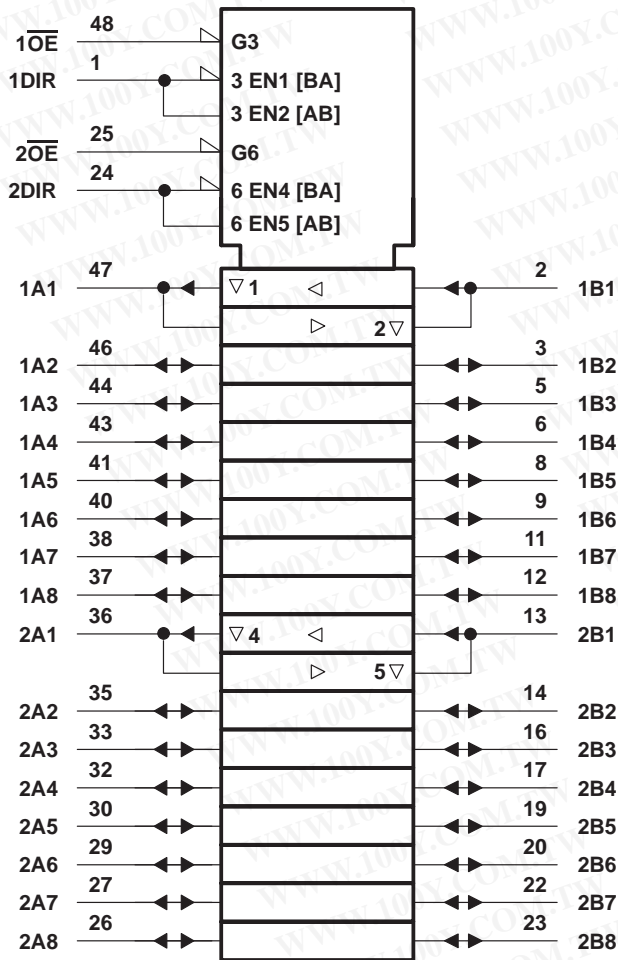
The SN54LVT16245A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVT16245A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each 8-bit section)

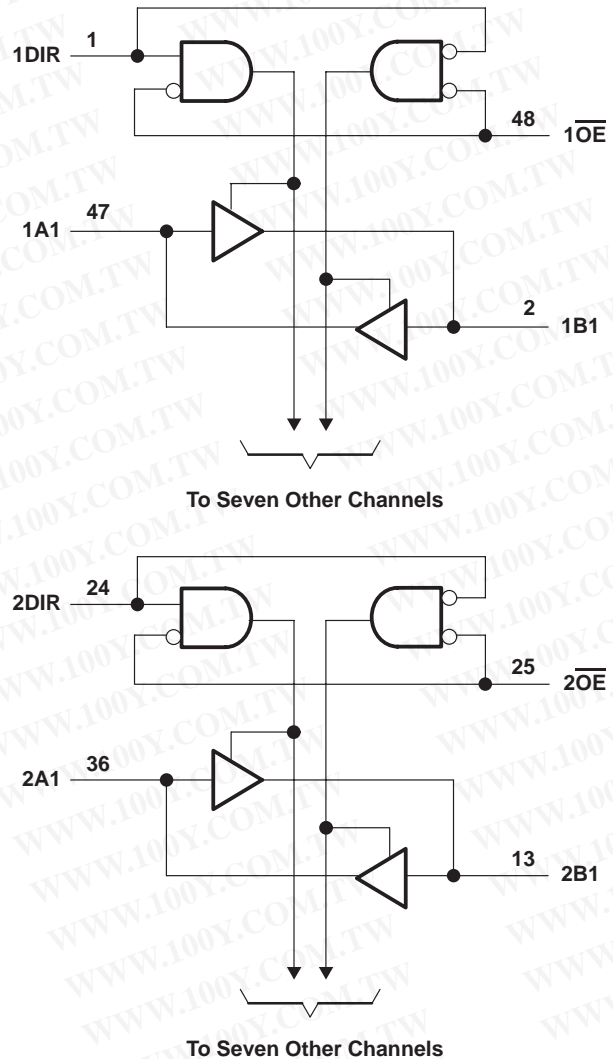
INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT16245A .....	96 mA
SN74LVT16245A .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT16245A .....	48 mA
SN74LVT16245A .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package .....	0.85 W
DL package .....	1.2 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## recommended operating conditions (see Note 4)

		SN54LVT16245A		SN74LVT16245A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16245A			SN74LVT16245A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V
$V_{OH}$	$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\ \mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$		2			2			
$V_{OL}$	$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\ \mu\text{A}$		0.2		0.2		V
			$I_{OL} = 24\text{ mA}$		0.5		0.5		
	$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4		0.4		
			$I_{OL} = 32\text{ mA}$		0.5		0.5		
			$I_{OL} = 48\text{ mA}$		0.55		0.55		
			$I_{OL} = 64\text{ mA}$				0.55		
$I_I$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND		Control inputs		$\pm 1$		$\pm 1$		$\mu\text{A}$
	$V_{CC} = 0$ or $\text{MAX}^\ddagger$ , $V_I = 5.5\text{ V}$				10		10		
	$V_{CC} = 3.6\text{ V}$		A or B ports§		100		20		
					$V_I = V_{CC}$		1		
$V_I = 0$				-5		-5			
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$						$\pm 100$		$\mu\text{A}$
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75		75		$\mu\text{A}$
			$V_I = 2\text{ V}$		-75		-75		
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$				5		1		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$				-5		-1		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND, $I_O = 0$		Outputs high		0.09		0.09		mA
			Outputs low		5		5		
			Outputs disabled		0.09		0.09		
$\Delta I_{CC}^\parallel$	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND				0.2		0.2		mA
$C_i$	$V_I = 3\text{ V}$ or 0				4		4		pF
$C_{io}$	$V_O = 3\text{ V}$ or 0				11		11		pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at  $V_{CC}$  or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16245A				SN74LVT16245A				UNIT	
			$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V			$V_{CC} = 2.7$ V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t <sub>PLH</sub>	A or B	B or A	0.5	4.4	5.3		1	2.4	4.1	5		ns
t <sub>PHL</sub>			0.5	4.7	5.5		1	2.3	4.1	5.2		
t <sub>PZH</sub>	$\overline{OE}$	A or B	0.5	7	7.7		1	3	5.3	6.3		ns
t <sub>PZL</sub>			0.5	5.8	7.2		1	3.1	5.2	6.7		
t <sub>PHZ</sub>	$\overline{OE}$	A or B	1	7.2	7.7		2.7	4.6	6.4	7.2		ns
t <sub>PLZ</sub>			1	6.3	6.5		2.6	4.3	5.8	6.1		

† All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$ .

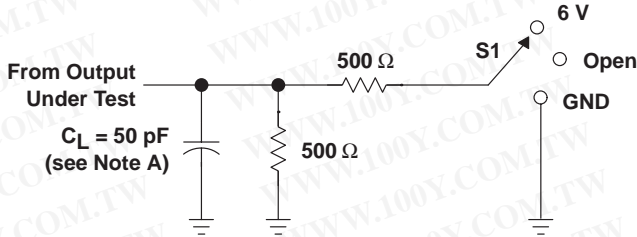
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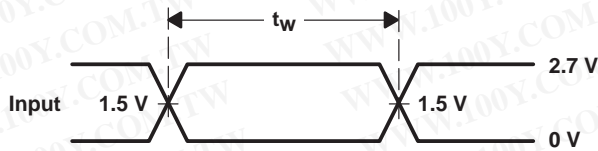
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## PARAMETER MEASUREMENT INFORMATION

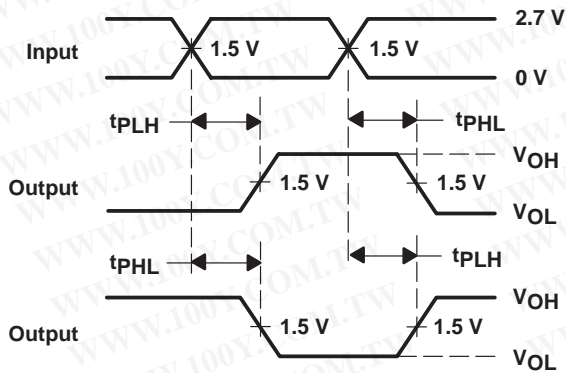


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

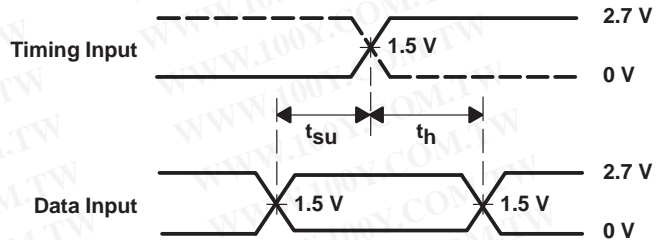
### LOAD CIRCUIT FOR OUTPUTS



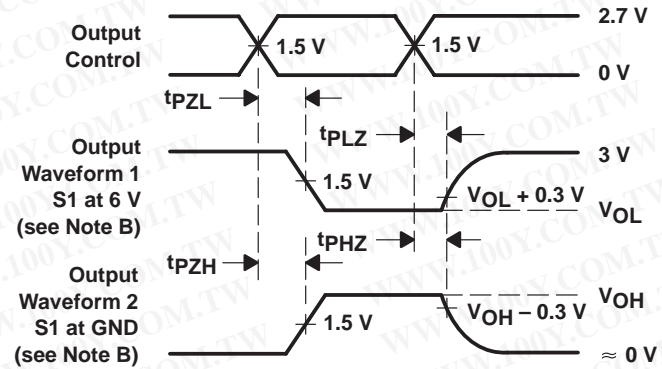
### VOLTAGE WAVEFORMS PULSE DURATION



### VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



### VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



### VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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