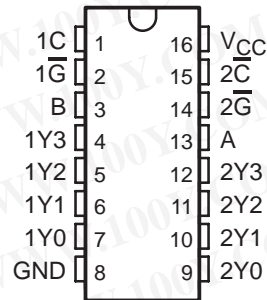


# SN74ALS156 DECODER/DEMULTIPLEXER WITH OPEN-COLLECTOR OUTPUTS

SDAS099C – JUNE 1986 – REVISED MAY 1996

- **Applications:**
  - Dual 2-Line to 4-Line Decoder
  - Dual 1-Line to 4-Line Demultiplexer
  - 3-Line to 8-Line Decoder
  - 1-Line to 8-Line Demultiplexer
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs**

D OR N PACKAGE  
(TOP VIEW)



## description

One of the main applications of the SN74ALS156 is as a dual 1-line to 4-line decoder/demultiplexer with individual strobes ( $\overline{G}$ ) and common binary-address inputs in a single 16-pin package. When both sections are enabled, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit enabling or disabling each of the 4-bit sections, as desired.

Data applied to input 1C is inverted at its outputs and data applied at input  $2\overline{C}$  is not inverted through its outputs. The inverter following the 1C data input permits use of the SN74ALS156 as a 3-line to 8-line demultiplexer without external gating. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

The SN74ALS156 is characterized for operation from 0°C to 70°C.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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**Function Tables**

**2-LINE TO 4-LINE DECODER OR  
 1-LINE TO 4-LINE DEMULTIPLEXER**

INPUTS				OUTPUTS			
SELECT		STROBE 1G	DATA 1C	1Y0	1Y1	1Y2	1Y3
B	A						
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

**2-LINE TO 4-LINE DECODER OR  
 1-LINE TO 4-LINE DEMULTIPLEXER**

INPUTS				OUTPUTS			
SELECT		STROBE 2G	DATA 2C	2Y0	2Y1	2Y2	2Y3
B	A						
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

**3-LINE TO 8-LINE DECODER OR  
 1-LINE TO 8-LINE DEMULTIPLEXER**

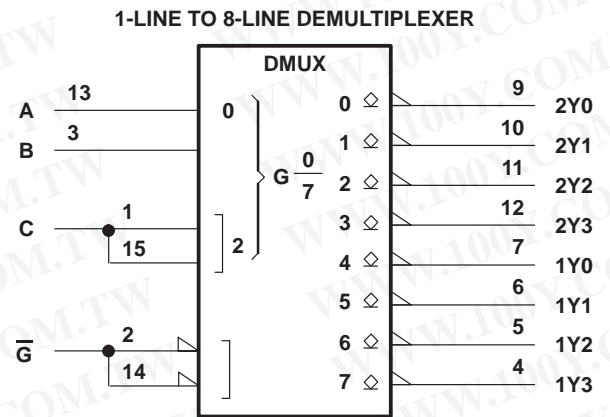
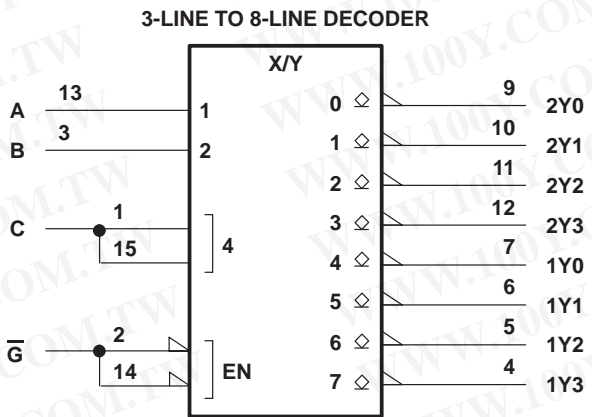
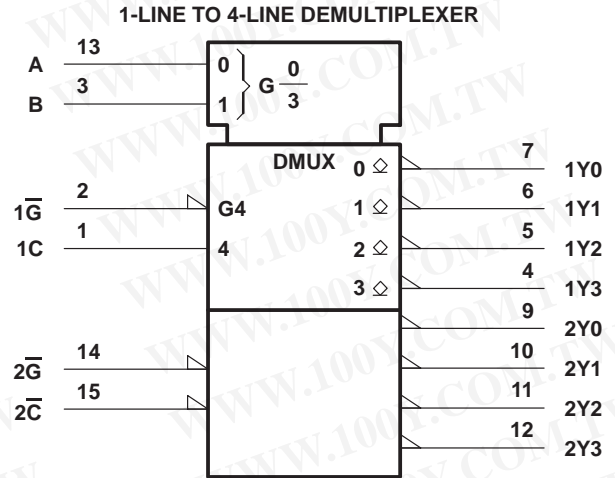
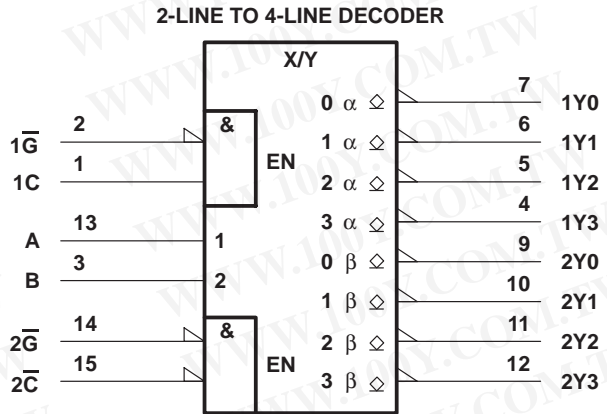
INPUTS				OUTPUTS							
SELECT			STROBE OR DATA G†	0	1	2	3	4	5	6	7
C†	B	A		2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	L	H	H	H
L	L	H	L	H	L	H	H	H	L	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	L	H	H	H	L	H
H	H	H	L	H	H	H	L	H	H	H	L

†C = inputs 1C and 2C connected together

‡G = inputs 1G and 2G connected together



logic symbols† (alternatives)



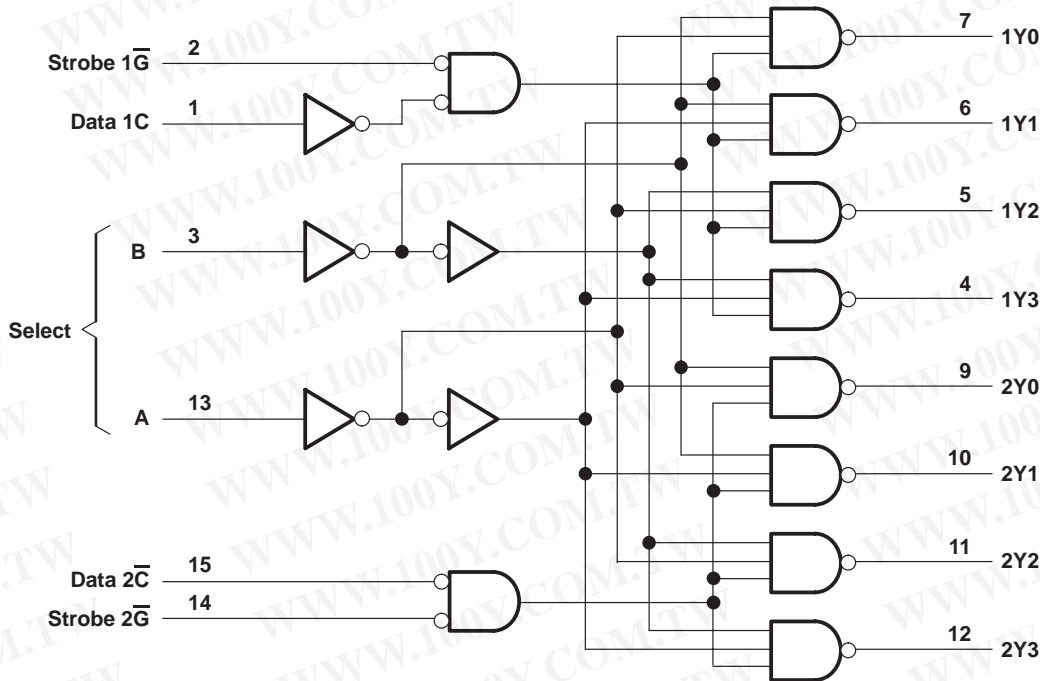
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN74ALS156**  
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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OH}$	High-level output voltage			5.5	V
$I_{OL}$	Low-level output current			8	mA
$T_A$	Operating free-air temperature	0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5 V,$	$I_I = -18 mA$			-1.5	V
$V_{OL}$	$V_{CC} = 4.5 V$	$I_{OL} = 4 mA$		0.25	0.4	V
		$I_{OL} = 8 mA$		0.35	0.5	
$I_{OH}$	$V_{CC} = 4.5 V,$	$V_{OH} = 5.5 V$			0.1	mA
$I_I$	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			20	$\mu A$
$I_{IL}$	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.1	$\mu A$
$I_{CCL}$	$V_{CC} = 5.5 V$			5	9	mA

† All typical values are at  $V_{CC} = 5 V, T_A = 25^\circ C$ .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 V$ to $5.5 V,$ $C_L = 50 pF,$ $R_L = 500 \Omega,$ $T_A = MIN$ to $MAX^\ddagger$		UNIT
			MIN	MAX	
$t_{PLH}$	A, B	1Y, 2Y	7	55	ns
$t_{PHL}$			6	25	
$t_{PLH}$	1C	1Y	7	50	ns
$t_{PHL}$			6	23	
$t_{PLH}$	$1\bar{G}$	1Y	7	38	ns
$t_{PHL}$			6	22	
$t_{PLH}$	$2\bar{C}, 2\bar{G}$	2Y	7	38	ns
$t_{PHL}$			6	22	

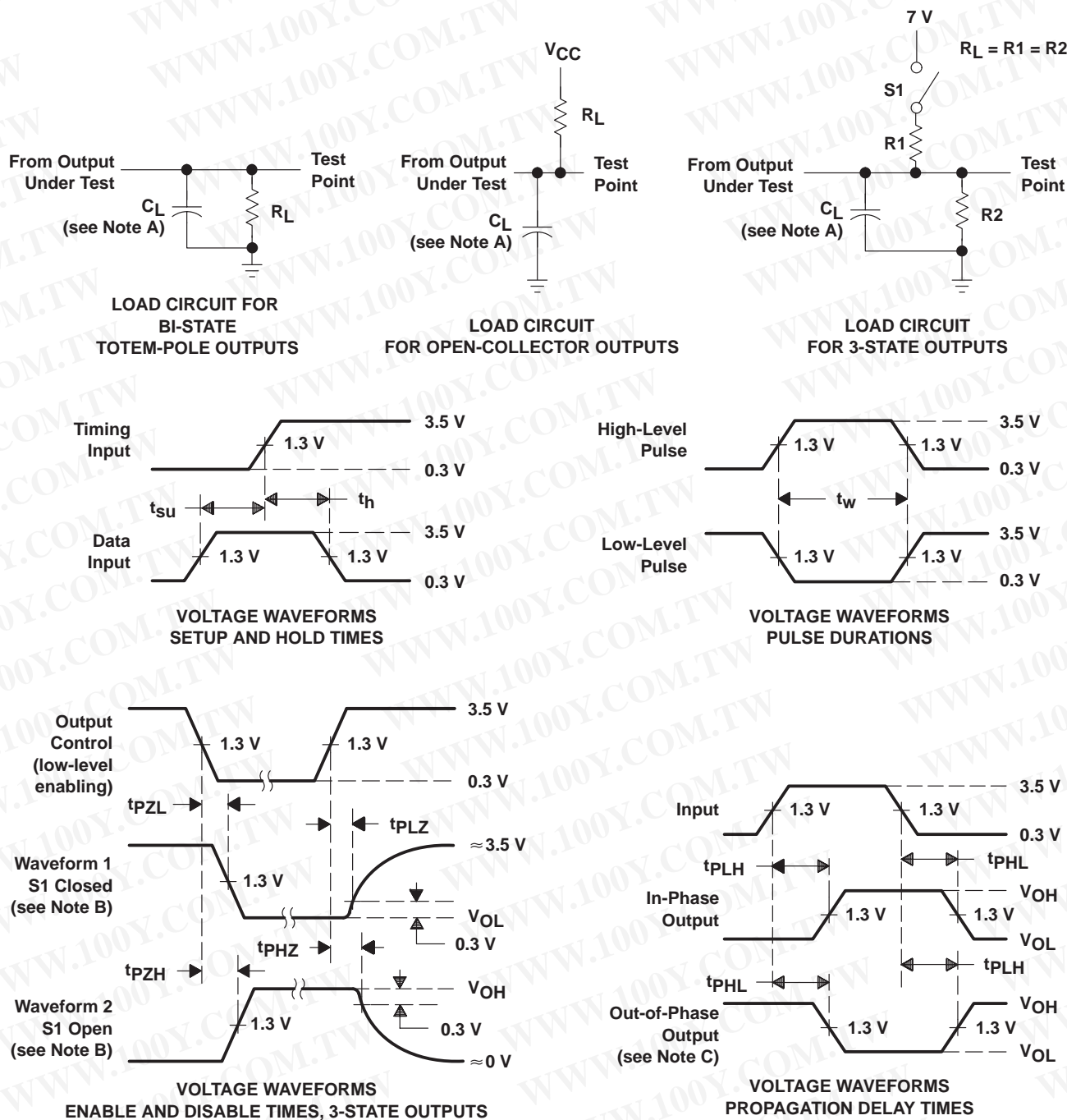
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN74ALS156**  
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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  - D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.
  - E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**



PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS156D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS156DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS156DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS156DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS156DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS156N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS156NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

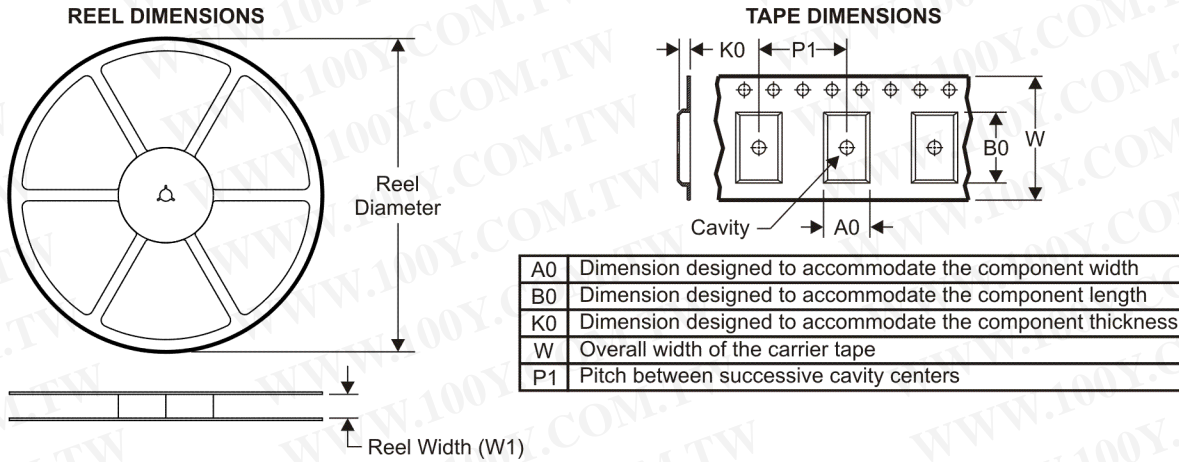
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

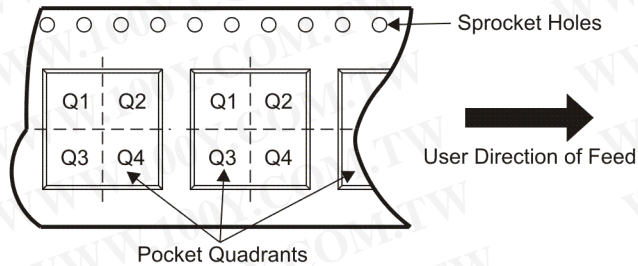
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**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

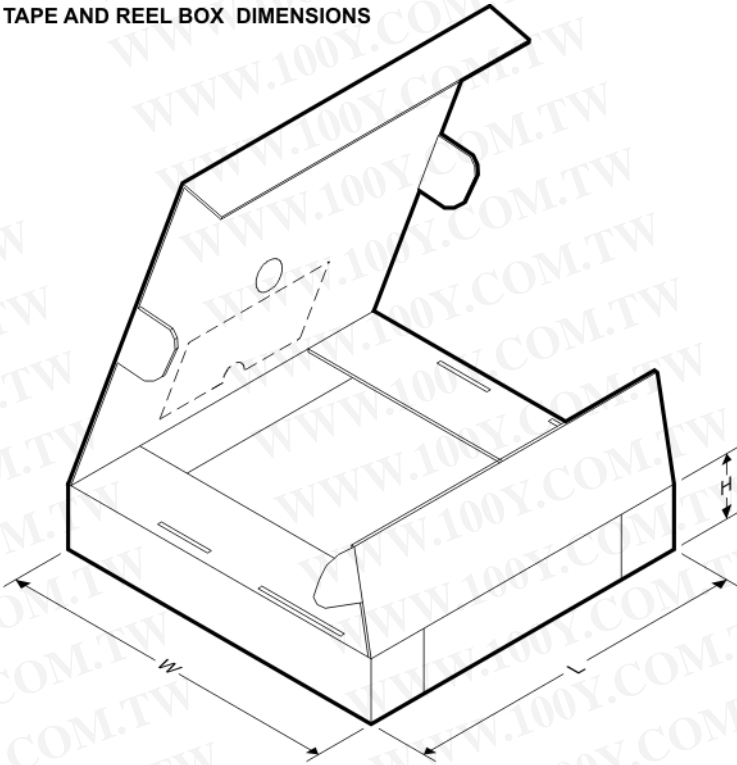


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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS156DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



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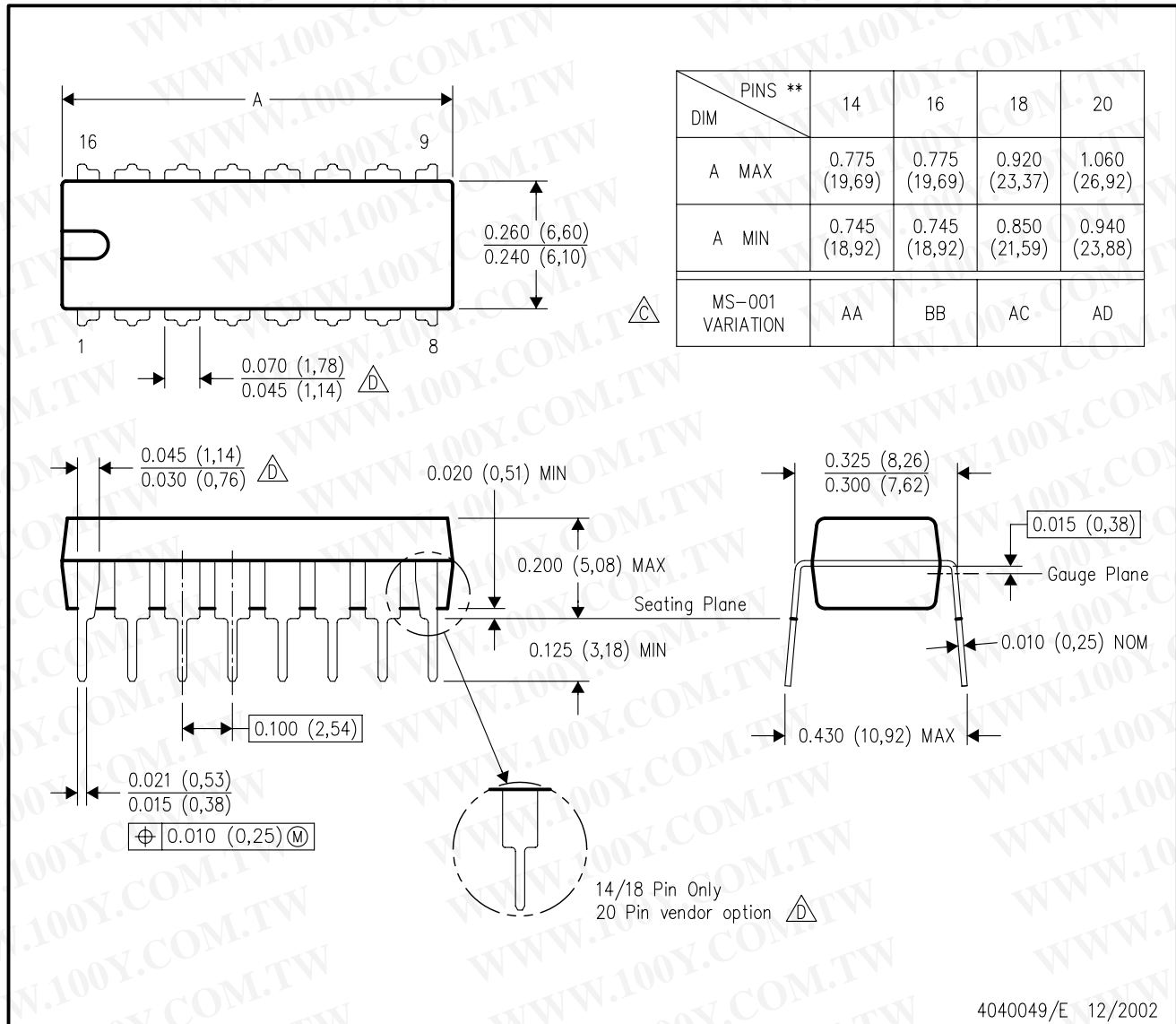
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS156DR	SOIC	D	16	2500	333.2	345.9	28.6

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

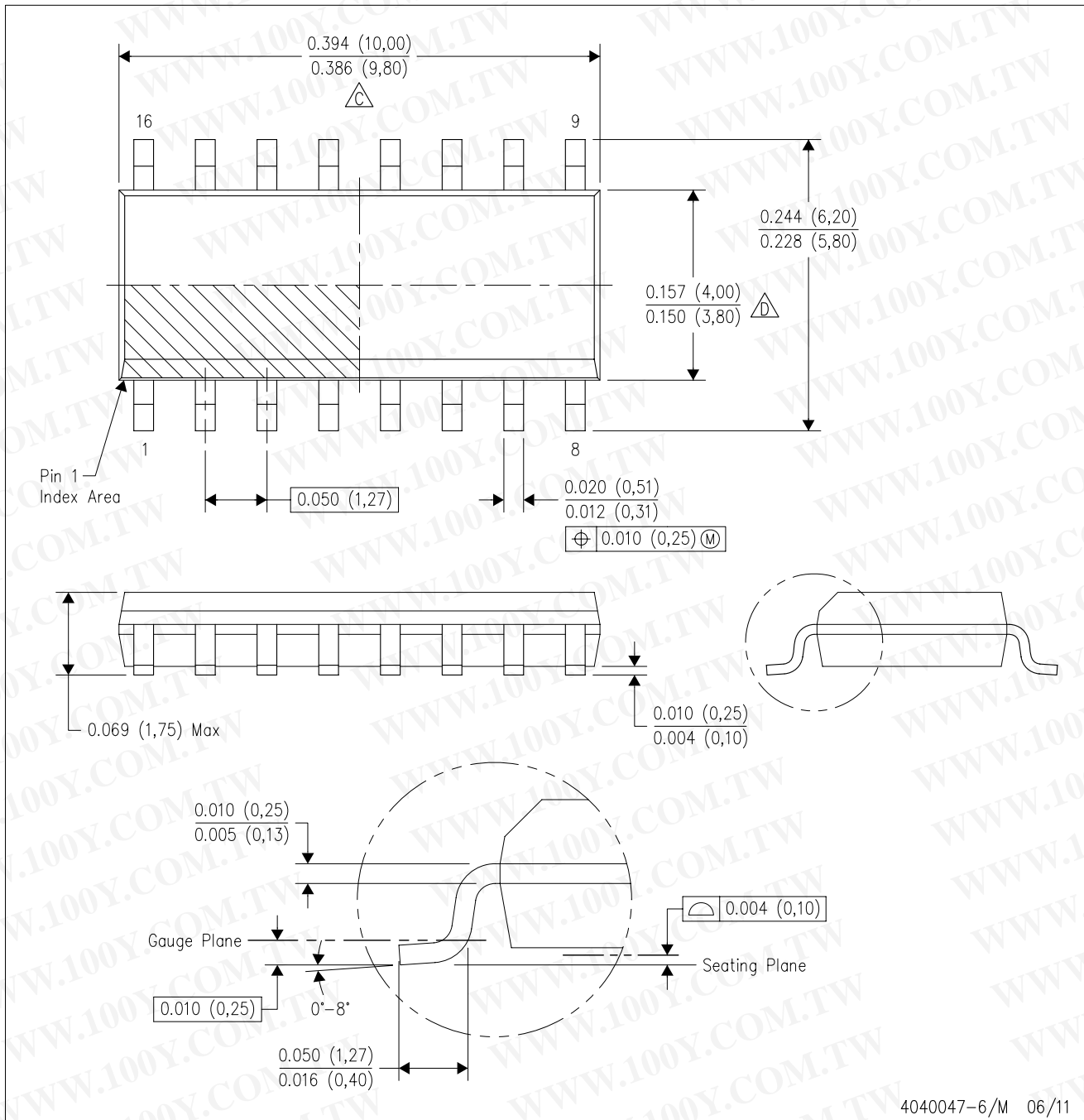
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

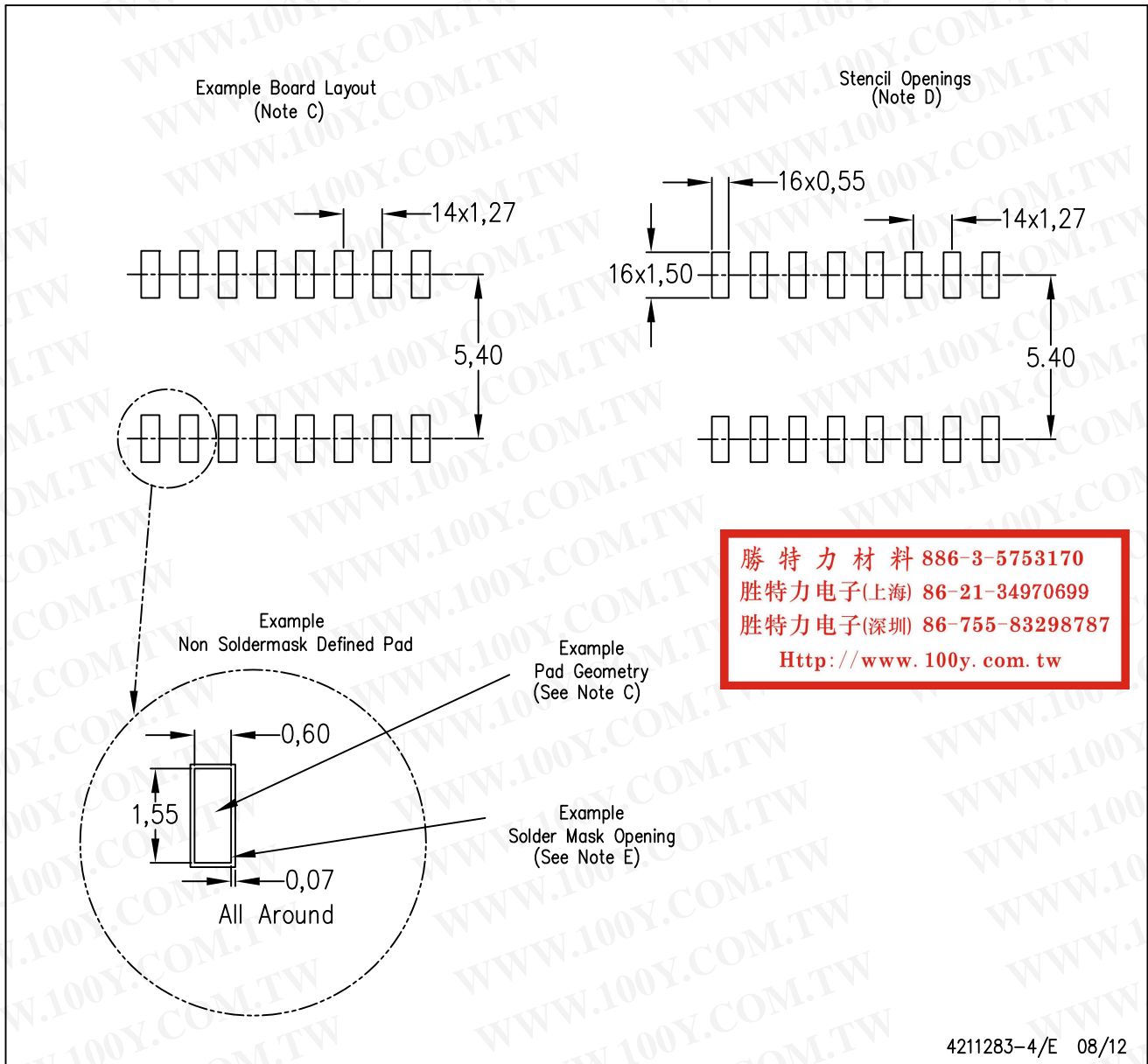


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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