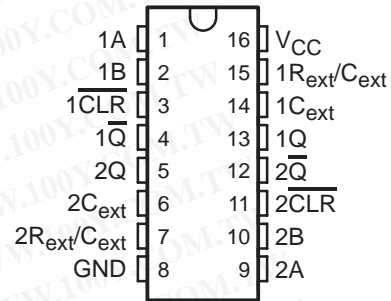


SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

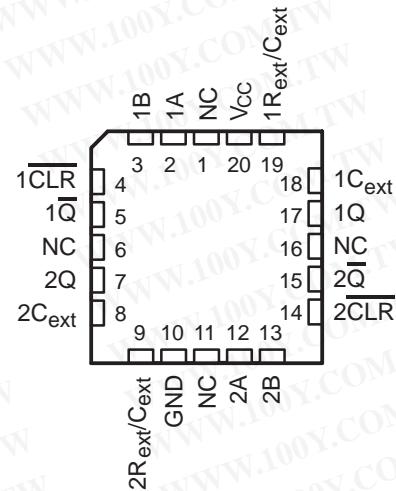
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- Dual Versions of Highly Stable SN54121 and SN74121 One Shots
- SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121 and SN74121 One Shots
- Pinout Is Identical to the SN54123, SN74123, SN54LS123, and SN74LS123
- Overriding Clear Terminates Output Pulse

SN54221, SN54LS221 . . . J PACKAGE
SN74221 . . . N PACKAGE
SN74LS221 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



SN54LS221 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

MAXIMUM
OUTPUT
PULSE
LENGTH(S)

| TYPE | MAXIMUM OUTPUT PULSE LENGTH(S) |
|-----------|---|
| SN54221 | 21 |
| SN74221 | 28 |
| SN54LS221 | 49 |
| SN74LS221 | 70 |

description/ordering information

The '221 and 'LS221 devices are dual multivibrators with performance characteristics virtually identical to those of the '121 devices. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input.

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ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74221N | SN74221N |
| | | Tube | SN74LS221N | SN74LS221N |
| | SOIC – D | Tube | SN74LS221D | LS221 |
| | | Tape and reel | SN74LS221DR | |
| | | Tape and reel | SN74LS221NSR | |
| –55°C to 125°C | SSOP – DB | Tape and reel | SN74LS221DBR | LS221 |
| | CDIP – J | Tube | SNJ54221J | SNJ54221J |
| | | Tube | SNJ54LS221J | SNJ54LS221J |
| | LCCC – FK | Tube | SNJ54LS221FK | SNJ54LS221FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

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description/ordering information (continued)

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition at rates as slow as 1 V/s, providing the circuit with excellent noise immunity, typically of 1.2 V. A high immunity to V_{CC} noise, typically of 1.5 V, also is provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses can be of any duration relative to the output pulse. Output pulse length can be varied from 35 ns to the maximum by choosing appropriate timing components. With $R_{ext} = 2 \text{ k}\Omega$ and $C_{ext} = 0$, an output pulse typically of 30 ns is achieved that can be used as a dc-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are shown as a part of the switching characteristics waveforms.

Pulse-width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability is limited only by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54221, 2 k Ω to 40 k Ω for the SN74221, 2 k Ω to 70 k Ω for the SN54LS221, and 2 k Ω to 100 k Ω for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_w(\text{out}) = C_{ext}R_{ext} \ln 2 \approx 0.7 C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 k Ω can be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 V and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T . Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device typically is less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the '221 is shown in Figure 3. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figures 4 and 5, respectively.

Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 devices can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext} ; however, the polarity of the capacitor must be changed.

FUNCTION TABLE
(each monostable multivibrator)

| INPUTS | | | OUTPUTS | |
|-------------------------|--------------|------------|---------|-----------------------|
| $\overline{\text{CLR}}$ | A | B | Q | $\overline{\text{Q}}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | \uparrow | | |
| H | \downarrow | H | | |
| $\uparrow\ddagger$ | L | H | | |

\dagger Pulsed-output patterns are tested during AC switching at 25°C with $R_{ext} = 2 \text{ k}\Omega$, and $C_{ext} = 80 \text{ pF}$.

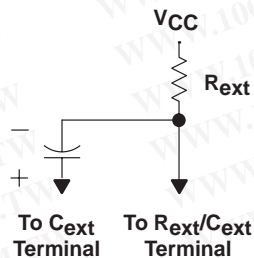
\ddagger This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logic 1 state prior to $\overline{\text{CLR}}$ going high. This latch is conditioned by taking either A high or B low while $\overline{\text{CLR}}$ is inactive (high).

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timing component connections



NOTE: Due to the internal circuit, the R_{ext}/C_{ext} terminal never is more positive than the C_{ext} terminal.

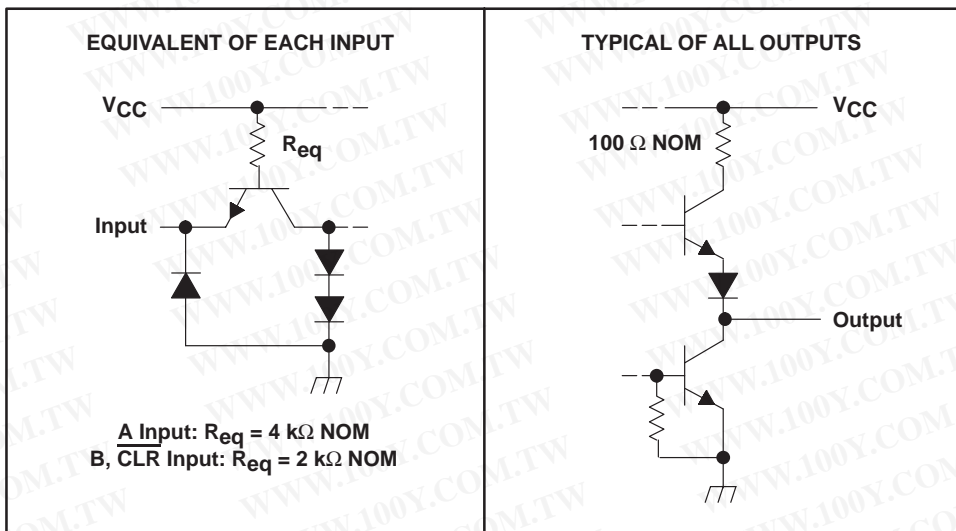
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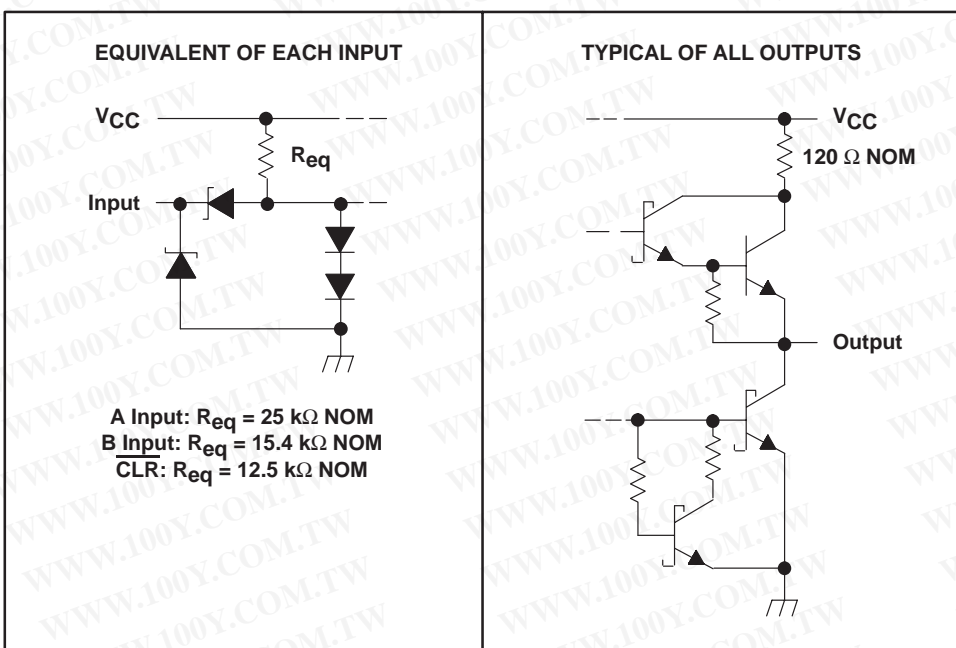
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schematics of inputs and outputs

SN54/74221



SN54/74LS221



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SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range, V_{CC} | 7 V |
| Input voltage range, V_I (see Note 1): 'LS221 | 7 V |
| '221 | 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| DB package | 82°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | SN54221 | | | SN74221 | | | UNIT |
|--|---------|-----|------|---------|-----|------|------------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| I_{OH} High-level output current | | | -800 | | | -800 | μ A |
| I_{OL} Low-level output current | | | 16 | | | 16 | mA |
| $\Delta v/\Delta t$ Rise or fall of input pulse rate | B input | | 1* | 1 | | | V/s |
| | A input | | 1* | 1 | | | V/ μ s |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54221 | | | SN74221 | | | UNIT |
|---------------|---|--|---------|------|------|---------|------|------|---------------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{T+} | Positive-going threshold voltage, B input | $V_{CC} = \text{MIN}$ | | 1.55 | 2* | | 1.55 | 2 | V |
| V_{T-} | Negative-going threshold voltage, B input | $V_{CC} = \text{MIN}$ | 0.8* | 1.35 | | 0.8 | 1.35 | | V |
| V_{IK} | | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | | $V_{CC} = \text{MIN}, I_{OH} = -800 \mu\text{A}$ | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V_{OL} | | $V_{CC} = \text{MIN}, I_{OL} = 16 \text{ mA}$ | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I_I | | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} | A input | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$ | | | 40 | | | 40 | μA |
| | $\overline{\text{CLR}}$, B input | | | | 80 | | | 80 | |
| I_{IL} | A input | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | -1.6 | | | -1.6 | mA |
| | $\overline{\text{CLR}}$, B input | | | | -3.2 | | | -3.2 | |
| I_{OS}^{\S} | | $V_{CC} = \text{MAX}$ | -20 | | -55 | -18 | | -55 | mA |
| I_{CC} | Quiescent | $V_{CC} = \text{MAX}$ | | 26 | 50* | | 26 | 50 | mA |
| | Triggered | | | 46 | 80* | | 46 | 80 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | | SN54221 | | SN74221 | | UNIT |
|-----------|-----------------------------|---------------------------------|---------|-------|---------|------|---------------|
| | | | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | A or B input | 50 | | 50 | | ns |
| | | $\overline{\text{CLR}}$ | 20 | | 20 | | |
| t_{su} | Setup time, inactive-state¶ | $\overline{\text{CLR}}$ | 15 | | 15 | | ns |
| R_{ext} | External timing resistance | | 1.4* | 30* | 1.4 | 40 | k Ω |
| C_{ext} | External timing capacitance | | 0* | 1000* | 0 | 1000 | μF |
| | Output duty cycle | $R_{ext} = 2 \text{ k}\Omega$ | | 67% | | 67% | |
| | | $R_{ext} = \text{MAX } R_{ext}$ | | 90% | | 90% | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

¶ Inactive-state setup time also is referred to as recovery time.

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switching characteristics $V_{CC} = 5\text{ V}$, $R_L = 400\ \Omega$, $T_A = 25^\circ\text{C}$ (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54221 | | | SN74221 | | | UNIT |
|-----------|------------------|---------------------|--|---------|-----|------|---------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t_{PLH} | A | Q | $C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$ | | 45 | 70 | | 45 | 70 | ns |
| | B | | | | 35 | 55 | | 35 | 55 | |
| t_{PHL} | A | \overline{Q} | | | 50 | 80 | | 50 | 80 | |
| | B | | | | 40 | 65 | | 40 | 65 | |
| t_{PHL} | \overline{CLR} | Q | $C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$ | | | | | 27 | ns | |
| t_{PLH} | | \overline{Q} | | | | | | 40 | | |
| t_w | A or B | Q or \overline{Q} | $C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$ | 70 | 110 | 150 | 70 | 110 | 150 | ns |
| | | | $C_{ext} = 0$, $R_{ext} = 2\text{ k}\Omega$ | 17 | 30 | 50 | 17 | 30 | 50 | |
| | | | $C_{ext} = 100\text{ pF}$, $R_{ext} = 10\text{ k}\Omega$ | 650 | 700 | 750 | 650 | 700 | 750 | |
| | | | $C_{ext} = 1\ \mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$ | 6.5* | 7 | 7.5* | 6.5 | 7 | 7.5 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

recommended operating conditions (see Note 4)

| | | SN54LS221 | | | SN74LS221 | | | UNIT |
|---------------------|----------------------------------|-----------|-----|------|-----------|-----|------|------------------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| I_{OH} | High-level output current | | | -400 | | | -400 | μA |
| I_{OL} | Low-level output current | | | 4 | | | 8 | mA |
| $\Delta v/\Delta t$ | Rise or fall of input pulse rate | B input | | 1* | | 1 | | V/s |
| | | A input | | 1* | | 1 | | V/ μs |
| T_A | Operating free-air temperature | | -55 | 125 | | 0 | 70 | $^\circ\text{C}$ |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54LS221 | | | SN74LS221 | | | UNIT | |
|---------------|---|---|-------------------------|------|------|-----------|-------------------------|------|---------------|-----|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V_{T+} | Positive-going threshold voltage, B input | $V_{CC} = \text{MIN}$ | | 1 | 2* | | 1 | 2 | V | |
| V_{T-} | Negative-going threshold voltage, B input | $V_{CC} = \text{MIN}$ | 0.7* | 0.9 | | 0.8 | 0.9 | | V | |
| V_{IK} | | $V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$ | | | -1.5 | | | -1.5 | V | |
| V_{OH} | | $V_{CC} = \text{MIN}$, $I_{OH} = -400 \mu\text{A}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V | |
| V_{OL} | | $V_{CC} = \text{MIN}$ | $I_{OL} = 4 \text{ mA}$ | | 0.25 | 0.4 | $I_{OL} = 4 \text{ mA}$ | | 0.25 | 0.4 |
| | | | $I_{OL} = 8 \text{ mA}$ | | | | $I_{OL} = 8 \text{ mA}$ | | 0.35 | 0.5 |
| I_I | | $V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$ | | | 0.1 | | | 0.1 | mA | |
| I_{IH} | | $V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$ | | | 20 | | | 20 | μA | |
| I_{IL} | A input | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | | -0.4 | | | -0.4 | mA | |
| | $\overline{\text{CLR}}$, B input | | | | -0.8 | | | -0.8 | | |
| I_{OS}^{\S} | | $V_{CC} = \text{MAX}$ | -20 | | -100 | -20 | | -100 | mA | |
| I_{CC} | Quiescent | $V_{CC} = \text{MAX}$ | | 4.7 | 11 | | 4.7 | 11 | mA | |
| | Triggered | | | 19 | 27* | | 19 | 27 | | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | | SN54LS221 | | SN74LS221 | | UNIT |
|-----------|-----------------------------|-----------------------------|-----------|-------|-----------|------|---------------|
| | | | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | A or B | 50 | | 50 | | ns |
| | | $\overline{\text{CLR}}$ | 40 | | 40 | | |
| t_{su} | Setup time, inactive state¶ | $\overline{\text{CLR}}$ | 15 | | 15 | | ns |
| R_{ext} | External timing resistance | | 1.4* | 70* | 1.4 | 100 | k Ω |
| C_{ext} | External timing capacitance | | 0* | 1000* | 0 | 1000 | μF |
| | Output duty cycle | $R_T = 2 \text{ k}\Omega$ | | 50% | | 50% | |
| | | $R_T = \text{MAX } R_{ext}$ | | 90% | | 90% | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

¶ Inactive-state setup time also is referred to as recovery time.

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switching characteristics $V_{CC} = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54LS221 | | | SN74LS221 | | | UNIT | |
|-----------|------------------|---------------------|--|---|-----|------|-----------|-----|-----|------|----|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| t_{PLH} | A | Q | $C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$ | 45 | 70 | | 45 | 70 | ns | | |
| | B | | | 35 | 55 | | 35 | 55 | | | |
| t_{PHL} | A | \overline{Q} | | 50 | 80 | | 50 | 80 | | | |
| | B | | | 40 | 65 | | 40 | 65 | | | |
| t_{PHL} | \overline{CLR} | Q | | $C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$ | 35 | 55 | | 35 | | 55 | ns |
| t_{PLH} | | \overline{Q} | | | 44 | 65 | | 44 | | 65 | |
| t_w | A or B | Q or \overline{Q} | $C_{ext} = 80\text{ pF}$, $R_{ext} = 2\text{ k}\Omega$ | 70 | 120 | 150 | 70 | 120 | 150 | ns | |
| | | | $C_{ext} = 0$, $R_{ext} = 2\text{ k}\Omega$ | 20 | 47 | 70 | 20 | 47 | 70 | | |
| | | | $C_{ext} = 100\text{ pF}$, $R_{ext} = 10\text{ k}\Omega$ | 670 | 740 | 810 | 670 | 740 | 810 | | |
| | | | $C_{ext} = 1\text{ }\mu\text{F}$, $R_{ext} = 10\text{ k}\Omega$ | 6* | 6.9 | 7.5* | 6 | 6.9 | 7.5 | | ms |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

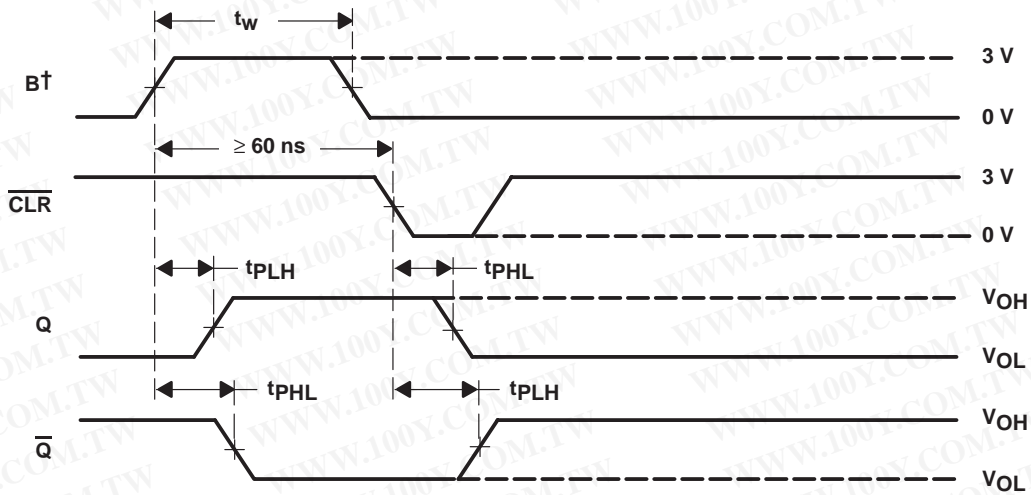
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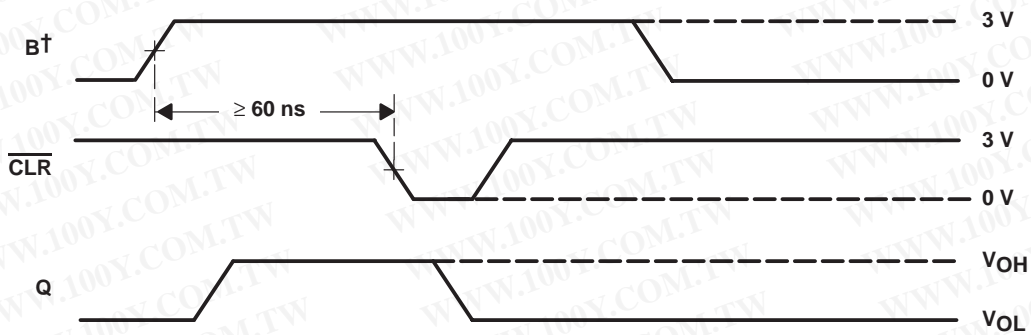
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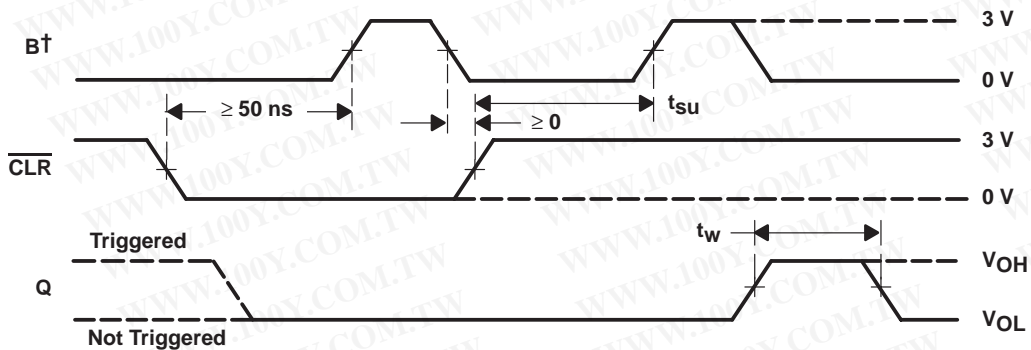
PARAMETER MEASUREMENT INFORMATION



CONDITION 1: TRIGGER FROM B, THEN $\overline{\text{CLR}}$



CONDITION 2: TRIGGER FROM B, THEN $\overline{\text{CLR}}$



CONDITION 3: $\overline{\text{CLR}}$ OVERRIDING B, THEN TRIGGER FROM B

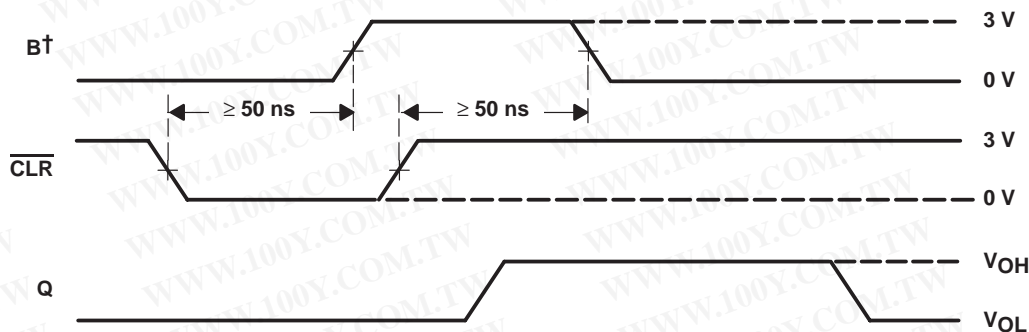
† A is low.

Figure 1. Switching Characteristics

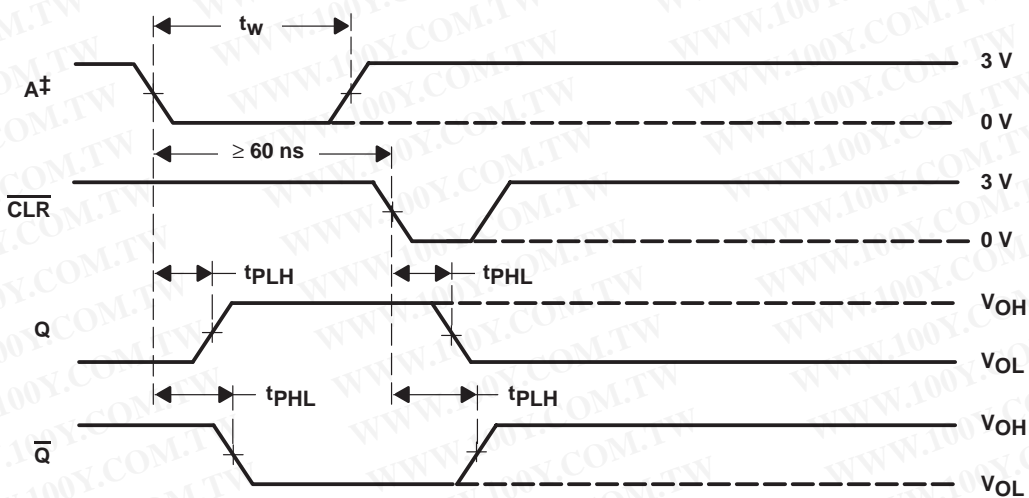


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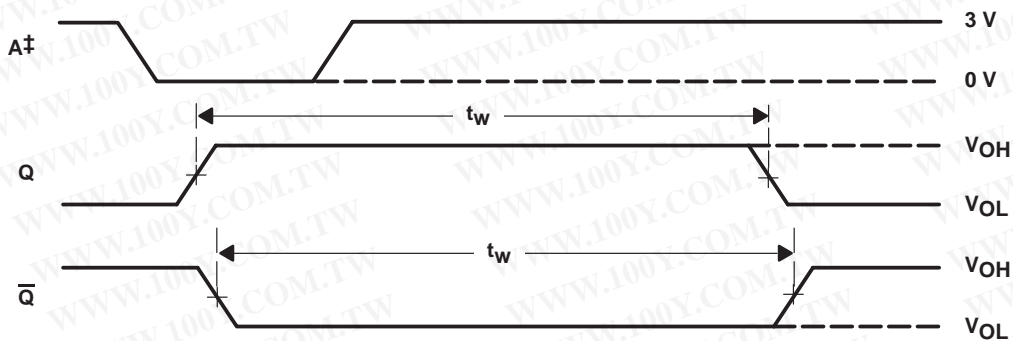
PARAMETER MEASUREMENT INFORMATION



CONDITION 4: TRIGGERING FROM POSITIVE TRANSITION OF $\overline{\text{CLR}}$



CONDITION 5: TRIGGER FROM A, THEN $\overline{\text{CLR}}$



CONDITION 6: TRIGGER FROM A

† A is low.
 ‡ B and $\overline{\text{CLR}}$ are high.

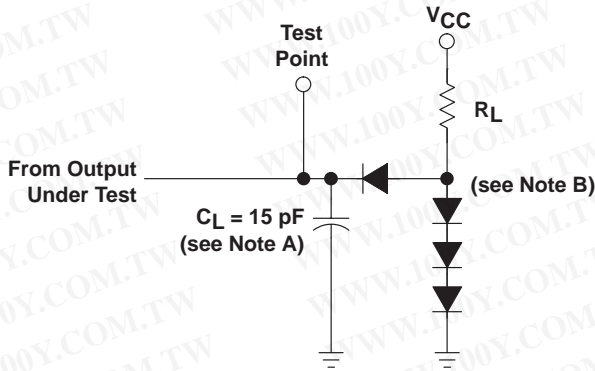
- NOTES: A. Input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, $Z_O \approx 50\Omega$; for SN54/74221, $t_r \leq 7 \text{ ns}$, $t_f \leq 7 \text{ ns}$, for SN54/74LS221, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
- B. All measurements are made between the 1.5-V points of the indicated transitions for the SN54/74221 or between the 1.3-V points for the SN54/74LS221.

Figure 1. Switching Characteristics (Continued)

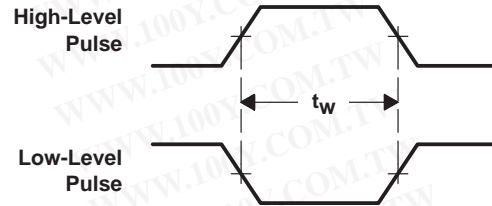
SN54221, SN54LS221, SN74221, SN74LS221 DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

SDLS213B – DECEMBER 1983 – REVISED NOVEMBER 2004

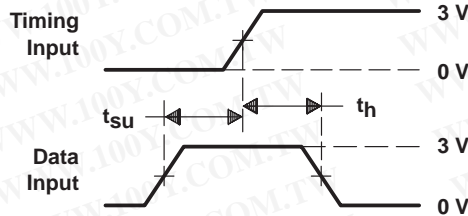
PARAMETER MEASUREMENT INFORMATION



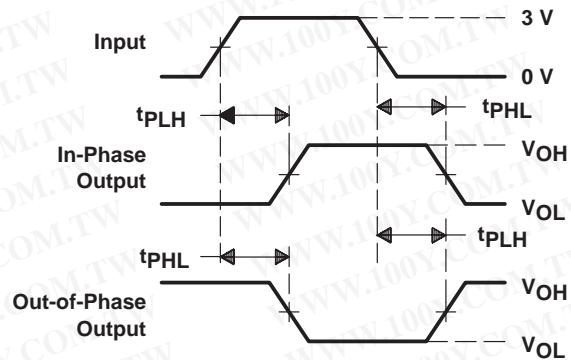
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 D. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$ and, for SN54/74221, $t_r \leq 7$ ns, $t_f \leq 7$ ns, for SN54/74LS221, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
 E. All measurements are made between the 1.5-V points of the indicated transitions for the SN54/74221 or between the 1.3-V points for the SN54/74LS221.

Figure 2. Load Circuits and Voltage Waveforms

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TYPICAL CHARACTERISTICS (SN54/74221 ONLY)†

DISTRIBUTION OF UNITS
 FOR
 OUTPUT PULSE

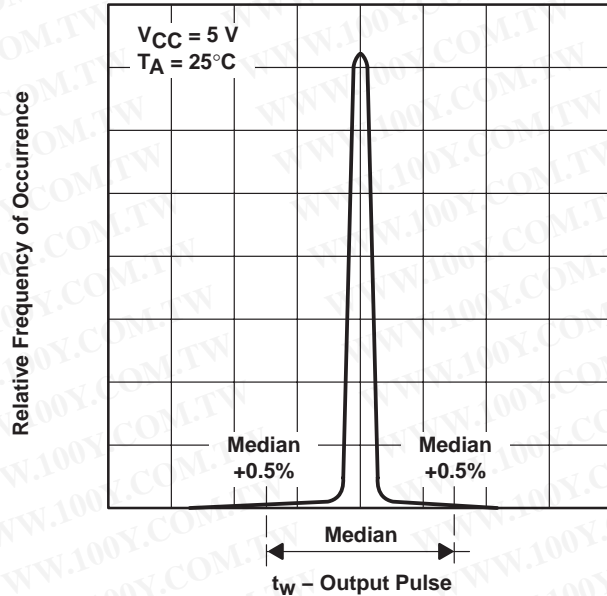


Figure 3

VARIATION IN OUTPUT PULSE
 vs
 SUPPLY VOLTAGE

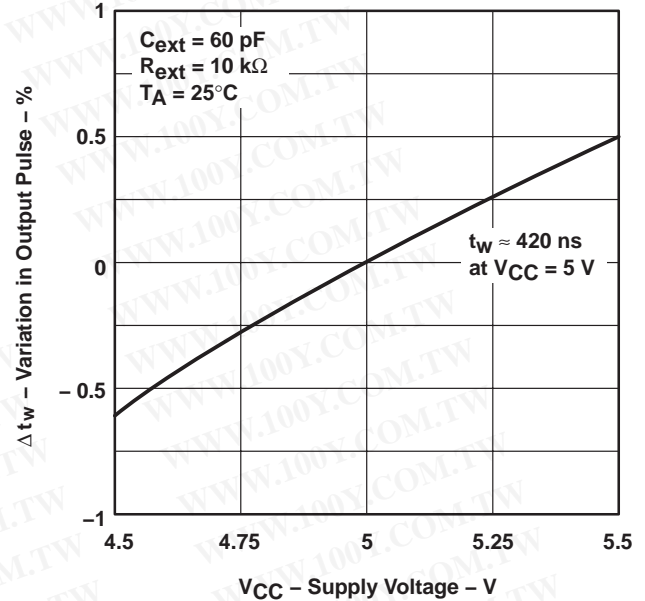


Figure 4

VARIATION IN OUTPUT PULSE
 vs
 FREE-AIR TEMPERATURE

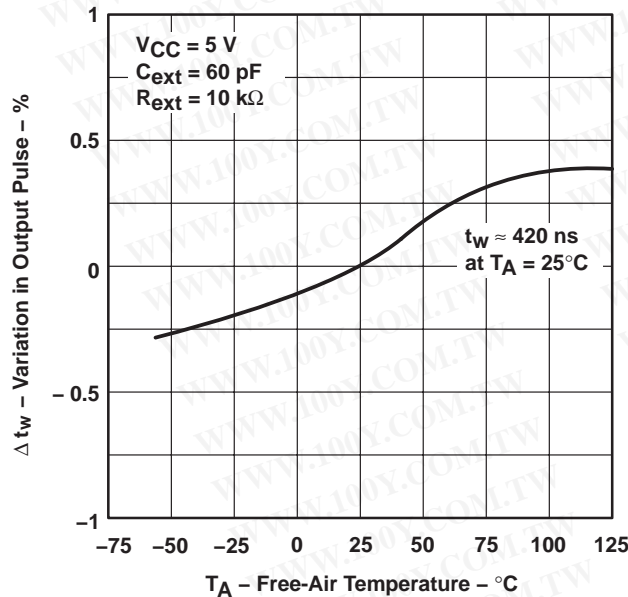


Figure 5

OUTPUT PULSE
 vs
 TIMING RESISTOR VALUE

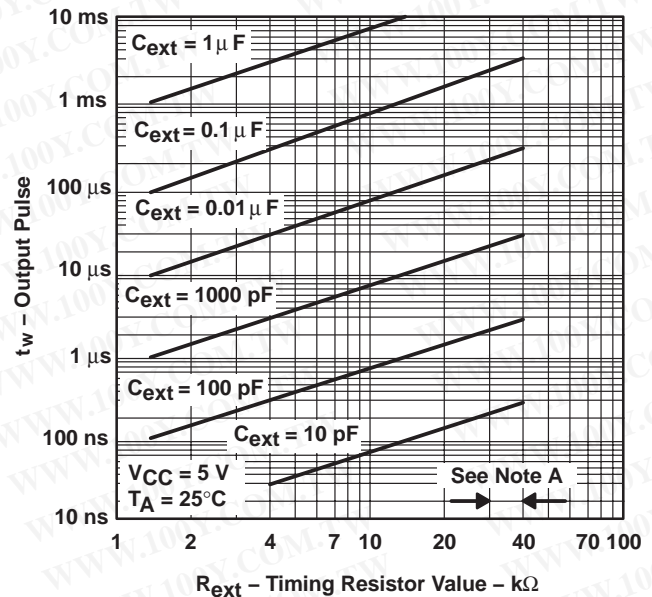


Figure 6

† Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.
 NOTE A: These values of resistance exceed the maximum recommended for use over the full military temperature range of the SN54221.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-8771101EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 76042012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 7604201EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 7604201FA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| JM38510/31402B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| JM38510/31402BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| JM38510/31402BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54221J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN54LS221J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN74221N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74221NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS221D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS221N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74LS221NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS221NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS221NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54221J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54LS221FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54LS221J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54LS221W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

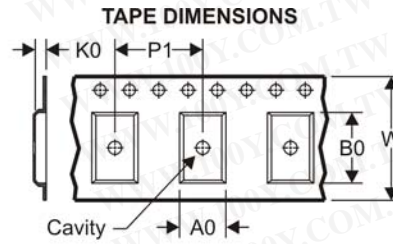
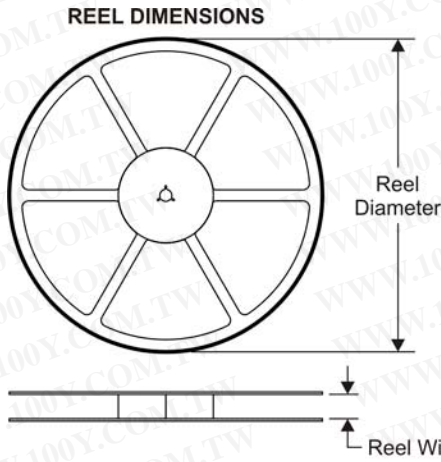
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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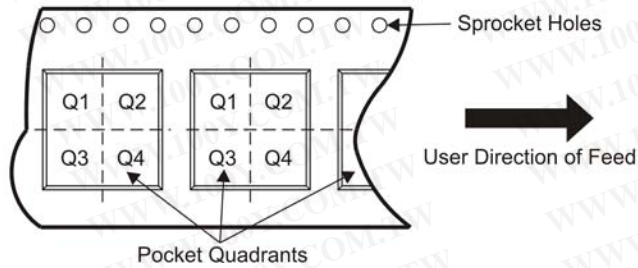
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TAPE AND REEL INFORMATION



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

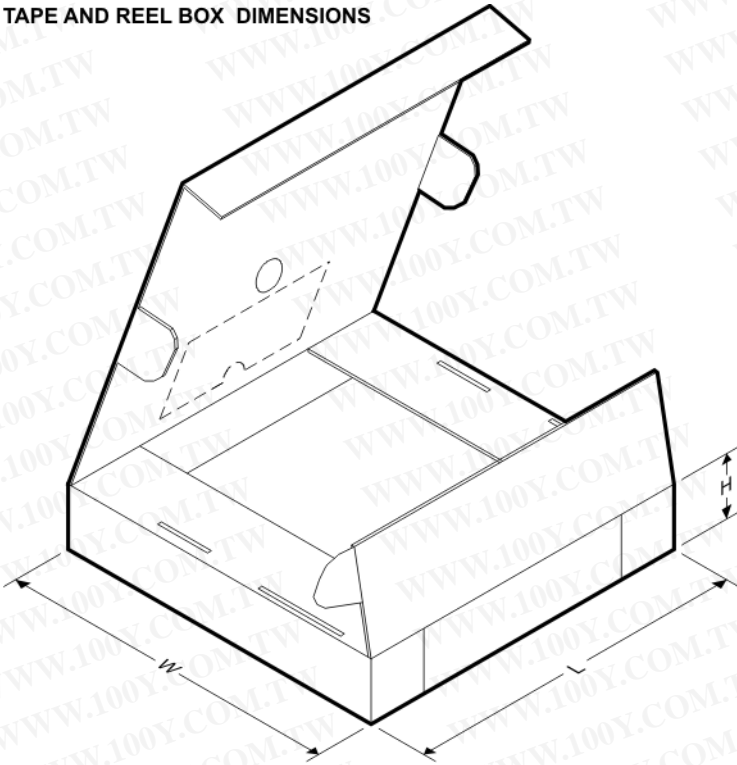


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS221DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS221DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS221NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

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TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

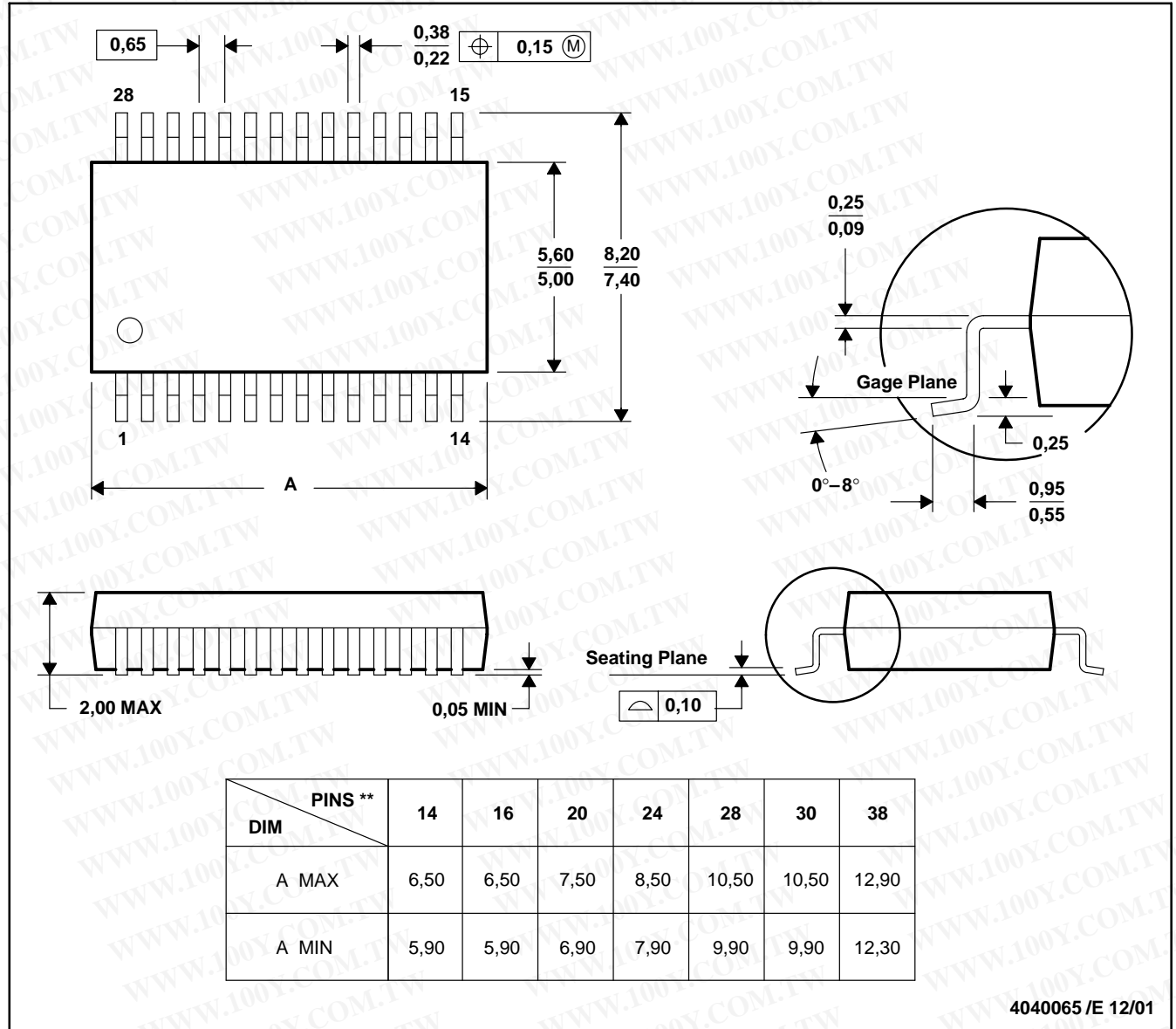
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS221DBR | SSOP | DB | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LS221DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LS221NSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

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DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

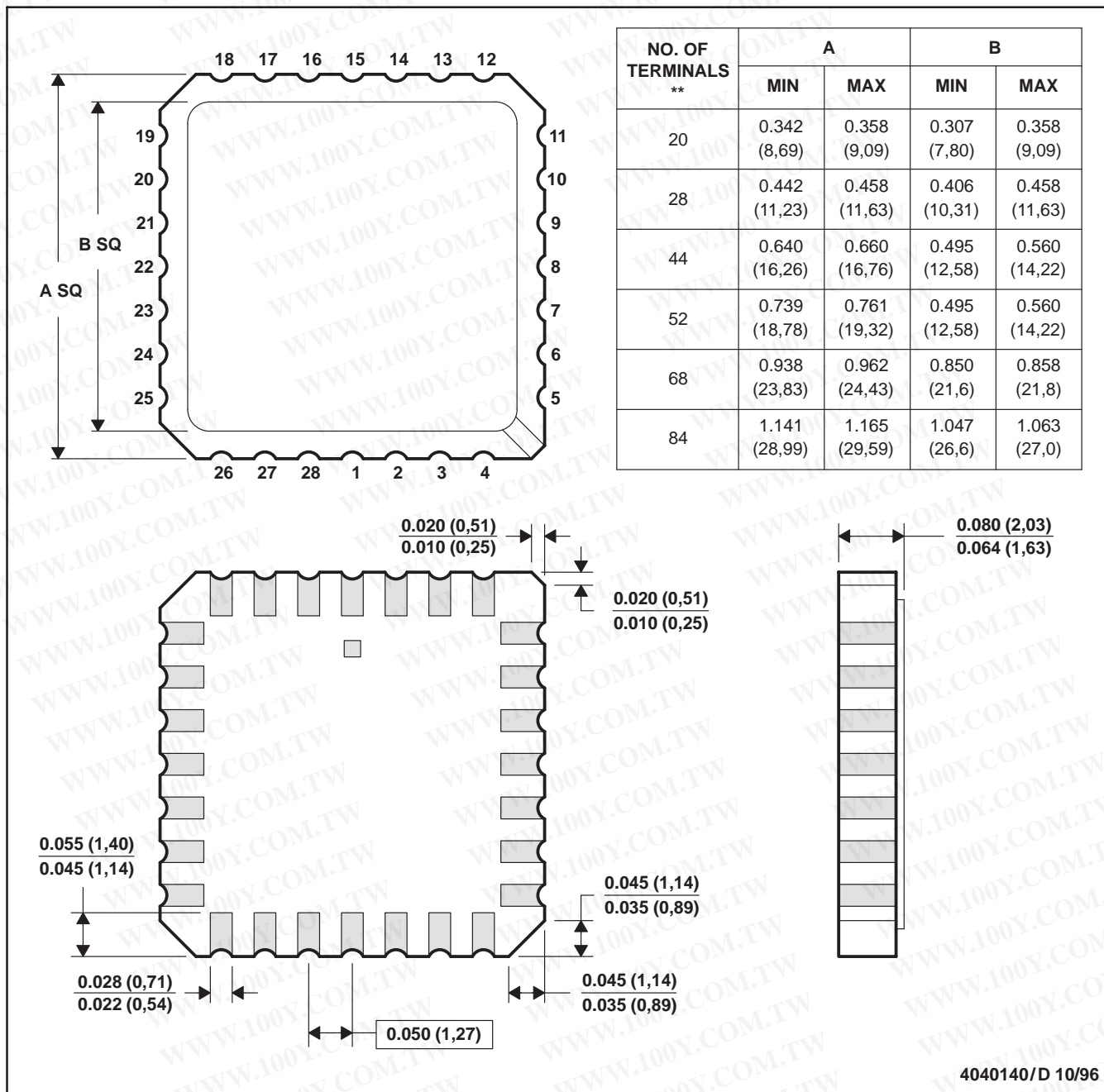
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FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



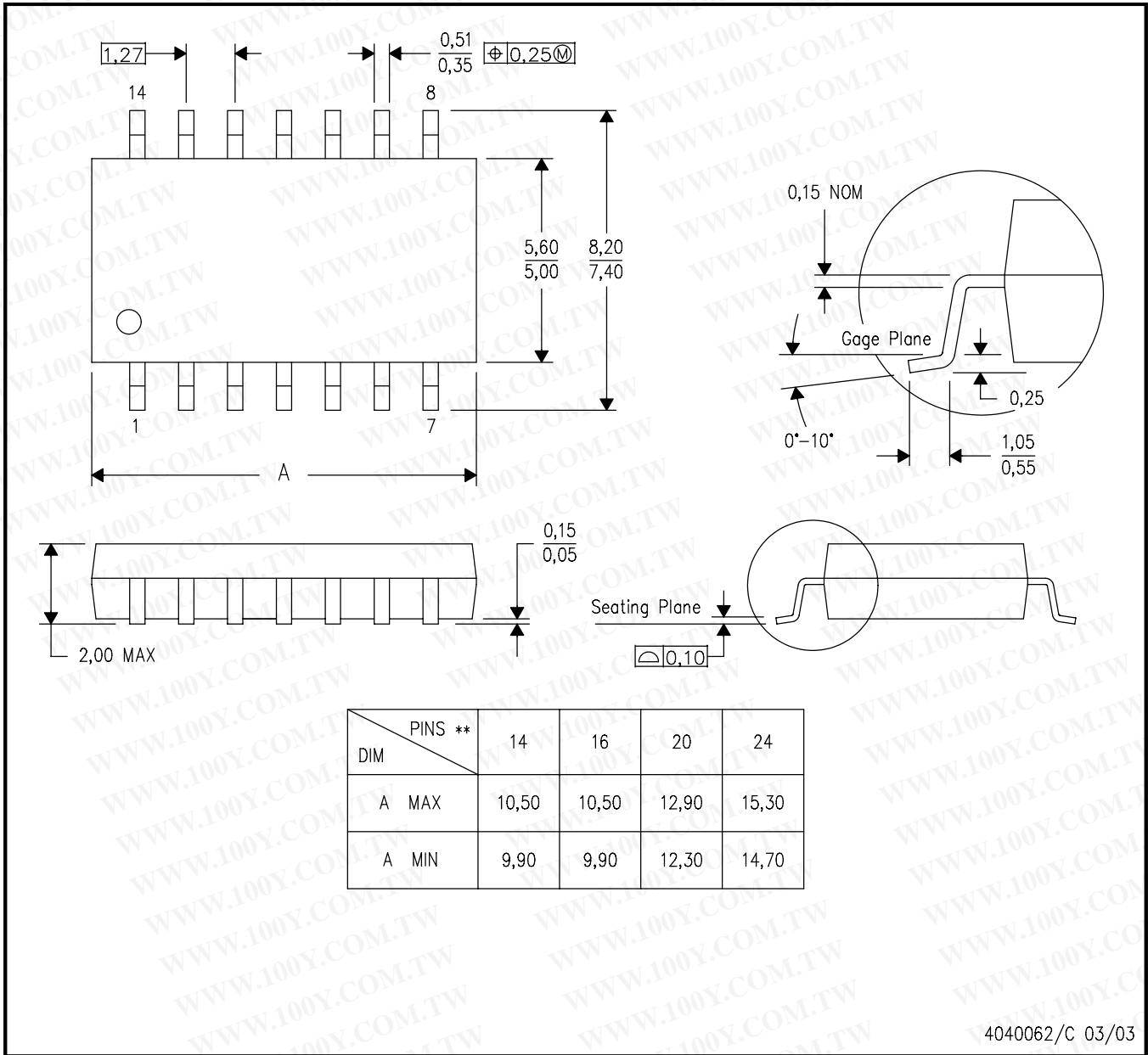
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

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MECHANICAL DATA

NS (R-PDSO-G**)
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



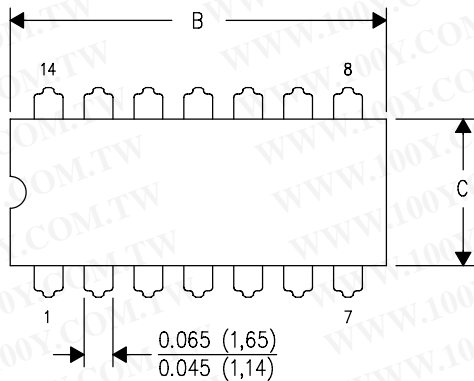
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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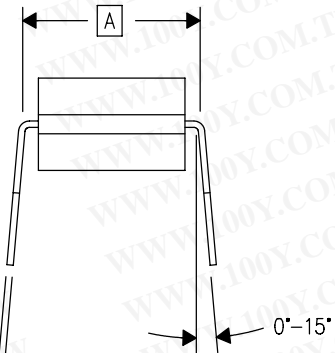
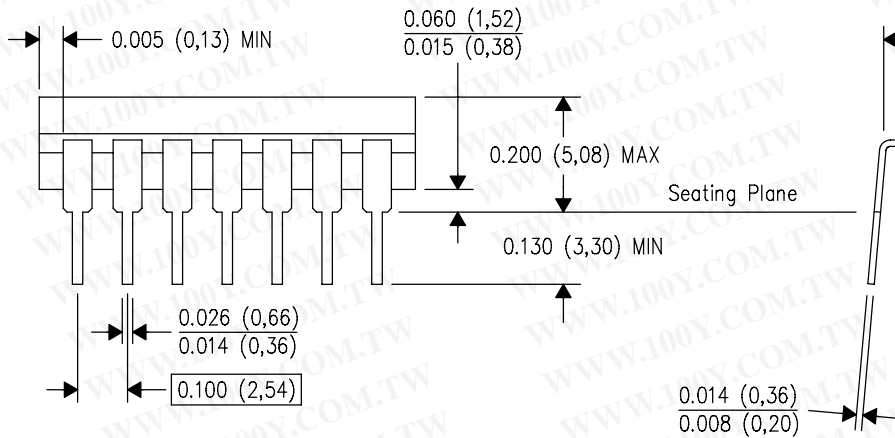
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



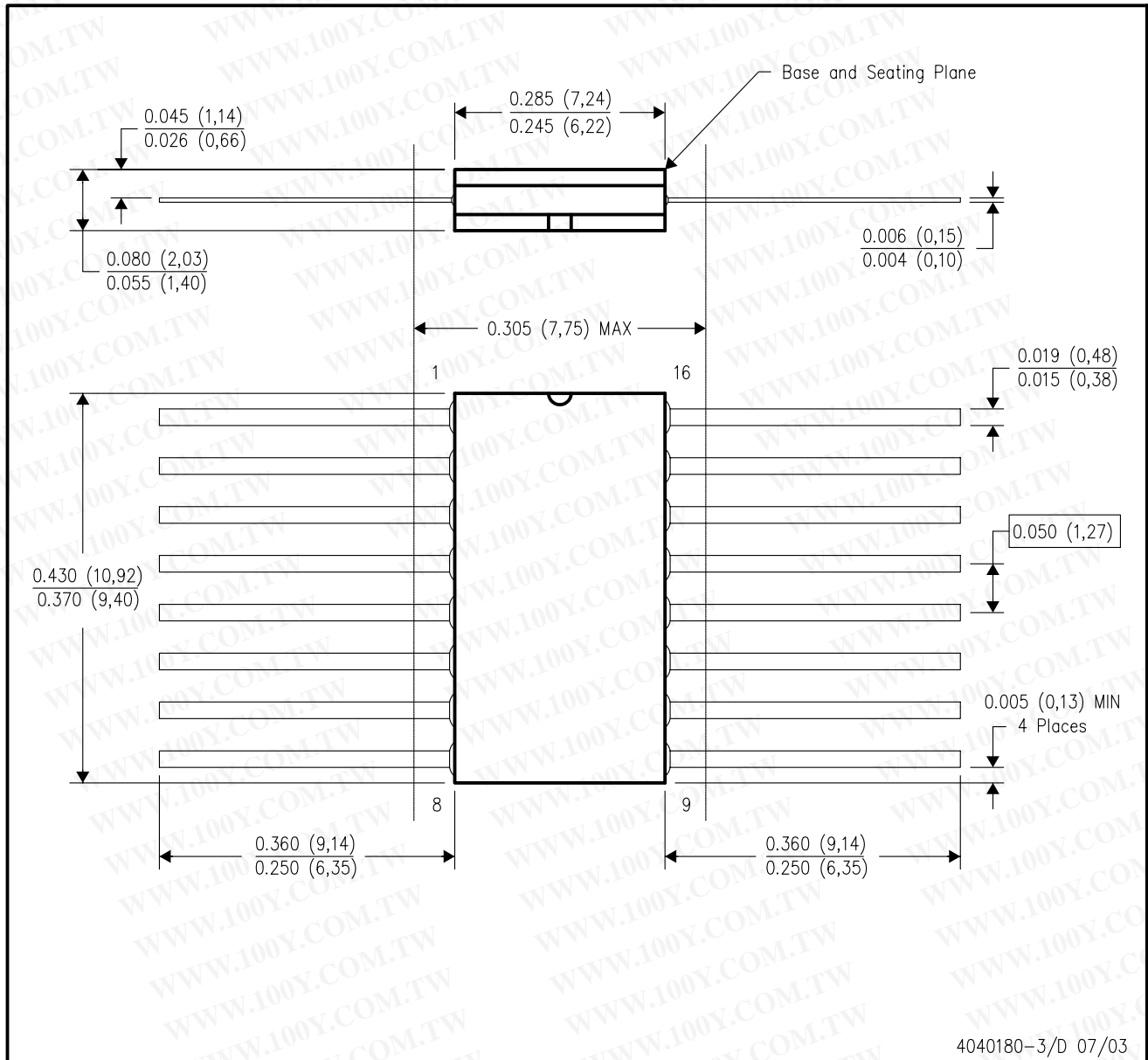
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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W (R-GDFP-F16)

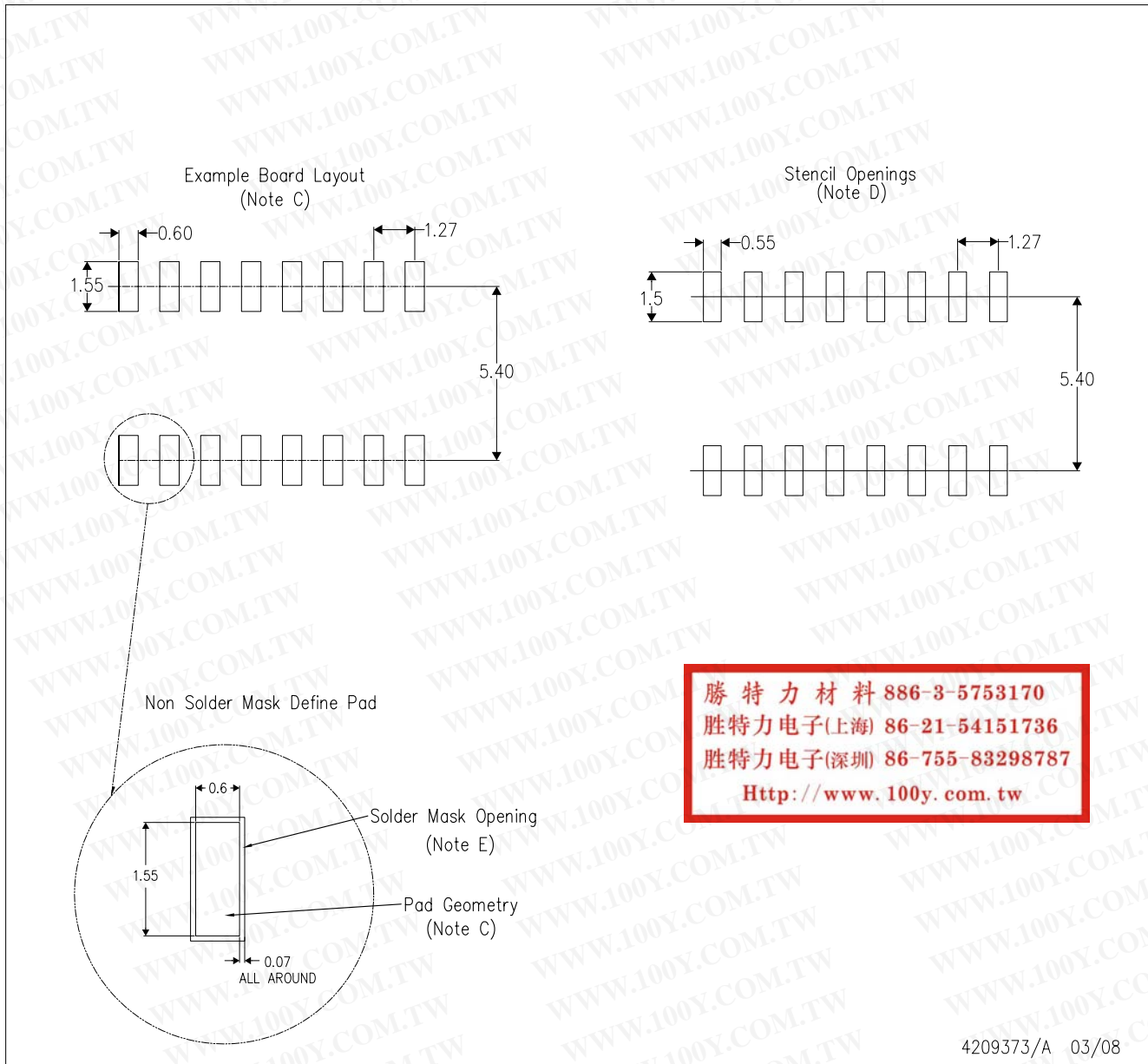
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

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D(R-PDSO-G16)



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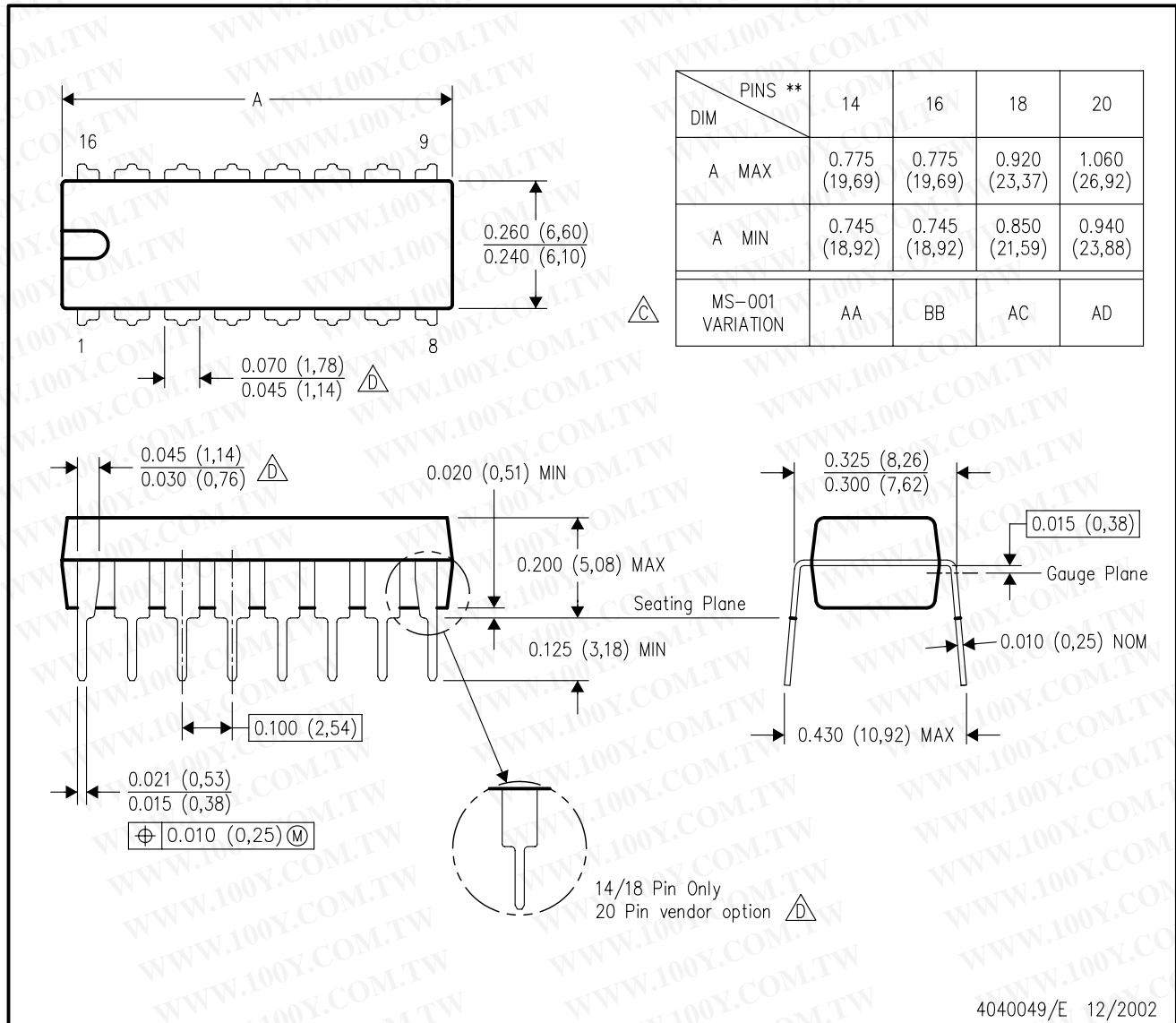
4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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