

SN54LV4051A, SN74LV4051A 8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS428H – MAY 1999 – REVISED APRIL 2005

- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

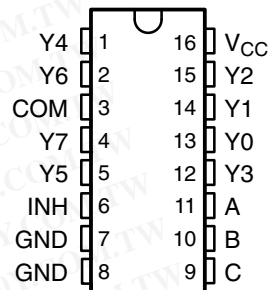
description/ordering information

These 8-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

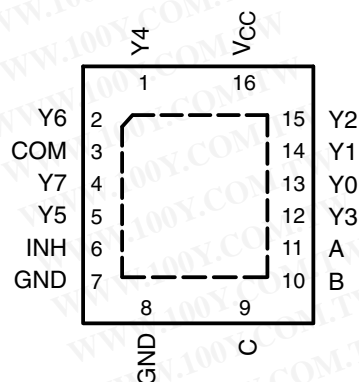
The 'LV4051A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

SN54LV4051A . . . J OR W PACKAGE
 SN74LV4051A . . . D, DB, DGV, N, NS, OR PW PACKAGE
 (TOP VIEW)



SN74LV4051A . . . RGY PACKAGE
 (TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	PDIP – N	Tube of 25	SN74LV4051AN	SN74LV4051AN	
	QFN – RGY	Reel of 1000	SN74LV4051ARGYR	LW051A	
	SOIC – D	Tube of 40	SN74LV4051AD	LV4051A	
		Reel of 2500	SN74LV4051ADR		
	SOP – NS	Reel of 2000	SN74LV4051ANSR	74LV4051A	
	TSSOP – PW	SSOP – DB	Reel of 2000	SN74LV4051ADBR	LW051A
			Tube of 90	SN74LV4051APW	
		Reel of 2000	SN74LV4051APWR		
Reel of 250			SN74LV4051APWT		
TVSOP – DGV	Reel of 2000	SN74LV4051ADGVR	LW051A		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV4051AJ	SNJ54LV4051AJ	
	CFP – W	Tube of 150	SNJ54LV4051AW	SNJ54LV4051AW	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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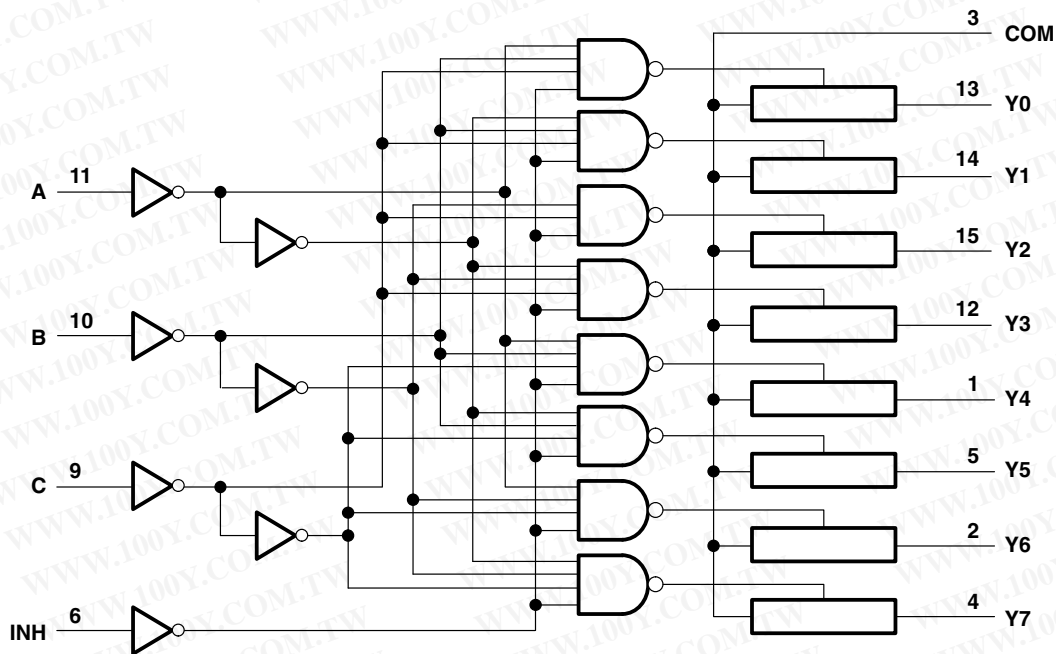
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FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7.0 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7.0 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$)	–50 mA
Switch through current, I_T ($V_{IO} = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): N package	67°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

		SN54LV4051A		SN74LV4051A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V	0.5	0.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$		
V_I	Control input voltage	0	5.5	0	5.5	V
V_{IO}	Input/output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	200	200		ns/V
		$V_{CC} = 3$ V to 3.6 V	100	100		
		$V_{CC} = 4.5$ V to 5.5 V	20	20		
T_A	Operating free-air temperature	–55	125	–40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54LV4051A		SN74LV4051A		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
r _{on} On-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 1)	2.3 V		38	180		225		225	Ω	
		3 V		30	150		190		190		
		4.5 V		22	75		100		100		
r _{on(p)} Peak on-state resistance	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V		113	500		600		600	Ω	
		3 V		54	180		225		225		
		4.5 V		31	100		125		125		
Δr _{on} Difference in on-state resistance between switches	I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V		2.1	30		40		40	Ω	
		3 V		1.4	20		30		30		
		4.5 V		1.3	15		20		20		
I _I Control input current	V _I = 5.5 V or GND	0 to 5.5 V				±0.1		±1		±1	μA
I _{S(off)} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 2)	5.5 V				±0.1		±1		±1	μA
I _{S(on)} On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 3)	5.5 V				±0.1		±1		±1	μA
I _{CC} Supply current	V _I = V _{CC} or GND	5.5 V						20		20	μA
C _{IC} Control input capacitance	f = 10 MHz	3.3 V		2							pF
C _{IS} Common terminal capacitance		3.3 V		23.4							pF
C _{OS} Switch terminal capacitance		3.3 V		5.7							pF
C _F Feedthrough capacitance		3.3 V		0.5							pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL} Propagation delay time	COM or Y _n	Y _n or COM	C _L = 15 pF, (see Figure 4)		1.9	10		16		16	ns
t _{PZH} t _{PZL} Enable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)		6.6	18		23		23	ns
t _{PHZ} t _{PLZ} Disable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)		7.4	18		23		23	ns
t _{PLH} t _{PHL} Propagation delay time	COM or Y _n	Y _n or COM	C _L = 50 pF, (see Figure 5)		3.8	12		18		18	ns
t _{PZH} t _{PZL} Enable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)		7.8	28		35		35	ns
t _{PHZ} t _{PLZ} Disable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)		11.5	28		35		35	ns

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 15 pF, (see Figure 4)	1.2	6	10	10	10	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	4.7	12	15	15	15	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	5.7	12	15	15	15	ns	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 50 pF, (see Figure 4)	2.5	9	12	12	12	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	5.5	20	25	25	25	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	8.8	20	25	25	25	ns	

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 15 pF, (see Figure 4)	0.6	4	7	7	7	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	3.5	8	10	10	10	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 15 pF, (see Figure 5)	4.4	8	10	10	10	ns	
t _{PLH} t _{PHL}	Propagation delay time	COM or Y _n	Y _n or COM	C _L = 50 pF, (see Figure 4)	1.5	6	8	8	8	ns	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	4	14	18	18	18	ns	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Y _n	C _L = 50 pF, (see Figure 5)	6.2	14	18	18	18	ns	

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analog switch characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	T _A = 25°C			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Note 6 and Figure 6)	2.3 V	20		MHz	
				3 V	25			
				4.5 V	35			
Crosstalk (control input to signal output)	INH	COM or Y _n	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 7)	2.3 V	20		mV	
				3 V	35			
				4.5 V	60			
Feedthrough attenuation (switch off)	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (see Note 7 and Figure 8)	2.3 V	-45		dB	
				3 V	-45			
				4.5 V	-45			
Sine-wave distortion	COM or Y _n	Y _n or COM	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 9)	V _I = 2 V _{p-p}	2.3 V	0.1		%
				V _I = 2.5 V _{p-p}	3 V	0.1		
				V _I = 4 V _{p-p}	4.5 V	0.1		

NOTES: 6. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads -3 dB.
7. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	5.9	pF

PARAMETER MEASUREMENT INFORMATION

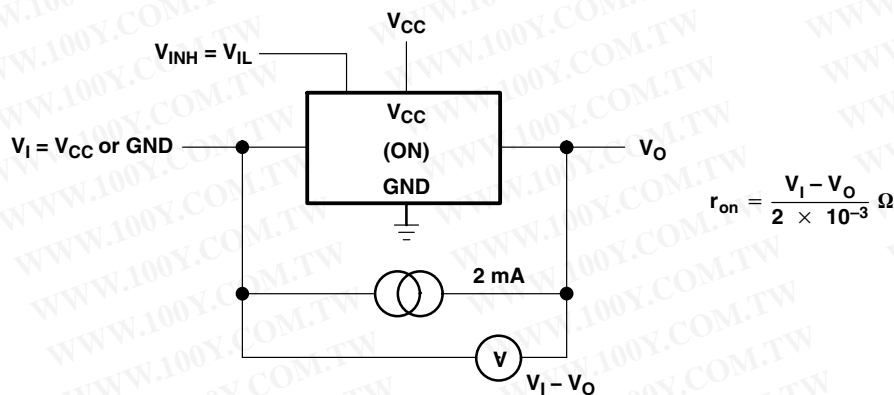
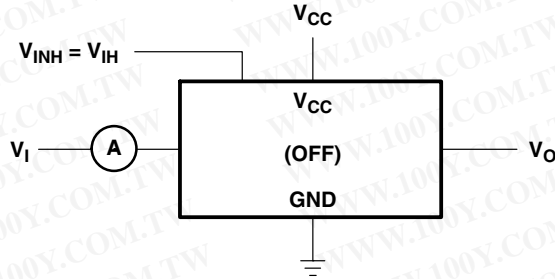


Figure 1. On-State Resistance Test Circuit

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PARAMETER MEASUREMENT INFORMATION



Condition 1: $V_I = 0, V_O = V_{CC}$
Condition 2: $V_I = V_{CC}, V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit

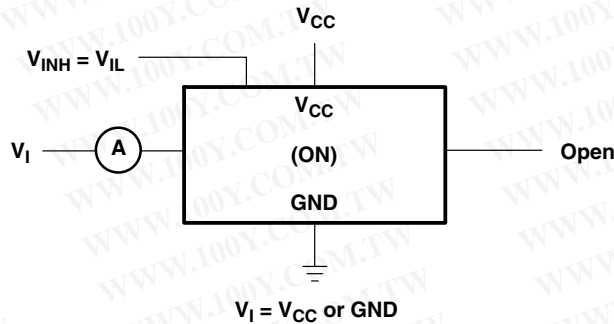


Figure 3. On-State Switch Leakage-Current Test Circuit

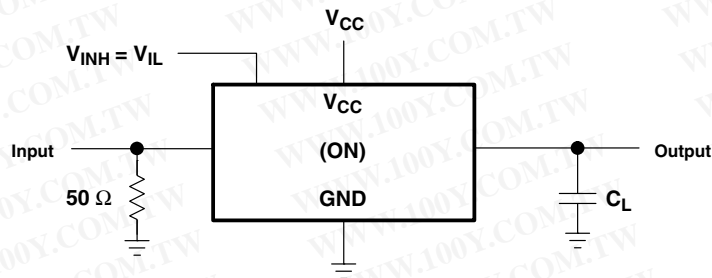
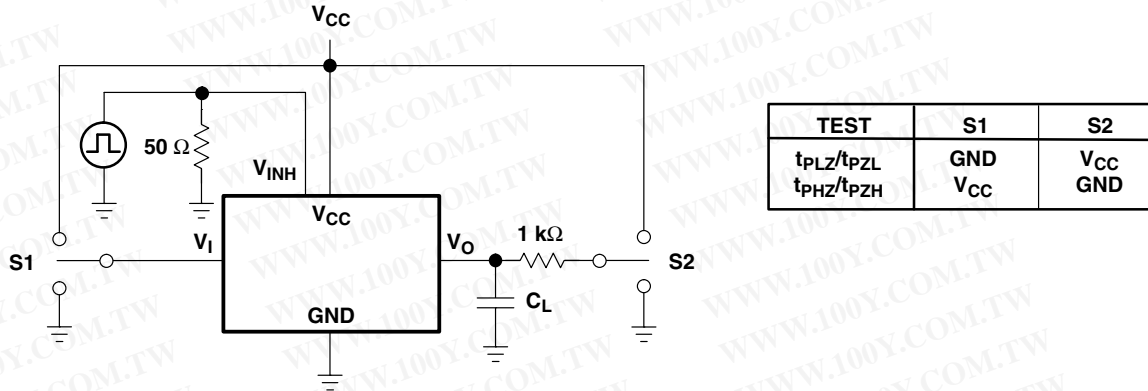


Figure 4. Propagation Delay Time, Signal Input to Signal Output

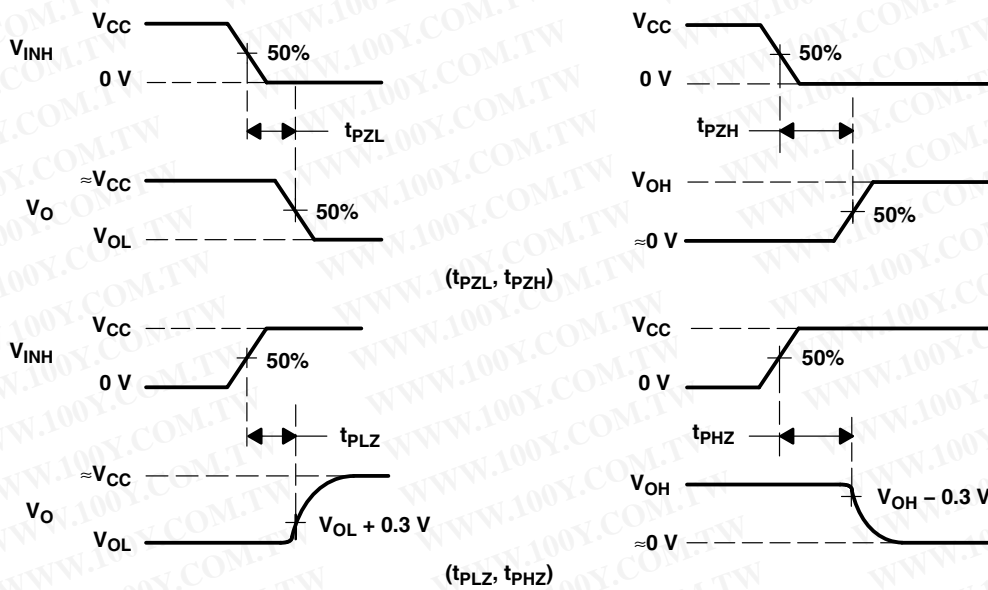
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PARAMETER MEASUREMENT INFORMATION



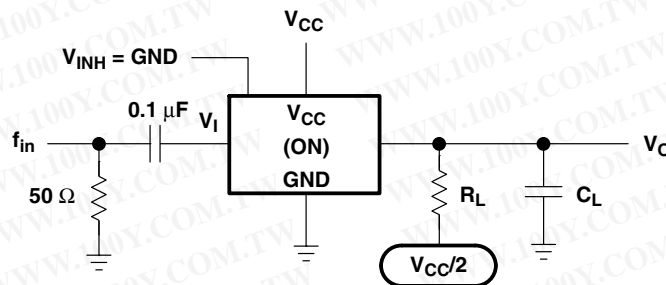
TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

PARAMETER MEASUREMENT INFORMATION

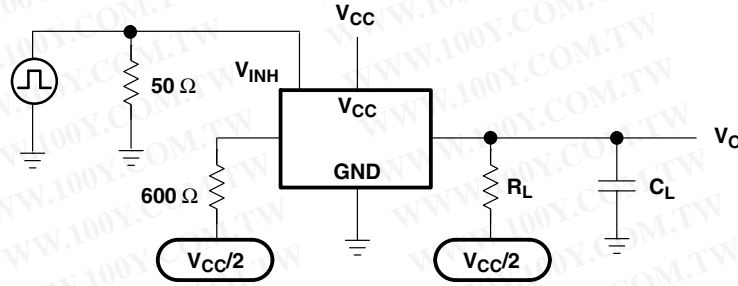


Figure 7. Crosstalk (Control Input, Switch Output)

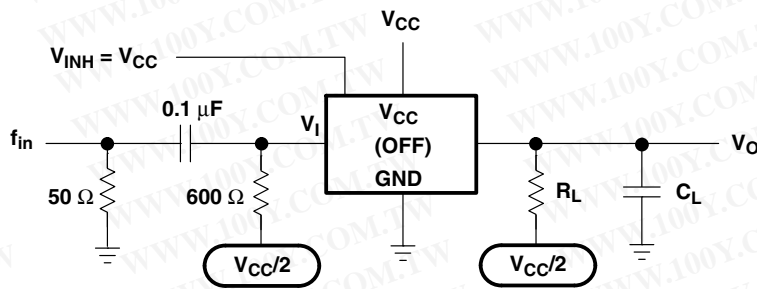


Figure 8. Feedthrough Attenuation (Switch Off)

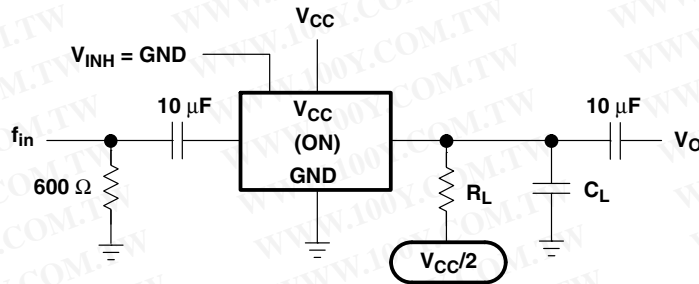


Figure 9. Sine-Wave Distortion

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15-Mar-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV4051AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV4051ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV4051ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APWRG3	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI
SN74LV4051APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

15-Mar-2010

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV4051APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4051ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LV4051ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4051A :

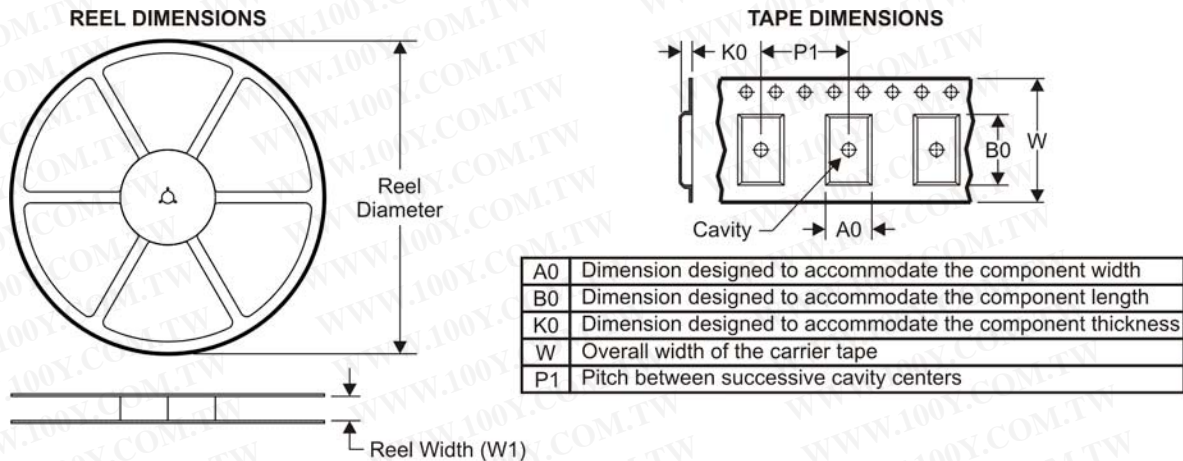
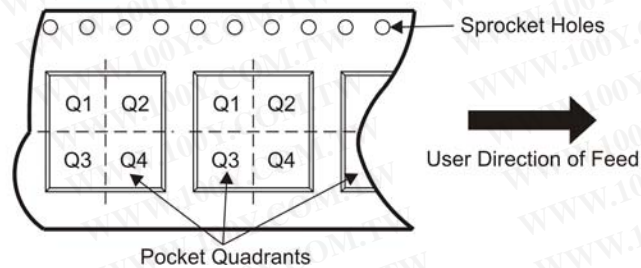
- Automotive: [SN74LV4051A-Q1](#)
- Enhanced Product: [SN74LV4051A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

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21-Dec-2009

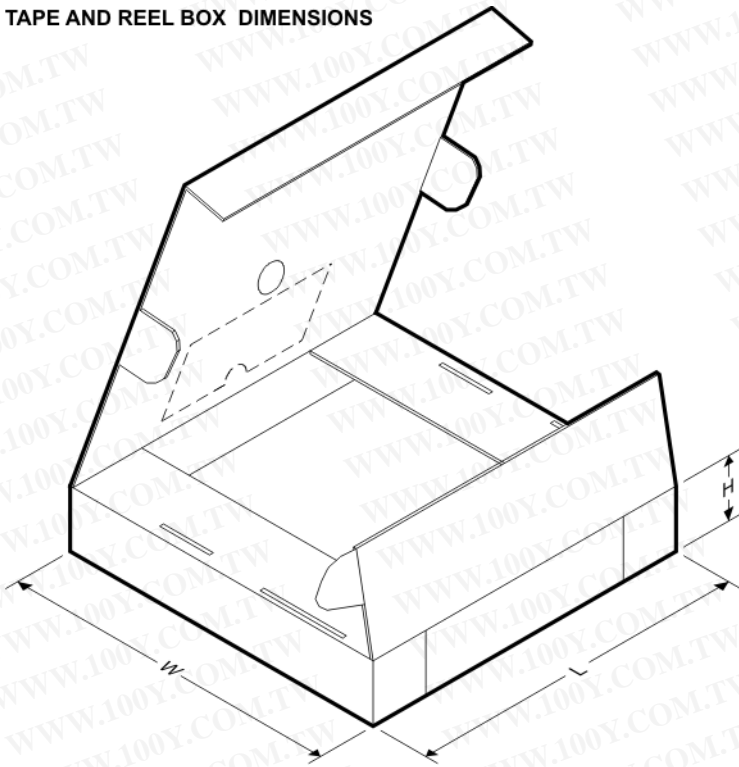
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4051ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV4051ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4051ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4051ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4051APWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LV4051ARGYR	VQFN	RGY	16	3000	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

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21-Dec-2009

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

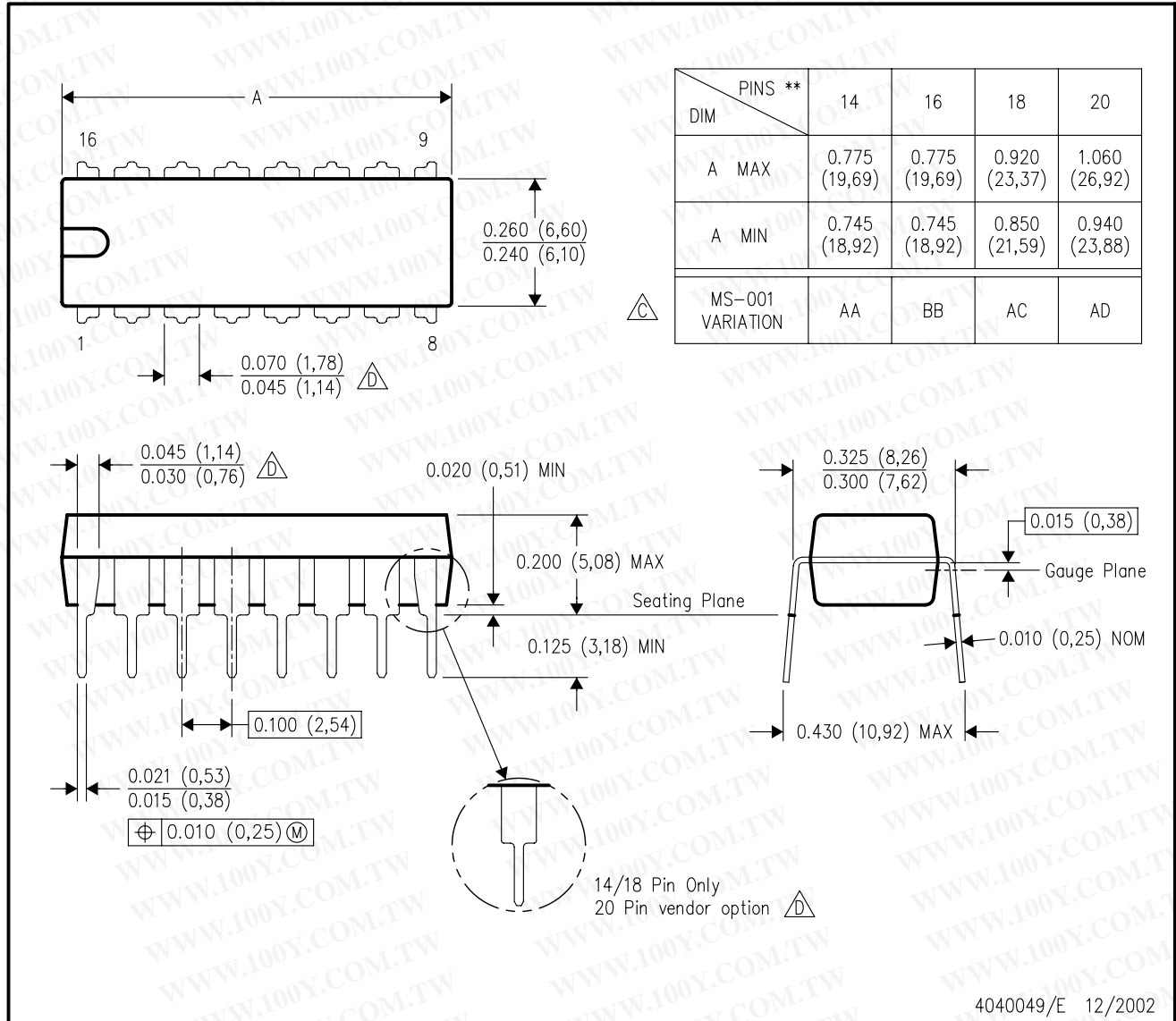
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4051ADBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74LV4051ADGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
SN74LV4051ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4051ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LV4051APWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74LV4051ARGYR	VQFN	RGY	16	3000	190.5	212.7	31.8



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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



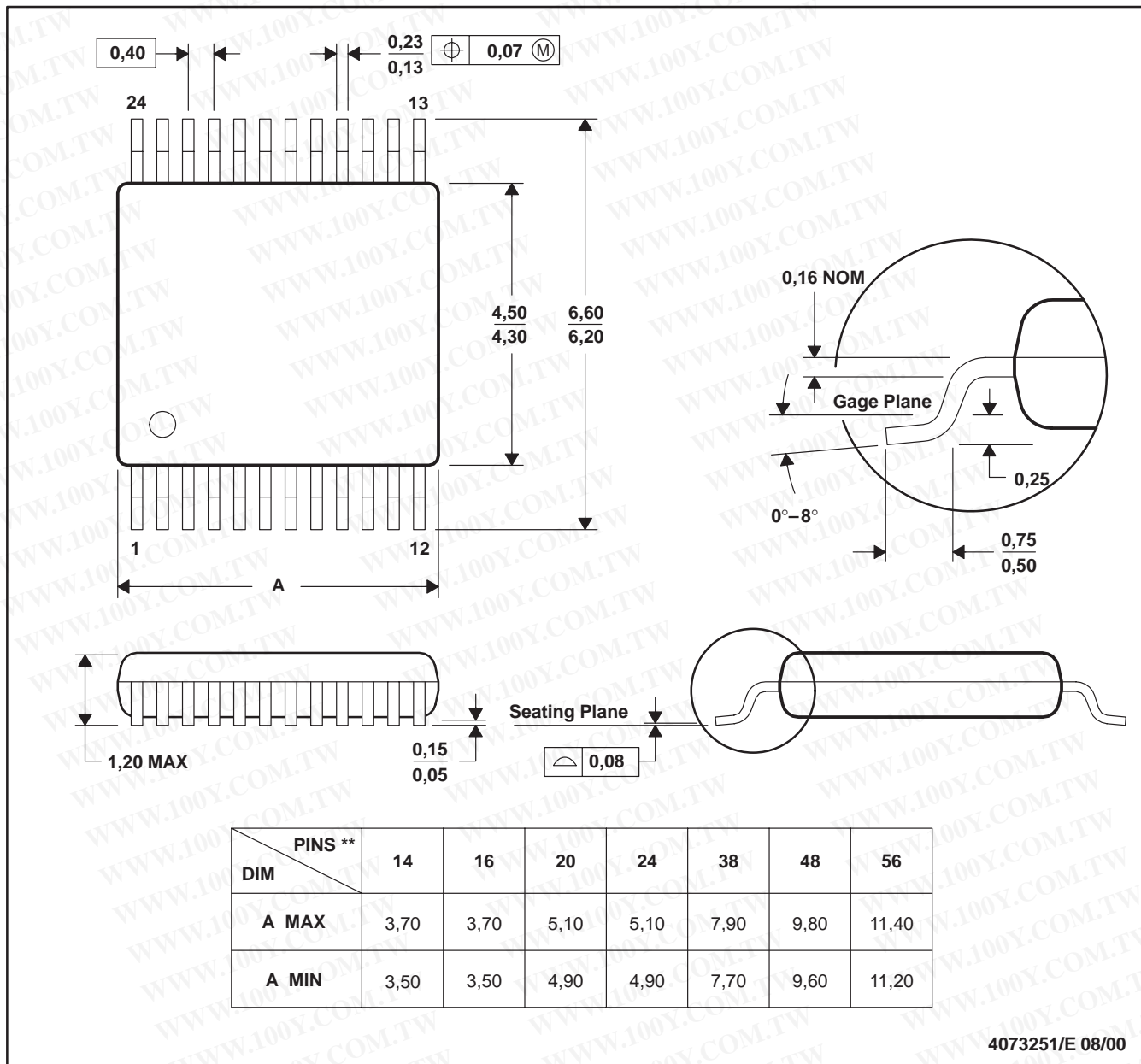
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

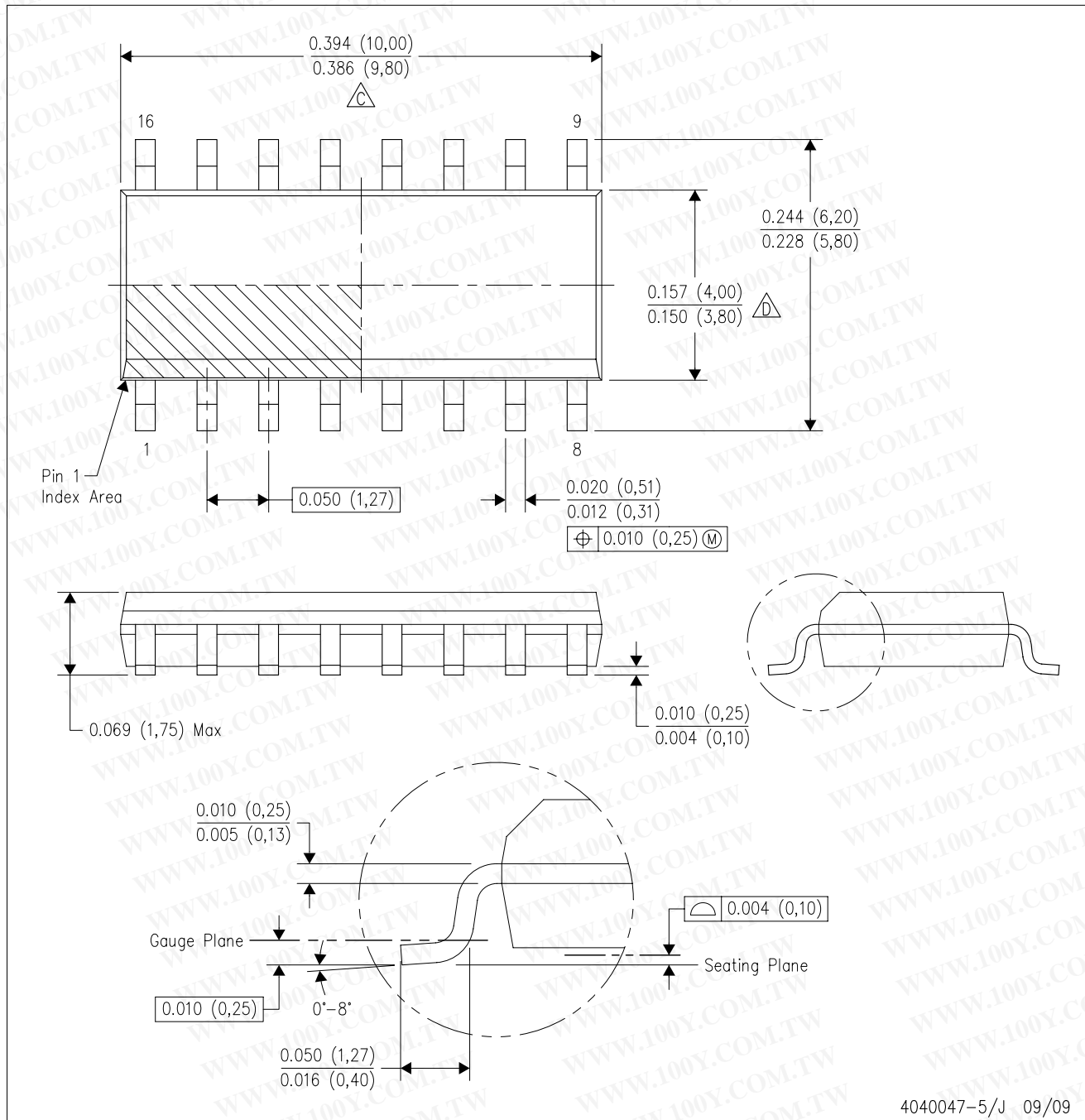


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - Reference JEDEC MS-012 variation AC.

THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N16)

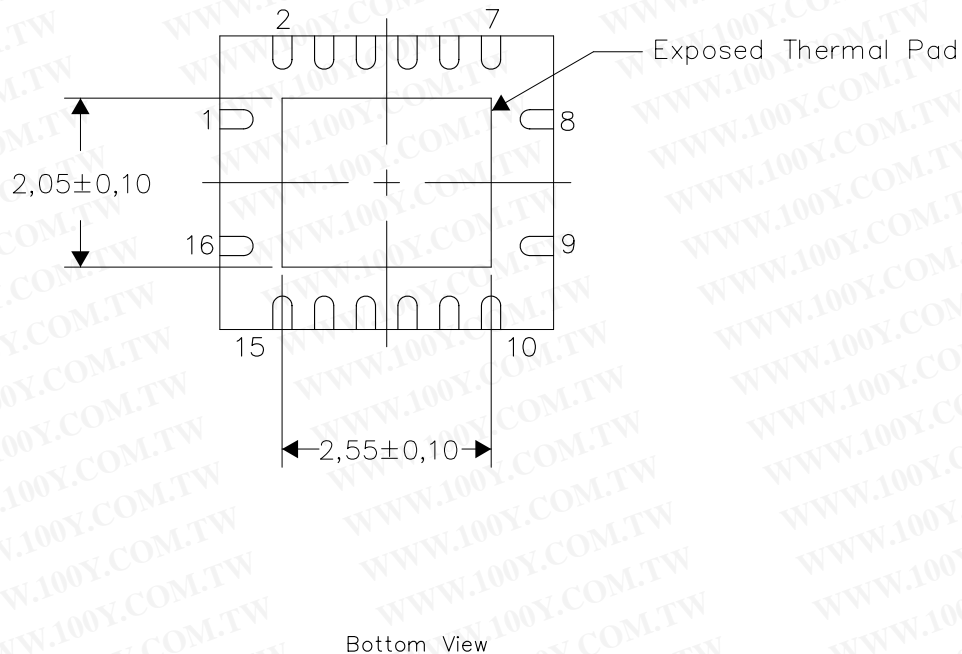
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

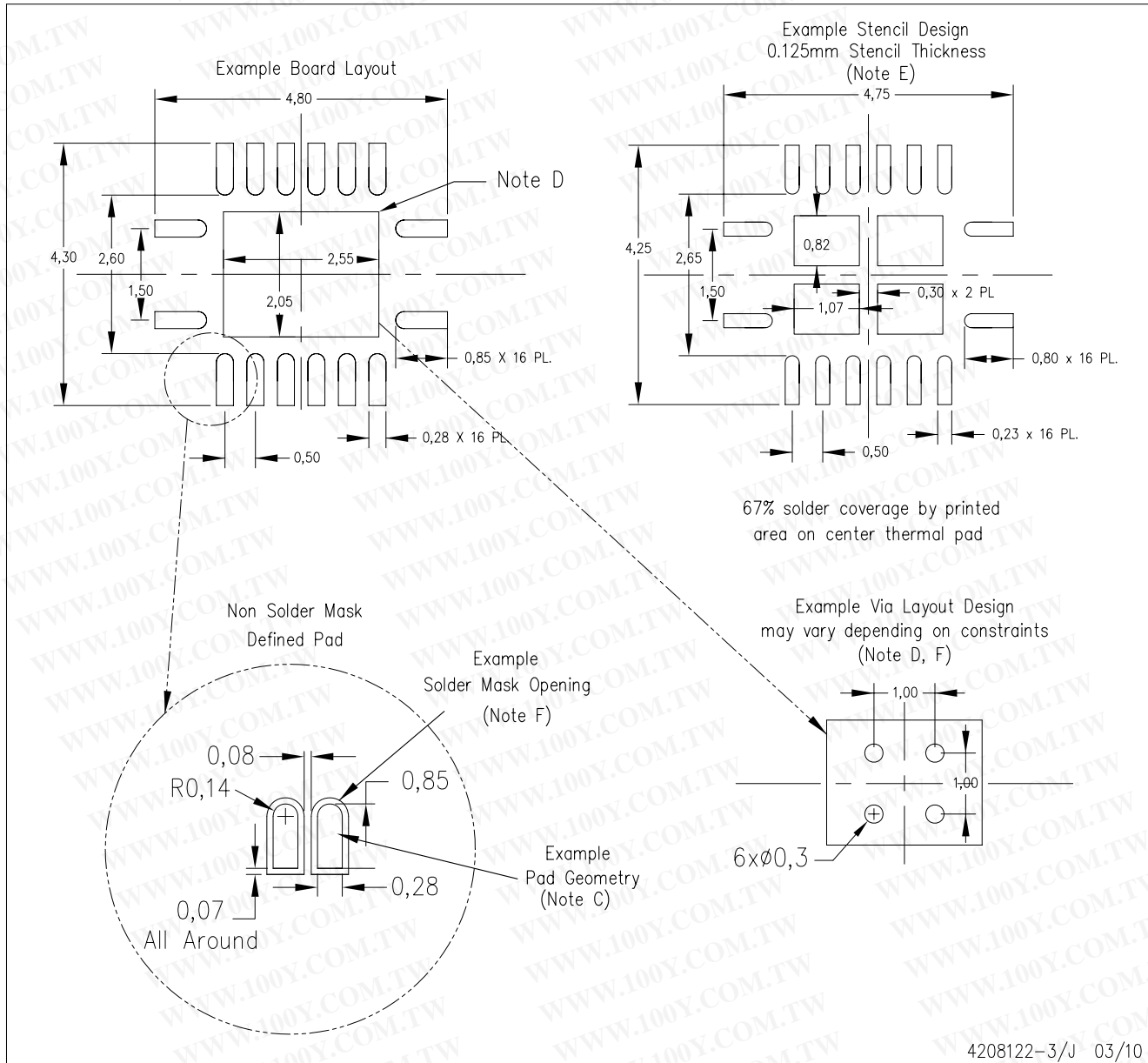
Exposed Thermal Pad Dimensions

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4206353-3/J 03/10

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/J 03/10

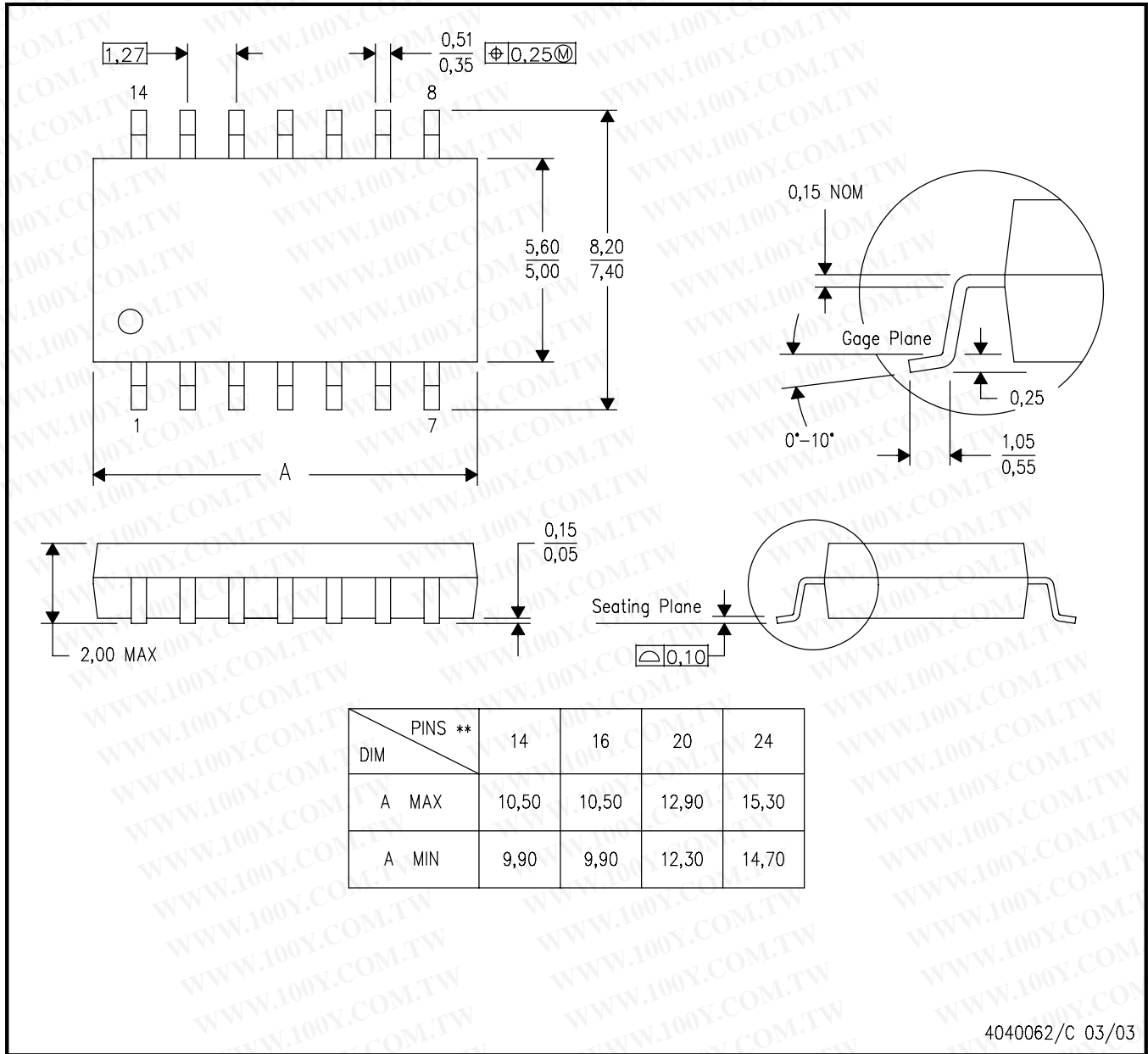
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



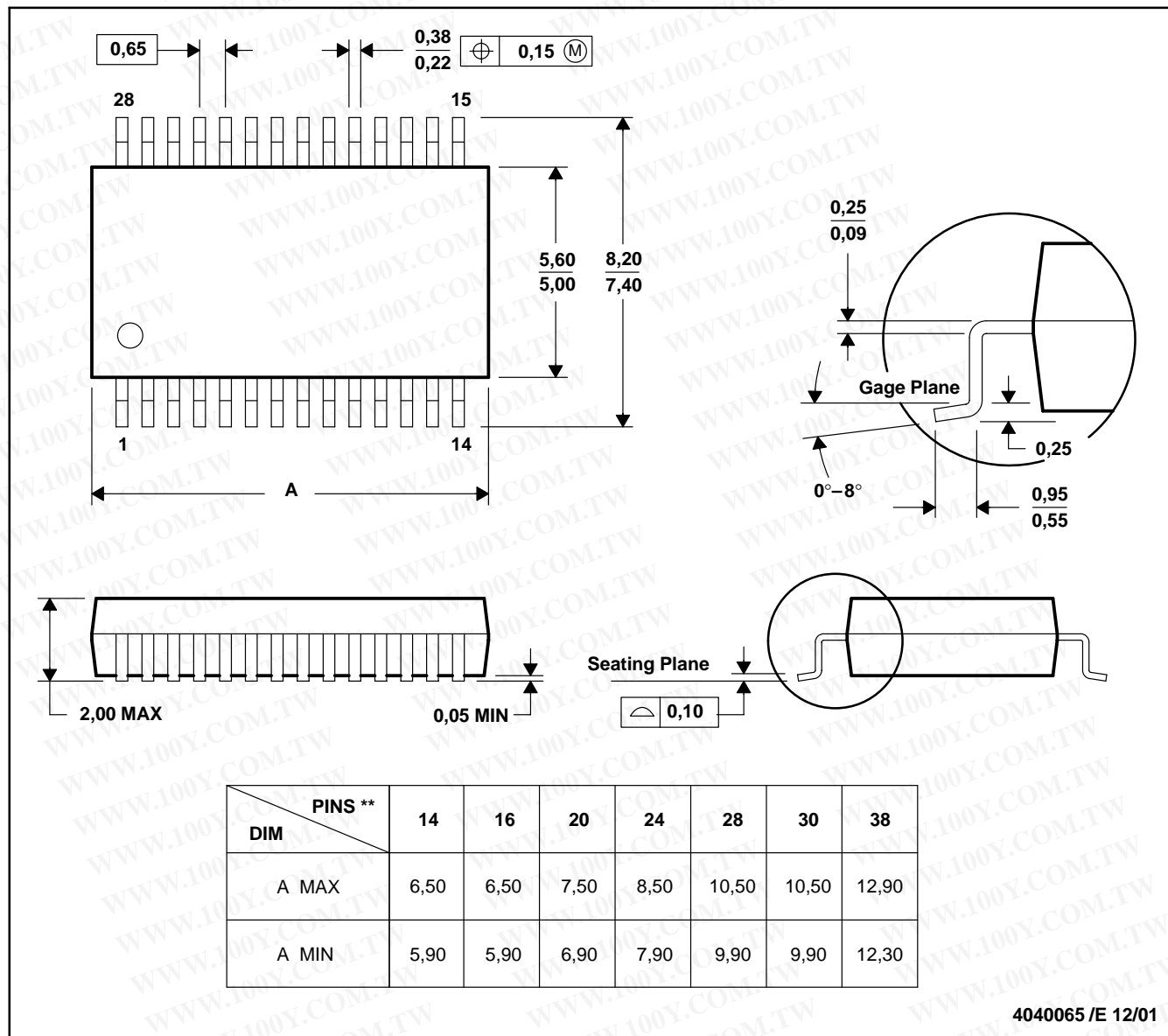
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



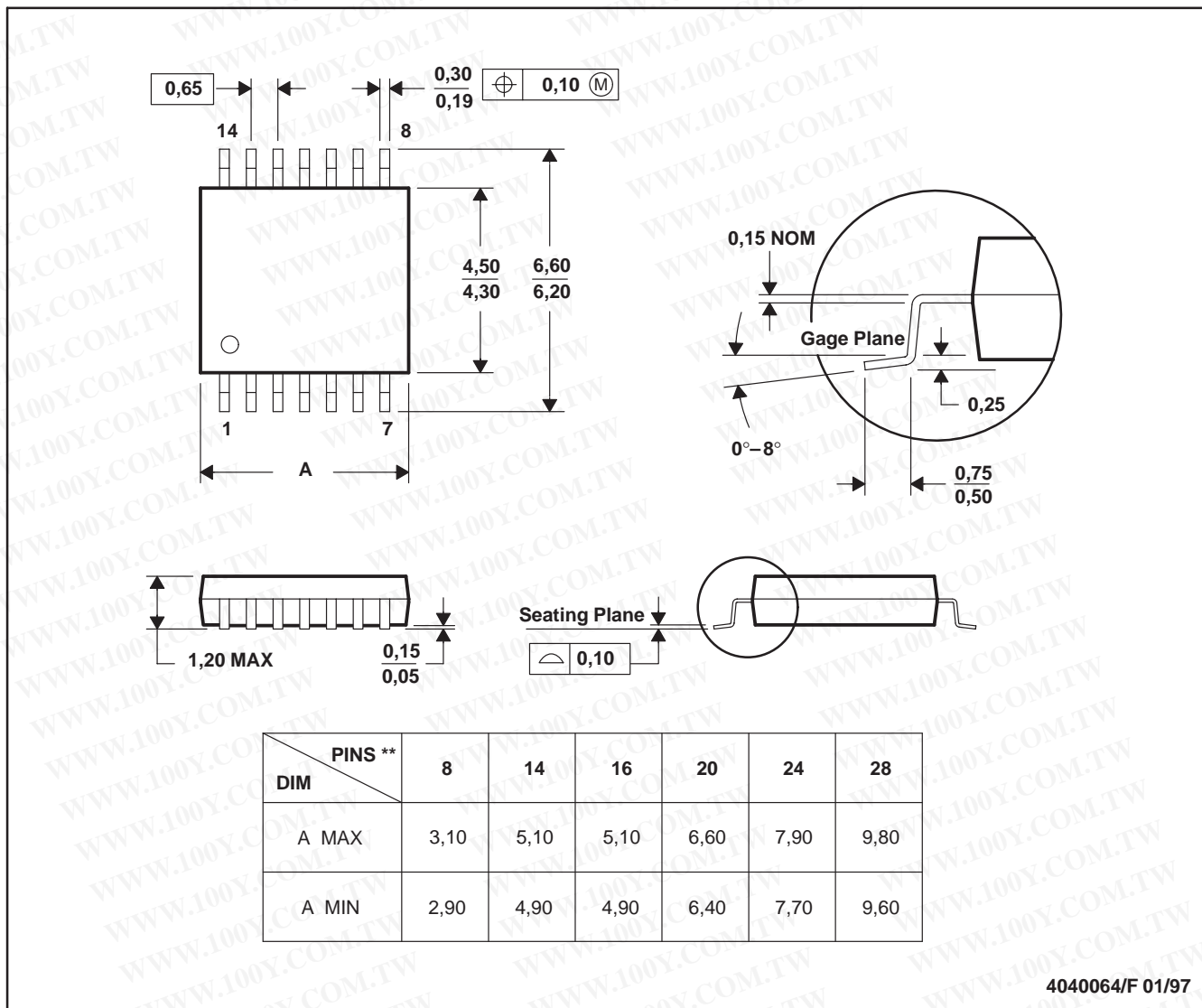
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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