

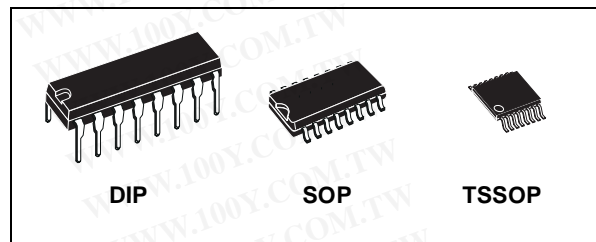


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M74HC4543

BCD TO 7 SEGMENT LATCH/DECODER/LCD DRIVER

- HIGH SPEED:
 $t_{PD} = 14ns$ (TYP.) at $V_{CC} = 6V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4mA$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES 4543



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC4543B1R	
SOP	M74HC4543M1R	M74HC4543RM13TR
TSSOP		M74HC4543TTR

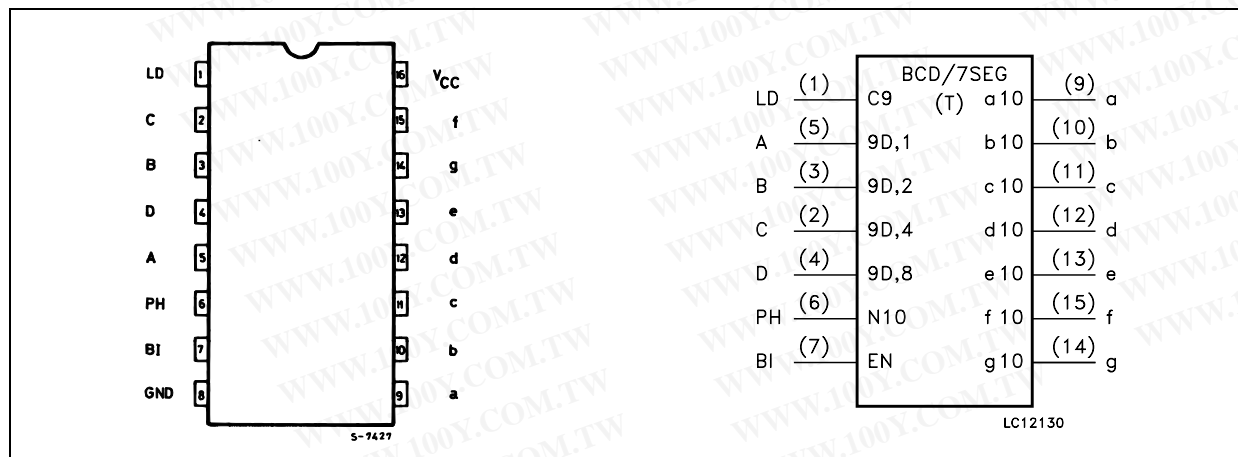
DESCRIPTION

The M74HC4543 is an high speed CMOS BCD-TO-7 SEGMENT DECODER WITH LCD DRIVER fabricated with silicon gate C²MOS technology.

This device consists of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for a liquid crystal display (LCD). When any illegal BCD input signal is applied or input BI is held high, the display is blanked. When driving

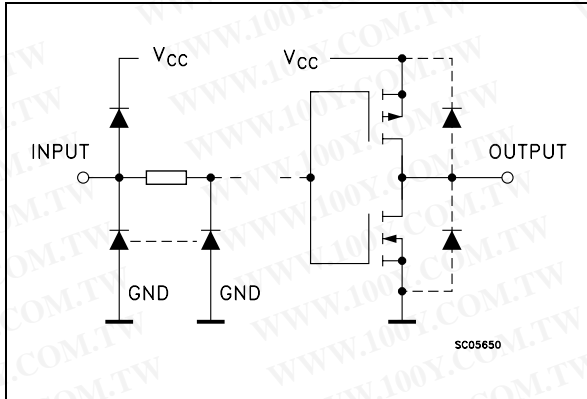
LCDs, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common backplane of the display. For other types of readouts, such as light-emitting diode (LED), some additional drivers, such as a transistor array is required. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



M74HC4543

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	LD	Latch Disable Input (Active HIGH)
5, 3, 2, 4	A to D	Address (Data) Inputs
6	PH	Phase Input (Active HIGH)
7	BI	Blanking Input (Active HIGH)
9, 10, 11, 12, 13, 15, 14	a to g	Segment Outputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

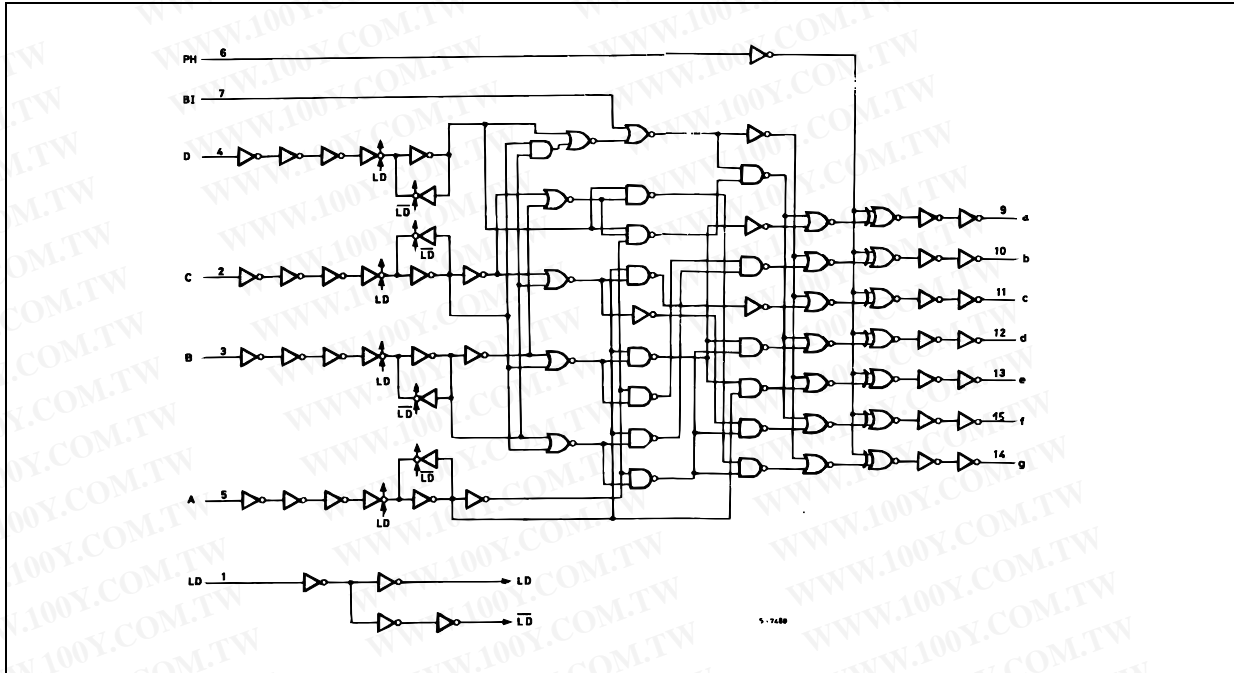
INPUT							OUTPUT							DISPLAY MODE	
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g		
X	H	L	X	X	X	X	L	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	H	3
H	L	L	L	H	L	H	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	H	9
H	L	L	H	H	X	X	L	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	#####							#####	
↑	↑	H	↑				INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE	

X : Don't Care

↑ : Same as above combinations

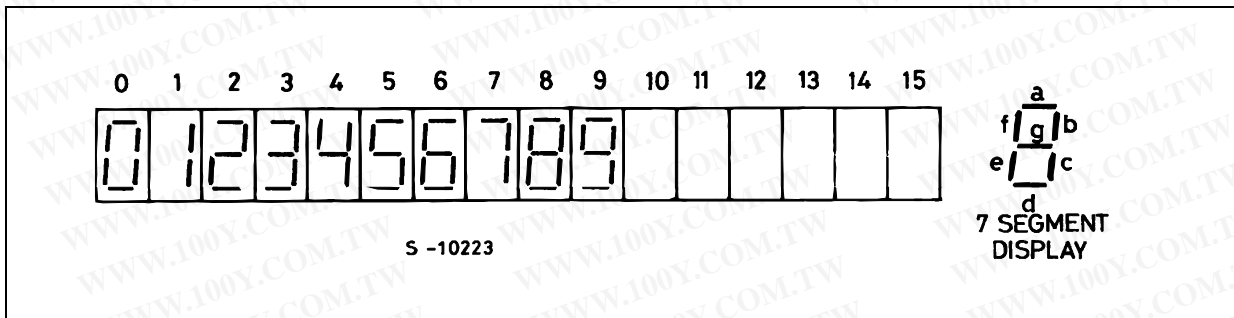
: Depends upon the BCD code previously applied when LD = 'H'

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

DISPLAY MODE



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500(*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	°C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit		
				$T_A = 25^\circ C$			$-40 \text{ to } 85^\circ C$		$-55 \text{ to } 125^\circ C$			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	$I_O = -20 \mu A$	1.9	2.0		1.9		1.9			V
		4.5	$I_O = -20 \mu A$	4.4	4.5		4.4		4.4			
		6.0	$I_O = -20 \mu A$	5.9	6.0		5.9		5.9			
		4.5	$I_O = -4.0 \text{ mA}$	4.18	4.31		4.13		4.10			
		6.0	$I_O = -5.2 \text{ mA}$	5.68	5.8		5.63		5.60			
V_{OL}	Low Level Output Voltage	2.0	$I_O = 20 \mu A$		0.0	0.1		0.1			0.1	V
		4.5	$I_O = 20 \mu A$		0.0	0.1		0.1			0.1	
		6.0	$I_O = 20 \mu A$		0.0	0.1		0.1			0.1	
		4.5	$I_O = 4.0 \text{ mA}$		0.17	0.26		0.37			0.40	
		6.0	$I_O = 5.2 \text{ mA}$		0.18	0.26		0.37			0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC} \text{ or GND}$			± 0.1		± 1		± 1	μA	
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC} \text{ or GND}$			4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

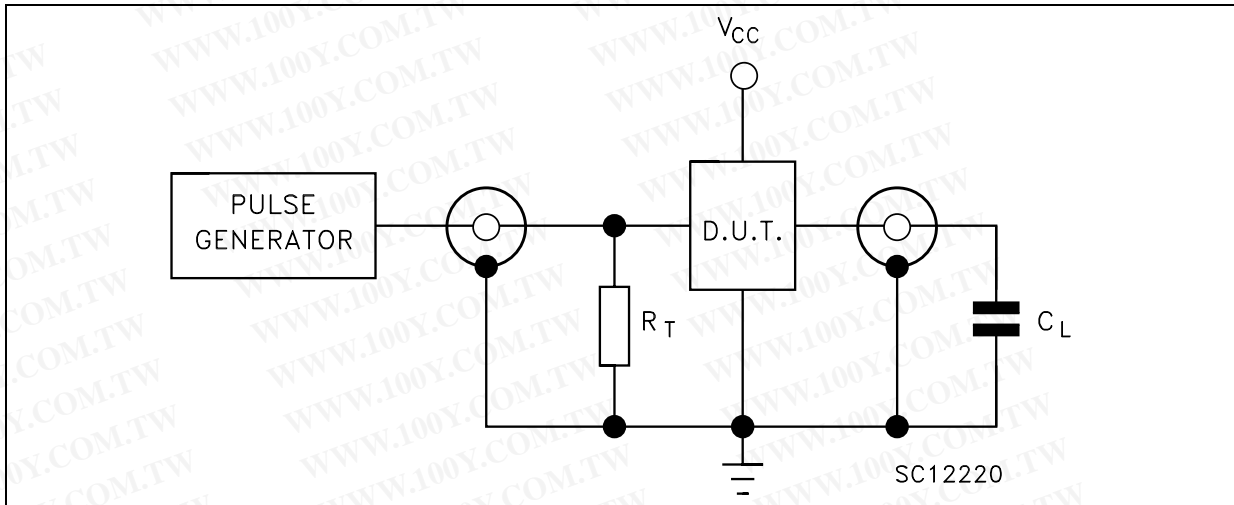
Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH} \ t_{THL}$	Output Transition Time	V_{CC} (V)	2.0	30	75		95		110	ns	
			4.5	8	15		19		22		
			6.0	7	13		16		19		
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (BCD - OUT)	V_{CC} (V)	2.0	160	300		375		450	ns	
			4.5	40	60		75		90		
			6.0	30	51		64		76		
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (BI - OUT)	V_{CC} (V)	2.0	80	175		220		265	ns	
			4.5	23	35		44		53		
			6.0	17	30		37		45		
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (PH - OUT)	V_{CC} (V)	2.0	58	130		165		195	ns	
			4.5	17	26		33		39		
			6.0	14	22		28		33		
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (LD - OUT)	V_{CC} (V)	2.0	130	265		335		400	ns	
			4.5	35	53		66		80		
			6.0	16	45		56		68		
$t_{W(H)}$	Minimum Pulse Width (LD)	V_{CC} (V)	2.0	30	75		95		110	ns	
			4.5	8	15		29		22		
			6.0	7	13		26		19		
t_s	Minimum Set Up Time	V_{CC} (V)	2.0	15	75		95		110	ns	
			4.5	4	15		19		22		
			6.0	3	13		16		19		
t_h	Minimum Hold Time	V_{CC} (V)	2.0		0		0		0	ns	
			4.5		0		0		0		
			6.0		0		0		0		

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	V_{CC} (V)	5.0		5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	V_{CC} (V)	5.0		115						pF

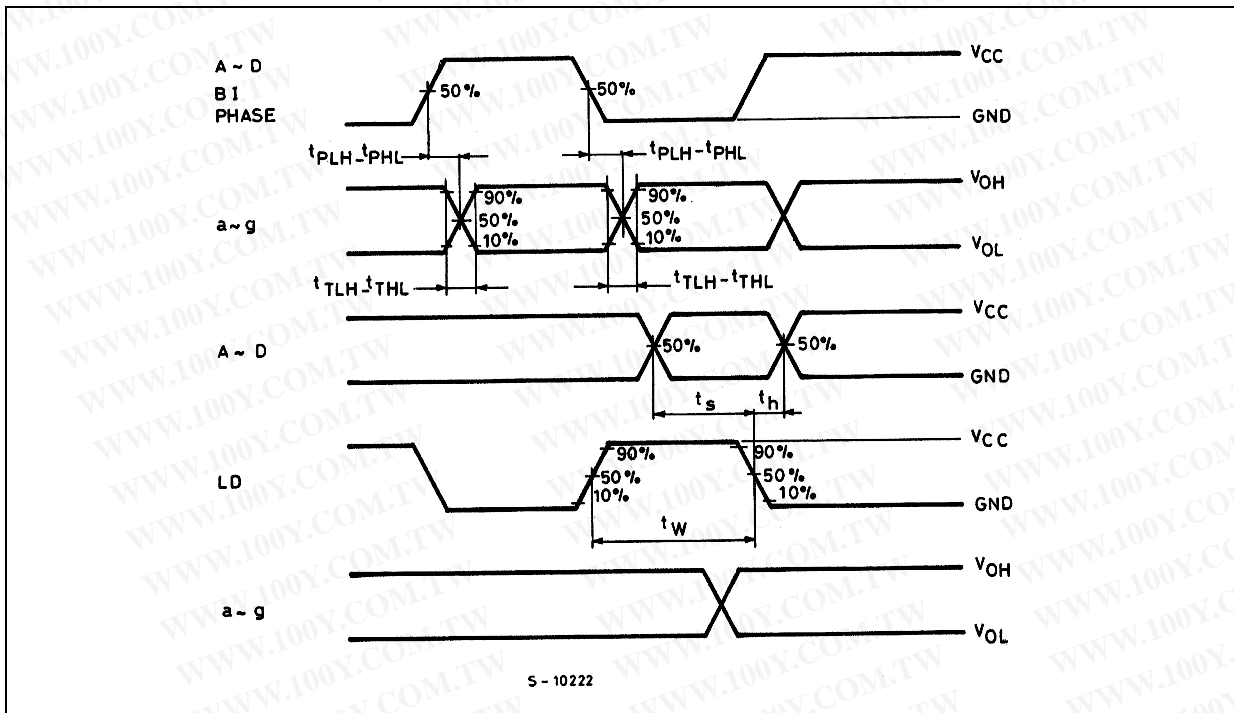
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

TEST CIRCUIT



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

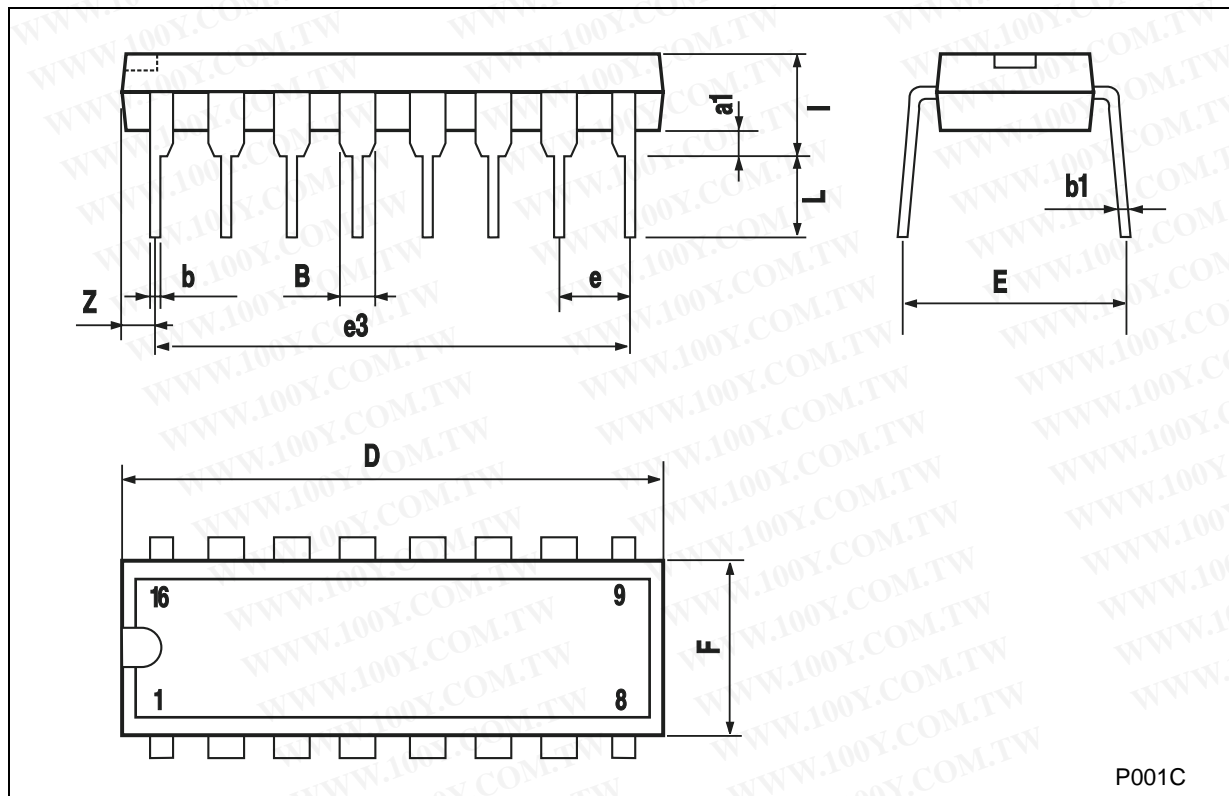
WAVEFORM : PROPAGATION DELAY, SETUP AND HOLD TIMES, MINIMUM PULSE WIDTH (LD)
 ($f=1\text{MHz}$; 50% duty cycle)



S - 10222

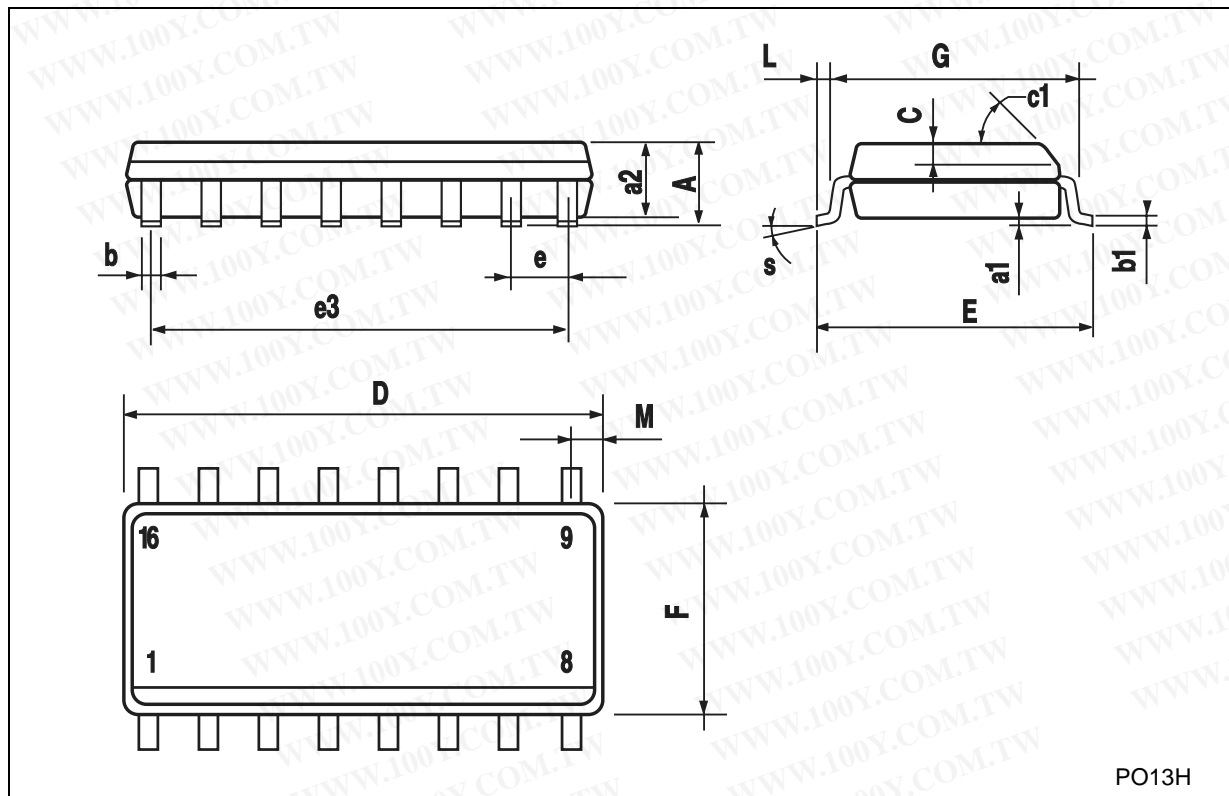
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

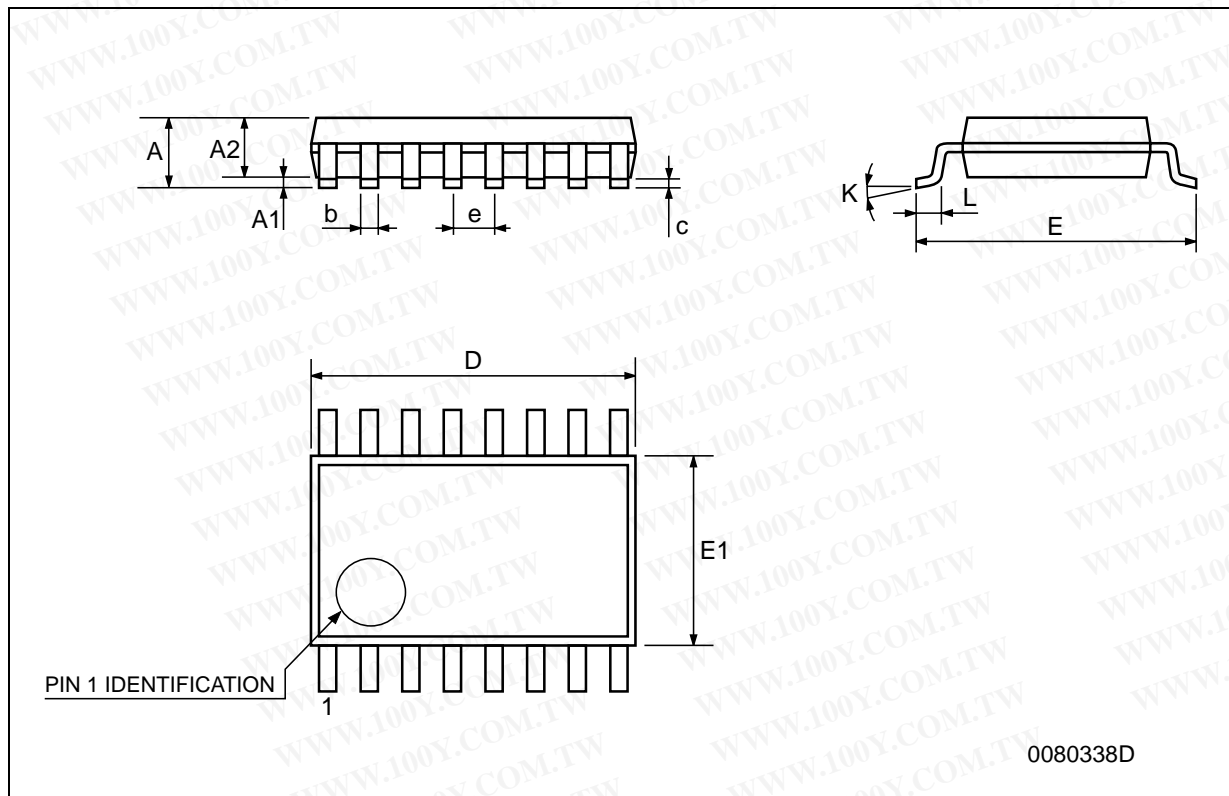
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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