



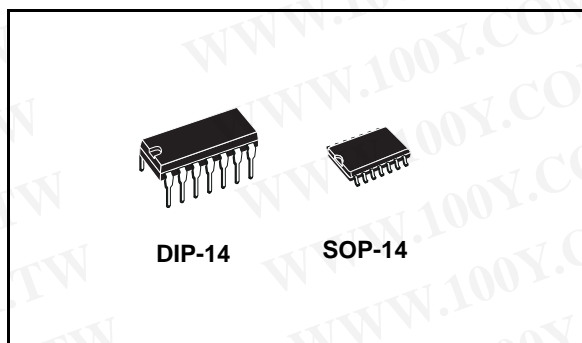
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HCF4093

QUAD 2-input NAND Schmitt trigger

Features

- Schmitt trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at $V_{DD} = 5\text{ V}$ and 2.3 V at $V_{DD} = 10\text{ V}$
- Noise immunity greater than 50% of V_{DD} (typ.)
- No limit on input rise and fall times
- Quiescent current specified up to 20 V
- Standardized symmetrical output characteristics
- 5 V, 10 V and 15 V parametric ratings
- Input leakage current
- $I_I = 100\text{ nA}$ (max) at $V_{DD} = 18\text{ V}$ $T_A = 25^\circ\text{C}$
- 100% tested for quiescent current
- Meets all requirements of JEDEC JESD13B "Standard Specifications for Description of B Series CMOS Devices"



Description

The HCF4093 is a monolithic integrated circuit fabricated in metal oxide semiconductor technology available in DIP and SOP packages.

The HCF4093 type consists of 4 schmitt trigger circuits. Each circuit functions has a 2-input NAND gate with schmitt trigger action on both inputs. The gate switches at different points for positive and negative going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H).

Table 1. Device summary

Order code	Package	Packaging
HCF4093BEY	DIP-14	Tube
HCF4093M013TR	SOP-14	Tape and Reel

1 Pin settings

1.1 Pin connection

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Figure 1. HCF4093B pin connection

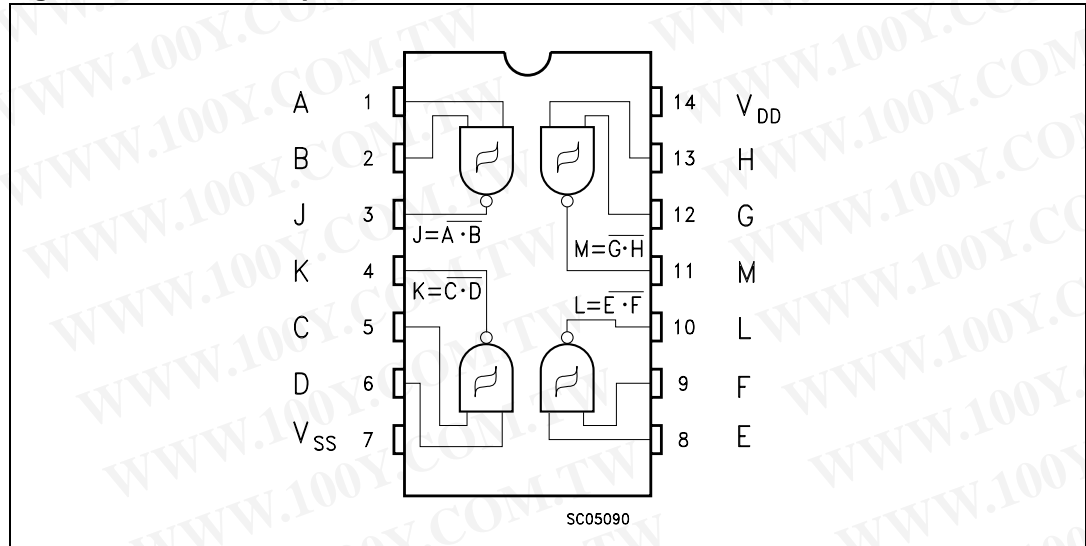


Figure 2. Input equivalent circuit

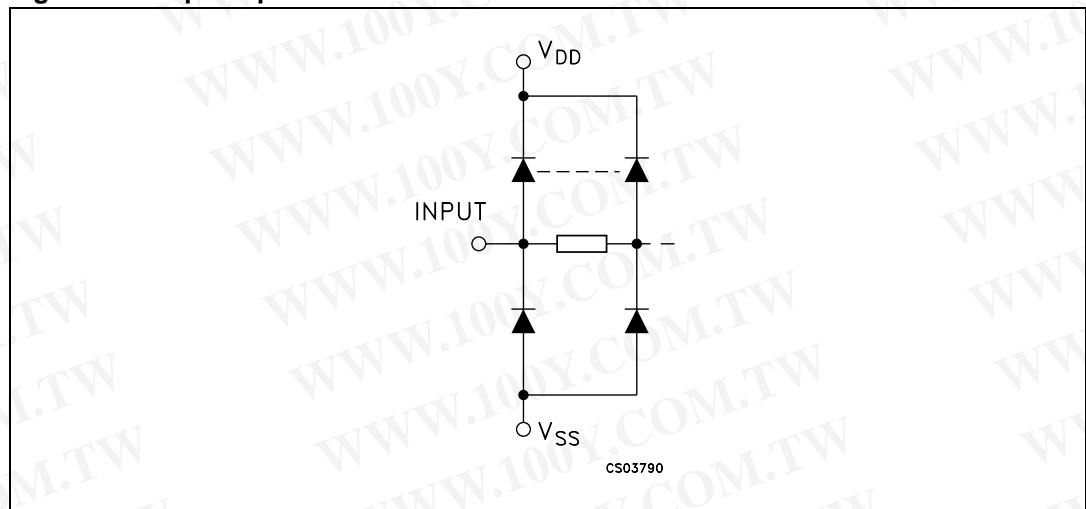


Table 2. Pin description

Pin number	Symbol	Name and function
1, 2, 5, 6, 8, 9, 12, 13	A, B, C, D, E, F, G, H	Data Inputs
3, 4, 10, 11	J, K, L, M	Data Outputs
7	V _{SS}	Negative Supply Voltage
14	V _{DD}	Positive Supply Voltage

Table 3. Truth table

Inputs		Outputs
A, C, E, G	B, D, F, H	J, K, L, M
L	L	H
L	H	H
H	L	H
H	H	L

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2 Maximum ratings

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +22	V
V_I	DC Input voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input current	± 10	mA
P_D	Power dissipation per package	200	mW
	Power dissipation per output transistor	100	mW
T_{op}	Operating temperature	-55 to +125	°C
T_{stg}	Storage temperature	-65 to +150	°C

2.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3 to 20	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature	-55 to 125	°C

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3 Electrical characteristics

Table 6. DC specification

Symbol	Parameter	Test Condition				Value						Unit	
		V _I (V)	V _O (V)	I _{OL} (μ A)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min	Typ	Max	Min	Max	Min		Max
I _L	Quiescent current	0/5			5		0.02	1		30		30	μ A
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	
V _{OH}	High level output voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low level output voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _P	Positive trigger threshold voltage	a			5	2.2	2.9	3.6	2.2	3.6	2.2	3.6	V
		a			10	4.6	5.9	7.1	4.6	7.1	4.6	7.1	
		a			15	6.8	8.8	10.8	6.8	10.8	6.8	10.8	
		b			5	2.6	3.3	4.0	2.6	4	2.6	4	
		b			10	5.6	7	8.2	5.6	8.2	5.6	8.2	
		b			15	6.3	9.4	12.7	6.3	12.7	6.3	12.7	
V _N	Negative trigger threshold voltage	a			5	0.9	1.9	2.8	0.9	2.8	0.9	2.8	V
		a			10	2.5	3.9	5.2	2.5	5.2	2.5	5.2	
		a			15	4	5.8	7.4	4	7.4	4	7.4	
		b			5	1.4	2.3	3.2	1.4	3.2	1.4	3.2	
		b			10	3.4	5.1	6.6	3.4	6.6	3.4	6.6	
		b			15	4.8	7.3	9.6	4.8	9.6	4.8	9.6	
V _H	Hysteresis voltage	a			5	0.3	0.9	1.6	0.3	1.6	0.3	1.6	V
		a			10	1.2	2.3	3.4	1.2	3.4	1.2	3.4	
		a			15	1.6	3.5	5	1.6	5	1.6	5	
		b			5	0.3	0.9	1.6	0.3	1.6	0.3	1.6	
		b			10	1.2	2.3	3.4	1.2	3.4	1.2	3.4	
		b			15	1.6	3.5	5	1.6	5	1.6	5	

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Table 6. DC specification (continued)

Symbol	Parameter	Test Condition				Value						Unit	
		V _I (V)	V _O (V)	I _{OL} (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min	Typ	Max	Min	Max	Min		Max
I _{OH}	Output drive current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output sink current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input leakage current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA
C _I	Input capacitance		Any Input				5	7.5					pF

- The noise margin for both "1" and "0" level is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, 2.5 V min with V_{DD} = 15 V
 - Input on terminals 1, 5, 8, 12 or 2, 6, 9, 13; other inputs to V_{DD}.
 - Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

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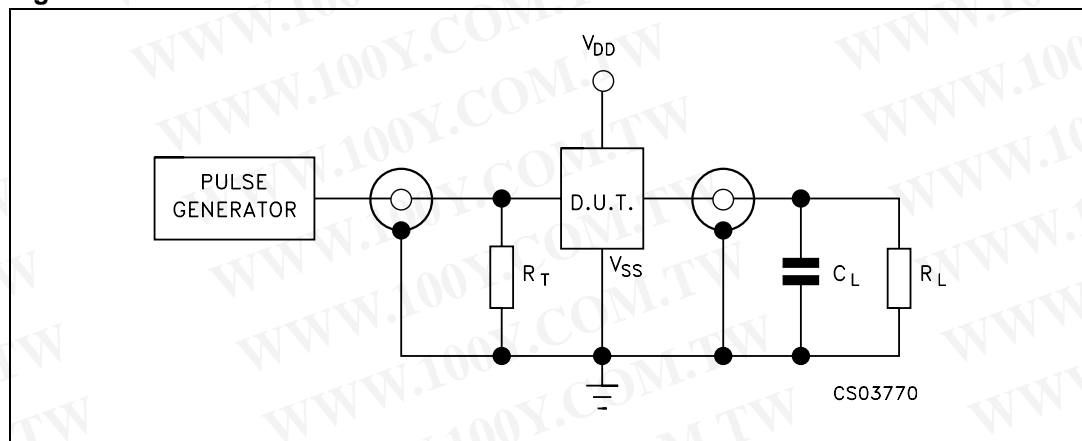
3.1 Dynamic electrical characteristics

Table 7. Dynamic electrical characteristics ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test Condition	Value (*)			Unit
		V_{DD} (V)	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation delay time	5		190	380	ns
		10		90	180	
		15		65	130	
t_{TLH} t_{THL}	Output transition time	5		100	200	ns
		10		50	100	
		15		40	80	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

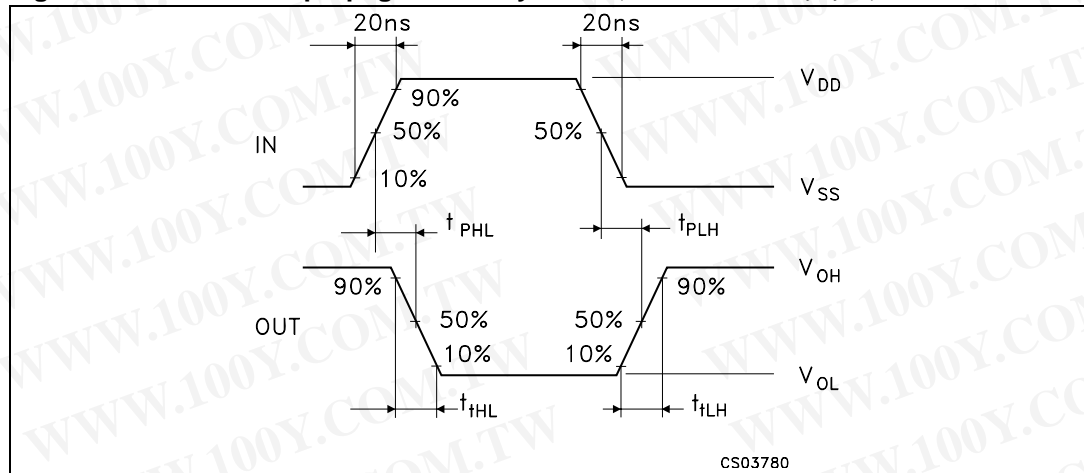
Figure 3. Test circuit



1. $C_L = 50\text{ pF}$ or equivalent (includes jig and probe capacitance)
2. $R_L = 200\text{ K}\Omega$
3. $R_T = Z_{OUT}$ of pulse generator (typically $50\ \Omega$)

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Figure 4. Waveform: propagation delay times (f = 1 MHz; 50% duty cycle)

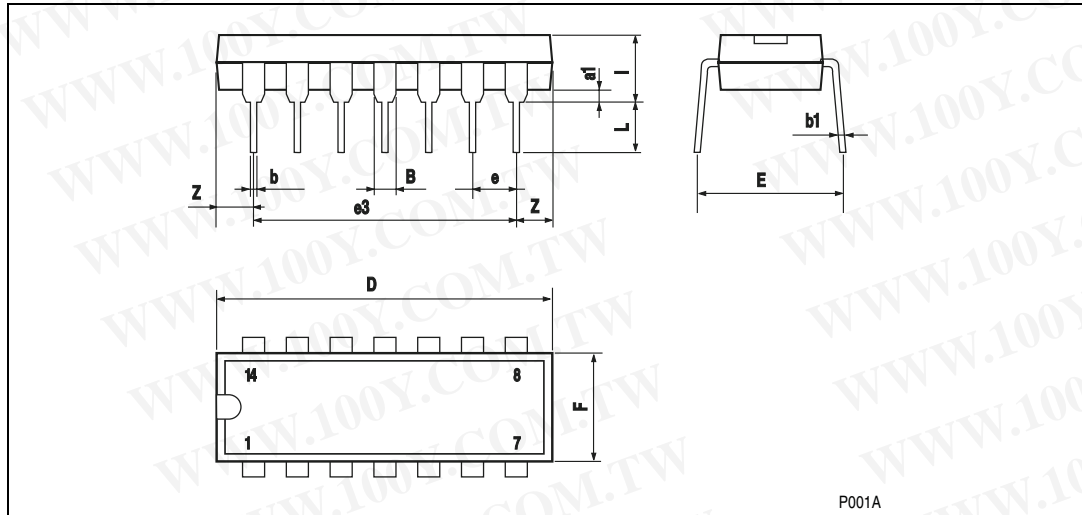


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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 5. Plastic DIP-14 package outline



1. Drawing not to scale.

Table 8. Plastic DIP-14 mechanical data

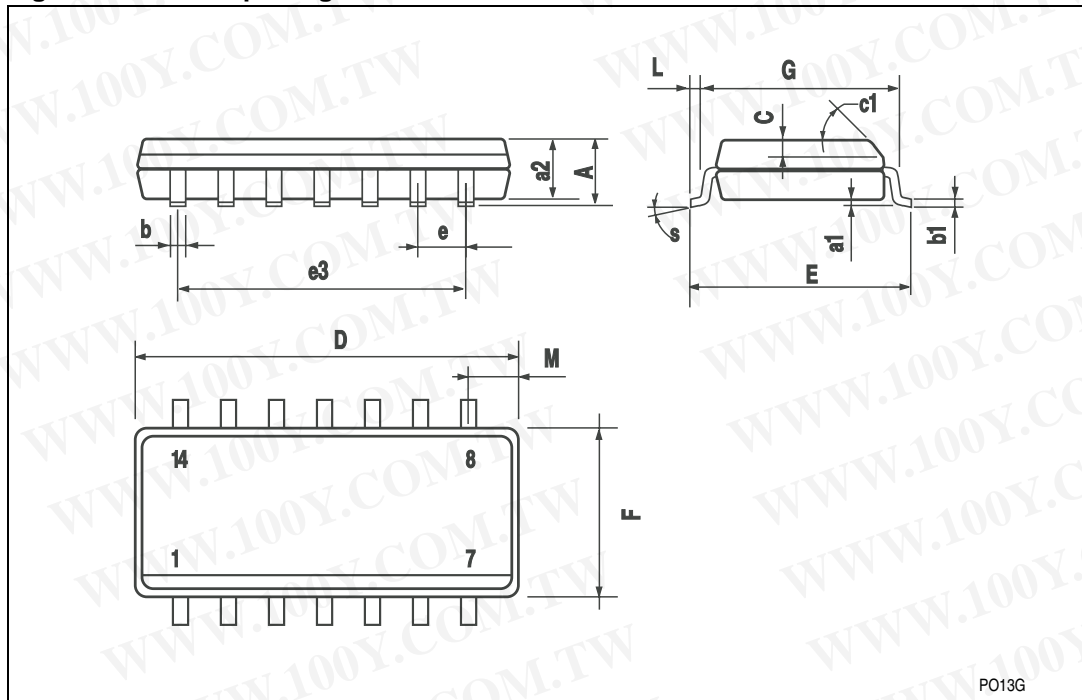
Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



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Figure 6. SO-14 package outline

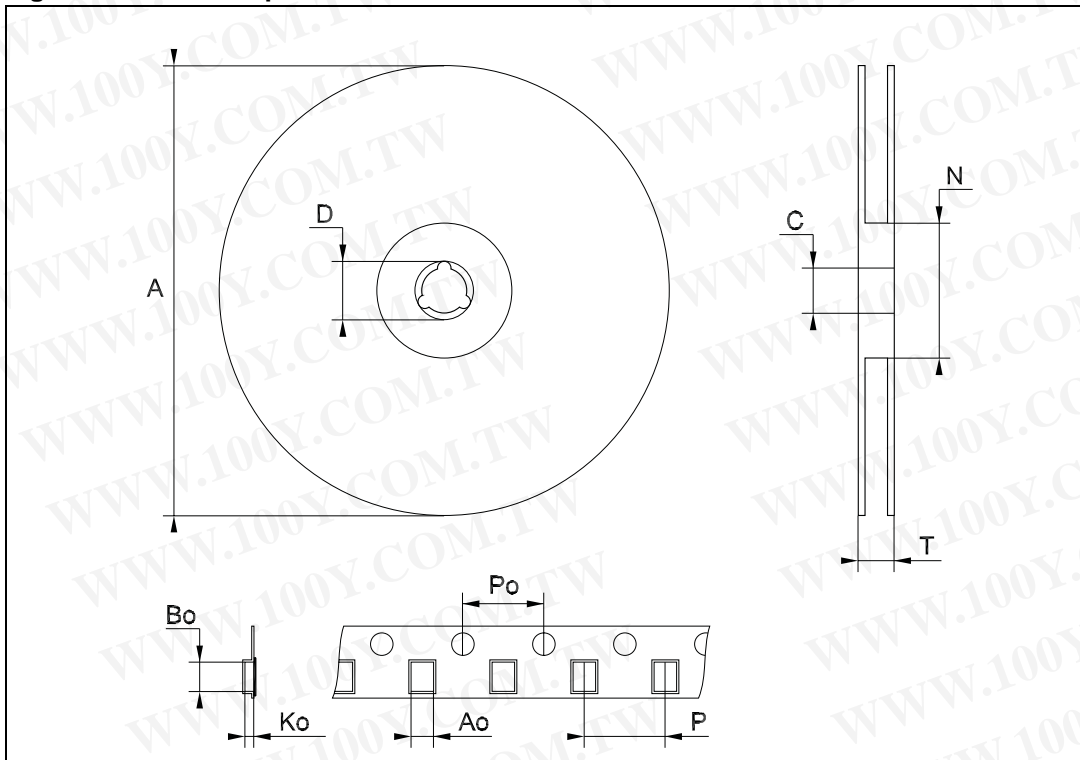


1. Drawing not to scale.

Table 9. SO-14 mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45°(typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8°(max.)					

Figure 7. SO-14 tape and reel information



1. Drawing not to scale.

Table 10. SO-14 tape and reel information

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	2.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

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5 Revision history

Table 11. Document revision history

Date	Revision	Changes
Sept-2001	1	First release
16-Aug-2007	2	Document converted to new ST template, added Figure 7: SO-14 tape and reel information on page 11 and Table 10: SO-14 tape and reel information on page 11 , small text changes.

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