DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4073B
gates
Triple 3-input AND gate

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

TRIPLE 3-INPUT AND GATE

The HEF4073B provides the positive triple 3-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

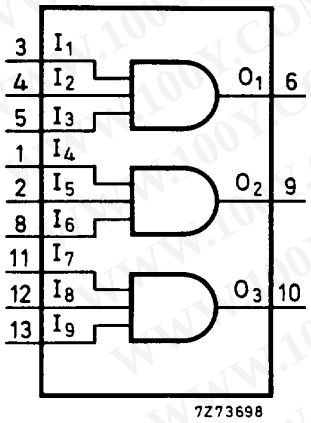

Fig.1 Functional diagram.

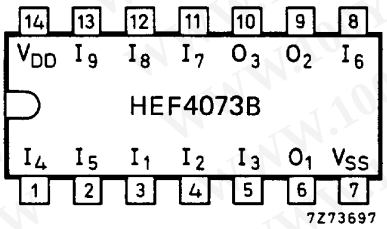

Fig.2 Pinning diagram.

HEF4073BP(N): 14-lead DIL; plastic (SOT27-1)
HEF4073BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
HEF4073BT(D): 14-lead SO; plastic (SOT108-1)
( ): Package Designator North America

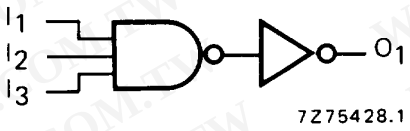

Fig.3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		55	110	ns	23 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		45	90	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	2700 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	8400 f_i + Σ($f_o C_L$) x V_{DD}^2	