DATA SHEET

74F194
4-bit bidirectional universal shift register

Product specification

1989 Apr 04

IC15 Data Handbook

Philips
Semiconductors

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4-bit bidirectional universal shift register 74F194

FEATURES

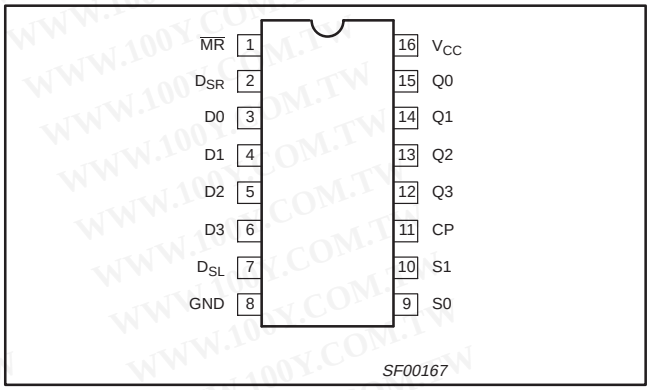
- Shift right and shift left capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the 74F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The 74F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S0 and S1. As shown in the Mode Select-Function Table, data can be entered and shifted from left to right (shift right, Q0→Q1, etc.), or right to left (shift left, Q3→Q2, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S0 and S1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation. Mode Select and data inputs on the 74F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Select and selected data inputs must be stable one setup time prior to the Low-to-High transition of the clock pulse. Signals on the Mode Select, Parallel Data (D0–D3) and Serial Data (D_{SR}, D_{SL}) can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed. The four Parallel Data inputs (D0–D3) are D-type inputs. Data appearing on (D0–D3) inputs when S0 and S1 are High is transferred to the Q0–Q3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

ORDERING INFORMATION

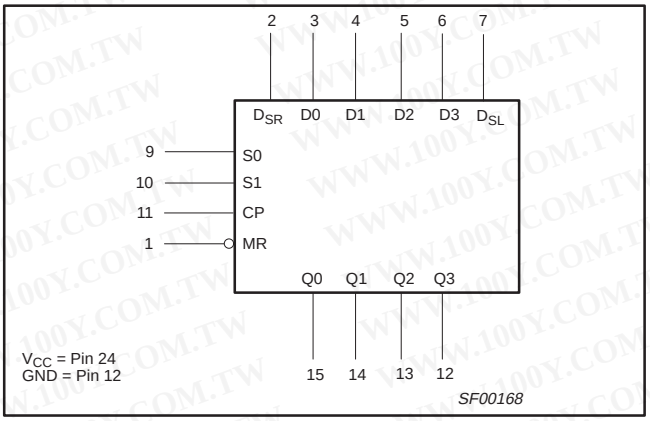
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F194N	SOT38-4
16-pin plastic SO	N74F194D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

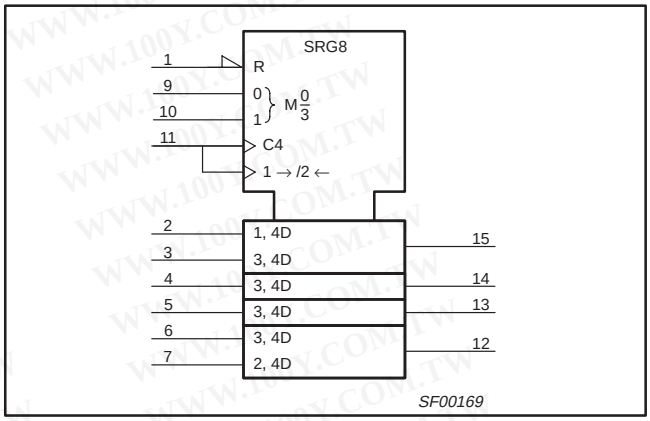
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D3	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S0, S1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q0–Q3	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

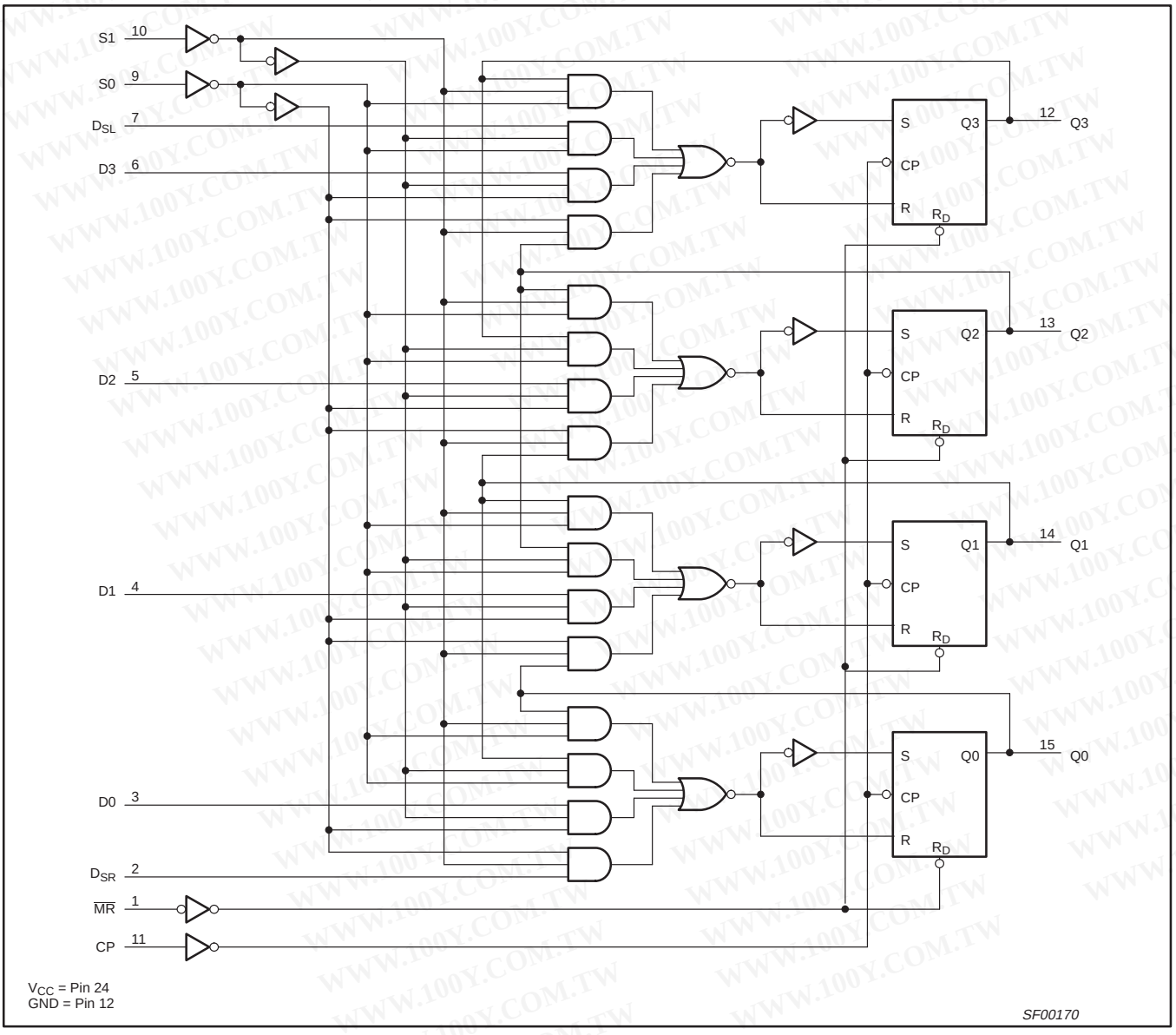
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODES
CP	$\overline{MR}$	S1	S0	D_{SR}	D_{SL}	Dn	Q0	Q1	Q2	Q3	
X	L	X	X	X	X	X	L	L	L	L	Reset (clear)
X	H	l	l	X	X	X	q0	q1	q2	q3	Hold (do nothing)
↑	H	h	l	X	l	X	q1	q2	q3	L	Shift left
↑	H	h	l	X	h	X	q1	q2	q3	H	
↑	H	l	h	l	X	X	L	q0	q1	q2	Shift right
↑	H	l	h	h	X	X	H	q0	q1	q2	
↑	H	h	h	X	X	dn	d0	d1	d2	d3	Parallel load

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
dn(qn) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[4]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)[5]	V_{CC} = MAX			33	46	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Output High state will change to Low stat if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. With all outputs open, D_i inputs grounded and a 4.5V applied to S0, S1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

AC ELECTRICAL CHARACTERISTICS

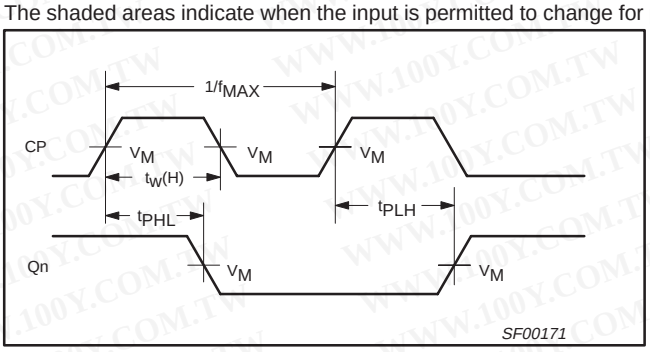
SYMBOL	PARAMETER	TEST CONDITION	LIMITS: V_{CC} = +5.0V, T_{amb} = +25°C, C_L = 50pF, R_L = 500Ω			LIMITS: V_{CC} = +5.0V ± 10%, T_{amb} = 0°C to +70°C, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 2	4.5	8.6	12.0	4.5	14.0	ns

AC SETUP REQUIREMENTS

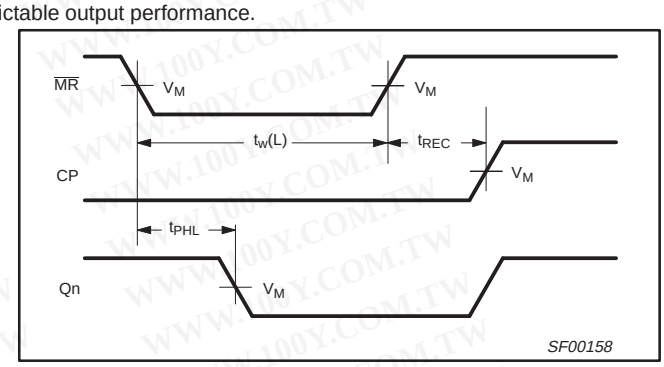
SYMBOL	PARAMETER	TEST CONDITION	LIMITS: V_{CC} = +5.0V, T_{amb} = +25°C, C_L = 50pF, R_L = 500Ω			LIMITS: V_{CC} = +5.0V ± 10%, T_{amb} = 0°C to +70°C, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_S(H) t_S(L)	Setup time, High or Low Dn, D_{SL}, D_{SR} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn, D_{SL}, D_{SR} to CP	Waveform 3	0 0			1.0 1.0		ns
t_S(H) t_S(L)	Setup time, High or Low Sn to CP	Waveform 3	8.0 8.0			9.0 8.0		ns
t_h(H) t_h(L)	Hold time, High or Low Sn to CP	Waveform 3	0 0			0 0		ns
t_W(H)	CP Pulse width, High	Waveform 1	5.0			5.5		ns
t_W(L)	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	7.0			8.0		ns

AC WAVEFORMS

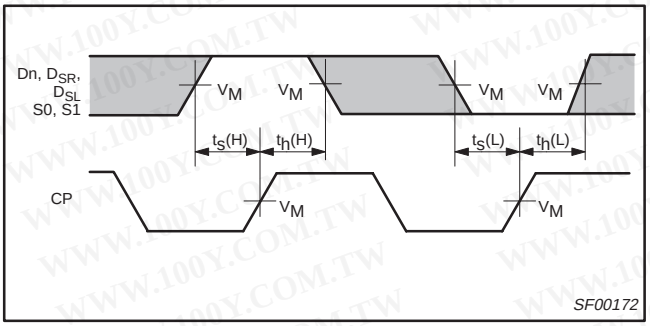
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



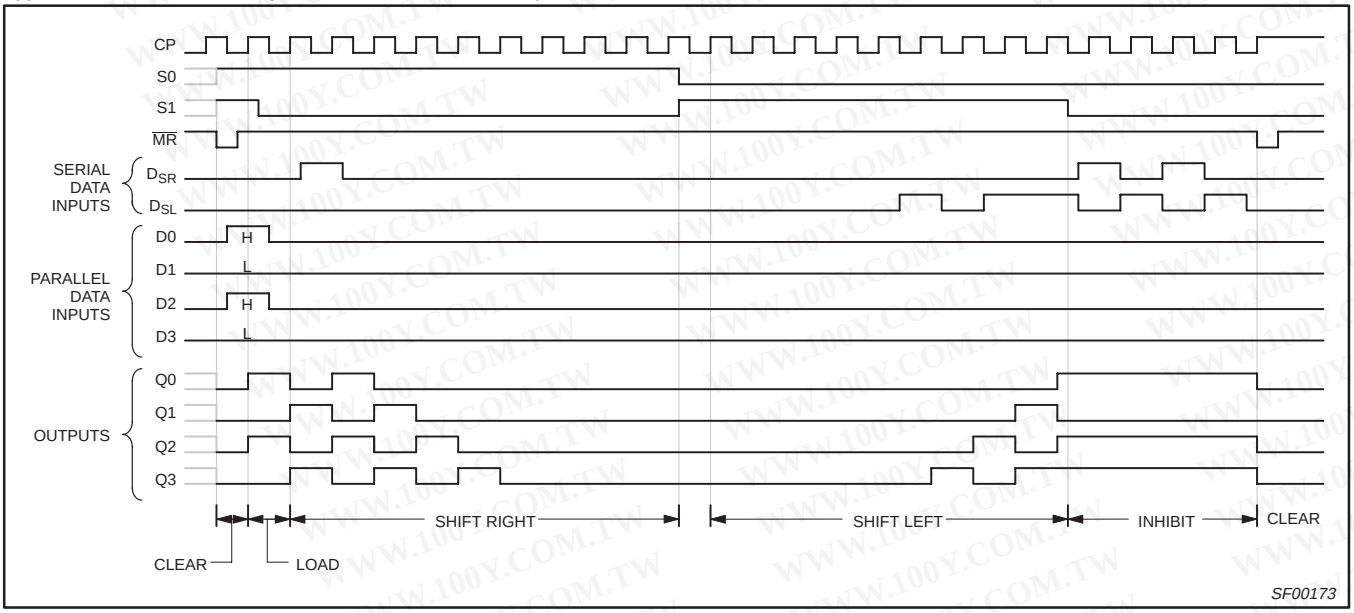
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



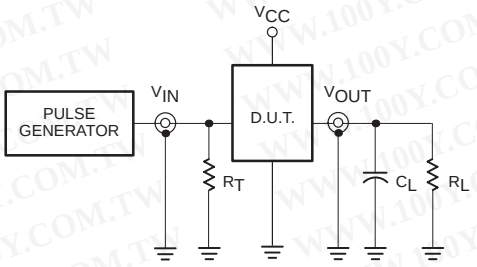
Waveform 3. Setup and Hold Times

TIMING DIAGRAM

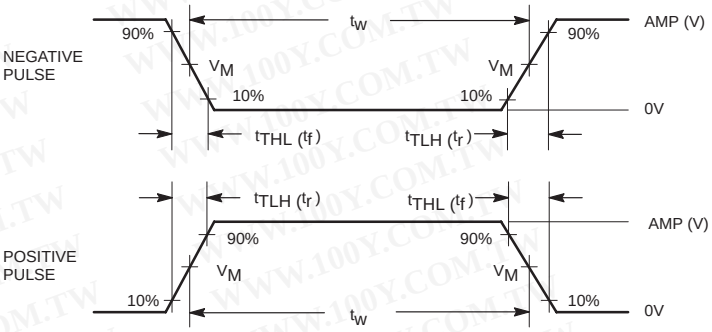
Typical Clear, Load, Shift-Right, Shift-Left and Inhibit Sequence



TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

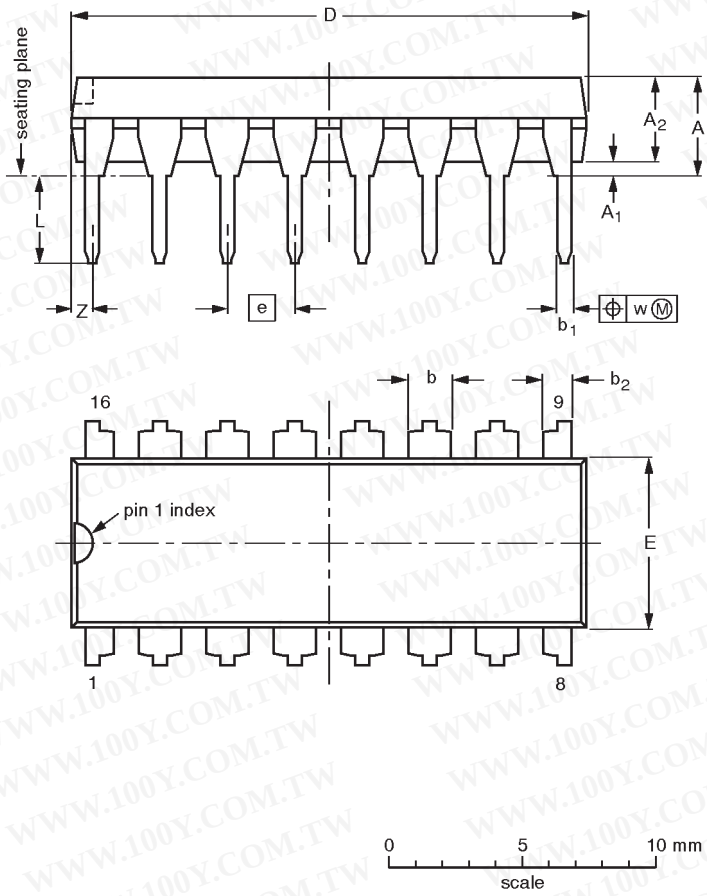
R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

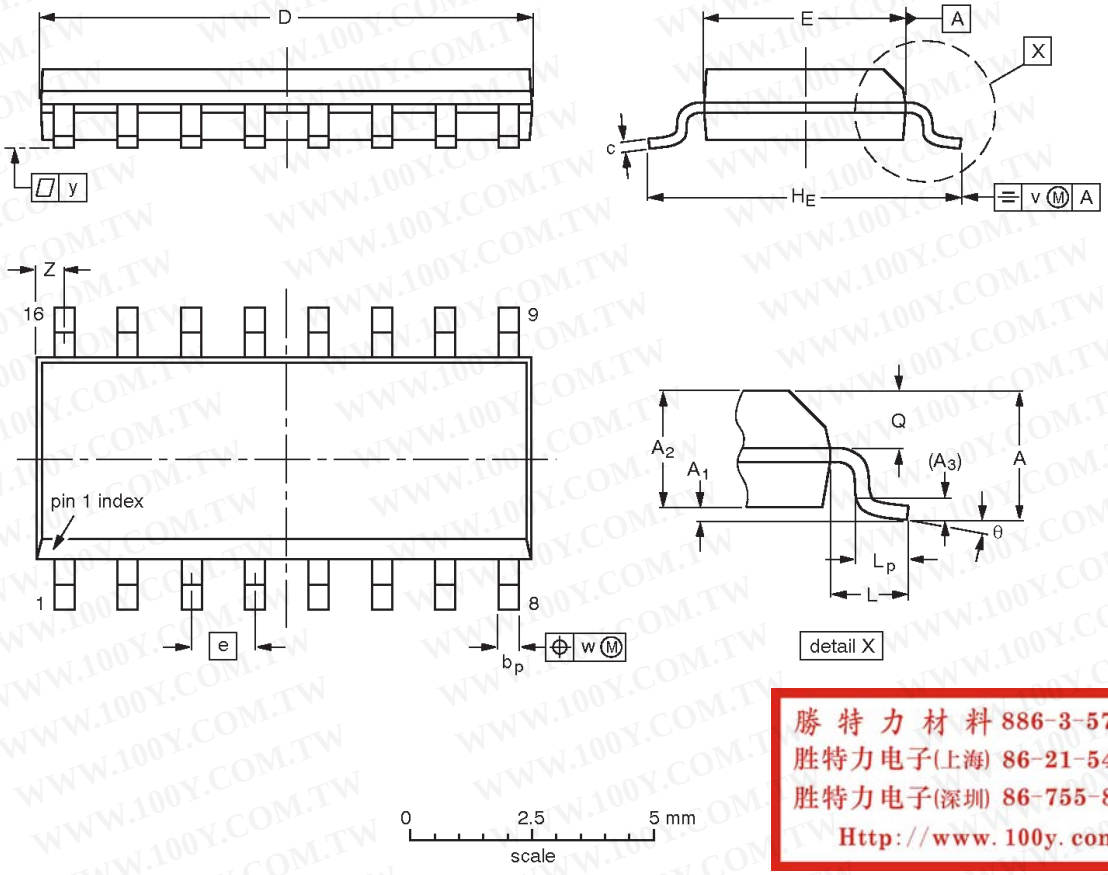
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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