

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-34970699  
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[Http://www.100y.com.tw](http://www.100y.com.tw)

## 74HC/HCT04 Hex inverter

Product specification  
File under Integrated Circuits, IC06

September 1993

## Hex inverter

## 74HC/HCT04

## FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

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## GENERAL DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT04 provide six inverting buffers.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	7	8	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## ORDERING INFORMATION

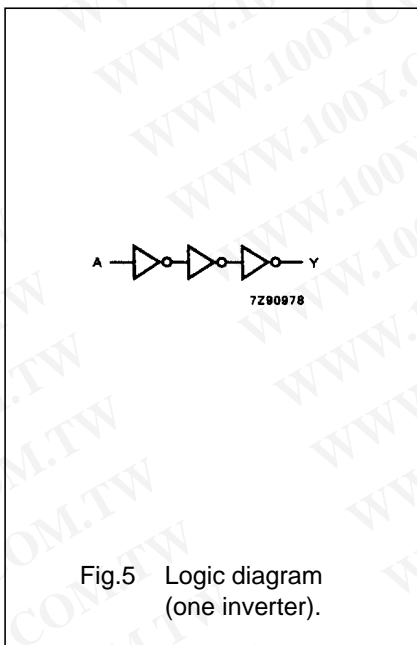
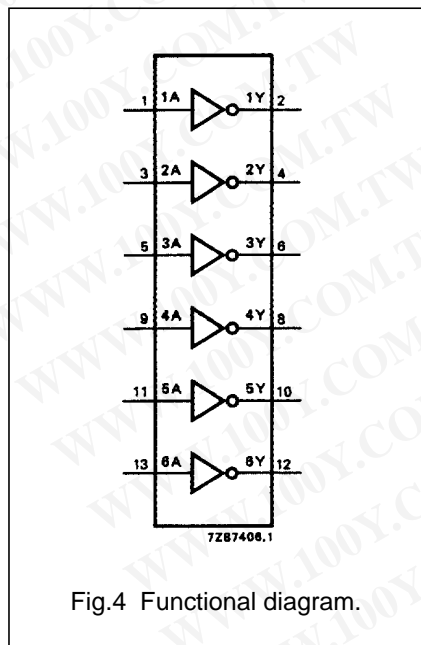
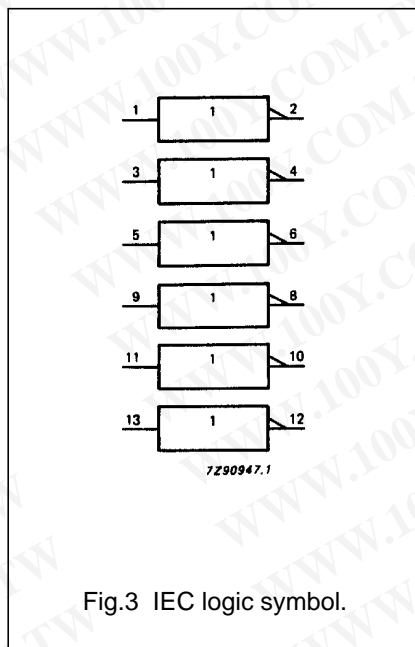
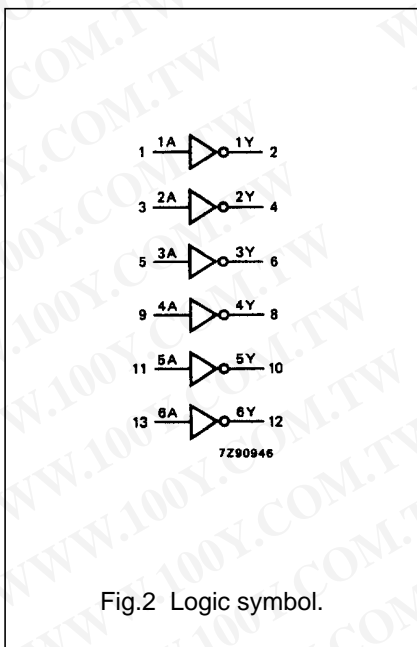
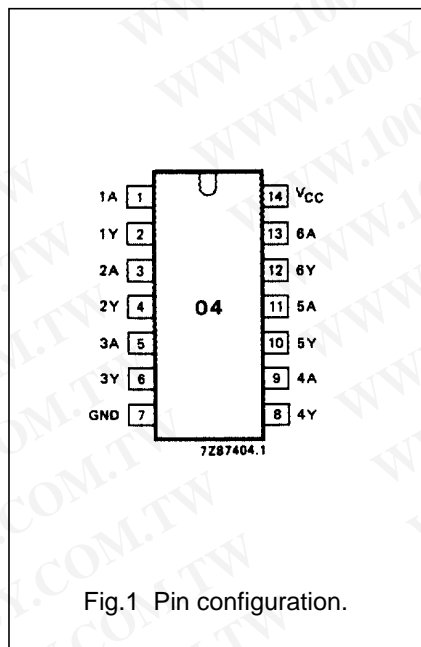
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# Hex inverter

# 74HC/HCT04

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



## FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

### Notes

1. H = HIGH voltage level  
L = LOW voltage level

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## 74HC/HCT04

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: standard

I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.		max.	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	25	85		105		130	ns	2.0 4.5 6.0	Fig.6
		9	17		21		26			
		7	14		18		22			
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19	75		95	110	ns	2.0 4.5 6.0	Fig.6
			7	15		19	22			
			6	13		16	19			

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# 74HC/HCT04

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard  
 $I_{CC}$  category: SSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per unit, multiply this value by the unit load coefficient shown in the table below.

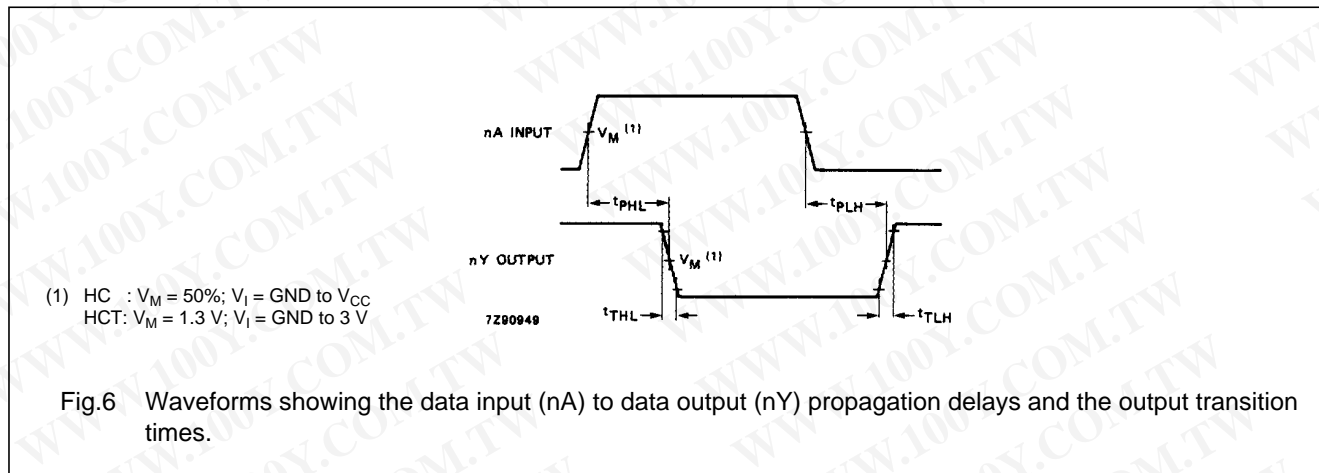
INPUT	UNIT LOAD COEFFICIENT
nA	1.20

### AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
$t_{PHL} / t_{PLH}$	propagation delay nA to nY		10	19		24		29	ns	4.5	Fig.6
$t_{THL} / t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig.6

### AC WAVEFORMS



### PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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