74HC21

Dual 4-input AND gate

Rev. 05 — 7 May 2009 **Product data sheet**

1. General description

The 74HC21 is a high-speed Si-gate CMOS device and is pin compatible with low-power Schottky TTL (LSTTL).

The 74HC21 provide the 4-input AND function.

2. Features

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
    - HBM JESD22-A114E exceeds 2000 V
    - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC21N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC21D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC21DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC21PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

founded by Philips

4. Functional diagram

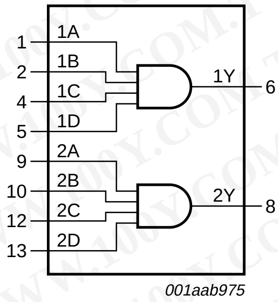


Fig 1. Functional diagram

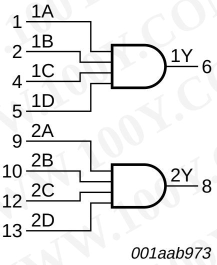


Fig 2. Logic symbol

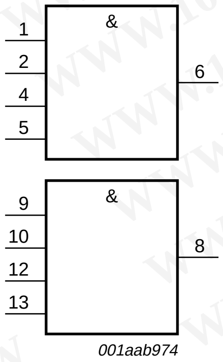


Fig 3. IEC Logic symbol

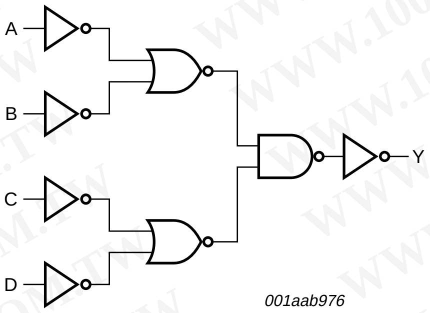


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

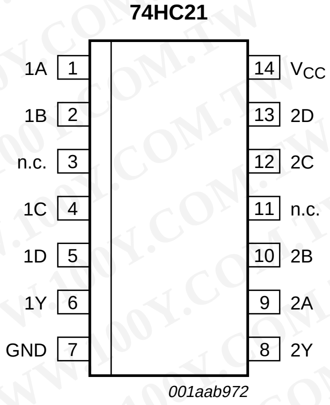


Fig 5. Pin configuration SOT27-1 and SOT108-1

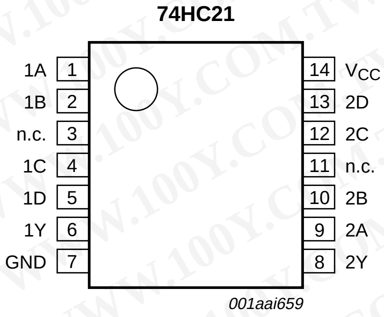


Fig 6. Pin configuration SOT337-1 and SOT402-1

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 1B, 1C, 1D	1, 2, 4, 5	data input
n.c.	3, 11	not connected
1Y	6	data output
GND	7	ground (0 V)
2Y	8	data output
2A, 2B, 2C, 2D	9, 10, 12, 13	data input
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input				Output
nA	**nB**	**nC**	**nD**	**nY**
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation		[2]			
	DIP14 package			-	750	mW
	SO14 and (T)SSOP14 packages			-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	ns/V
T_{amb}	ambient temperature		–40	-	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5$ V	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0$ V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5$ V	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0$ V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = –20$ µA; $V_{CC} = 2.0$ V	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = –20$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = –20$ µA; $V_{CC} = 6.0$ V	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = –4.0$ mA; $V_{CC} = 4.5$ V	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = –5.2$ mA; $V_{CC} = 6.0$ V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20$ µA; $V_{CC} = 2.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 6.0$ V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	2.0	-	20	-	40	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; test circuit see Figure 8.

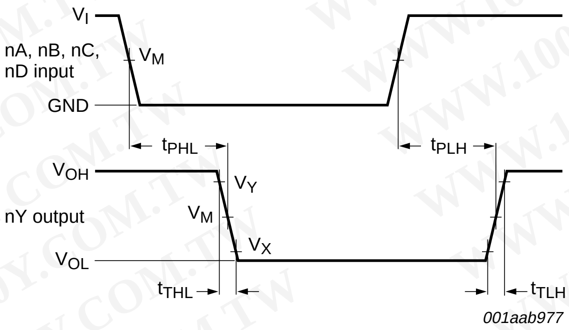
Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nA, nB, nC or nD to nY; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	33	110	-	140	-	165	ns
		V_{CC} = 4.5 V	-	12	22	-	28	-	33	ns
		V_{CC} = 6.0 V	-	10	19	-	24	-	28	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	-	-	ns
t_t	transition time	nY output; see Figure 7 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [3]	-	15	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



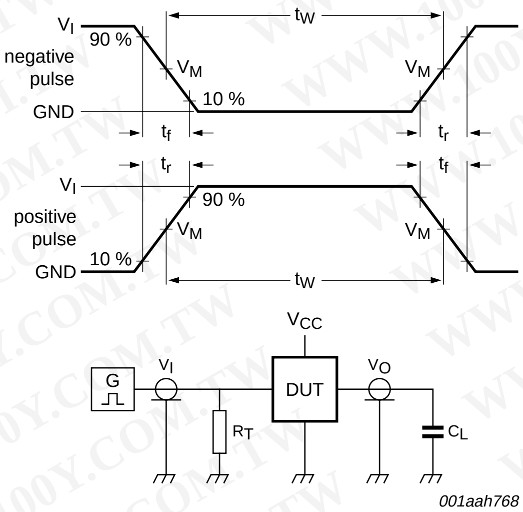
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC21	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

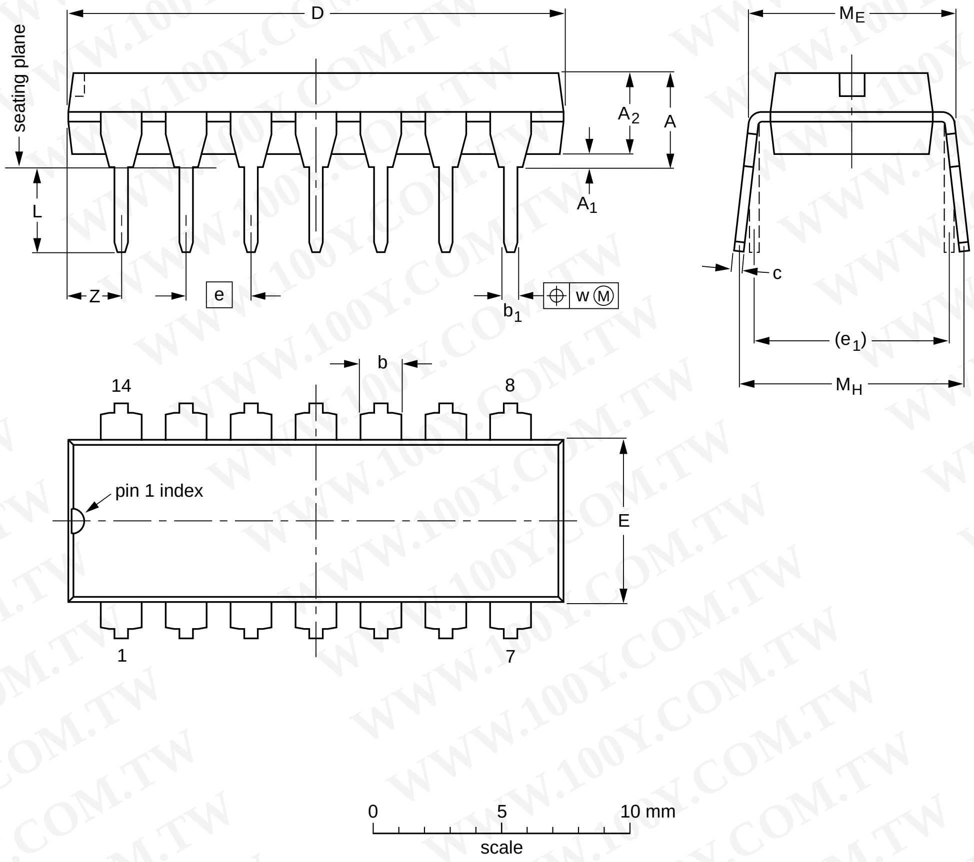
Fig 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC21	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D [1]	E [1]	e	e_1	L	M_E	M_H	w	Z [1] max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

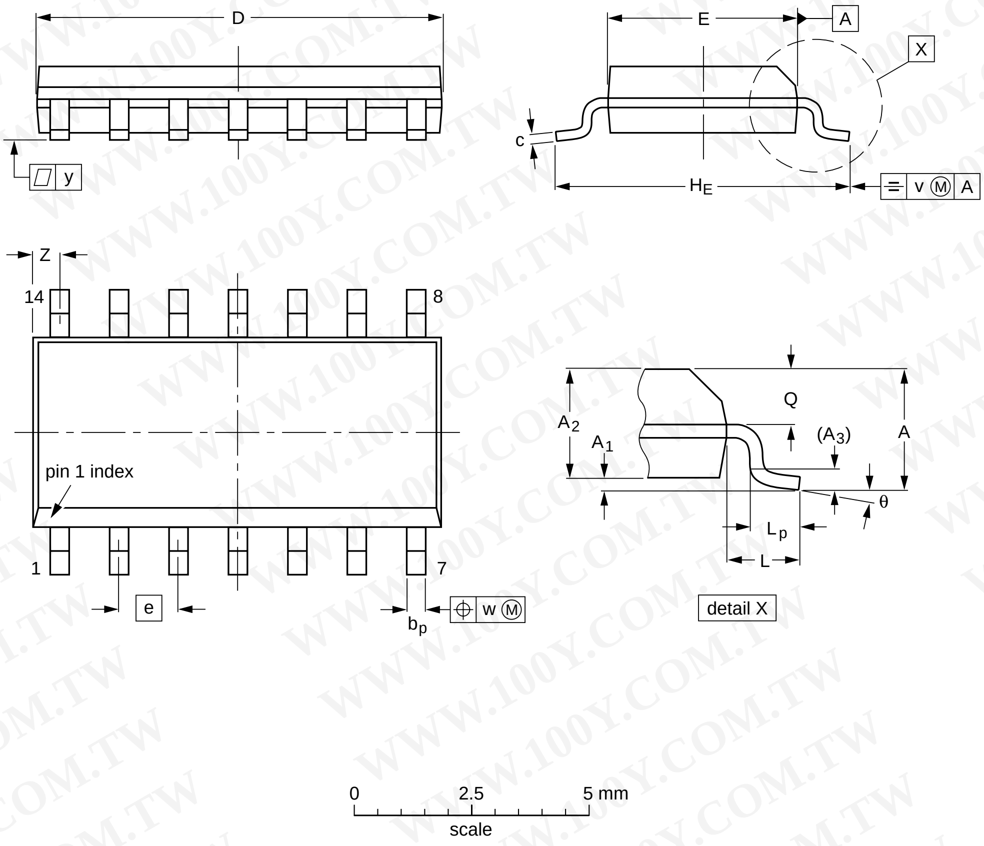
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

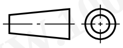
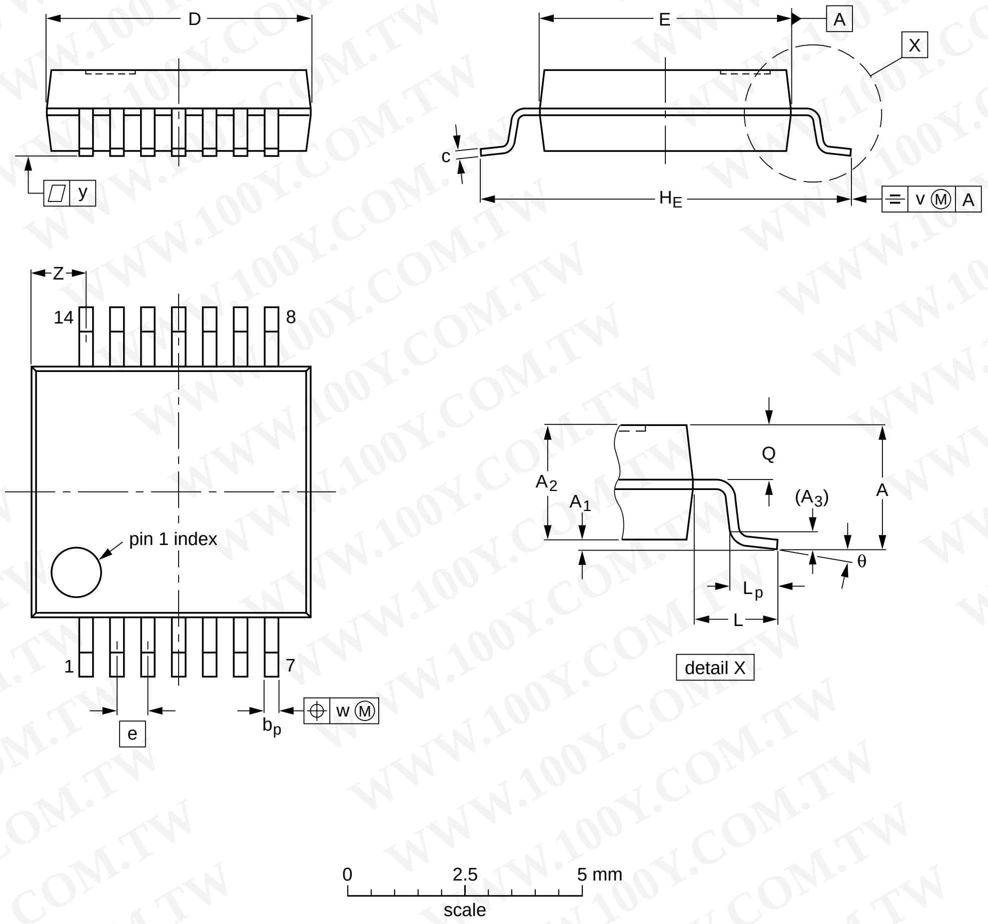
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

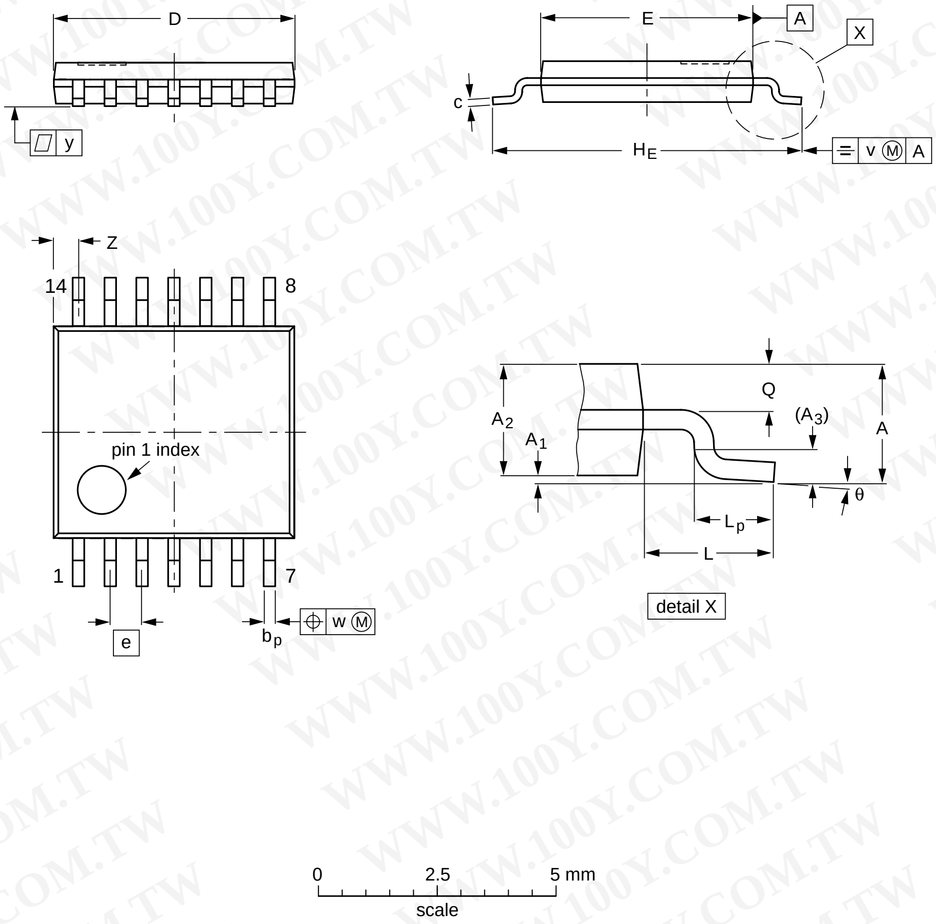
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC21_5	20090507	Product data sheet	-	74HC21_4
Modifications:	Table 1: Type number 74HCT21PW changed to 74HC21PW.			
74HC21_4	20090407	Product data sheet	-	74HC21_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added type number 74HC21PW (TSSOP14 package).			
74HC21_3	20041112	Product data sheet	-	74HC_HCT21_CNV_2
74HC_HCT21_CNV_2	19970828	Product specification	-	74HC_HCT21_1
74HC_HCT21_1	19901201	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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