

74HC157; 74HCT157

Quad 2-input multiplexer

Rev. 5 — 25 April 2012

Product data sheet

1. General description

The 74HC157; 74HCT157 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S). The enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the 74HC/HCT157. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common. The 74HC/HCT157 is logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$$1Y = \bar{E} \times (1I1 \times S + 1I0 \times \bar{S})$$

$$2Y = \bar{E} \times (2I1 \times S + 2I0 \times \bar{S})$$

$$3Y = \bar{E} \times (3I1 \times S + 3I0 \times \bar{S})$$

$$4Y = \bar{E} \times (4I1 \times S + 4I0 \times \bar{S})$$

The 74HC/HCT157 is identical to the 74HC158 but has non-inverting (true) outputs.

2. Features and benefits

- Low-power dissipation
- Non-inverting data path
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC157N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT157N				
74HC157D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT157D				
74HC157DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT157DB				
74HC157PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT157PW				
74HC157BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT157BQ				

4. Functional diagram

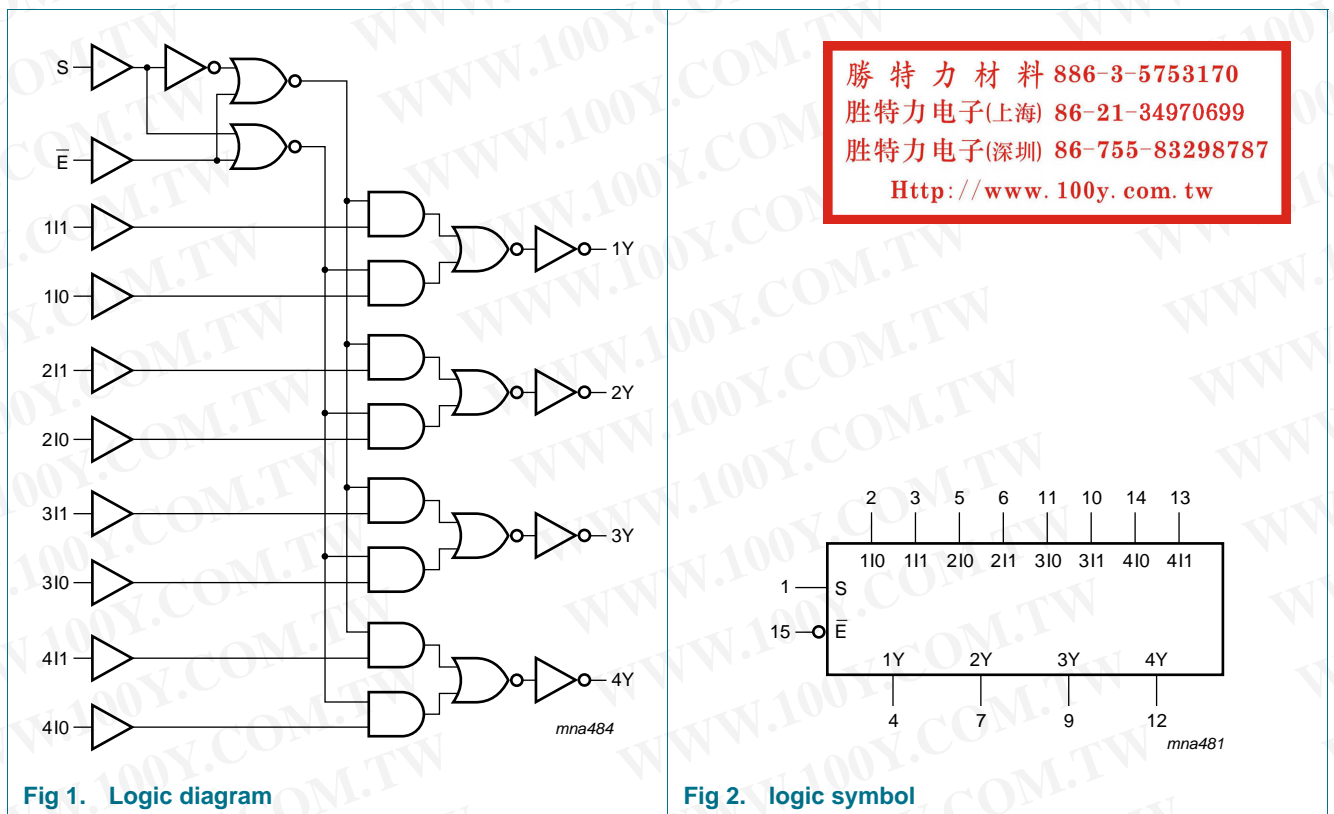


Fig 1. Logic diagram

Fig 2. logic symbol

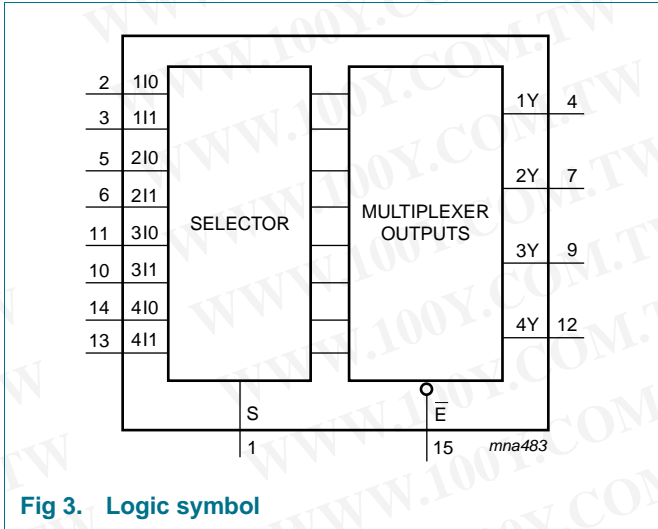


Fig 3. Logic symbol

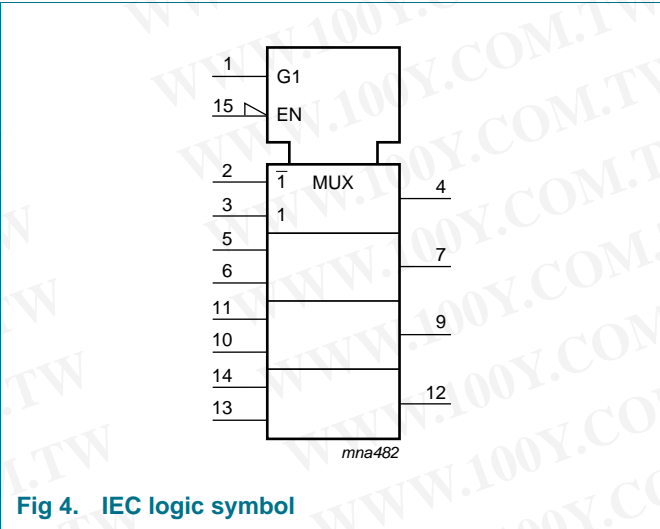


Fig 4. IEC logic symbol

5. Pinning information

5.1 Pinning

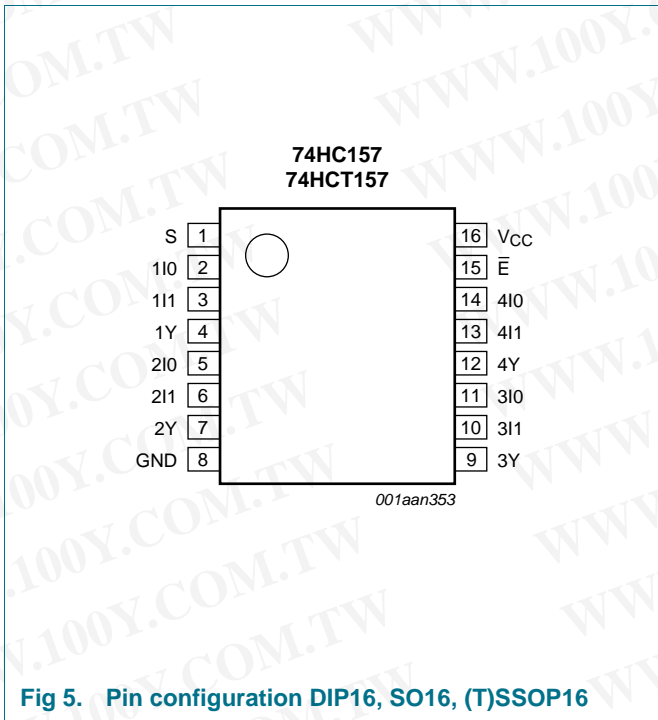


Fig 5. Pin configuration DIP16, SO16, (T)SSOP16

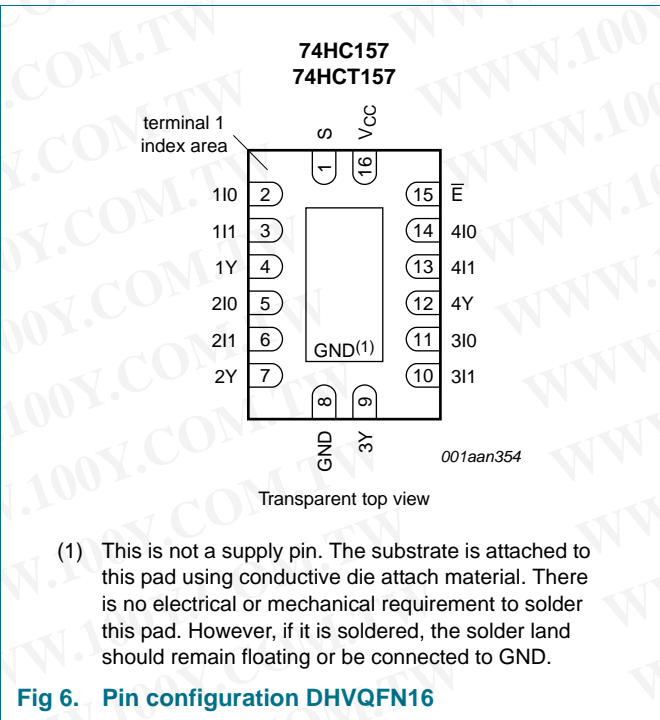


Fig 6. Pin configuration DHVQFN16

- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0 to 4I0	2, 5, 11, 14	data inputs from source 0
1I1 to 4I1	3, 6, 10, 13	data inputs from source 1
1Y to 4Y	4, 7, 9, 12	multiplexer outputs
GND	8	ground (0 V)
\bar{E}	15	enable input (active LOW)
V _{CC}	16	supply voltage

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6. Functional description

Table 3. Function table^[1]

Input					Output
\bar{E}	S	nI0	nI1	nY	
H	X	X	X	L	
L	L	L	X	L	
L	L	H	X	H	
L	H	X	L	L	
L	H	X	H	H	

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-	-50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
	SO16 package		[1]	500	mW
	TSSOP16 package		[2]	500	mW
	DHVQFN16 package		[3]	500	mW

- [1] P_{tot} derates linearly with 8 mW/K above 70 °C.
 [2] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[3] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC157			74HCT157			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			$T_{amb} = -40\text{ °C to }+85\text{ °C}$		$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC157										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-					pF
74HCT157										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; nIn inputs	-	100	360	-	450	-	490	μA
		per input pin; \bar{E} input	-	60	216	-	270	-	294	μA
		per input pin; S input	-	100	360	-	450	-	490	μA
C _I	input capacitance		-	3.5	-					pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ }^\circ\text{C}$			$T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$		$T_{amb} = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	

For type 74HC157

t_{pd}	propagation delay	nI0, nI1 to nY; see Figure 7 ^[1]								
		$V_{CC} = 2.0$ V	-	36	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	13	25	-	31	-	38	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	11	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	10	21	-	26	-	32	ns
	S to nY; see Figure 7 ^[1]	$V_{CC} = 2.0$ V	-	41	125	-	155	-	190	ns
		$V_{CC} = 4.5$ V	-	15	25	-	31	-	38	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	12	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	12	21	-	26	-	32	ns
	\bar{E} to nY; see Figure 8 ^[1]	$V_{CC} = 2.0$ V	-	39	115	-	145	-	175	ns
		$V_{CC} = 4.5$ V	-	14	23	-	29	-	35	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	11	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	11	20	-	25	-	30	ns
t_t	transition time	nY; see Figure 7 ^[2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
	$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns	
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ ^[3]	-	70	-	-	-	-	-	pF

For type 74HCT157

t_{pd}	propagation delay	nI0, nI1 to nY; see Figure 7 ^[1]								
		$V_{CC} = 4.5$ V	-	16	27	-	34	-	41	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	13	-	-	-	-	-	ns
	S to nY; see Figure 7 ^[1]	$V_{CC} = 4.5$ V	-	22	37	-	46	-	56	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
	\bar{E} to nY; see Figure 8 ^[1]	$V_{CC} = 4.5$ V	-	15	26	-	33	-	39	ns
$V_{CC} = 5$ V; $C_L = 15$ pF		-	12	-	-	-	-	-	ns	

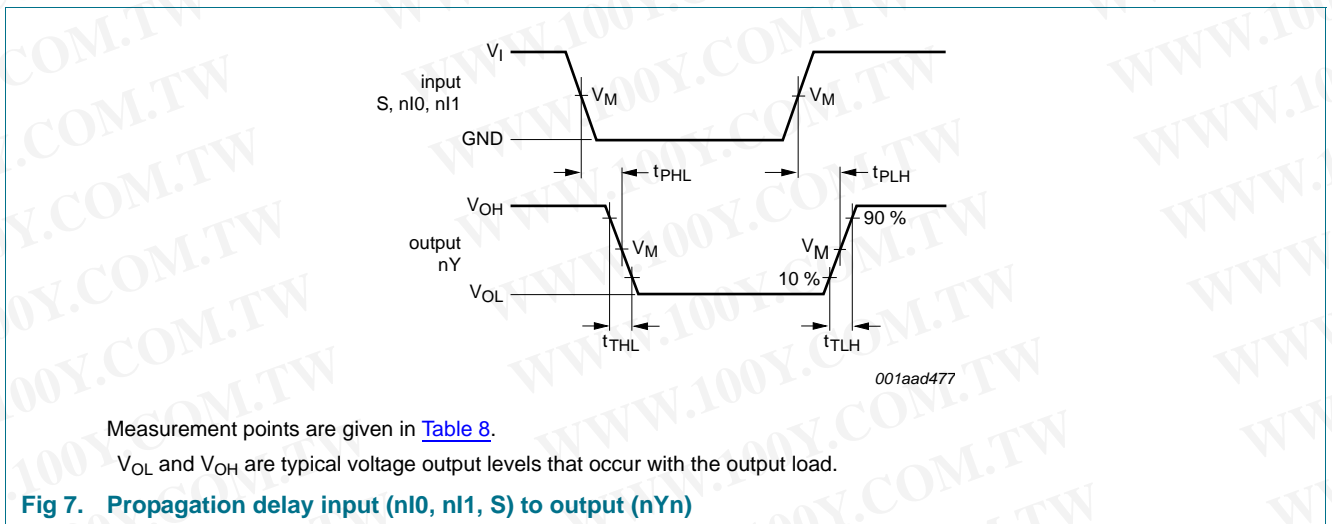
Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ }^\circ\text{C}$			$T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$		$T_{amb} = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	nY; see Figure 7 $V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$	-	70	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



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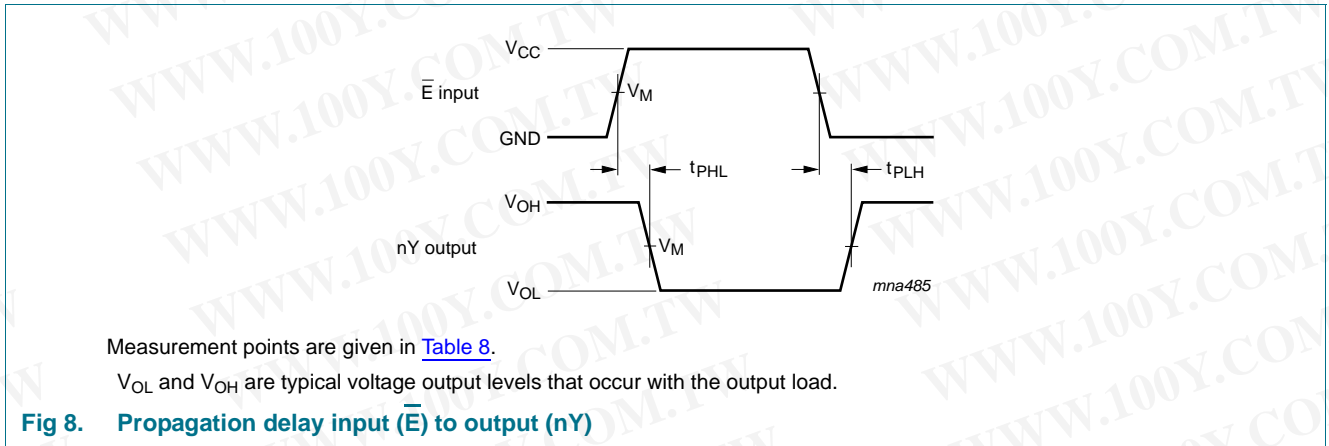


Table 8. Measurement points

Type	Input V_M	Output V_M
74HC157	$0.5V_{CC}$	$0.5V_{CC}$
74HCT157	1.3 V	1.3 V

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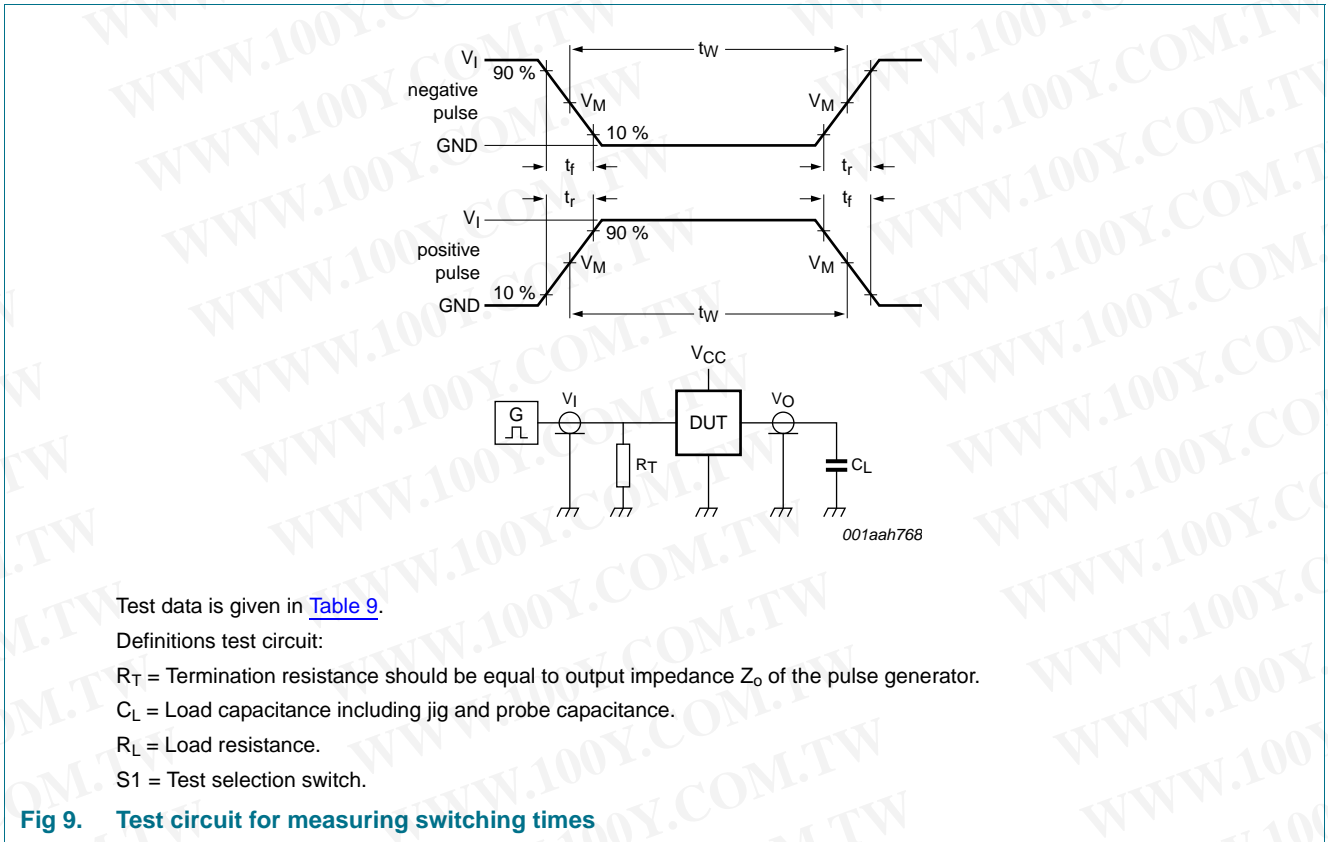


Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC157	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT157	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

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12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

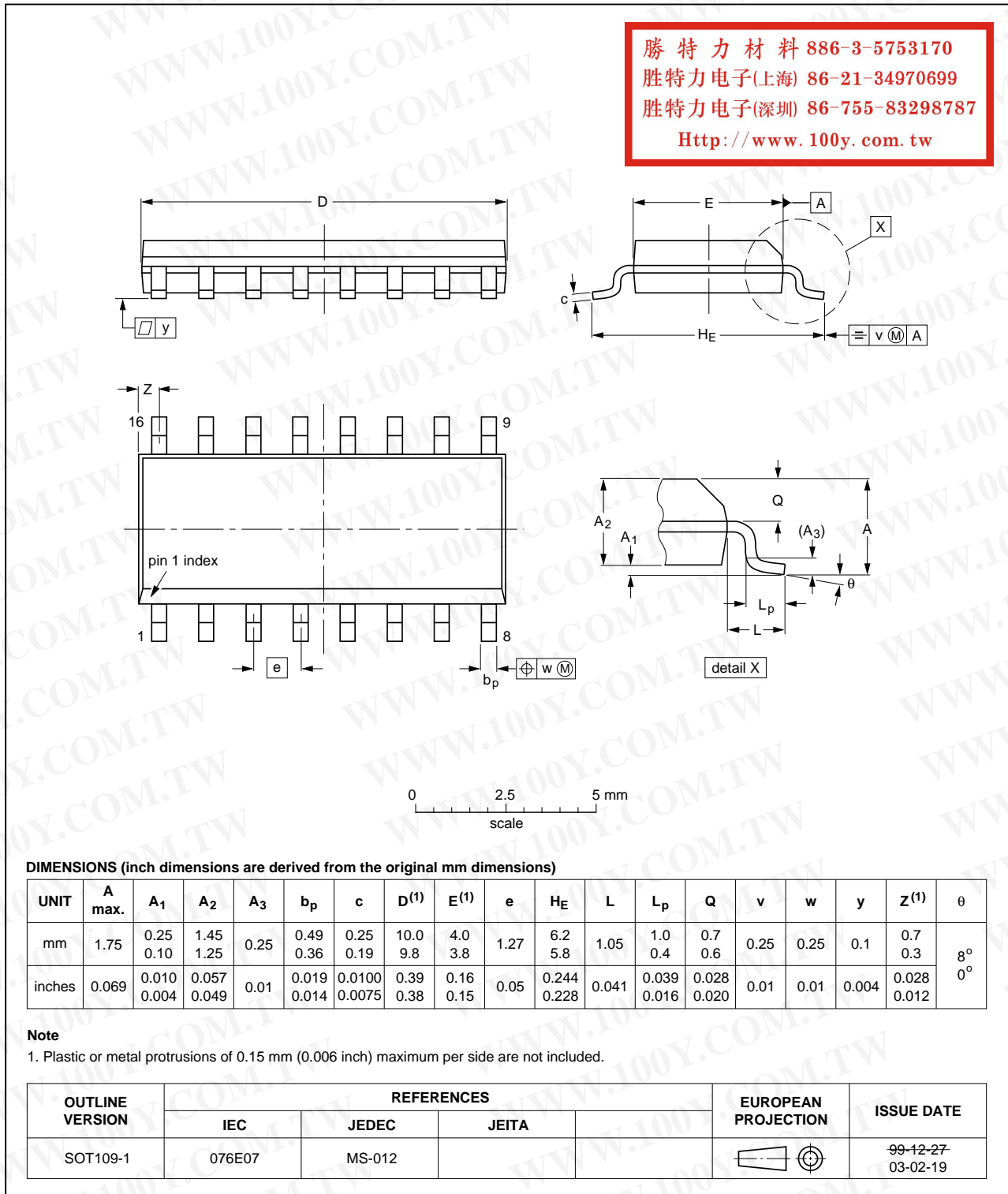


Fig 10. Package outline SOT109-1 (SO16)

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

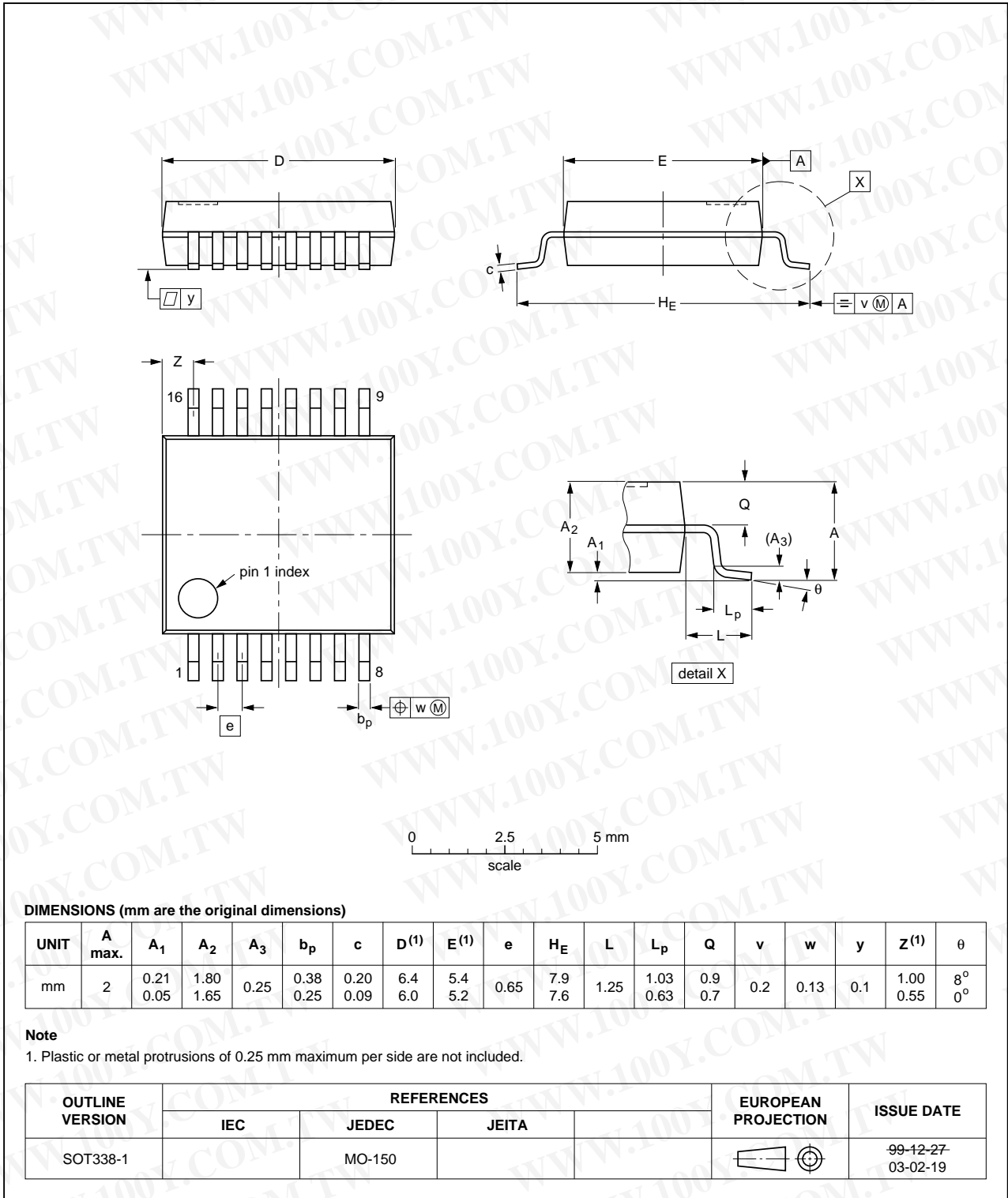


Fig 11. Package outline SOT338-1 (SSOP16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

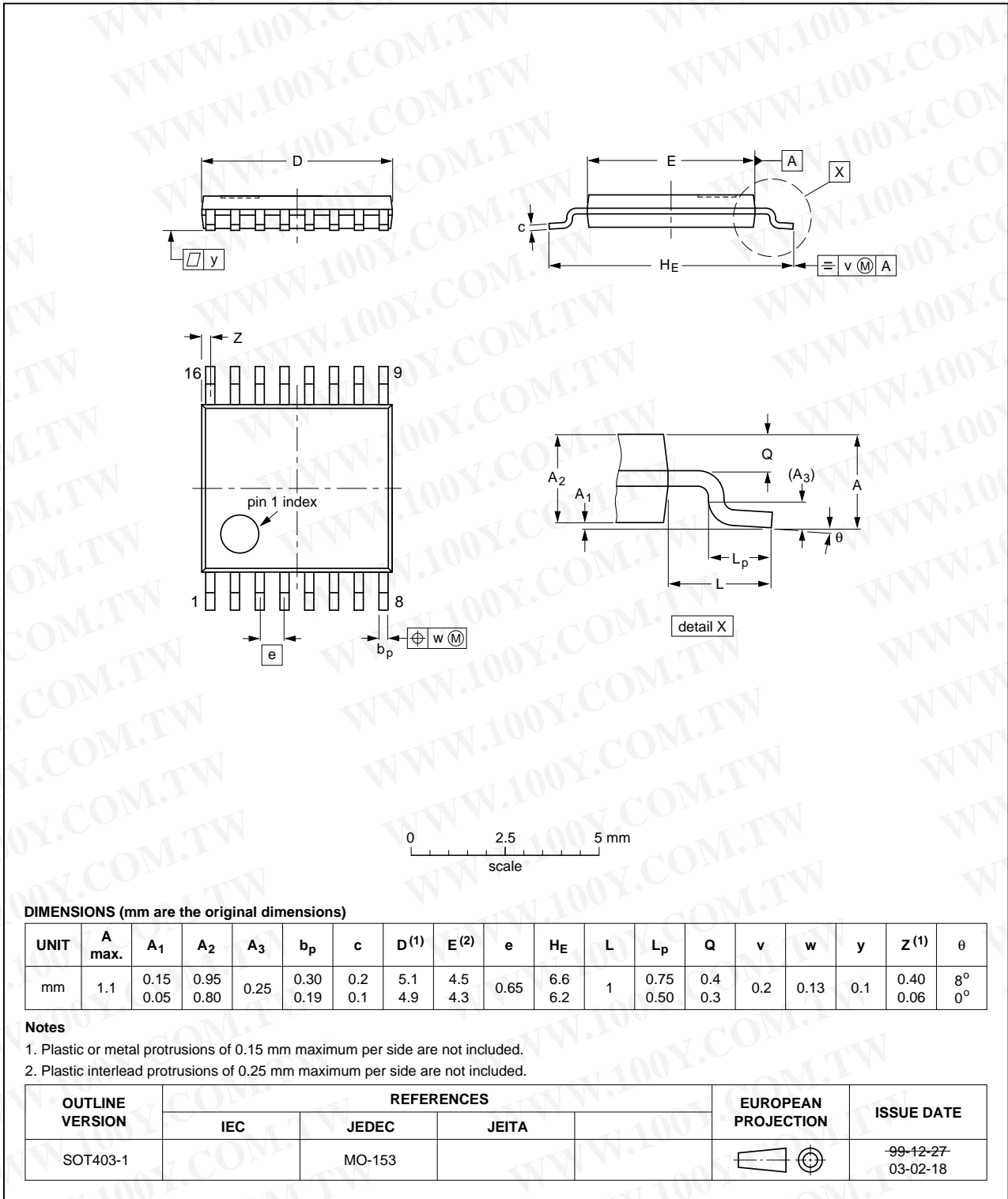
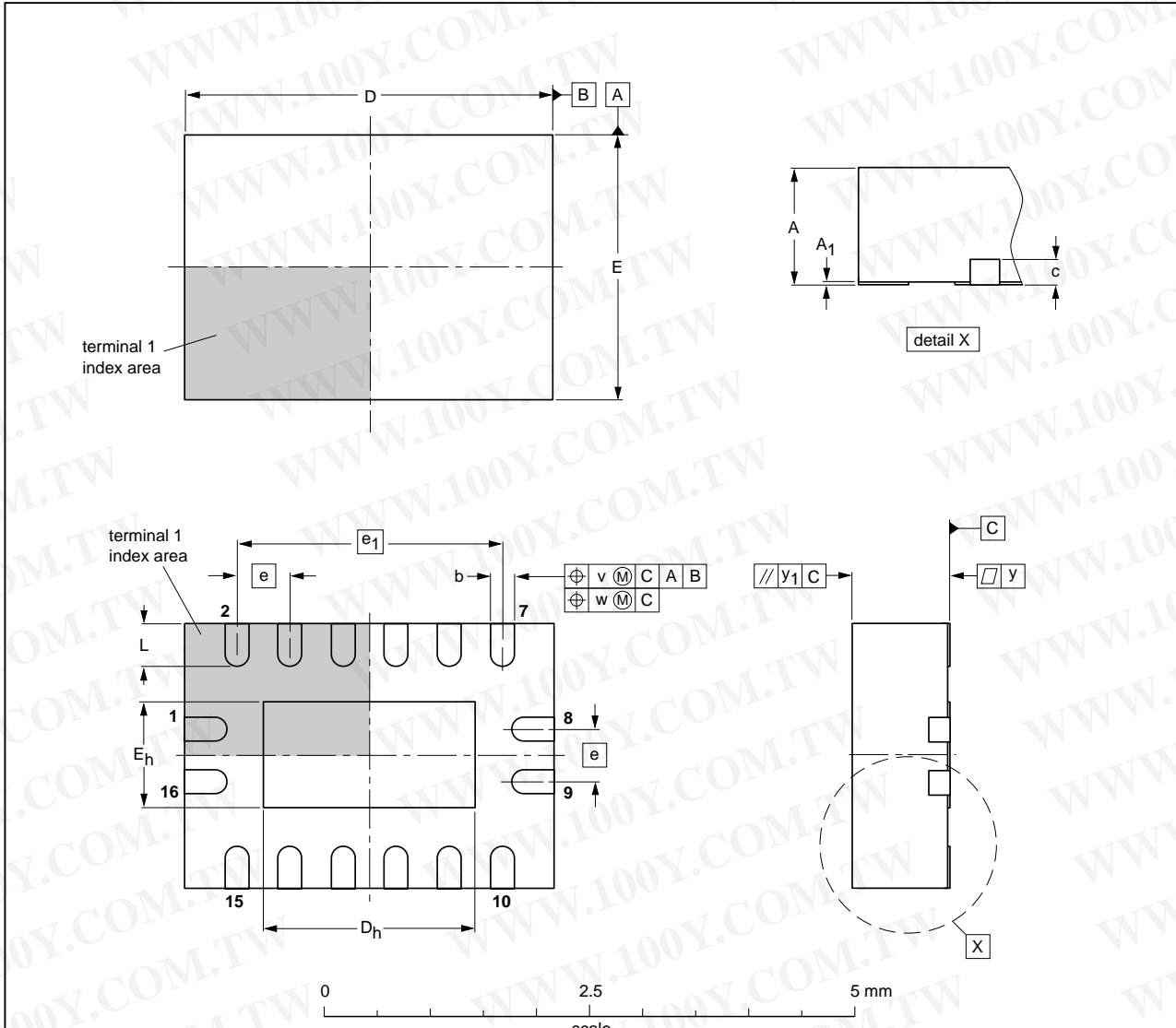


Fig 12. Package outline SOT403-1 (TSSOP16)

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DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	---	MO-241	---			02-10-17 03-01-27

Fig 13. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT157 v.5	20120425	Product data sheet	-	74HC_HCT157 v.4
Modifications:	<ul style="list-style-type: none"> Figure 7 updated with transition times. 			
74HC_HCT157 v.4	20111219	Product data sheet	-	74HC_HCT157 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74HC_HCT157 v.3	20101231	Product data sheet	-	74HC_HCT157_CNV v.2
74HC_HCT157_CNV v.2	19970827	Product specification	-	-

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15. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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