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FAIRCHILD
 SEMICONDUCTOR™

October 1987
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MM74C14

Hex Schmitt Trigger

General Description

The MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The positive and negative going threshold voltages V_{T+} and V_{T-} , show low variation with respect to temperature (typ. $0.0005V/^{\circ}C$ at $V_{CC} = 10V$), and hysteresis, $V_{T+} - V_{T-} \geq 0.2 V_{CC}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

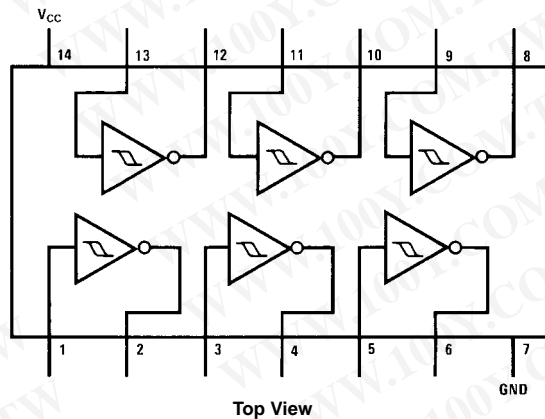
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.70 V_{CC}$ (typ.)
- Low power: TTL compatibility:
0.4 V_{CC} (typ.) 0.2 V_{CC} guaranteed
- Hysteresis: 0.4 V_{CC} (typ.): 0.2 V_{CC} guaranteed

Ordering Code:

Order Number	Package Number	Package Description
MM74C14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74C14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



MM74C14 Hex Schmitt Trigger

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive Going Threshold Voltage	$V_{CC} = 5V$	3.0	3.6	4.3	V
		$V_{CC} = 10V$	6.0	6.8	8.6	
		$V_{CC} = 15V$	9.0	10.0	12.9	
V_{T-}	Negative Going Threshold Voltage	$V_{CC} = 5V$	0.7	1.4	2.0	V
		$V_{CC} = 10V$	1.4	3.2	4.0	
		$V_{CC} = 15V$	2.1	5.0	6.0	
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC} = 5V$	1.0	2.2	3.6	V
		$V_{CC} = 10V$	2.0	3.6	7.2	
		$V_{CC} = 15V$	3.0	5.0	10.8	
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$	4.5			V
		$V_{CC} = 10V, I_O = -10 \mu A$	9.0			
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10 \mu A$			0.5	V
		$V_{CC} = 10V, I_O = 10 \mu A$			1.0	
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V, V_{IN} = 0V/15V$		0.05	15	μA
		$V_{CC} = 5V, V_{IN} = 2.5V$ (Note 2)		20		
		$V_{CC} = 10V, V_{IN} = 5V$ (Note 2)		200		
		$V_{CC} = 15V, V_{IN} = 7.5V$ (Note 2)		600		
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	74C, $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	74C, $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4	V
OUTPUT DRIVE (see Family Characteristics Data Sheet) $T_A = 25^\circ C$ (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$	8.0	16		mA

Note 2: Only one of the six inputs is at $\frac{1}{2} V_{CC}$; the others are either at V_{CC} or GND.

AC Electrical Characteristics (Note 3)

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD0}	Propagation Delay	$V_{CC} = 5\text{V}$		220	400	n
t_{PD1}	from Input to Output	$V_{CC} = 10\text{V}$		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5.0		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 5)		20		pF

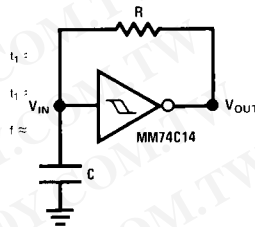
Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Typical Applications

Low Power Oscillator

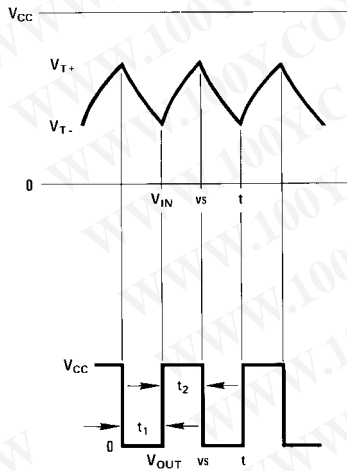


$$t_1 \approx RC \ln \frac{V_{T+}}{V_T}$$

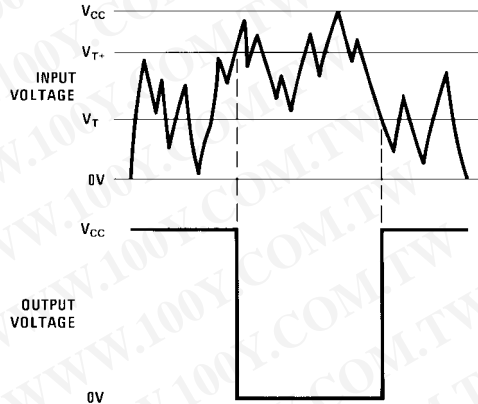
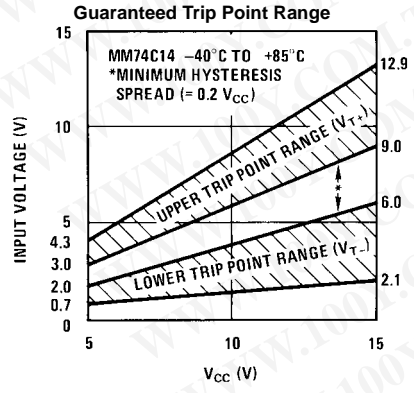
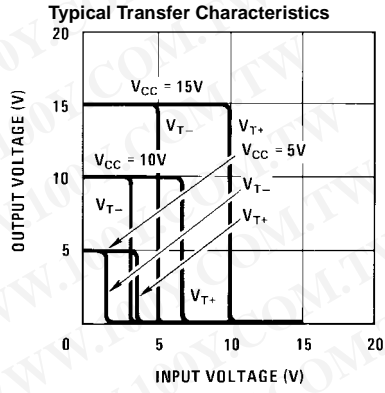
$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}}{V_T} (V_{CC} - V_{T-})} \approx \frac{1}{1.7 RC}$$

Note: The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$

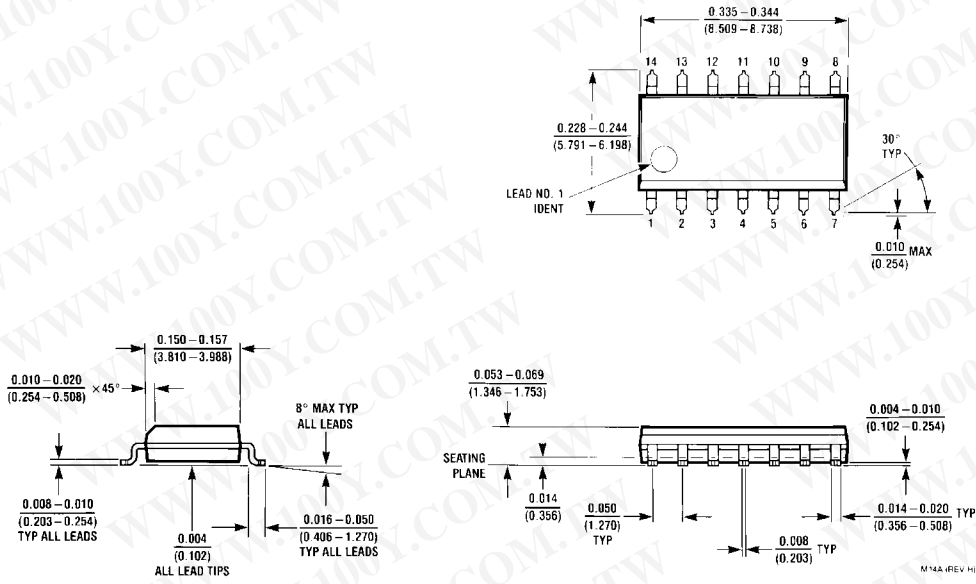


Typical Performance Characteristics



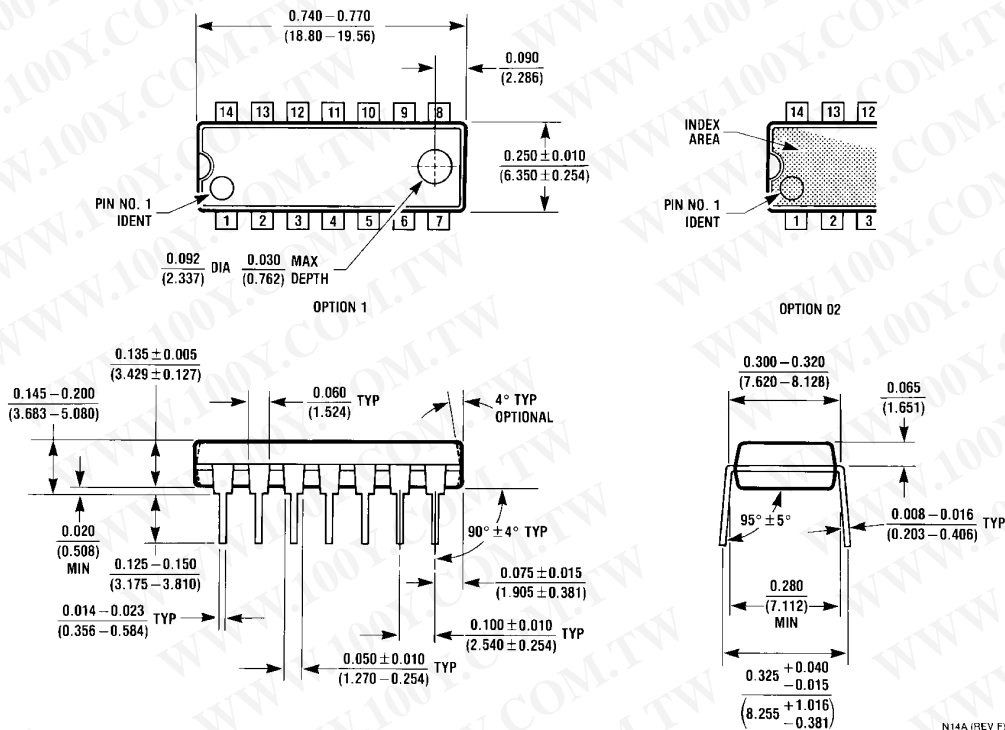
Note: For more information on output drive characteristics, power dissipation, and propagation delays, see AN-90.

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

N14A (REV F)

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