THC63LVD1023

135MHz 67Bits LVDS Transmitter

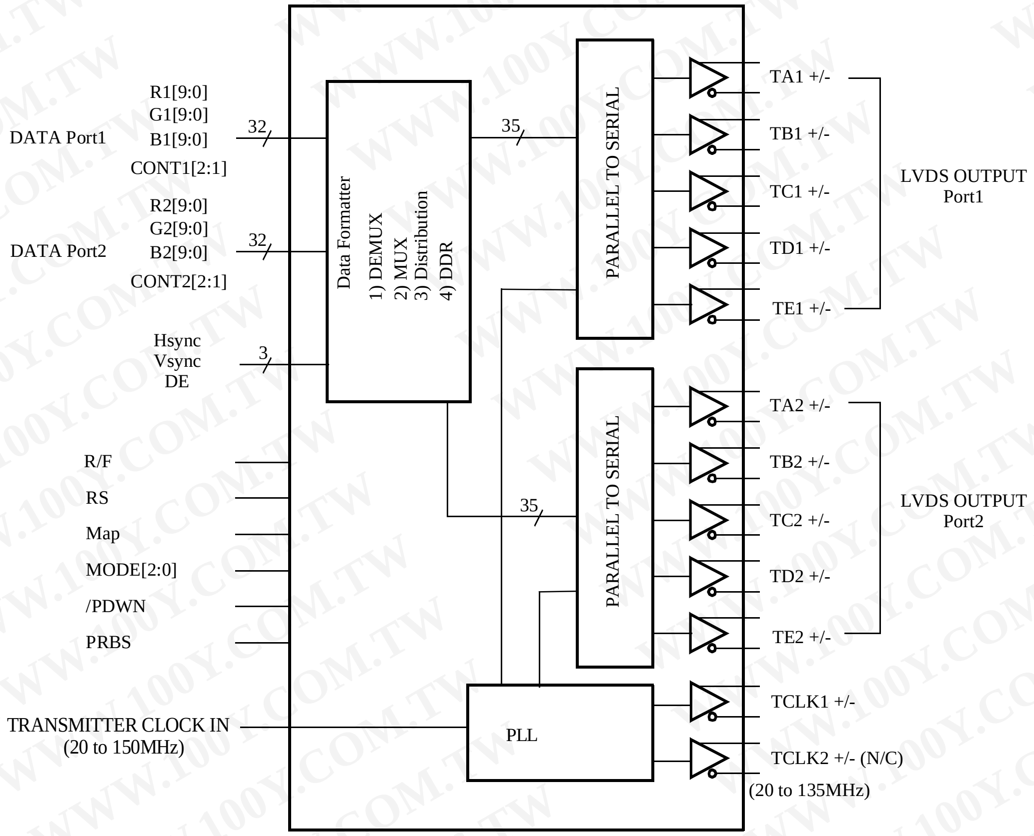
General Description

The THC63LVD1023 transmitter is designed to support Single Link transmission between Host and Flat Panel Display up to 1080p resolutions and Dual Link transmission between Host and Flat Panel Display up to QXGA resolutions.
The THC63LVD1023 converts 67its of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin, and support double edge inputs.
In Dual Link, the transmit clock frequency of 135MHz, 67bits of RGB data are transmitted at an effective rate of 945Mbps per LVDS channel. Using a 135MHz clock, the data throughput is 1.1Gbytes per second.

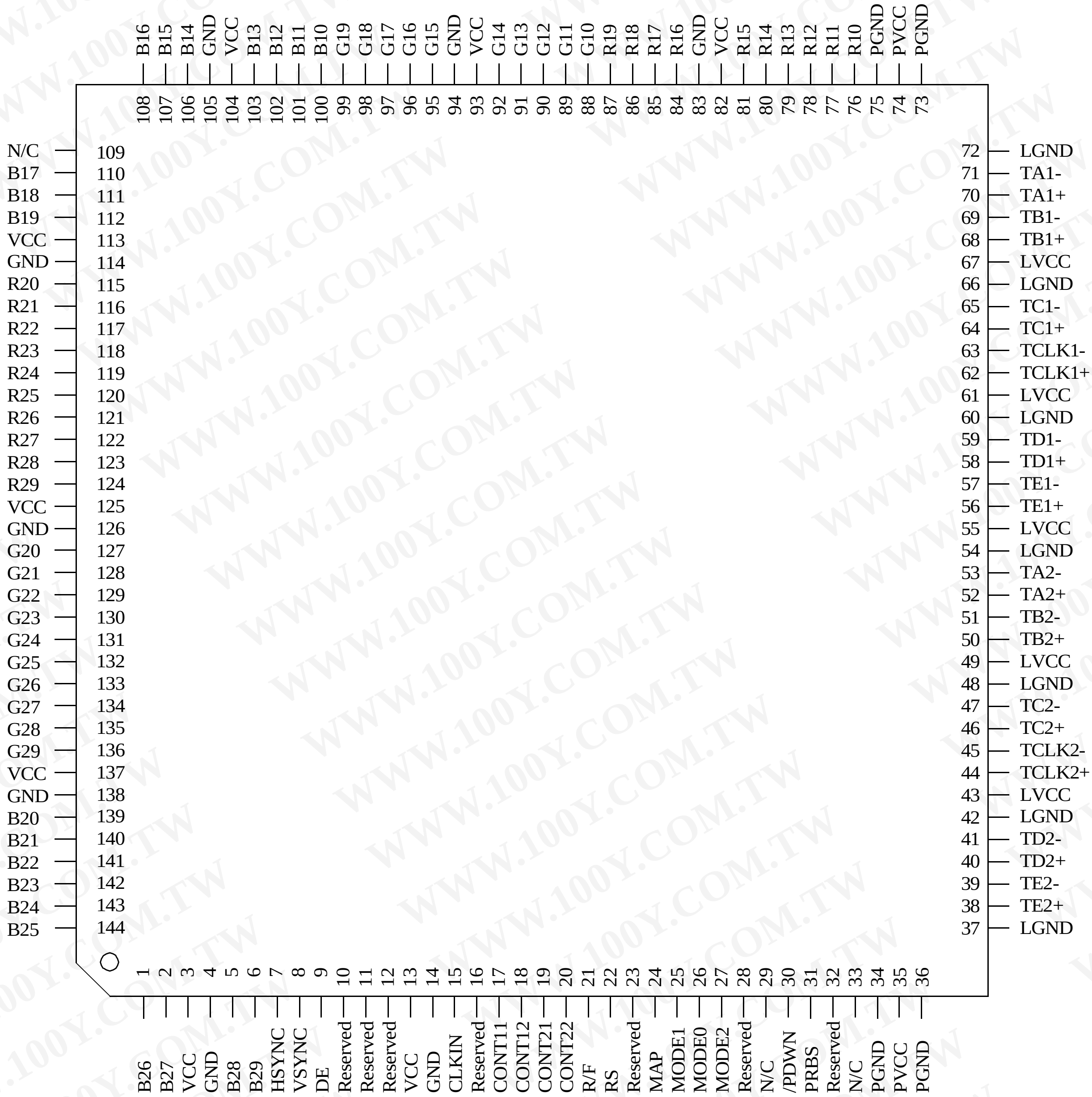
Features

- Wide dot clock range suited for TV Signal (480p-1080p), PC Signal (VGA-QXGA)
  Single TTL port IN/Dual LVDS port Out Mode:
  40 - 150MHz(CLK IN)
  Dual TTL port IN/Dual LVDS port Out Mode:
  20 - 135MHz(CLK IN)
- PLL requires No external components
- Flexible Input/Output mode
  1. Single/Dual TTL port IN-Single/Dual LVDS port OUT
  2. Double edge input
- Clock edge selectable
- 2 LVDS data mapping for simplifying PCB layout.
- Pseudo Random pattern generation circuit
- Supports Reduced swing LVDS for Low EMI
- Power down mode
- Low power single 3.3V CMOS design
- 144pin LQFP

Block Diagram



Pin Out


1 B26
2 B27
3 VCC
4 GND
5 B28
6 B29
7 HSYNC
8 VSYNC
9 DE
10 Reserved
11 Reserved
12 Reserved
13 VCC
14 GND
15 CLKIN
16 Reserved
17 CONT11
18 CONT12
19 CONT21
20 CONT22
21 R/F
22 RS
23 Reserved
24 MAP
25 MODE1
26 MODE0
27 MODE2
28 Reserved
29 N/C
30 /PDWN
31 PRBS
32 Reserved
33 N/C
34 PGND
35 PVCC
36 PGND
37 LGND
38 TE2+
39 TE2-
40 TD2+
41 TD2-
42 LGND
43 LVCC
44 TCLK2+
45 TCLK2-
46 TC2+
47 TC2-
48 LGND
49 LVCC
50 TB2+
51 TB2-
52 TA2+
53 TA2-
54 LGND
55 LVCC
56 TE1+
57 TE1-
58 TD1+
59 TD1-
60 LGND
61 LVCC
62 TCLK1+
63 TCLK1-
64 TC1+
65 TC1-
66 LGND
67 LVCC
68 TB1+
69 TB1-
70 TA1+
71 TA1-
72 LGND
73 PGND
74 PVCC
75 PGND
76 R10
77 R11
78 R12
79 R13
80 R14
81 R15
82 VCC
83 GND
84 R16
85 R17
86 R18
87 R19
88 G10
89 G11
90 G12
91 G13
92 G14
93 VCC
94 GND
95 G15
96 G16
97 G17
98 G18
99 G19
100 B10
101 B11
102 B12
103 B13
104 VCC
105 GND
106 B14
107 B15
108 B16
109 N/C
110 B17
111 B18
112 B19
113 VCC
114 GND
115 R20
116 R21
117 R22
118 R23
119 R24
120 R25
121 R26
122 R27
123 R28
124 R29
125 VCC
126 GND
127 G20
128 G21
129 G22
130 G23
131 G24
132 G25
133 G26
134 G27
135 G28
136 G29
137 VCC
138 GND
139 B20
140 B21
141 B22
142 B23
143 B24
144 B25

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>TA1+, TA1-</td><td>70, 71</td><td rowspan="5">LVDS OUT</td><td rowspan="5">The 1st Link.
The 1st pixel output data when Dual-Link.</td></tr>
<tr><td>TB1+, TB1-</td><td>68, 69</td></tr>
<tr><td>TC1+, TC1-</td><td>64, 65</td></tr>
<tr><td>TD1+, TD1-</td><td>58, 59</td></tr>
<tr><td>TE1+, TE1-</td><td>56, 57</td></tr>
<tr><td>TCLK1+, TCLK1-</td><td>62, 63</td><td>LVDS OUT</td><td>LVDS Clock Out for 1st and 2nd Link.</td></tr>
<tr><td>TA2+, TA2-</td><td>52, 53</td><td rowspan="5">LVDS OUT</td><td rowspan="5">The 2nd Link.
These pins are disabled when Single Link.</td></tr>
<tr><td>TB2+, TB2-</td><td>50, 51</td></tr>
<tr><td>TC2+, TC2-</td><td>46, 47</td></tr>
<tr><td>TD2+, TD2-</td><td>40, 41</td></tr>
<tr><td>TE2+, TE2-</td><td>38, 39</td></tr>
<tr><td>TCLK2+, TCLK2-</td><td>44, 45</td><td>LVDS OUT</td><td>Additional LVDS Clock Out. Identical to TCLK1+,-.
No connect if not used.</td></tr>
<tr><td>R19 ~ R10</td><td>87 - 84, 81 - 76</td><td rowspan="3">IN</td><td rowspan="3">The 1st Pixel Data Inputs.</td></tr>
<tr><td>G19 ~ G10</td><td>99 - 95, 92 - 88</td></tr>
<tr><td>B19 ~ B10</td><td>112 -110,
108 -106,
103 - 100</td></tr>
<tr><td>R29 ~ R20</td><td>124 - 115</td><td rowspan="3">IN</td><td rowspan="3">The 2nd Pixel Data Inputs.</td></tr>
<tr><td>G29 ~ G20</td><td>136 - 127</td></tr>
<tr><td>B29 ~ B20</td><td>6, 5, 2, 1,
144 - 139</td></tr>
<tr><td>CONT11,CONT12</td><td>17, 18</td><td rowspan="2">IN</td><td rowspan="2">CONTROL Data Inputs.</td></tr>
<tr><td>CONT21,CONT22</td><td>19, 20</td></tr>
<tr><td>DE</td><td>9</td><td>IN</td><td>Data Enable Input.</td></tr>
<tr><td>VSYNC</td><td>8</td><td>IN</td><td>Vsync Input.</td></tr>
<tr><td>HSYNC</td><td>7</td><td>IN</td><td>Hsync Input.</td></tr>
<tr><td>CLKIN</td><td>15</td><td>IN</td><td>Clock Input.</td></tr>
<tr><td>R/F</td><td>21</td><td>IN</td><td>Input Clock Triggering Edge Select.
H: Rising edge, L: Falling edge</td></tr>
<tr><td>RS</td><td>22</td><td>IN</td><td>The use of these multi-function depends on input voltage of RS pin.
<table>
<tr><th>Input Voltage of RS Pin</th><th>LVDS Output Swing Control</th><th>TTL/CMOS Input VIH/VIL Control for Small Swing Input</th></tr>
<tr><td>VCC</td><td rowspan="2">Normal Swing
VOD=350mV(typ)</td><td>V_{IH}/V_{IL} is fixed.</td></tr>
<tr><td>0.6 ~ 1.4V</td><td>Support Small Swing Input.
V_{IH}/V_{IL} depends on input voltage of RS pin.
See V_{IH}/V_{IL} Spec.</td></tr>
<tr><td>GND</td><td>Reduced Swing
VOD=200mV(typ)</td><td>V_{IH}/V_{IL} is fixed.</td></tr>
</table></td></tr>
</table>

Pin Description (Continued)

Pin Name	Pin #	Type	Description
MAP	24	IN	LVDS mapping table select. See Fig8 - 10 and Table4 - 8. H: Mapping Mode1 L: Mapping Mode2
MODE1, MODE0	25, 26	IN	Pixel Data Mode. MODE1 | MODE0 | Mode L | L | Dual Link (Dual-in/Dual-out) H | L | Dual Link (Single-in/Dual-out) L | H | Single Link (Dual-in/Single-out) H | H | Single Link (Single-in/Single-out)
MODE2	27	IN	Distribution, DDR function enable. The use of these multi-function depends on the setting of MODE<1:0>. MODE<1:0>=HH(Single-in/Single-out Mode) H: Distribution function enable. L: Distribution function disable. MODE<1:0>=HL(Single-in/Dingle-out Mode) H: DDR (Double Edge input) function enable. L: DDR (Double Edge input) function disable.
/PDWN	30	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
PRBS	31	IN	PRBS generator is active when MODE<1:0> = LL(Dual-in/Dual-out mode). H: PRBS generator is enable.Pattern is PRBS-23. L: Normal Operation
Reserved	10, 11, 12, 16, 28, 32	IN	Must be tied to GND.
Reserved	23	IN	Must be Open.
N/C	29, 33, 109		Must be Open.
VCC	3, 13, 82, 93, 104, 113, 125, 137	Power	Power Supply Pins for TTL inputs, output and digital circuitry.
GND	4, 14, 83, 94, 105, 114, 126, 138	Ground	Ground Pins for TTL inputs, outputs and digital circuitry.
LVCC	43, 49, 55, 61, 67	Power	Power Supply Pins for LVDS Outputs.
LGND	37, 42, 48, 54, 60, 66, 72	Ground	Ground Pins for LVDS Outputs.
PVCC	35, 74	Power	Power Supply for PLL circuitry.
PGND	34, 36, 73, 75	Ground	Ground Pin for PLL circuitry.

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Lead Temperature (Soldering, 4sec)	+260°C
Maximum Power Dissipation @+25°C	1.15W

Recommended Operating Conditions

Parameter				Min	Typ	Max	Units
All Supply Voltage				3.0	3.3	3.6	V
Operating Ambient Temperature				0		70	°C
CLK Frequency	MODE<1:0>=LL Dual-in/Dual-out		Input	20		135	MHz
			LVDS Output	20		135	MHz
	MODE<1:0>=LH Dual-in/Single-out		Input	10		67.5	MHz
			LVDS Output	20		135	MHz
	MODE<1:0>=HL Single-in/Dual-out	Single Edge Input (MODE2=L)	Input	40		150	MHz
			LVDS Output	20		75	MHz
		Double Edge Input (MODE2=H)	Input	20		135	MHz
			LVDS Output	20		135	MHz
	MODE<1:0>=HH Single-in/Single-out	Distribution Off (MODE2=L)	Input	20		135	MHz
			LVDS Output	20		135	MHz
		Distribution ON (MODE2=H)	Input	20		135	MHz
			LVDS Output	20		135	MHz

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage	RS = V_{CC} or GND	2.0		V_{CC}	V
		$0.6V < RS < 1.4V$	V_{REF}[a]+0.1			V
V_{IL}	Low Level Input Voltage	RS = V_{CC} or GND	GND		0.8	V
		$0.6V < RS < 1.4V$			V_{REF}-0.1	V
I_{INC}	Input Current	$0V \leq V_{IN} \leq V_{CC}$			±10	μA

a. V_{REF} is input voltage of RS pin.

LVDS Transmitter DC Specifications

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS= V_{CC}	250	350	450	mV
			Reduced swing RS= GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=0V, RL=100Ω				-24	mA
I_{OZ}	Output TRI-State current	/PDWN=0V, VOUT=0V to V_{CC}				±10	μA

Electrical Characteristics (Continued)

Supply Current

VCC

Symbol	Parameter	Condition			Typ.	Max.	Units
I_{TCCW}	Transmitter Supply Current (Worst Case Pattern) Fig1.	CLKIN=65MHz	RL=100Ω CL=5pF RS=V_{CC}	MODE<1:0>=HH Single-in/Single-out MODE2=L Distribution Off		67	mA
		CLKIN=85MHz				74	mA
		CLKIN=135MHz				92	mA
		CLKIN=65MHz		MODE<1:0>=HH Single-in/Single-out MODE2=H Distribution On		123	mA
		CLKIN=85MHz				137	mA
		CLKIN=135MHz				171	mA
		CLKIN=65MHz		MODE<1:0>=HL Single-in/Dual-out MODE2=L DDR Input Off		106	mA
		CLKIN=85MHz				115	mA
		CLKIN=135MHz				137	mA
		CLKIN=150MHz				145	mA
		CLKIN=65MHz		MODE<1:0>=HL Single-in/Dual-out MODE2=L DDR Input On		123	mA
		CLKIN=85MHz				138	mA
		CLKIN=135MHz				172	mA
		CLKIN=32.5MHz		MODE<1:0>=LH Dual-in/ Single-out		78	mA
		CLKIN=42.5MHz				88	mA
		CLKIN=67.5MHz				118	mA
		CLKIN=65MHz		MODE<1:0>=LL Dual-in/Dual-out		123	mA
		CLKIN=85MHz				136	mA
		CLKIN=135MHz				171	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L, All Inputs = Fixed L or H				10	μA

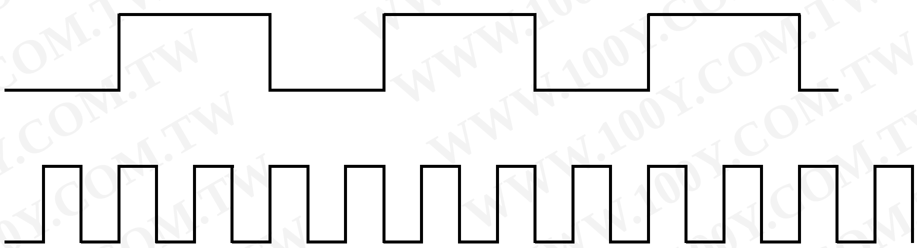


Fig1. Test Pattern
(LVDS Output Full Toggle Pattern)

Switching Characteristics

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{TCIT}	CLK IN Transition time (Fig2)	f= 75MHz			2.0	ns
		f= 150MHz			1.0	ns
t_{TCIP}	CLK IN Period(Fig5,6)		6.7		100	ns
t_{TCH}	CLK IN High Time(Fig5,6)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLK IN Low Time(Fig5,6)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLK IN(Fig5,6)		2.5			ns
t_{TH}	TTL Data Hold from CKL IN(Fig5,6)		0.0			ns
t_{TCD}	CLK IN to TCLK+/- Delay(Fig5,6) MODE<1:0>=LL Dual-in/Dual-out			$(3+3/7)t_{TCIP}$		ns
t_{TCOP}	CLK OUT Period(Fig7)		7.4		50	ns
t_{LVT}	LVDS Transition Time(Fig3)			0.6	1.5	ns
t_{TOP1}	Output Data Position0 (Fig7)	t_{TCOP} = 7.4ns	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (Fig7)		$\frac{t_{TCOP}}{7} - 0.15$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP6}	Output Data Position2 (Fig7)		$2\frac{t_{TCOP}}{7} - 0.15$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP5}	Output Data Position3 (Fig7)		$3\frac{t_{TCOP}}{7} - 0.15$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP4}	Output Data Position4 (Fig7)		$4\frac{t_{TCOP}}{7} - 0.15$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP3}	Output Data Position5 (Fig7)		$5\frac{t_{TCOP}}{7} - 0.15$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP2}	Output Data Position6 (Fig7)		$6\frac{t_{TCOP}}{7} - 0.15$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TPLL}	Phase Lock Loop Set(Fig4)				10.0	ms

AC Timing Diagrams

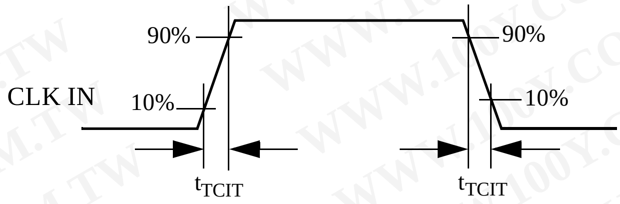


Fig2. CLKIN Transition Time

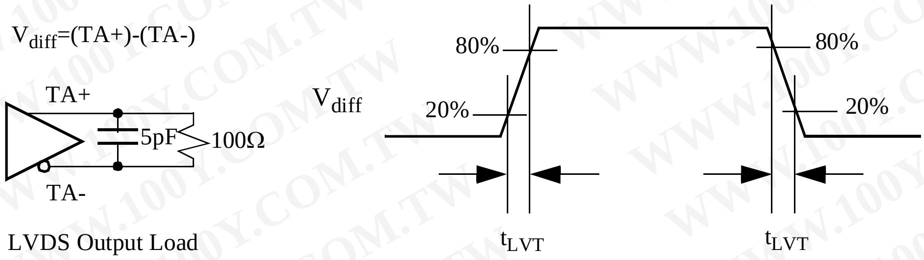


Fig3. LVDS Output Load and Transition Time

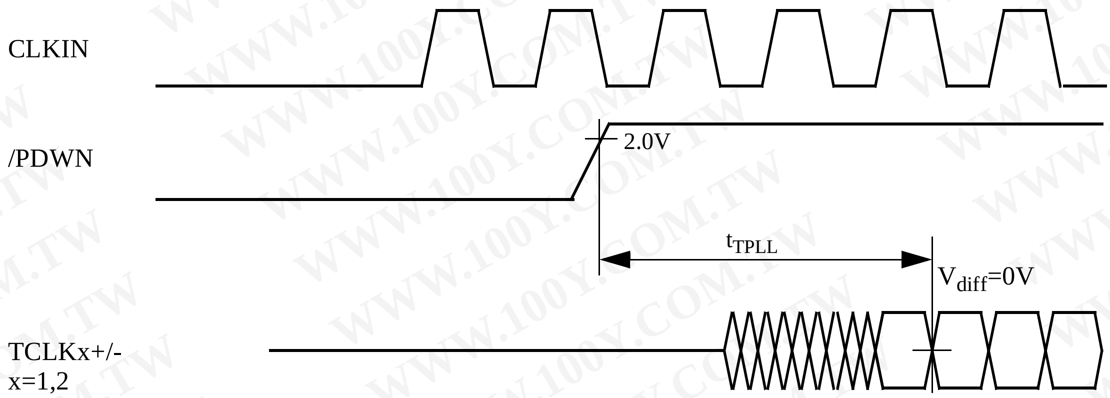
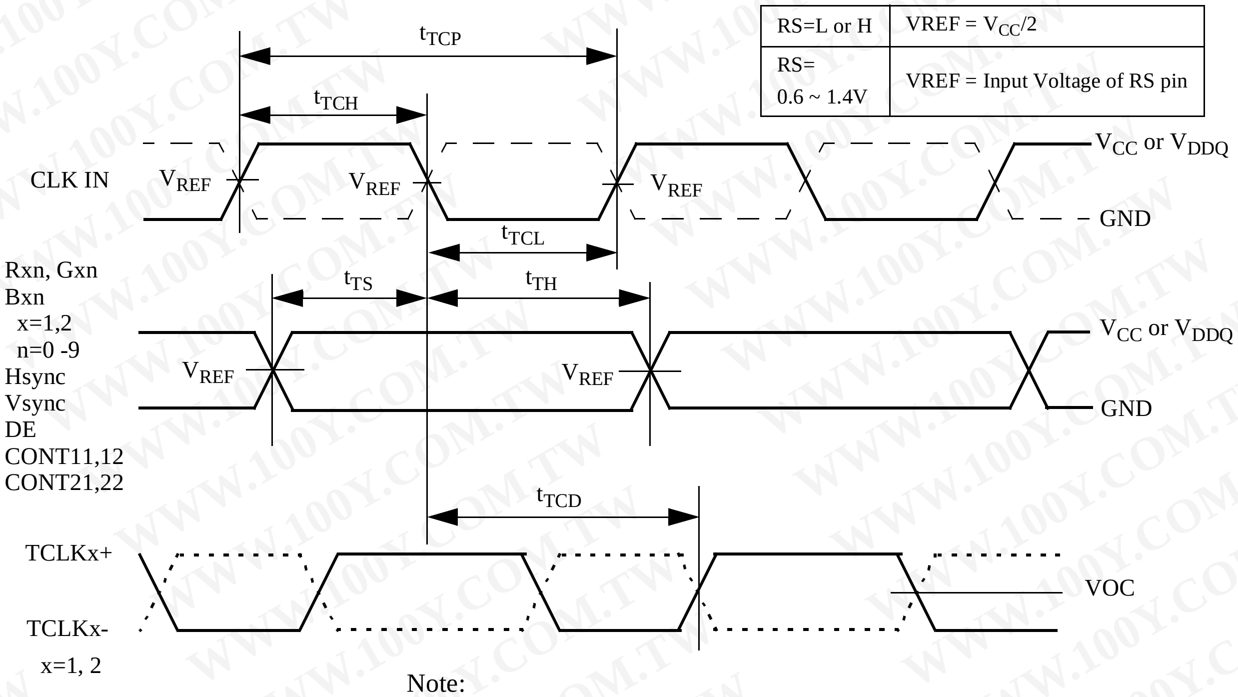


Fig4. PLL Lock Loop Set Time

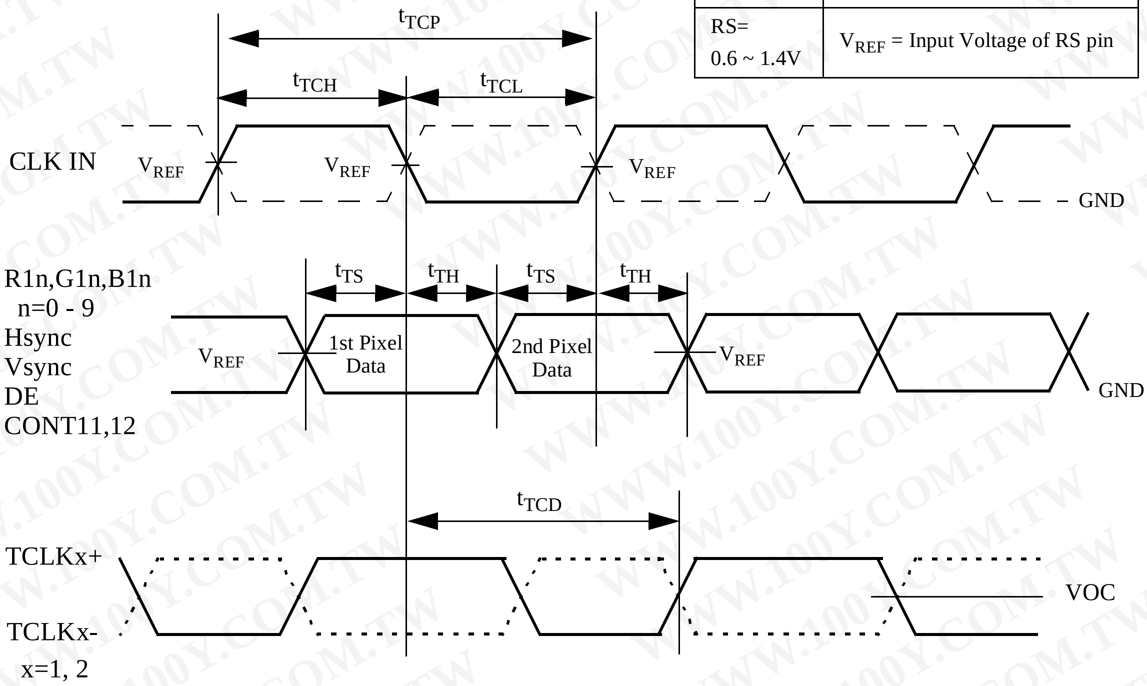
RS=L or H	$VREF = V_{CC}/2$
RS= 0.6 ~ 1.4V	VREF = Input Voltage of RS pin



Note:
CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line

Fig5. CLKIN Period, High/Low Time, Setup/Hold Timing

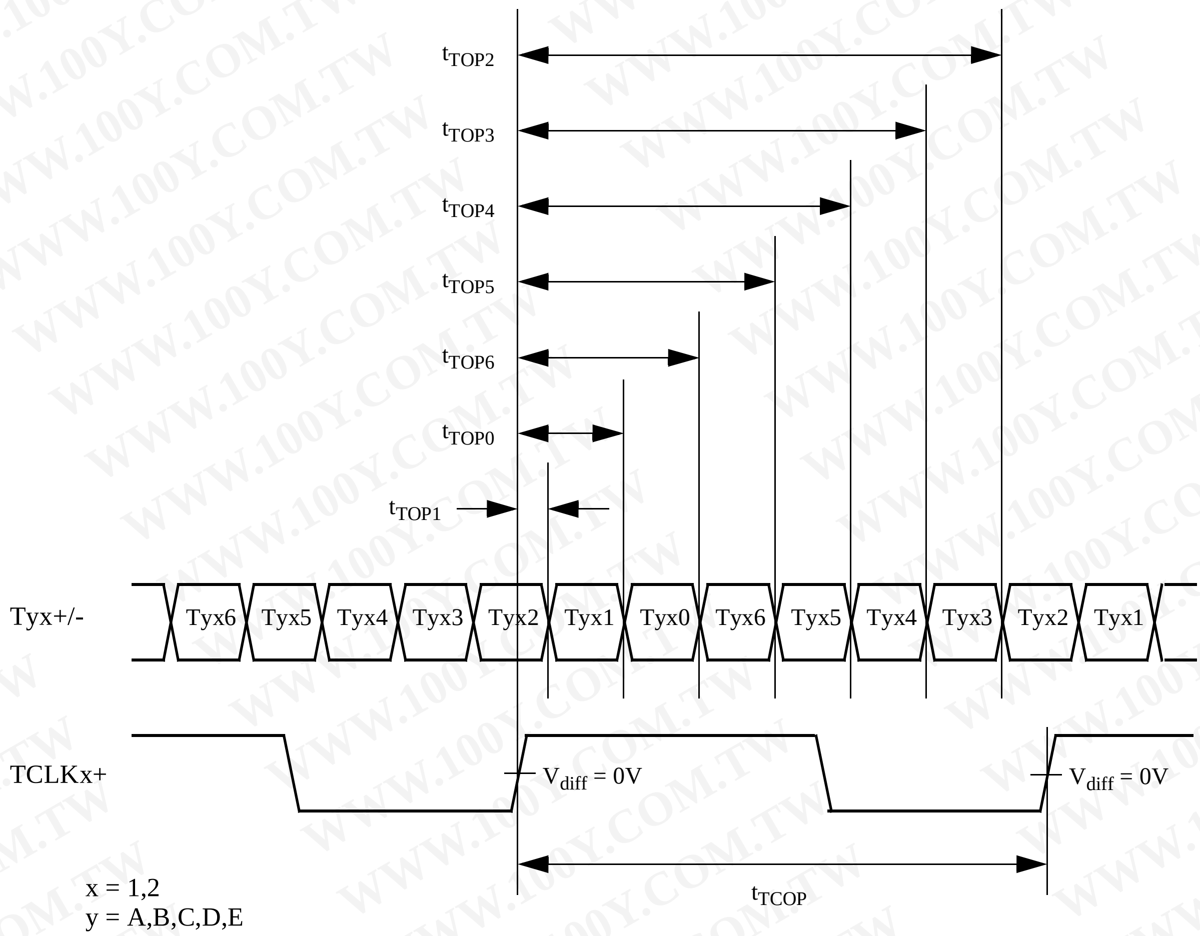
RS=L or H	$V_{REF} = V_{CC}/2$
RS= 0.6 ~ 1.4V	V_{REF} = Input Voltage of RS pin



Note:
CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line

Fig6. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode
MODE<1:0>=HL, MODE2=H

AC Timing Diagrams (Continued)



Note:
V_{diff} = (Tyx+) - (Tyx-) , (TCLKx+) - (TCLKx-)

Fig7. LVDS Output Data Position

Input Data Mapping

•Table1. Input Color Data naming rule

X	Y	Z	Description	
X=R			Red Color Data	
X=G			Green Color Data	
X=B			Blue Color Data	
	Y= None		Single Pixel	
	Y=E		Dual Pixel	1st Pixel Data
	Y=O			2nd Pixel Data
		Z=0-9	Bit number 0: LSB (Least Significant Bit) 9: MSB (Most Significant Bit)	

•Table2. TTL/CMOS Input Data Mapping (Single-in mode, MODE1=H)

Data Signals			Transmitter Input Pin Names		
30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
R0			R10		
R1			R11		
R2	R0		R12	R12	
R3	R1		R13	R13	
R4	R2	R0	R14	R14	R14
R5	R3	R1	R15	R15	R15
R6	R4	R2	R16	R16	R16
R7	R5	R3	R17	R17	R17
R8	R6	R4	R18	R18	R18
R9	R7	R5	R19	R19	R19
G0			G10		
G1			G11		
G2	G0		G12	G12	
G3	G1		G13	G13	
G4	G2	G0	G14	G14	G14
G5	G3	G1	G15	G15	G15
G6	G4	G2	G16	G16	G16
G7	G5	G3	G17	G17	G17
G8	G6	G4	G18	G18	G18
G9	G7	G5	G19	G19	G19
B0			B10		
B1			B11		
B2	B0		B12	B12	
B3	B1		B13	B13	
B4	B2	B0	B14	B14	B12
B5	B3	B1	B15	B15	B13
B6	B4	B2	B16	B16	B14
B7	B5	B3	B17	B17	B15
B8	B6	B4	B18	B18	B16
B9	B7	B5	B19	B19	B17

Input Data Mapping (Continued)

•Table3. TTL/CMOS Input Data Mapping (Dual-in mode, MODE1=L)

1st Pixel Data						2nd Pixel Data					
Data Signals			Transmitter Input Pin Names			Data Signals			Transmitter Input Pin Names		
30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
RE0			R10			RO0			R20		
RE1			R11			RO1			R22		
RE2	RE0		R12	R12		RO2	RO0		R22	R22	
RE3	RE1		R13	R13		RO3	RO1		R23	R23	
RE4	RE2	RE0	R14	R14	R14	RO4	RO2	RO0	R24	R24	R24
RE5	RE3	RE1	R15	R15	R15	RO5	RO3	RO1	R25	R25	R25
RE6	RE4	RE2	R16	R16	R16	RO6	RO4	RO2	R26	R26	R26
RE7	RE5	RE3	R17	R17	R17	RO7	RO5	RO3	R27	R27	R27
RE8	RE6	RE4	R18	R18	R18	RO8	RO6	RO4	R28	R28	R28
RE9	RE7	RE5	R19	R19	R19	RO9	RO7	RO5	R29	R29	R29
GE0			G10			GO0			G20		
GE1			G11			GO1			G22		
GE2	GE0		G12	G12		GO2	GO0		G22	G22	
GE3	GE1		G13	G13		GO3	GO1		G23	G23	
GE4	GE2	GE0	G14	G14	G14	GO4	GO2	GO0	G24	G24	G24
GE5	GE3	GE1	G15	G15	G15	GO5	GO3	GO1	G25	G25	G25
GE6	GE4	GE2	G16	G16	G16	GO6	GO4	GO2	G26	G26	G26
GE7	GE5	GE3	G17	G17	G17	GO7	GO5	GO3	G27	G27	G27
GE8	GE6	GE4	G18	G18	G18	GO8	GO6	GO4	G28	G28	G28
GE9	GE7	GE5	G19	G19	G19	GO9	GO7	GO5	G29	G29	G29
BE0			B10			BO0			B20		
BE1			B11			BO1			B22		
BE2	BE0		B12	B12		BO2	BO0		B22	B22	
BE3	BE1		B13	B13		BO3	BO1		B23	B23	
BE4	BE2	BE0	B14	B14	B14	BO4	BO2	BO0	B24	B24	B24
BE5	BE3	BE1	B15	B15	B15	BO5	BO3	BO1	B25	B25	B25
BE6	BE4	BE2	B16	B16	B16	BO6	BO4	BO2	B26	B26	B26
BE7	BE5	BE3	B17	B17	B17	BO7	BO5	BO3	B27	B27	B27
BE8	BE6	BE4	B18	B18	B18	BO8	BO6	BO4	B28	B28	B28
BE9	BE7	BE5	B19	B19	B19	BO9	BO7	BO5	B29	B29	B29

LVDS Output Data Mapping

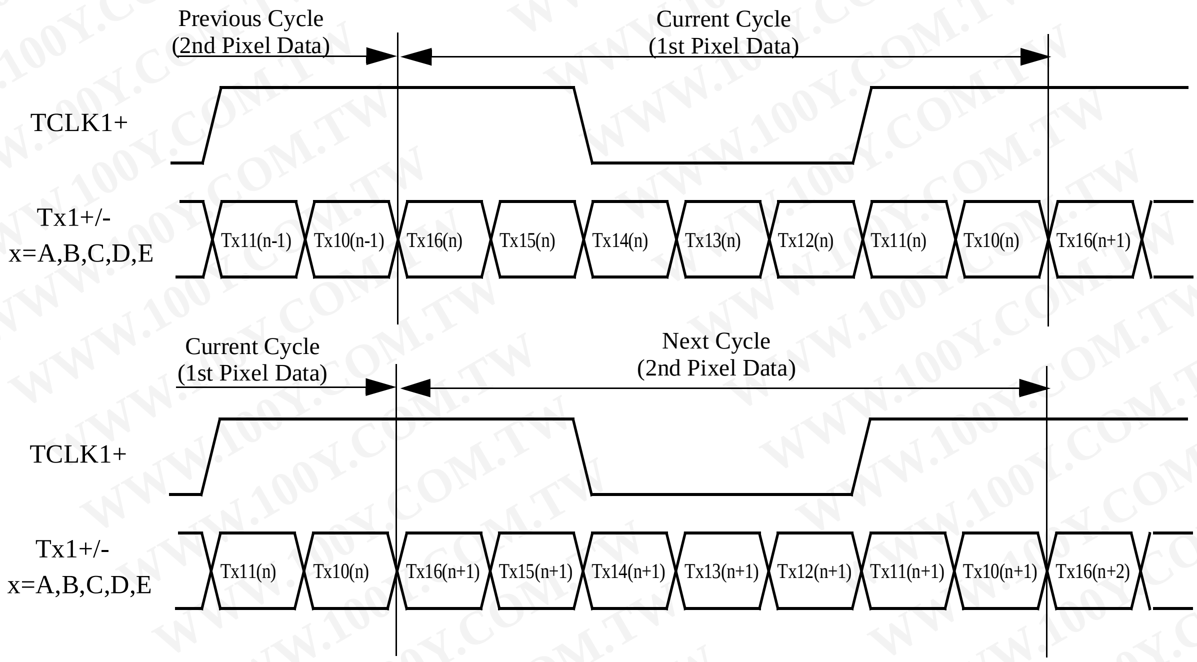


Fig8. TTL Data Inputs Mapped to LVDS outputs
MODE0= H (Single-out Mode)

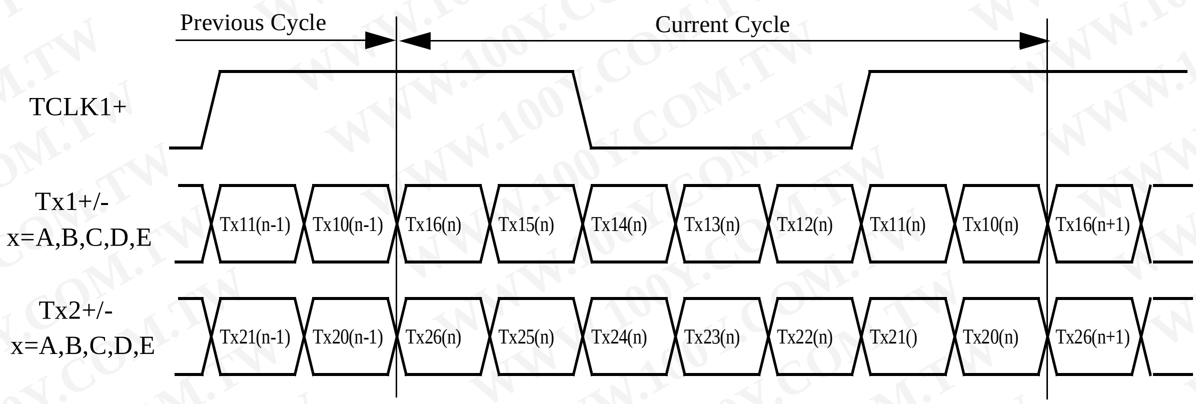


Fig9. TTL Data Inputs Mapped to LVDS outputs
MODE0= L (Dual-out Mode)

LVDS Output Data Mapping (Continued)

•Table4. LVDS Output Data Mapping (Single-in/Single-out Distribution Off, MODE<1:0>=HH, MODE2=L)

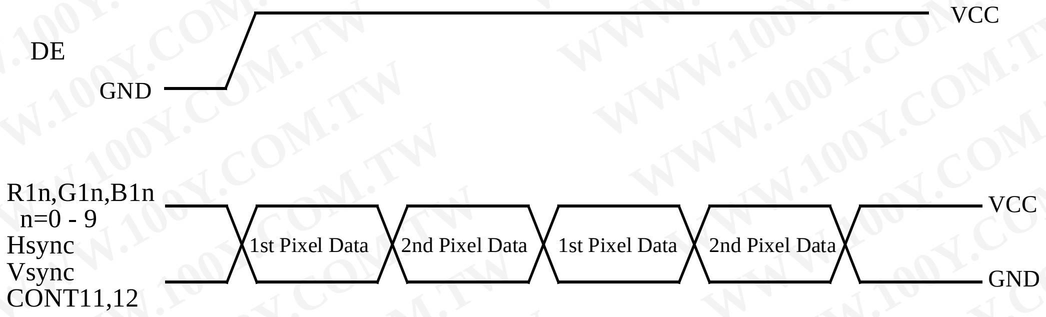
LVDS Output Data	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)
TA10	R14	R12
TA11	R15	R13
TA12	R16	R14
TA13	R17	R15
TA14	R18	R16
TA15	R19	R17
TA16	G14	G12
TB10	G15	G13
TB11	G16	G14
TB12	G17	G15
TB13	G18	G16
TB14	G19	G17
TB15	B14	B12
TB16	B15	B13
TC10	B16	B14
TC11	B17	B15
TC12	B18	B16
TC13	B19	B17
TC14	HSYNC	HSYNC
TC15	VSYNC	VSYNC
TC16	DE	DE
TD10	R12	R18
TD11	R13	R19
TD12	G12	G18
TD13	G13	G19
TD14	B12	B18
TD15	B13	B19
TD16	CONT11	CONT11
TE10	R10	R10
TE11	R11	R11
TE12	G10	G10
TE13	G11	G11
TE14	B10	B10
TE15	B11	B11
TE16	CONT12	CONT12

LVDS Output Data Mapping (Continued)

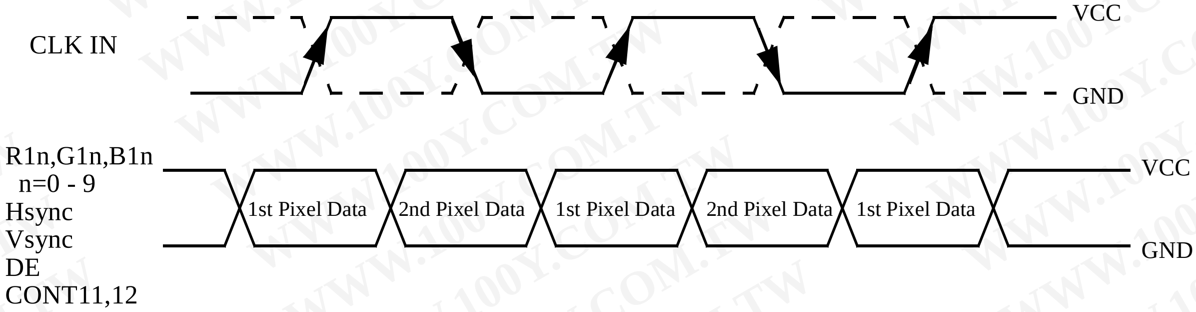
•Table5. LVDS Output Data Mapping (Single-in/Single-out Distribution On, MODE<1:0>=HH, MODE2=H)

1st Link			2nd Link		
LVDS Output Data (1st Link)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)	LVDS Output Data (2nd Link)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)
TA10	R14	R12	TA20	R14	R12
TA11	R15	R13	TA21	R15	R13
TA12	R16	R14	TA22	R16	R14
TA13	R17	R15	TA23	R17	R15
TA14	R18	R16	TA24	R18	R16
TA15	R19	R17	TA25	R19	R17
TA16	G14	G12	TA26	G14	G12
TB10	G15	G13	TB20	G15	G13
TB11	G16	G14	TB21	G16	G14
TB12	G17	G15	TB22	G17	G15
TB13	G18	G16	TB23	G18	G16
TB14	G19	G17	TB24	G19	G17
TB15	B14	B12	TB25	B14	B12
TB16	B15	B13	TB26	B15	B13
TC10	B16	B14	TC20	B16	B14
TC11	B17	B15	TC21	B17	B15
TC12	B18	B16	TC22	B18	B16
TC13	B19	B17	TC23	B19	B17
TC14	HSYNC	HSYNC	TC24	HSYNC	HSYNC
TC15	VSYNC	VSYNC	TC25	VSYNC	VSYNC
TC16	DE	DE	TC26	DE	DE
TD10	R12	R18	TD20	R12	R18
TD11	R13	R19	TD21	R13	R19
TD12	G12	G18	TD22	G12	G18
TD13	G13	G19	TD23	G13	G19
TD14	B12	B18	TD24	B12	B18
TD15	B13	B19	TD25	B13	B19
TD16	CONT11	CONT11	TD26	CONT11	CONT11
TE10	R10	R10	TE20	R10	R10
TE11	R11	R11	TE21	R11	R11
TE12	G10	G10	TE22	G10	G10
TE13	G11	G11	TE23	G11	G11
TE14	B10	B10	TE24	B10	B10
TE15	B11	B11	TE25	B11	B11
TE16	CONT12	CONT12	TE26	CONT12	CONT12

LVDS Output Data Mapping (Continued)



a) MODE2=L(Single Edge Input)



b) MODE2=H(Double Edge Input)

Note:

CLK IN: for R/F=VCC, denote as solid line,

for R/F=GND, denote as dashed line

Fig8. The decision rule of 1st Pixel data in Single IN/Dual Out (MODE<1:0>=HL)

LVDS Output Data Mapping (Continued)

•Table6. LVDS Output Data Mapping (Single-in/Dual-out DDR On or Off, MODE<1:0>=HL, MODE2=H or L)

1st Pixel Data			2nd Pixel Data		
LVDS Output Data (1st Pixel Data)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)	LVDS Output Data (1st Pixel Data)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)
TA10	R14	R12	TA20	R14	R12
TA11	R15	R13	TA21	R15	R13
TA12	R16	R14	TA22	R16	R14
TA13	R17	R15	TA23	R17	R15
TA14	R18	R16	TA24	R18	R16
TA15	R19	R17	TA25	R19	R17
TA16	G14	G12	TA26	G14	G12
TB10	G15	G13	TB20	G15	G13
TB11	G16	G14	TB21	G16	G14
TB12	G17	G15	TB22	G17	G15
TB13	G18	G16	TB23	G18	G16
TB14	G19	G17	TB24	G19	G17
TB15	B14	B12	TB25	B14	B12
TB16	B15	B13	TB26	B15	B13
TC10	B16	B14	TC20	B16	B14
TC11	B17	B15	TC21	B17	B15
TC12	B18	B16	TC22	B18	B16
TC13	B19	B17	TC23	B19	B17
TC14	HSYNC	HSYNC	TC24	HSYNC	HSYNC
TC15	VSYNC	VSYNC	TC25	VSYNC	VSYNC
TC16	DE	DE	TC26	DE	DE
TD10	R12	R18	TD20	R12	R18
TD11	R13	R19	TD21	R13	R19
TD12	G12	G18	TD22	G12	G18
TD13	G13	G19	TD23	G13	G19
TD14	B12	B18	TD24	B12	B18
TD15	B13	B19	TD25	B13	B19
TD16	CONT11	CONT11	TD26	CONT11	CONT11
TE10	R10	R10	TE20	R10	R10
TE11	R11	R11	TE21	R11	R11
TE12	G10	G10	TE22	G10	G10
TE13	G11	G11	TE23	G11	G11
TE14	B10	B10	TE24	B10	B10
TE15	B11	B11	TE25	B11	B11
TE16	CONT12	CONT12	TE26	CONT12	CONT12

LVDS Output Data Mapping (Continued)

•Table7. LVDS Output Data Mapping (Dual-in/Single-out, MODE<1:0>=LH)

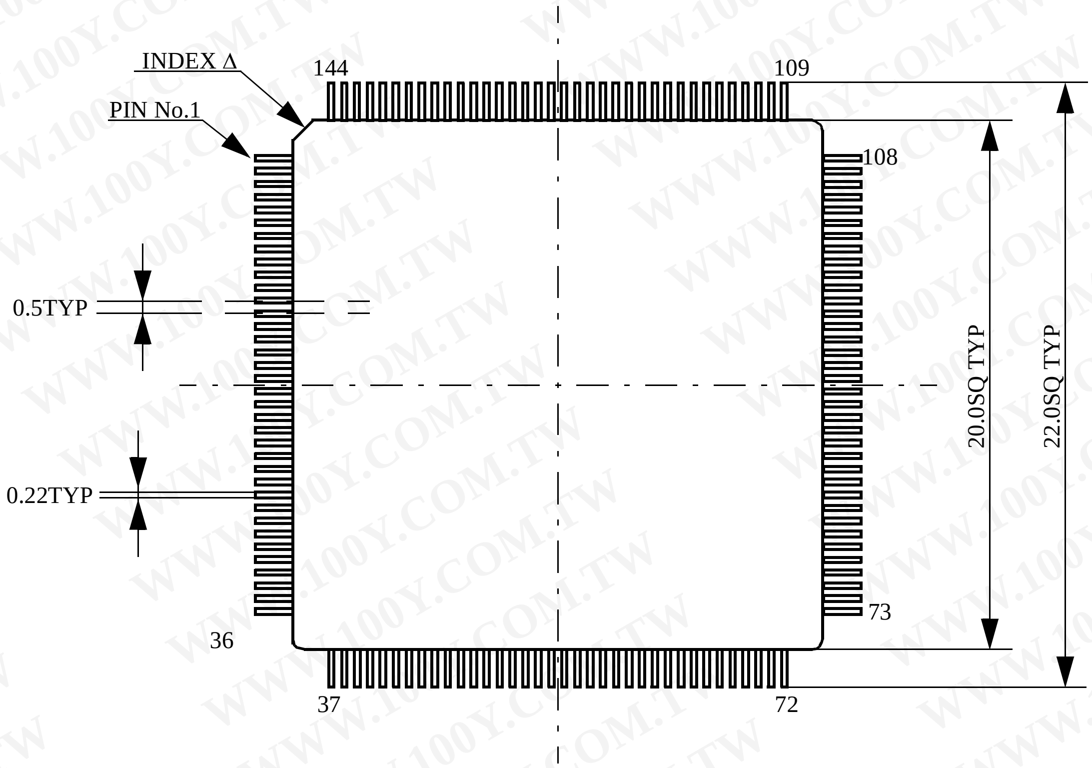
1st Pixel Data			2nd Pixel Data		
LVDS Output Data (1st Pixel Data)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)	LVDS Output Data (2nd Pixel Data)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)
TA10(n)	R14	R12	TA10(n+1)	R24	R22
TA11(n)	R15	R13	TA11(n+1)	R25	R23
TA12(n)	R16	R14	TA12(n+1)	R26	R24
TA13(n)	R17	R15	TA13(n+1)	R27	R25
TA14(n)	R18	R16	TA14(n+1)	R28	R26
TA15(n)	R19	R17	TA15(n+1)	R29	R27
TA16(n)	G14	G12	TA16(n+1)	G24	G22
TB10(n)	G15	G13	TB10(n+1)	G25	G23
TB11(n)	G16	G14	TB11(n+1)	G26	G24
TB12(n)	G17	G15	TB12(n+1)	G27	G25
TB13(n)	G18	G16	TB13(n+1)	G28	G26
TB14(n)	G19	G17	TB14(n+1)	G29	G27
TB15(n)	B14	B12	TB15(n+1)	B24	B22
TB16(n)	B15	B13	TB16(n+1)	B25	B23
TC10(n)	B16	B14	TC10(n+1)	B26	B24
TC11(n)	B17	B15	TC11(n+1)	B27	B25
TC12(n)	B18	B16	TC12(n+1)	B28	B26
TC13(n)	B19	B17	TC13(n+1)	B29	B27
TC14(n)	HSYNC	HSYNC	TC14(n+1)	HSYNC	HSYNC
TC15(n)	VSYNC	VSYNC	TC15(n+1)	VSYNC	VSYNC
TC16(n)	DE	DE	TC16(n+1)	DE	DE
TD10(n)	R12	R18	TD10(n+1)	R22	R28
TD11(n)	R13	R19	TD11(n+1)	R23	R29
TD12(n)	G12	G18	TD12(n+1)	G22	G28
TD13(n)	G13	G19	TD13(n+1)	G23	G29
TD14(n)	B12	B18	TD14(n+1)	B22	B28
TD15(n)	B13	B19	TD15(n+1)	B23	B29
TD16(n)	CONT11	CONT11	TD16(n+1)	CONT21	CONT21
TE10(n)	R10	R10	TE10(n+1)	R20	R20
TE11(n)	R11	R11	TE11(n+1)	R21	R21
TE12(n)	G10	G10	TE12(n+1)	G20	G20
TE13(n)	G11	G11	TE13(n+1)	G21	G21
TE14(n)	B10	B10	TE14(n+1)	B20	B20
TE15(n)	B11	B11	TE15(n+1)	B21	B21
TE16(n)	CONT12	CONT12	TE16(n+1)	CONT22	CONT22

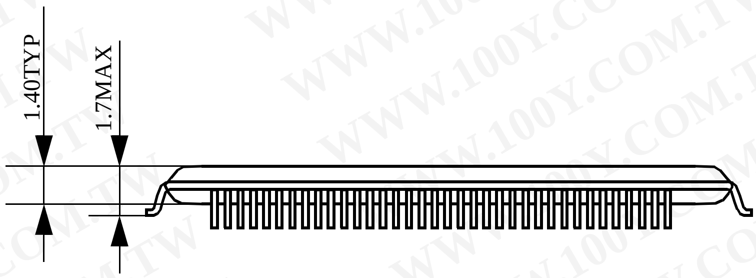
LVDS Output Data Mapping (Continued)

•Table8. LVDS Output Data Mapping (Dual-in/Dual-out, MODE<1:0>=LL)

1st Pixel Data			2nd Pixel Data		
LVDS Output Data (1st Pixel Data)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)	LVDS Output Data (2nd Pixel Data)	Mapping Mode1 (Input Pin Name)	Mapping Mode2 (Input Pin Name)
TA10	R14	R12	TA20	R24	R22
TA11	R15	R13	TA21	R25	R23
TA12	R16	R14	TA22	R26	R24
TA13	R17	R15	TA23	R27	R25
TA14	R18	R16	TA24	R28	R26
TA15	R19	R17	TA25	R29	R27
TA16	G14	G12	TA26	G24	G22
TB10	G15	G13	TB20	G25	G23
TB11	G16	G14	TB21	G26	G24
TB12	G17	G15	TB22	G27	G25
TB13	G18	G16	TB23	G28	G26
TB14	G19	G17	TB24	G29	G27
TB15	B14	B12	TB25	B24	B22
TB16	B15	B13	TB26	B25	B23
TC10	B16	B14	TC20	B26	B24
TC11	B17	B15	TC21	B27	B25
TC12	B18	B16	TC22	B28	B26
TC13	B19	B17	TC23	B29	B27
TC14	HSYNC	HSYNC	TC24	HSYNC	HSYNC
TC15	VSYNC	VSYNC	TC25	VSYNC	VSYNC
TC16	DE	DE	TC26	DE	DE
TD10	R12	R18	TD20	R22	R28
TD11	R13	R19	TD21	R23	R29
TD12	G12	G18	TD22	G22	G28
TD13	G13	G19	TD23	G23	G29
TD14	B12	B18	TD24	B22	B28
TD15	B13	B19	TD25	B23	B29
TD16	CONT11	CONT11	TD26	CONT21	CONT21
TE10	R10	R10	TE20	R20	R20
TE11	R11	R11	TE21	R21	R21
TE12	G10	G10	TE22	G20	G20
TE13	G11	G11	TE23	G21	G21
TE14	B10	B10	TE24	B20	B20
TE15	B11	B11	TE25	B21	B21
TE16	CONT12	CONT12	TE26	CONT22	CONT22

Package





UNIT:mm

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