PRELIMINARY

# THC63LVDM83A/THC63LVDF84A

## 85MHz LVDS 24 Bit COLOR HOST-LCD PANEL INTERFACE



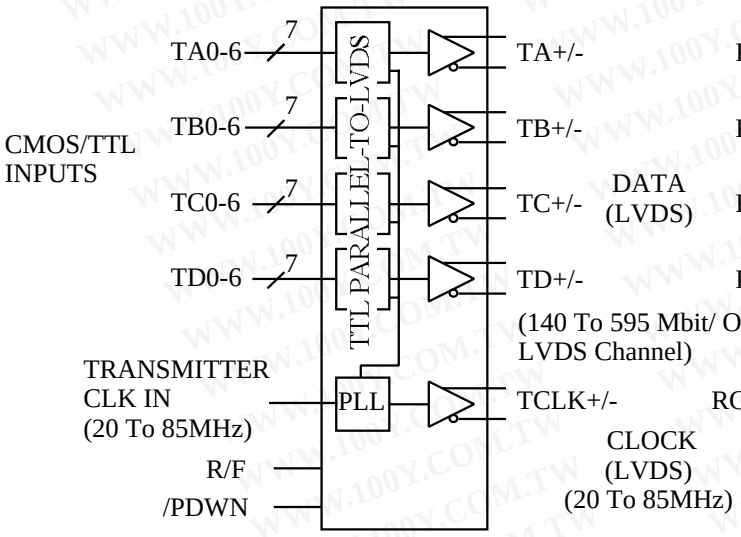
## General Description

The THC63LVDM83A transmitter converts 28 bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. The THC63LVDM83A can be programmed for rising edge or falling edge clocks through a dedicated pin.
The THC63LVDF84A receiver convert the LVDS data streams back into 28 bits of CMOS/TTL data with falling edge clock.
At a transmit clock frequency of 85MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at a rate of 595 Mbps per LVDS data channel.

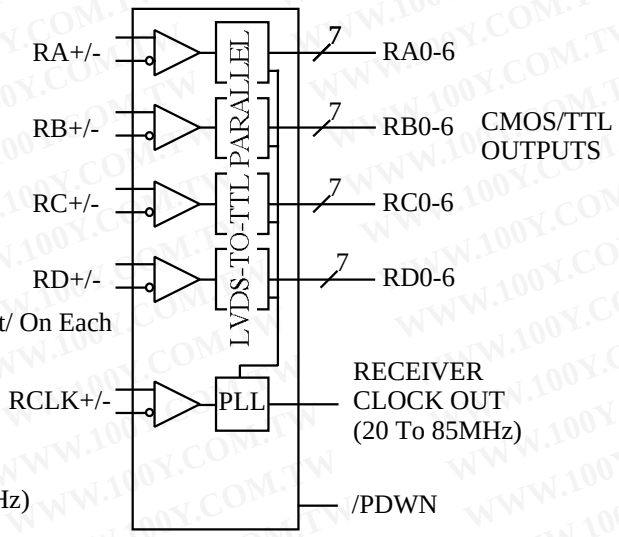
## Features

- 28:4 Data channel compression at up to 298 Megabytes per sec throughput
- Wide Frequency Range: 20 - 85MHz suited for VGA,SVGA,XGA and SXGA
- Narrow bus (10 lines) reduces cable size
- 345mV swing LVDS devices for Low EMI
- Supports Spread Spectrum Clock Generator
- On chip Input Jitter Filtering
- PLL requires No External Components
- Single 3.3V supply with 125mW(TYP)
- Low Power CMOS Design
- Power-Down Mode
- Low profile 56 Lead TSSOP Package
- Clock Edge Programmable for Transmitter
- Improved Replacement for the National DS90C383/384

### THC63LVDM83A




### THC63LVDF84A




### OPTIONS

| CLOCK TRIGGERING | TRANSMITTER DEVICE | RECEIVER DEVICE |
|---|---|---|
| Falling Edge | **THC63LVDM83A(R/F pin=GND)** | **THC63LVDF84A** |
| Rising Edge | **THC63LVDM83A(R/F pin=Vcc)** | **----** |

# PIN OUT

## TRANSMITTER DEVICE

### THC63LVDM83A

| | | | |
|---|---|---|---|
| VCC | 1 | 56 | TA4 |
| TD1 | 2 | 55 | TA3 |
| TA5 | 3 | 54 | TA2 |
| TA6 | 4 | 53 | GND |
| GND | 5 | 52 | TA1 |
| TB0 | 6 | 51 | TA0 |
| TB1 | 7 | 50 | TD0 |
| TD2 | 8 | 49 | LVDS GND |
| VCC | 9 | 48 | TA- |
| TD3 | 10 | 47 | TA+ |
| TB2 | 11 | 46 | TB- |
| TB3 | 12 | 45 | TB+ |
| GND | 13 | 44 | LVDS VCC |
| TB4 | 14 | 43 | LVDS GND |
| TB5 | 15 | 42 | TC- |
| TD4 | 16 | 41 | TC+ |
| R/F | 17 | 40 | TCLK- |
| TD5 | 18 | 39 | TCLK+ |
| TB6 | 19 | 38 | TD- |
| TC0 | 20 | 37 | TD+ |
| GND | 21 | 36 | LVDS GND |
| TC1 | 22 | 35 | PLL GND |
| TC2 | 23 | 34 | PLL VCC |
| TC3 | 24 | 33 | PLL GND |
| TD6 | 25 | 32 | /PDWN |
| VCC | 26 | 31 | CLK IN |
| TC4 | 27 | 30 | TC6 |
| TC5 | 28 | 29 | GND |

## RECEIVER DEVICE

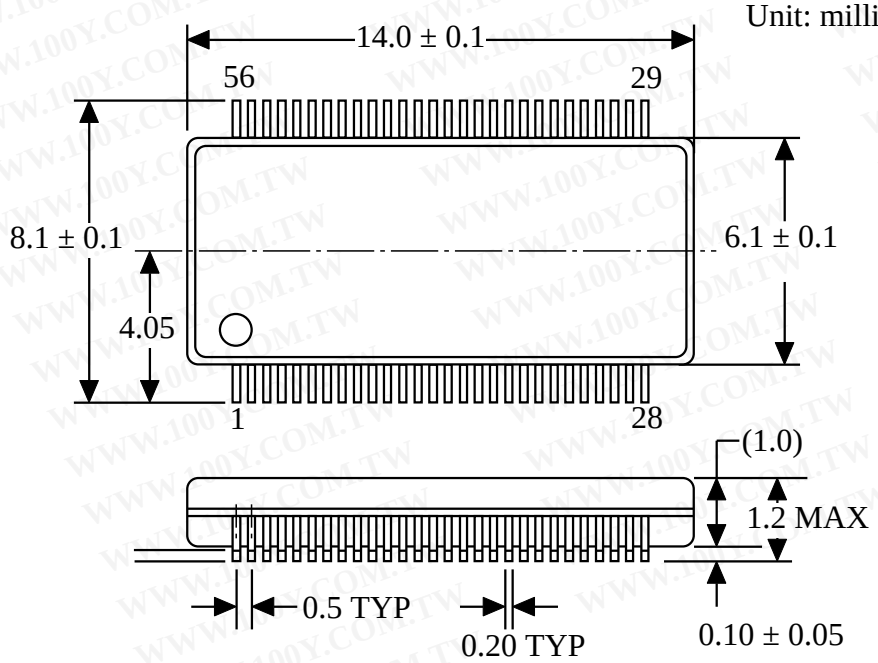
### THC63LVDF84A

| | | | |
|---|---|---|---|
| RC3 | 1 | 56 | VCC |
| RD6 | 2 | 55 | RC2 |
| RC4 | 3 | 54 | RC1 |
| GND | 4 | 53 | RC0 |
| RC5 | 5 | 52 | GND |
| RC6 | 6 | 51 | RB6 |
| RD0 | 7 | 50 | RD5 |
| LVDS GND | 8 | 49 | RD4 |
| RA- | 9 | 48 | VCC |
| RA+ | 10 | 47 | RB5 |
| RB- | 11 | 46 | RB4 |
| RB+ | 12 | 45 | RB3 |
| LVDS VCC | 13 | 44 | GND |
| LVDS GND | 14 | 43 | RB2 |
| RC- | 15 | 42 | RD3 |
| RC+ | 16 | 41 | RD2 |
| RCLK- | 17 | 40 | VCC |
| RCLK+ | 18 | 39 | RB1 |
| RD- | 19 | 38 | RB0 |
| RD+ | 20 | 37 | RA6 |
| LVDS GND | 21 | 36 | GND |
| PLL GND | 22 | 35 | RA5 |
| PLL VCC | 23 | 34 | RD1 |
| PLL GND | 24 | 33 | RA4 |
| /PDWN | 25 | 32 | RA3 |
| CLKOUT | 26 | 31 | VCC |
| RA0 | 27 | 30 | RA2 |
| GND | 28 | 29 | RA1 |

# PACKAGE

**56 Lead Molded Thin Shrink Small Outline Package, JEDEC**

Unit: millimeters



# Electrical Characteristics

Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CMOS/TTL DC SPECIFICATIONS** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | Vcc | V |
| $V_{IL}$ | Low Level Input Voltage | | GND | | 0.8 | V |
| $V_{OH}$ | High Level output Voltage | $I_{OH}$=-4mA | 2.4 | | | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$=4mA | | | 0.4 | V |
| $I_{IN}$ | Input Current | 0V ≦ $V_{IN}$ ≦ Vcc | | | ±10 | µA |
| $I_{PD}$ | Pull Down Current | R/F pin,$V_{IH}$=Vcc | | | 100 | µA |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$=0V | | | -50 | mA |
| **LVDS DRIVER DC SPECIFICATIONS** | | | | | | |
| $V_{OD}$ | Differential Output Voltage | RL=100Ω | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in VOD between Complimentary Output States | | | | 35 | mV |
| $V_{OC}$ | Common Mode Voltage | | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OC}$ | Change in VOC between Complimentary Output States | | | | 35 | mV |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$=0V,RL=100Ω | | | -24 | mA |
| $I_{OZ}$ | Output TRI-STATE Current | /PDWN=0V, $V_{OUT}$=0V to Vcc | | | ±10 | µA |
| **LVDS RECEIVER DC SPECIFICATIONS** | | | | | | |
| $V_{TH}$ | Differential Input High Threshold | $V_{OC}$=+1.2V | | | +100 | mV |
| $V_{TL}$ | Differential Input low Threshold | | -100 | | | mV |
| $I_{IN}$ | Input Current | $V_{IN}$=+2.4V/ 0V Vcc=3.6V | | | ±10 | µA |

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage (Vcc) | -0.3 to +4V |
| CMOS/TTL Input Voltage | -0.3V to (Vcc + 0.3V) |
| CMOS/TTL Output Voltage | -0.3V to (Vcc + 0.3V) |
| LVDS Receiver Input Voltage | -0.3V to (Vcc + 0.3V) |
| LVDS Driver Output Voltage | -0.3V to (Vcc + 0.3V) |
| Output Short Circuit Duration | continuous |
| Junction Temperature | +150˚C |
| Storage Temperature Range | -65˚C to 150˚C |
| Lead Temperature(Soldering, 4 sec.) | +260˚C |
| Maximum Power Dissipation @25˚C | 1.4W |



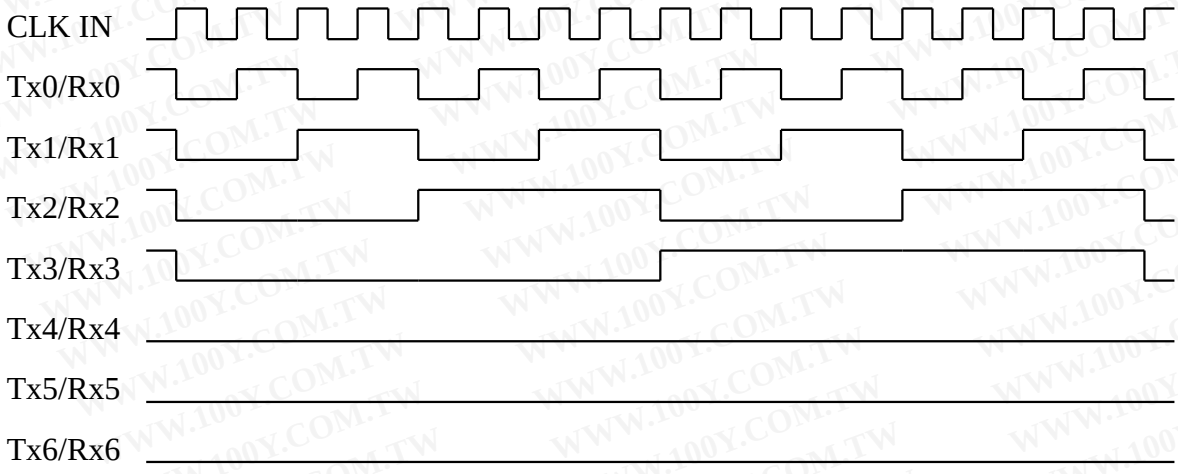
Note 1:"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not ment to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

## Supply Current

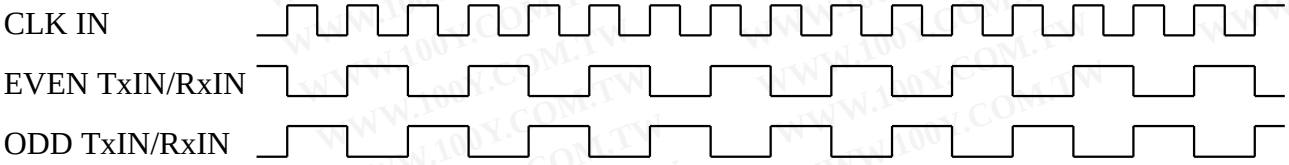
Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

| SYMBOL | PARAMETER | CONDITIONS | | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $I_{TCCG}$ | Transmitter Supply Current | RL=100Ω,CL=5pF, Vcc=3.3V, 16 Grayscale Pattern | f=65MHz | 36 | 46 | mA |
| | | | f=85MHz | 39 | 49 | mA |
| $I_{TCCW}$ | Transmitter Supply Current | RL=100Ω,CL=5pF, Vcc=3.3V, Worst Case Pattern | f=65MHz | 38 | 48 | mA |
| | | | f=85MHz | 41 | 51 | mA |
| $I_{TCCS}$ | Transmitter Power Down Supply Current | /PDWN =0 V | | | 10 | µA |
| $I_{RCCG}$ | Receiver Supply Current | CL=8pF, Vcc=3.3V, 16 Grayscale Pattern | f=65MHz | 41 | 53 | mA |
| | | | f=85MHz | 52 | 64 | mA |
| $I_{RCCW}$ | Receiver Supply Current | CL=8pF, Vcc=3.3V, Worst Case Pattern | f=65MHz | 72 | 94 | mA |
| | | | f=85MHz | 84 | 96 | mA |
| $I_{RCCS}$ | Receiver Power Down Supply Current | /PDWN =0 V | | | 10 | µA |

**16 Grayscale Pattern**




**Worst Case Pattern**



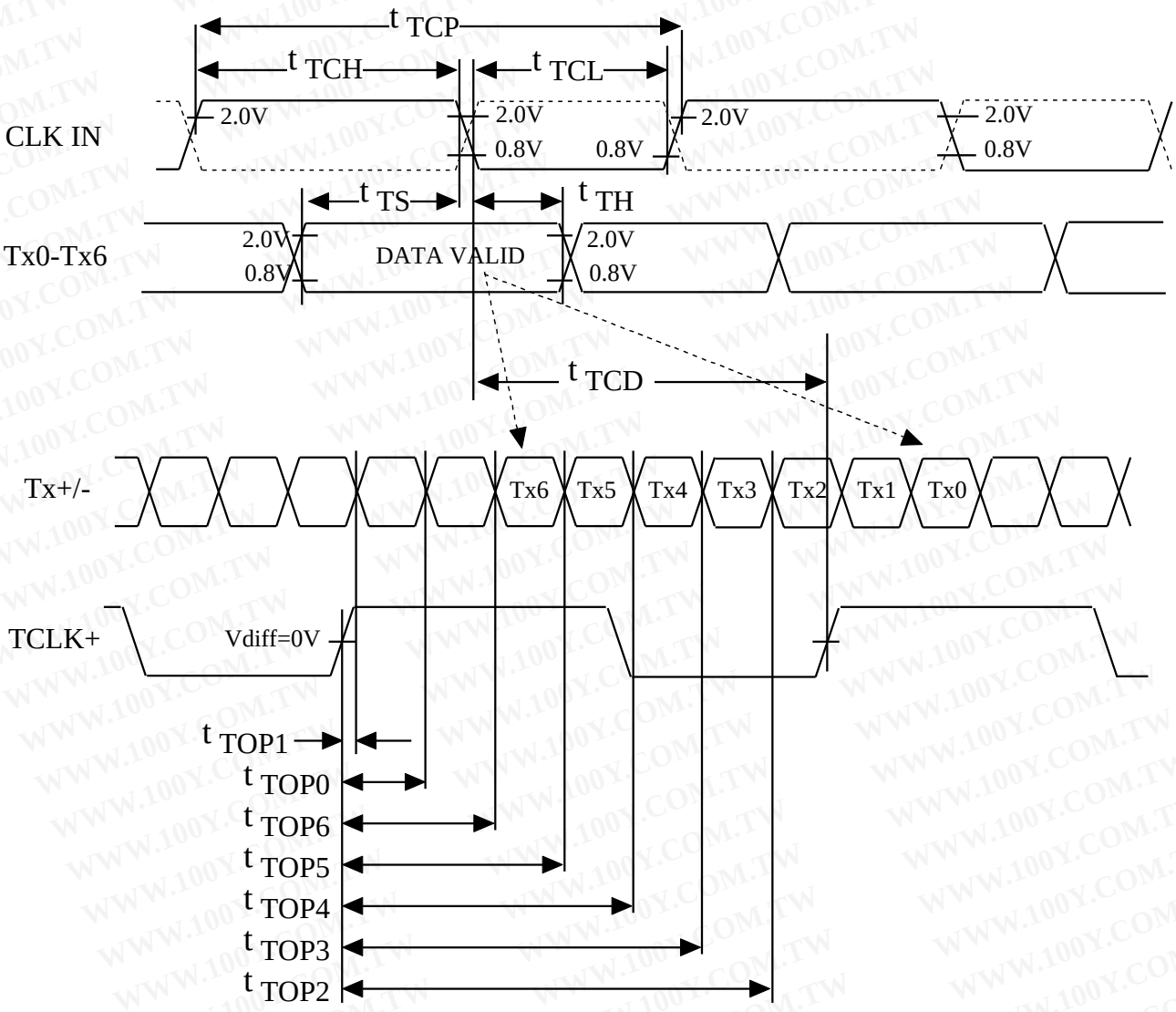
## Switching Characteristics

Vcc = 3.0 - 3.6V, Ta = -10 - +70 ˚C

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TRANSMITTER** | | | | | |
| $t_{TCIT}$ | CLK IN Transition Time | | | 5.0 | ns |
| $t_{TCP}$ | CLK IN Period | 11.76 | T | 50.0 | ns |
| $t_{TCH}$ | CLK IN High Time | 0.35T | 0.5T | 0.65T | ns |
| $t_{TCL}$ | CLK IN Low Time | 0.35T | 0.5T | 0.65T | ns |
| $t_{TCD}$ | CLK IN to TCLK+/- Delay | | 2T/7 | | ns |
| $t_{TS}$ | TTL Data Setup to CLK IN | 2.5 | | | ns |
| $t_{TH}$ | TTL Data Hold from CLK IN | 2.5 | | | ns |
| $t_{LVT}$ | LVDS Transition Time | | 0.6 | 1.5 | ns |
| $t_{TOP1}$ | Output Data Position 0 (T=11.76ns) | -0.2 | 0.0 | 0.2 | ns |
| $t_{TOP0}$ | Output Data Position 1 (T=11.76ns) | T/7-0.2 | T/7 | T/7+0.2 | ns |
| $t_{TOP6}$ | Output Data Position 2 (T=11.76ns) | 2T/7-0.2 | 2T/7 | 2T/7+0.2 | ns |
| $t_{TOP5}$ | Output Data Position 3 (T=11.76ns) | 3T/7-0.2 | 3T/7 | 3T/7+0.2 | ns |
| $t_{TOP4}$ | Output Data Position 4 (T=11.76ns) | 4T/7-0.2 | 4T/7 | 4T/7+0.2 | ns |
| $t_{TOP3}$ | Output Data Position 5 (T=11.76ns) | 5T/7-0.2 | 5T/7 | 5T/7+0.2 | ns |
| $t_{TOP2}$ | Output Data Position 6 (T=11.76ns) | 6T/7-0.2 | 6T/7 | 6T/7+0.2 | ns |
| $t_{TPLL}$ | Phase Lock Loop Set | | | 10 | ms |
| **RECEIVER** | | | | | |
| $t_{RCP}$ | CLK OUT Period | 11.76 | T | 50.0 | ns |
| $t_{RCH}$ | CLK OUT High Time | | 4T/7 | | ns |
| $t_{RCL}$ | CLK OUT Low Time | | 3T/7 | | ns |
| $t_{RCD}$ | RCLK+/- to CLK OUT Delay | | 5T/7 | | ns |
| $t_{RS}$ | TTL Data Setup to CLK OUT | 3T/7-2.5 | | | ns |
| $t_{RH}$ | TTL Data Hold from CLK OUT | 4T/7-3.5 | | | ns |
| $t_{TLH}$ | TTL Low to High Transition Time | | 3.0 | 5.0 | ns |
| $t_{THL}$ | TTL High to Low Transition Time | | 3.0 | 5.0 | ns |
| $t_{RIP1}$ | Input Data Position 0 (T=11.76ns) | -0.4 | 0.0 | 0.4 | ns |
| $t_{RIP0}$ | Input Data Position 1 (T=11.76ns) | T/7-0.4 | T/7 | T/7+0.4 | ns |
| $t_{RIP6}$ | Input Data Position 2 (T=11.76ns) | 2T/7-0.4 | 2T/7 | 2T/7+0.4 | ns |
| $t_{RIP5}$ | Input Data Position 3 (T=11.76ns) | 3T/7-0.4 | 3T/7 | 3T/7+0.4 | ns |
| $t_{RIP4}$ | Input Data Position 4 (T=11.76ns) | 4T/7-0.4 | 4T/7 | 4T/7+0.4 | ns |
| $t_{RIP3}$ | Input Data Position 5 (T=11.76ns) | 5T/7-0.4 | 5T/7 | 5T/7+0.4 | ns |
| $t_{RIP2}$ | Input Data Position 6 (T=11.76ns) | 6T/7-0.4 | 6T/7 | 6T/7+0.4 | ns |
| $t_{RPLL}$ | Phase Lock Loop Set | | | 10.0 | ms |

# AC TIMING DIAGRAMS

## TRANSMITTER DEVICE

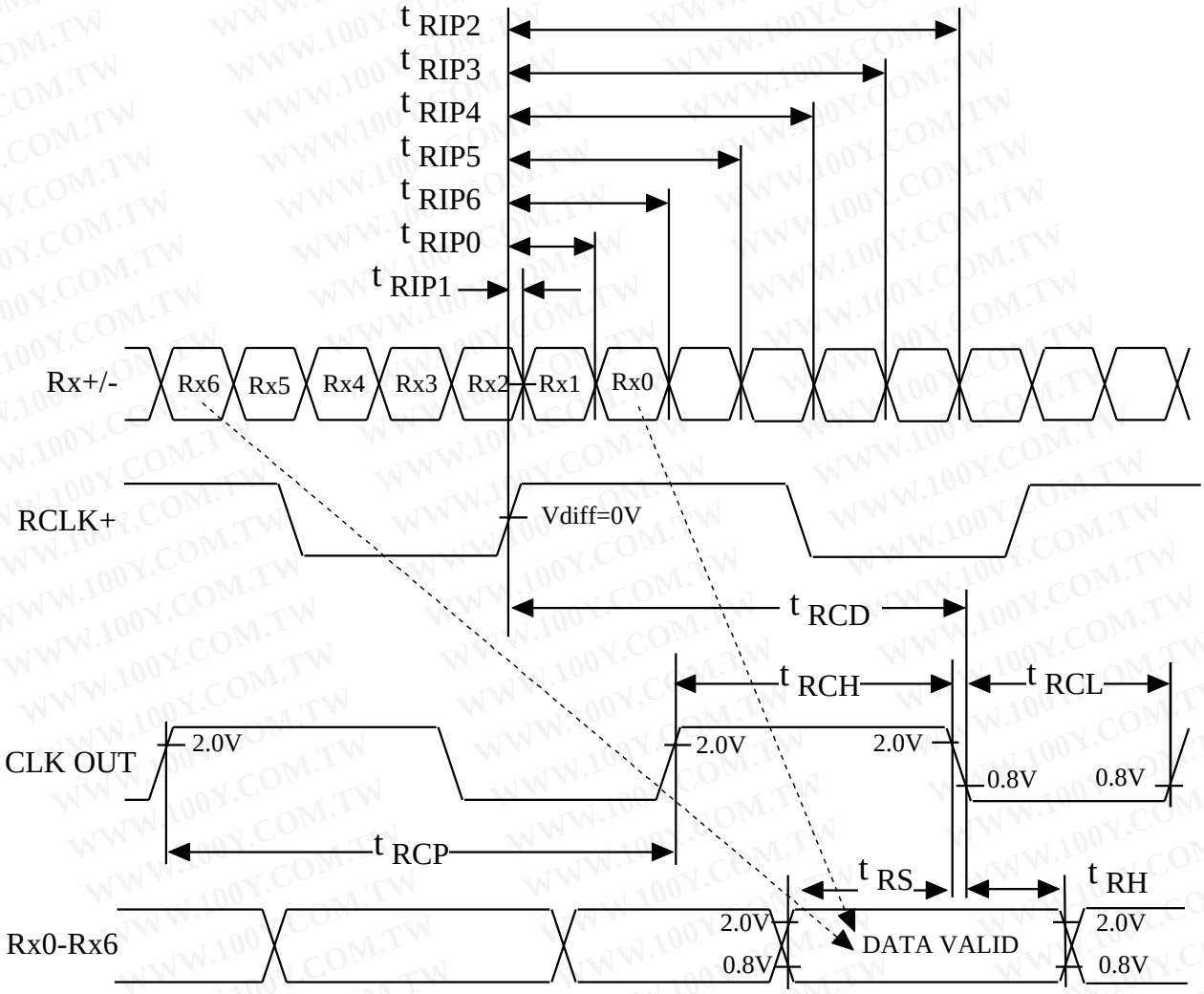



Note:

1) CLK IN: for THC63LVDM83A(R/F=GND), denoted as solid line,
for THC63LVDM83A(R/F=Vcc), denoted as dashed line
2) Vdiff = (TA+) - (TA-), .... (TCLK+) - (TCLK-)

# AC TIMING DIAGRAMS

## RECEIVER DEVICE

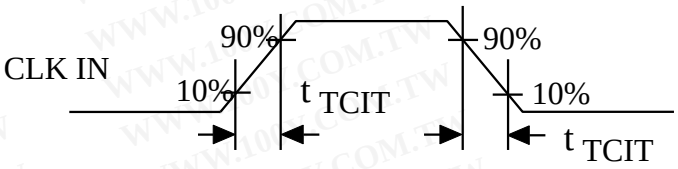



Note:
1) Vdiff = (RA+) - (RA-), .... (RCLK+) - (RCLK-)

# AC TIMING DIAGRAMS

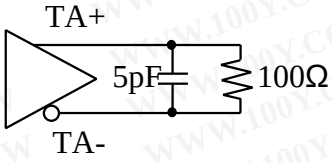
## TRANSMITTER DEVICE TRANSITION TIMES

**TTL Input**

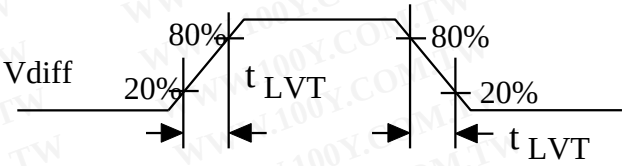



**LVDS Output**

Vdiff = (TA+)-(TA-)

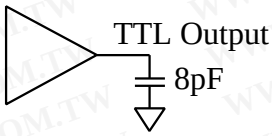



**LVDS output load**

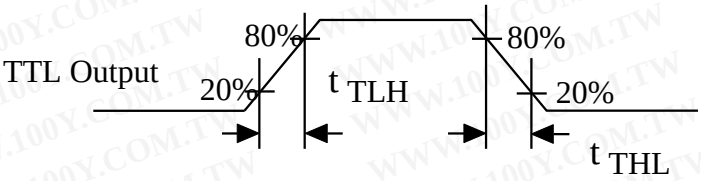



## RECEIVER DEVICE TRANSITION TIMES

**TTL Output**

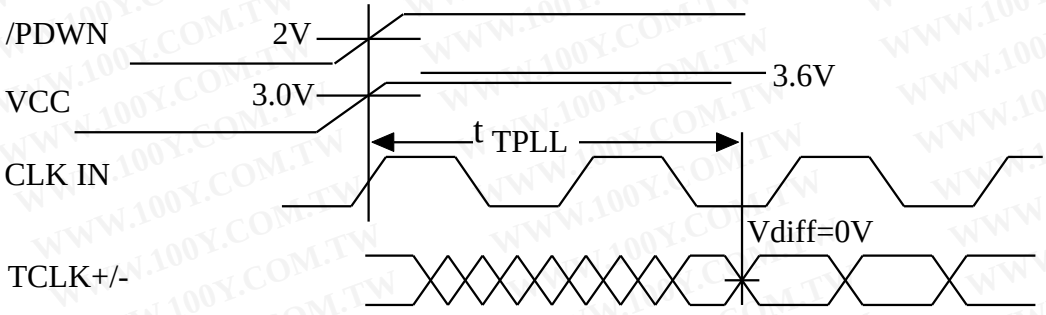



**TTL output load**

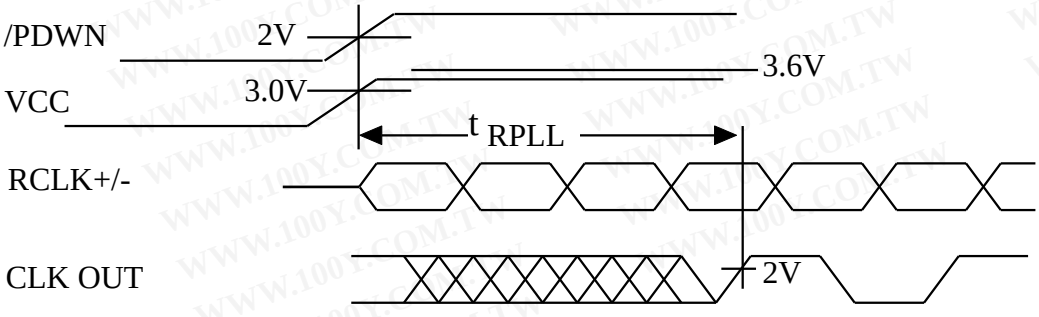



## PHASE LOCK LOOP SET TIME

**TRANSMITTER DEVICE**




**RECEIVER DEVICE**



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