



DS55460/DS75460 Series Dual Peripheral Drivers

General Description

The DS55460/DS75460 series of dual peripheral drivers are functionally interchangeable with DS55450/DS75450 series peripheral drivers, but are designed for use in systems that require higher breakdown voltages than DS55450/DS75450 series can provide at the expense of slightly slower switching speeds. Typical applications include power drivers, logic buffers, lamp drivers, relay drivers, MOS drivers, line drivers and memory drivers.

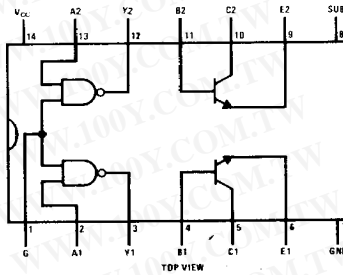
The DS55460 and DS75460 are unique general-purpose devices each featuring two standard 54/74 series TTL gates and two uncommitted, high current, high voltage, NPN transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The DS55461/DS75461, DS55462/DS75462, DS55463/DS75463 and DS55464/DS75464 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

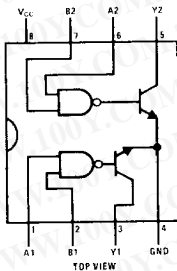
Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 30V
- Medium speed switching
- Circuit flexibility for varied applications and choice of logic function
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages

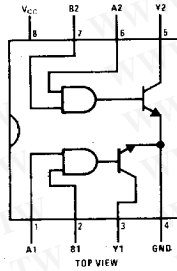
Connection Diagrams (Dual-In-Line and Metal Can Packages)



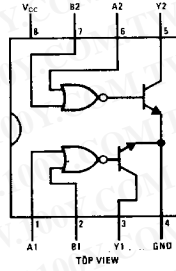
Order Number
DS55460J, DS75460J, or DS75460N
See NS Package J14A or N14A



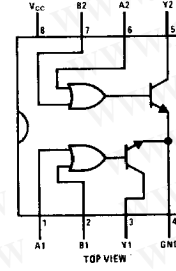
Order Number DS55461J-8,
DS75461J-8 or DS75461N-8



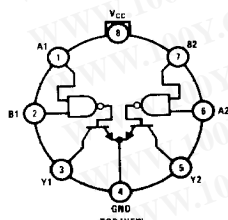
Order Number DS55462J-8,
DS75462J-8 or DS75462N-8



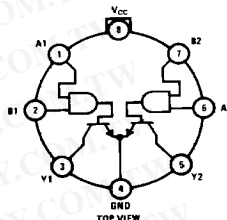
Order Number DS55463J-8,
DS75463J-8 or DS75463N-8
See NS Package J08A or N08A



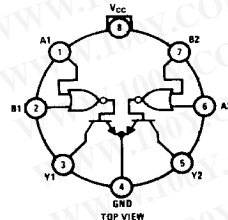
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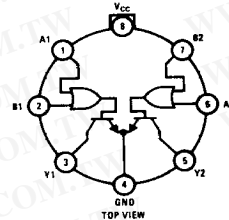
Pin 4 is in electrical contact with the case.
Order Number
DS55461H or DS75461H



Pin 4 is in electrical contact with the case.
Order Number
DS55462H or DS75462H
See NS Package H08C



Pin 4 is in electrical contact with the case.
Order Number
DS55463H or DS75463H



Pin 4 is in electrical contact with the case.
Order Number
DS55464H or DS75464H

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Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	7V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
V _{CC} -to-Substrate Voltage DS55460/DS75460	40V
Collector-to-Substrate Voltage DS55460/DS75460	40V
Collector-Base Voltage DS55460/DS75460	40V
Collector-Emitter Voltage DS55460/DS75460 (Note 4) DS55460/DS75463 (Note 5)	40V 25V
Emitter-Base Voltage DS55460/DS75460	5V
Output Voltage (Note 6) DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	35V
Collector Current (Note 7) DS55460/DS75460	300 mA
Output Current (Note 7) DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	300 mA
Continuous Total Dissipation	800 mW
Storage Temperature Range	-65° C to +150° C
Lead Temperature (Soldering, 10 seconds)	260° C

Operating Conditions (Note 7)

	MIN	MAX	UNITS
Supply Voltage (V _{CC})			
DS5546X	4.5	5.5	V
DS7546X	4.75	5.25	V
Temperature (T _A)			
DS5546X	-55	+125	°C
DS7546X	0	+70	°C

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Electrical Characteristics

DS55460/DS75460 (Notes 8 and 9)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
TTL GATES						
V _{IH} High Level Input Voltage	(Figure 1)	2			V	
V _{IL} Low Level Input Voltage	(Figure 2)			0.8	V	
V _I Input Clamp Voltage	V _{CC} = Min, I _I = -12 mA, (Figure 3)		-1.2	-1.5	V	
V _{OH} High Level Output Voltage	V _{CC} = Min, V _{IL} = 0.8V, I _{OH} = -400μA, (Figure 2)	2.4	3.3		V	
V _{OL} Low Level Output Voltage	V _{CC} = Min, V _{IH} = 2V, I _{OL} = 16 mA, (Figure 1)	DS55460	0.25	0.5	V	
		DS75460	0.25	0.4	V	
I _I Input Current at Maximum Input Voltage	V _{CC} = Max, V _I = 5.5V, (Figure 4)	Input A		1	mA	
		Input G		2	mA	
I _{IH} High Level Input Current	V _{CC} = Max, V _I = 2.4V, (Figure 4)	Input A		40	μA	
		Input G		80	μA	
I _{IL} Low Level Input Current	V _{CC} = Max, V _I = 0.4V, (Figure 3)	Input A		-1.6	mA	
		Input G		-3.2	mA	
I _{OS} Short Circuit Output Current	V _{CC} = Max, (Note 10), (Figure 5)	-18	-35	-55	mA	
I _{CCH} Supply Current	V _{CC} = Max, V _I = 0V, Outputs High, (Figure 6)		2.8	4	mA	
I _{CCL} Supply Current	V _{CC} = Max, V _I = 5V, Outputs Low, (Figure 6)		7	11	mA	
OUTPUT TRANSISTORS						
V _{(BR)CBO} Collector-Base Breakdown Voltage	I _C = 100μA, I _E = 0	40			V	
V _{(BR)CER} Collector-Emitter Breakdown Voltage	I _C = 100μA, R _{BE} = 500Ω, I _E = 10 mA, I _B = 0 (Note 12)	DS55460	40		V	
		DS75460	25		V	
V _{(BR)EBO} Emitter-Base Breakdown Voltage	I _E = 100μA, I _C = 0	5			V	
h _{FE} Static Forward Current Transfer Ratio	V _{CE} = 3V, (Note 12)	DS55460, T _A = 25° C	I _C = 100 mA	25		
			I _C = 300 mA	30		
		DS55460, T _A = -55° C	I _C = 100 mA	10		
			I _C = 300 mA	15		
		DS75460, T _A = 25° C	I _C = 100 mA	25		
			I _C = 300 mA	30		
DS75460, T _A = 0° C	I _C = 100 mA	20				
	I _C = 300 mA	25				

Electrical Characteristics DS55460/DS75460 (Continued)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{BE} Base-Emitter Voltage	(Note 12)	DS55460	I _B = 10 mA, I _C = 100 mA	0.85	1.2	V
			I _B = 30 mA, I _C = 300 mA	1	1.4	V
		DS75460	I _B = 10 mA, I _C = 100 mA	0.85	1	V
			I _B = 30 mA, I _C = 300 mA	1	1.2	V
V _{CE(SAT)} Collector-Emitter Saturation Voltage	(Note 12)	DS55460	I _B = 10 mA, I _C = 100 mA	0.25	0.5	V
			I _B = 30 mA, I _C = 300 mA	0.45	0.8	V
		DS75460	I _B = 10 mA, I _C = 100 mA	0.25	0.4	V
			I _B = 30 mA, I _C = 300 mA	0.45	0.7	V

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Switching Characteristics

DS55460/DS75460 V_{CC} = 5V, T_A = 25°C

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t _{PLH} Propagation Delay Time, Low-To-High Level Output	C _L = 15 pF	R _L = 400Ω, TTL Gates Only, (Figure 12)		22		ns
		R _L = 50Ω, I _C ≈ 200 mA, Gates and Transistors Combined, (Figure 14)		45	65	ns
t _{PHL} Propagation Delay Time, High-To-Low Level Output	C _L = 15 pF	R _L = 400Ω, TTL Gates Only, (Figure 12)		8		ns
		R _L = 50Ω, I _C ≈ 200 mA, Gates and Transistors Combined, (Figure 14)		35	50	ns
t _{TLH} Transition Time, Low-To-High Level Output	C _L = 15 pF, R _L = 50Ω, I _C ≈ 200 mA, Gates and Transistors Combined, (Figure 14)			10	20	ns
t _{THL} Transition Time, High-To-Low Level Output	C _L = 15 pF, R _L = 50Ω, I _C ≈ 200 mA, Gates and Transistors Combined, (Figure 14)			10	20	ns
V _{OH} High Level Output Voltage After Switching	V _S = 30V, I _C ≈ 300 mA, R _{BE} = 500Ω, (Figure 15)		V _S -10			mV
t _d Delay Time	I _C = 200 mA, I _{B(1)} = 20 mA, I _{B(2)} = -40 mA, V _{BE(OFF)} = -1V, C _L = 15 pF, R _L = 50Ω, (Note 13), (Figure 13)			10		ns
t _r Rise Time	I _C = 200 mA, I _{B(1)} = 20 mA, I _{B(2)} = -40 mA, V _{BE(OFF)} = -1V, C _L = 15 pF, R _L = 50Ω, (Note 13), (Figure 13)			16		ns
t _s Storage Time	I _C = 200 mA, I _{B(1)} = 20 mA, I _{B(2)} = -40 mA, V _{BE(OFF)} = -1V, C _L = 15 pF, R _L = 50Ω, (Note 13), (Figure 13)			23		ns
t _f Fall Time	I _C = 200 mA, I _{B(1)} = 20 mA, I _{B(2)} = -40 mA, V _{BE(OFF)} = -1V, C _L = 15 pF, R _L = 50Ω, (Note 13), (Figure 13)			14		ns

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Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 8 and 9)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{IH} High Level Input Voltage	(Figure 7)	2			V	
V_{IL} Low Level Input Voltage	(Figure 7)			0.8	V	
V_I Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12 \text{ mA}$		-1.2	-1.5	V	
V_{OL} Low Level Output Voltage	$V_{CC} = \text{Min}, (\text{Figure 7})$	DS55461, $V_{IL} = 0.8\text{V}$	$I_{OL} = 100 \text{ mA}$	0.15	0.5	V
			$I_{OL} = 300 \text{ mA}$	0.36	0.8	V
		DS55462, $V_{IH} = 2\text{V}$	$I_{OL} = 100 \text{ mA}$	0.16	0.5	V
			$I_{OL} = 300 \text{ mA}$	0.35	0.8	V
		DS55463, $V_{IL} = 0.8\text{V}$	$I_{OL} = 100 \text{ mA}$	0.18	0.5	V
			$I_{OL} = 300 \text{ mA}$	0.39	0.8	V
		DS55464, $V_{IH} = 2\text{V}$	$I_{OL} = 100 \text{ mA}$	0.17	0.5	V
			$I_{OL} = 300 \text{ mA}$	0.38	0.8	V
		DS75461, $V_{IL} = 0.8\text{V}$	$I_{OL} = 100 \text{ mA}$	0.15	0.4	V
			$I_{OL} = 300 \text{ mA}$	0.36	0.7	V
DS75462, $V_{IH} = 2\text{V}$	$I_{OL} = 100 \text{ mA}$	0.16	0.4	V		
	$I_{OL} = 300 \text{ mA}$	0.35	0.7	V		
DS75463, $V_{IL} = 0.8\text{V}$	$I_{OL} = 100 \text{ mA}$	0.18	0.4	V		
	$I_{OL} = 300 \text{ mA}$	0.39	0.7	V		
DS75464, $V_{IH} = 2\text{V}$	$I_{OL} = 100 \text{ mA}$	0.17	0.4	V		
	$I_{OL} = 300 \text{ mA}$	0.38	0.7	V		
I_{OH} High Level Output Current	$V_{CC} = \text{Min}, V_{OH} = 35\text{V}, (\text{Figure 7})$	$V_{IH} = 2\text{V}$	DS55461, DS55463		300	μA
			DS75461, DS75463		100	μA
		$V_{IL} = 0.8\text{V}$	DS55462, DS55464		300	μA
			DS75462, DS75464		100	μA
I_I Input Current at Maximum Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5\text{V}, (\text{Figure 9})$			1	mA	
I_{IH} High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4\text{V}, (\text{Figure 9})$			40	μA	
I_{IL} Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}, (\text{Figure 8})$		-1	-1.6	mA	
I_{CCH} Supply Current	$V_{CC} = \text{Max}, \text{Outputs High}, (\text{Figure 11})$	$V_I = 5\text{V}$	DS55461/ DS75461, DS55463/ DS75463	8	11	mA
		$V_I = 0\text{V}$	DS55462/ DS75462	13	17	mA
			DS55464/ DS75464	14	19	mA
I_{CCL} Supply Current	$V_{CC} = \text{Max}, \text{Outputs Low}, (\text{Figure 11})$	$V_I = 0\text{V}$	DS55461/ DS75461	61	76	mA
			DS55463/ DS75463	63	76	mA
		$V_I = 5\text{V}$	DS55462/ DS75462	65	76	mA
			DS55464/ DS75464	72	85	mA

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Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH} Propagation Delay Time, Low-To-High Level Output	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}, R_L = 50\Omega,$ (Figure 14)	DS55461/ DS75461, DS55463/ DS75463	45	55	ns
		DS55462/ DS75462, DS55464/ DS75464	50	65	ns
t_{PHL} Propagation Delay Time, High-To-Low Level Output	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}, R_L = 50\Omega,$ (Figure 14)	DS55461/ DS75461, DS55463/ DS75463	30	40	ns
		DS55462/ DS75462, DS55464/ DS75464	40	50	ns
t_{TLH} Transition Time, Low-To-High Level Output	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}, R_L = 50\Omega,$ (Figure 14)	DS55461/ DS75461	8	20	ns
		DS55462/ DS75462	12	25	ns
		DS55463/ DS75463	8	25	ns
		DS55464/ DS75464	12	20	ns
t_{THL} Transition Time, High-To-Low Level Output	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}, R_L = 50\Omega,$ (Figure 14)	DS55461/ DS75461	10	20	ns
		DS55462/ DS75462, DS55464/ DS75464	15	20	ns
		DS55463/ DS75463	10	25	ns
V_{OH} High-Level Output Voltage After Switching	$V_S = 30V, I_O \approx 300 \text{ mA},$ (Figure 15)	$V_S - 10$			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: This is the voltage between two emitters of a multiple-emitter transistor.

Note 4: This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω .

Note 5: This value applies between 0 and 10 mA collector current when the base-emitter diode is open circuited.

Note 6: This is the maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 7: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 8: Unless otherwise specified min/max limits apply across the $-55^\circ C$ to $+125^\circ C$ temperature range for the DS55460 series and across the $0^\circ C$ to $+70^\circ C$ range for the DS75460 series. All typicals are given for $V_{CC} = +5V$ and $T_A = 25^\circ C$.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 10: Only one output at a time should be shorted.

Note 11: For the DS55460/DS75460 only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.

Note 12: These parameters must be measured using pulse techniques. $t_W = 300\mu s$, duty $< 2\%$.

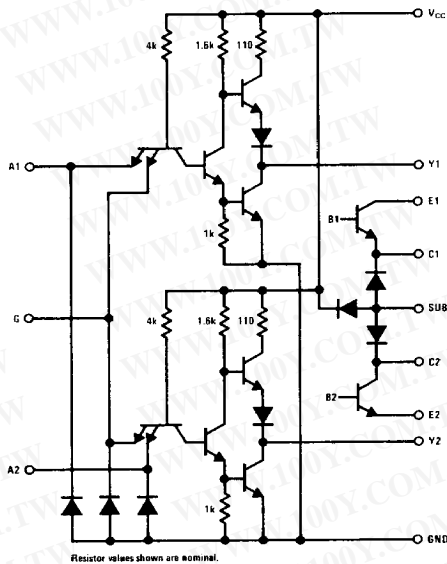
Note 13: Applies to output transistors only.

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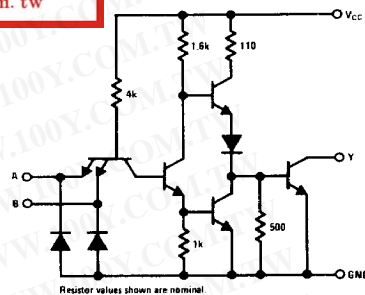
Schematic Diagrams

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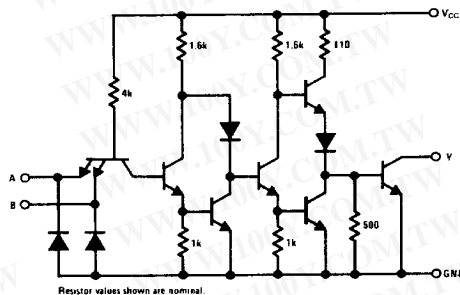
DS55460/DS75460



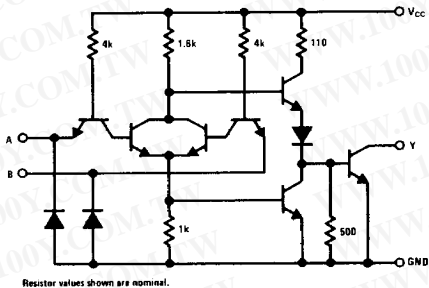
DS55461/DS75461



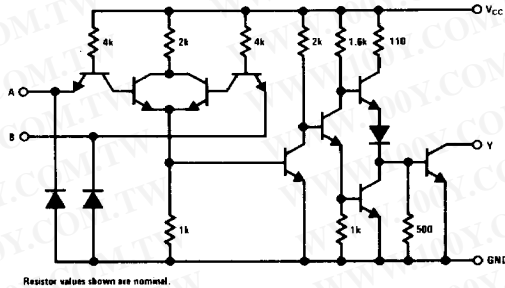
DS55462/DS75462



DS55463/DS75463



DS55464/DS75464



Truth Tables (H = high level, L = low level)

DS55461/DS75461

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55462/DS75462

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

DS55463/DS75463

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

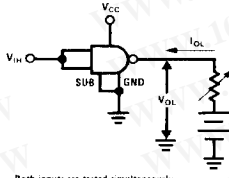
DS55464/DS75464

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

DC Test Circuits

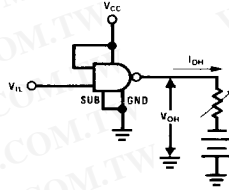
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DS55460/DS75460 Series



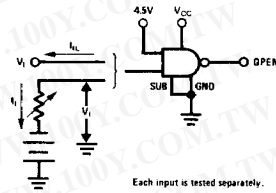
Both inputs are tested simultaneously.

FIGURE 1. V_{IH} , V_{OL}



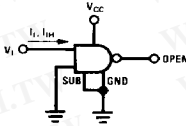
Each input is tested separately.

FIGURE 2. V_{IL} , V_{OH}



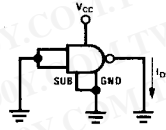
Each input is tested separately.

FIGURE 3. V_I , I_{IL}



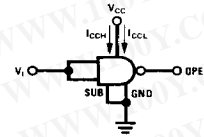
Each input is tested separately.

FIGURE 4. I_1 , I_{1H}



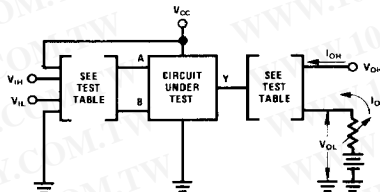
Each gate is tested separately.

FIGURE 5. I_{OS}



Both gates are tested simultaneously.

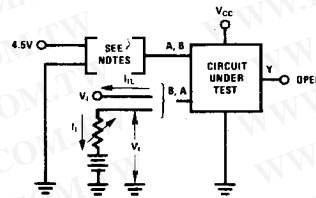
FIGURE 6. I_{CCH} , I_{CCL}



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS55461	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55462	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55463	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
DS55464	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

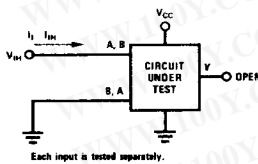
Each input is tested separately.

FIGURE 7. V_{IH} , V_{IL} , I_{OH} , V_{OL}



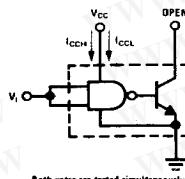
Note 1: Each input is tested separately.
 Note 2: When testing DS55463/DS75463 and DS75464, input not under test is grounded.
 For all other circuits it is at 4.5V.

FIGURE 8. V_I , I_{IL}



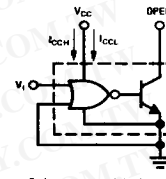
Each input is tested separately.

FIGURE 9. I_1 , I_{1H}



Both gates are tested simultaneously.

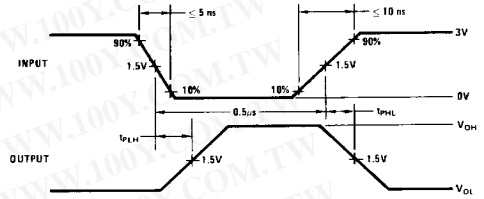
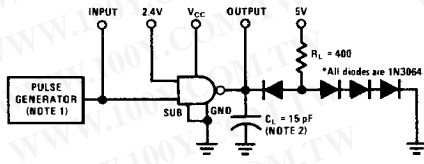
FIGURE 10. I_{CCH} , I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

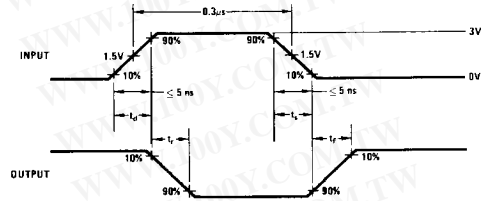
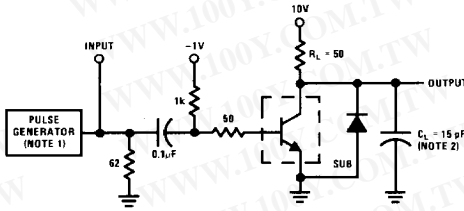
FIGURE 11. I_{CCH} , I_{CCL} for OR, NOR Circuits

Switching Characteristics



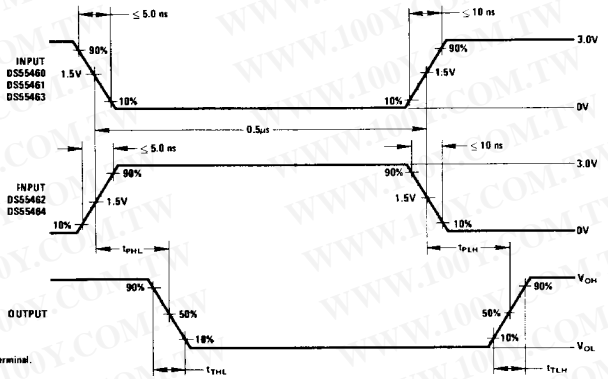
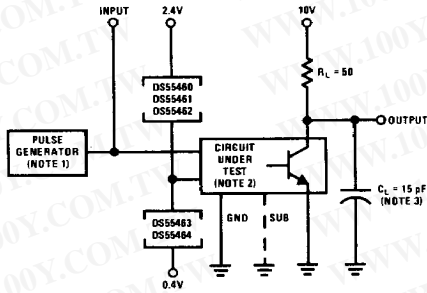
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
 Note 2: C_L includes probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS55460 and DS75460 Only)



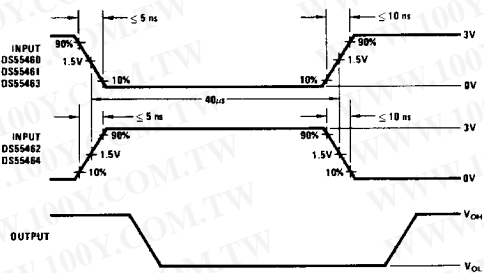
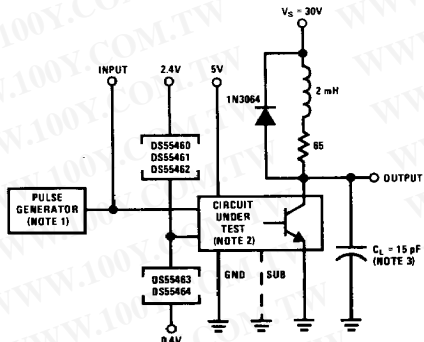
Note 1: The pulse generator has the following characteristics: duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.
 Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor (DS55460 and DS75460 Only)



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
 Note 2: When testing DS55468 or DS75460, connect output Y to transistor base and ground the substrate terminal.
 Note 3: C_L includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.
 Note 2: When testing DS55468 or DS75460, connect output Y to transistor base with a 500 Ω resistor from there to ground, and ground the substrate terminal.
 Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-Up Test of Complete Drivers

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