Directed Energy, Inc.
An IXYS Company

DEIC420

20 Ampere Low-Side Ultrafast RF MOSFET Driver

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- High Peak Output Current: 20A Peak
- Wide Operating Range: 8V to 30V
- Rise And Fall Times of <4ns
- Minimum Pulse Width Of 8ns
- High Capacitive Load Drive Capability: 4nF in <4ns
- Matched Rise And Fall Times
- 32ns Input To Output Delay Time
- Low Output Impedance
- Low Quiescent Supply Current**t**

Applications

- Driving RF MOSFETs
- Class D or E Switching Amplifier Drivers
- Multi MHz Switch Mode Power Supplies (SMPS)
- Pulse Generators
- Acoustic Transducer Drivers
- Pulsed Laser Diode Drivers
- DC to DC Converters
- Pulse Transformer Driver

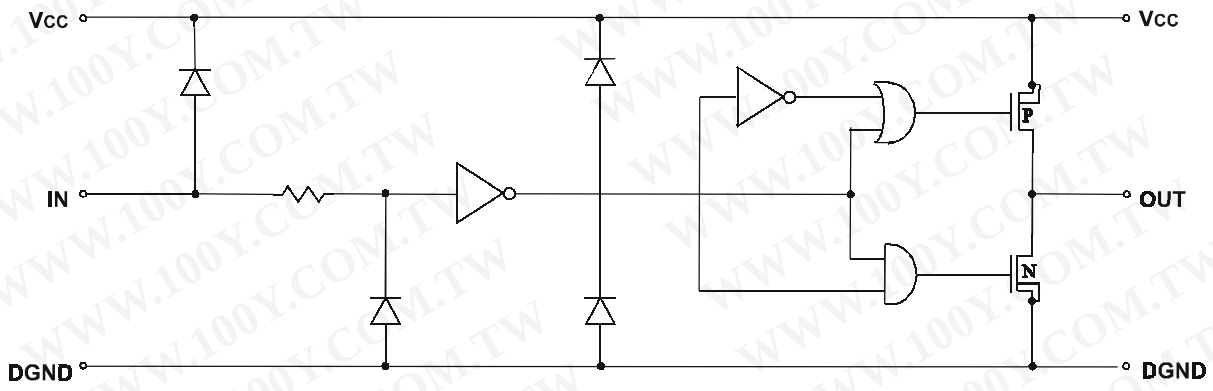
Description

TheDEIC420 is a CMOS high speed high current gate driver specifically designed to drive MOSFETs in Class D and E HF RF applications at up to 45MHz, as well as other applications requiring ultrafast rise and fall times or short minimum pulse widths. The DEIC420 can source and sink 20A of peak current while producing voltage rise and fall times of less than 4ns, and minimum pulse widths of 8ns. The input of the driver is compatible with TTL or CMOS and is fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in the DEIC420. Its features and wide safety margin in operating voltage and power make the DEIC420 unmatched in performance and value.

The DEIC420 is packaged in DEI's low inductance RF package incorporating DEI's patented [1] RF layout techniques to minimize stray lead inductances for optimum switching performance. For applications that do not require the power dissipation of the DEIC420, the driver is also available in a 28 pin SOIC package. See the IXDD415SI data sheet for additional information. The DEIC420 is a surface-mount device, and incorporates patented RF layout techniques to minimize stray lead inductances for optimum switching performance.

[1] DEI U.S. Patent #4,891,686

Figure 1 - DEIC420 Functional Diagram



Absolute Maximum Ratings

Parameter	Value
Supply Voltage	30V
All Other Pins	-0.3V to V_{CC} + 0.3V
Power Dissipation	
$T_{AMBIENT}$ ≤25 °C	2W
T_{CASE} ≤25 °C	100W
Storage Temperature	-65°C to 150°C
Soldering Lead Temperature (10 seconds maximum)	300°C

Parameter	Value
Maximum Junction Temperature	150°C
Operating Temperature Range	-40°C to 85°C
Thermal Impedance (Junction To Case) θ_{JC}	0.13°C/W

Electrical Characteristics

Unless otherwise noted, T_A = 25 °C, 8V ≤ V_{CC} ≤ 30V .
All voltage measurements with respect to DGND. DEIC420 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		3.5			V
V_{IL}	Low input voltage				0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - .025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	I_{OUT} = 10mA, V_{CC} = 15V		0.4	0.6	Ω
R_{OL}	Output resistance @ Output Low	I_{OUT} = 10mA, V_{CC} = 15V		0.4	0.6	Ω
I_{PEAK}	Peak output current	V_{CC} = 15V		20		A
I_{DC}	Continuous output current				4	A
f_{MAX}	Maximum frequency	C_L=4nF Vcc=15V			45	MHz
t_R	Rise time (1)	C_L=1nF Vcc=15V V_{OH}=2V to 12V		3		ns
		C_L=4nF Vcc=15V V_{OH}=2V to 12V		4		ns
t_F	Fall time (1)	C_L=1nF Vcc=15V V_{OH}=12V to 2V		3		ns
		C_L=4nF Vcc=15V V_{OH}=12V to 2V		3.5		ns
t_{ONDLY}	On-time propagation delay (1)	C_L=4nF Vcc=15V		32	38	ns
t_{OFFDLY}	Off-time propagation delay (1)	C_L=4nF Vcc=15V		29	35	ns
P_{Wmin}	Minimum pulse width	FWHM C_L=1nF Vcc=15V		8		ns
		+3V to +3V C_L=1nF Vcc=15V		9		ns
V_{CC}	Power supply voltage		8	15	30	V
I_{CC}	Power supply current	V_{IN} = 3.5V		1	3	mA
		V_{IN} = 0V		0	10	µA
		V_{IN} = + V_{CC}			10	µA

(1) Refer to Figures 3a and 3b
Specifications Subject To Change Without Notice

Lead Description - DEIC420

SYMBOL	FUNCTION	DESCRIPTION
VCC	Supply Voltage	Positive power-supply voltage input. These leads provide power to the entire chip. The range for this voltage is from 8V to 30V.
IN	Input	Input signal-TTL or CMOS compatible.
OUT	Output	Driver Output. For application purposes, this lead is connected, directly to the Gate of a MOSFET
GND	Power Ground	The system ground leads. Internally connected to all circuitry, these leads provide ground reference for the entire chip. These leads should be connected to a low noise analog ground plane for optimum performance.

Note 1: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - DEIC420 Package Photo And Outline

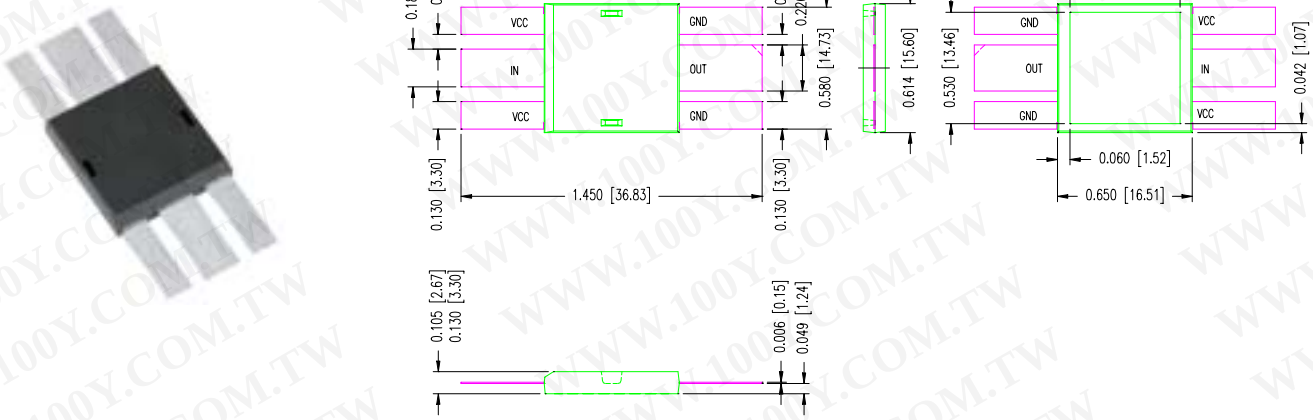


Figure 3a - Characteristics Test Diagram

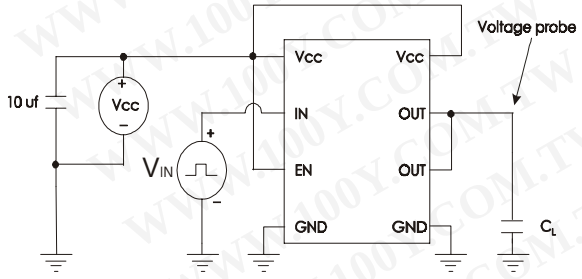
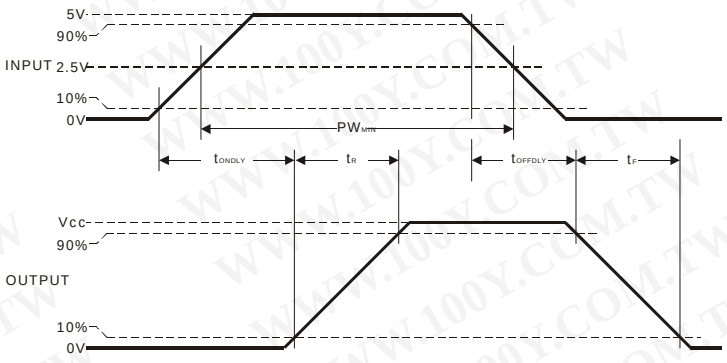


Figure 3b - Timing Diagram



Typical Performance Characteristics

Fig. 4 Rise Time vs. Load Capacitance
V_{CC} = 15V, V_{OH} = 2V To 12V

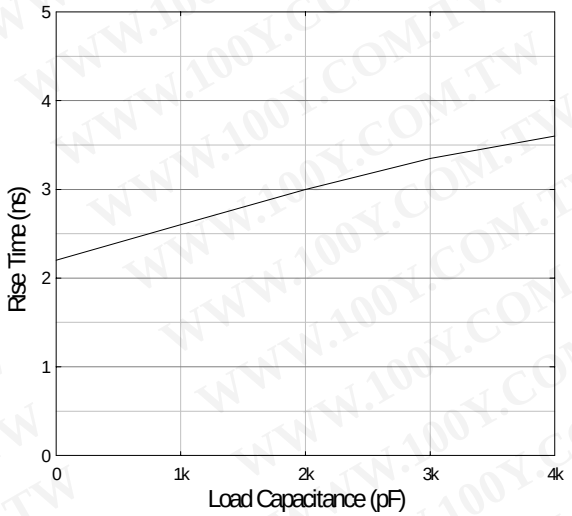


Fig. 5 Fall Time vs. Load Capacitance
V_{CC} = 15V, V_{OH} = 12V To 2V

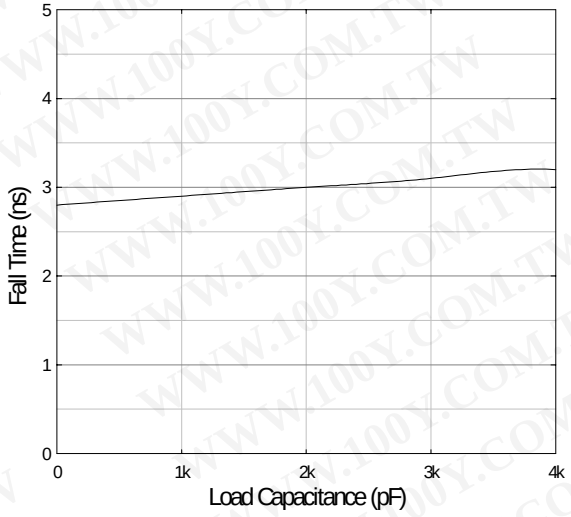


Fig. 6 Supply Current vs. Frequency
Vcc=15V

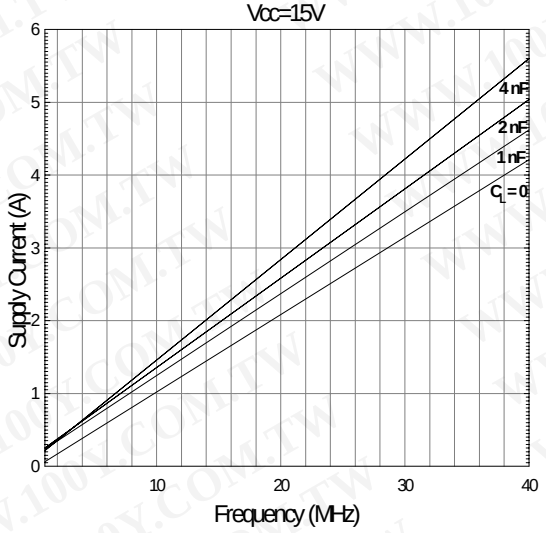


Fig. 7 Supply Current vs. Load Capacitance
Vcc=15V

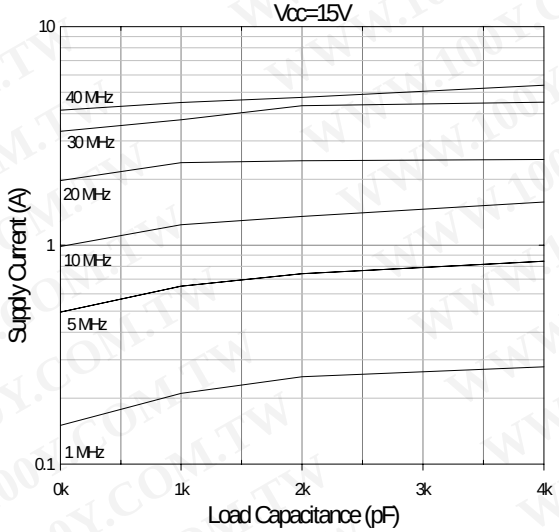


Fig. 8 Propagation Delay Times vs. Input Voltage
C_L=4nF V_{CC}=15V

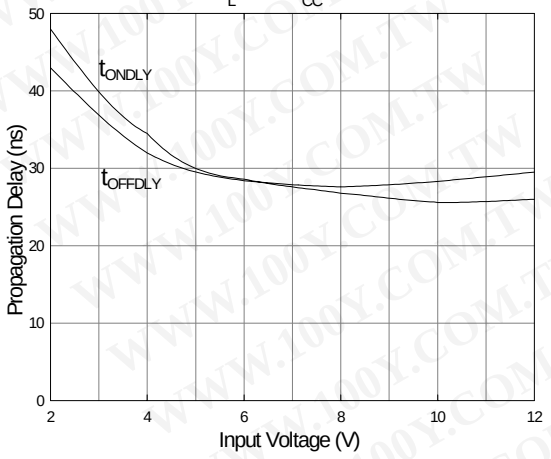


Fig. 9 Propagation Delay Times vs. Junction Temperature
C_L = 4nF, V_{CC} = 15V

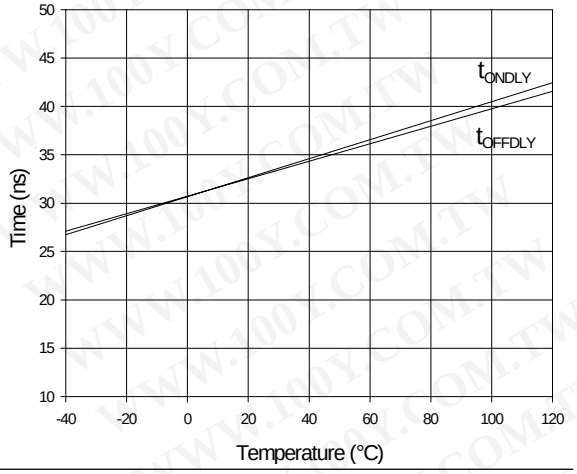
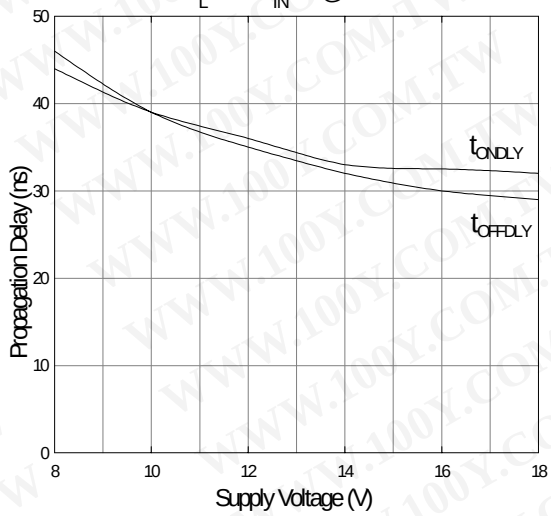


Fig. 10 Propagation Delay vs. Supply Voltage
C_L=4nF V_{IN}=5V@100kHz



Typical Output Waveforms

Unless otherwise noted, all waveforms are taken driving a 1nF load, 1MHz repetition frequency, V_{CC}=15V, Case Temperature = 25°C

Figure 11 3ns Rise Time

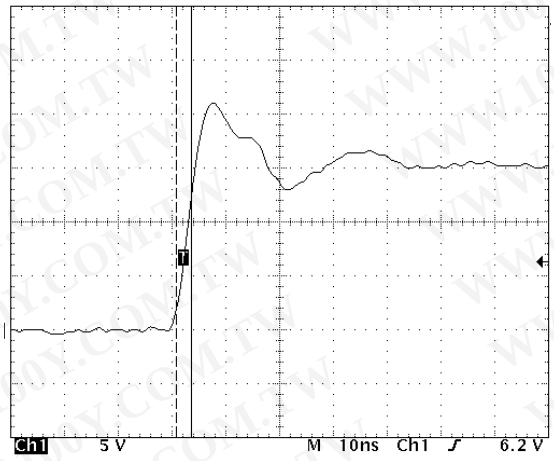


Figure 12 3ns Fall Time

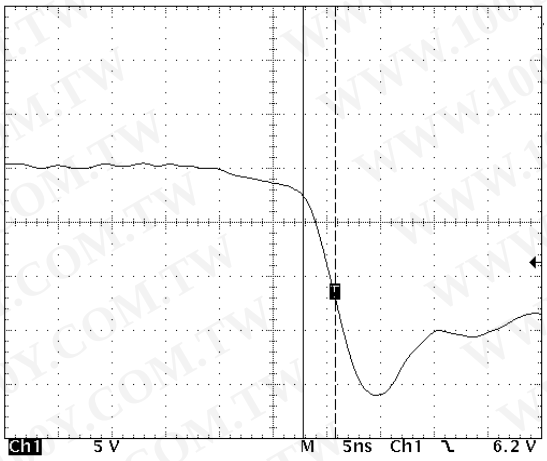


Figure 13 <8ns Minimum Pulse Width

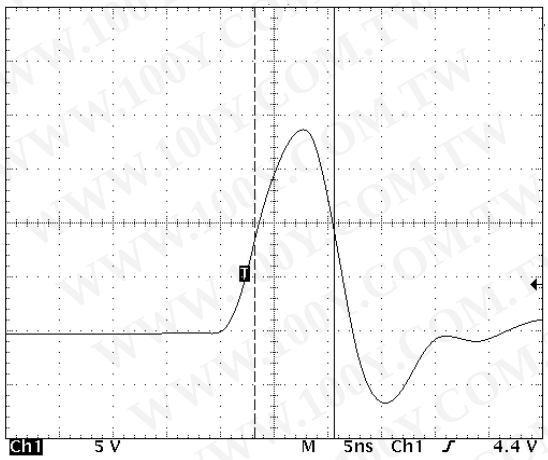


Figure 14 1MHz CW Repetition Frequency

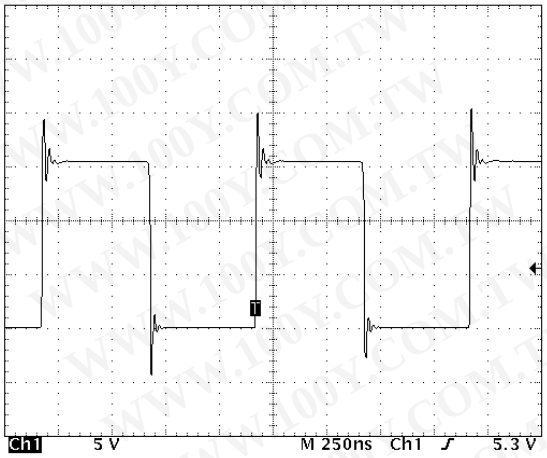


Figure 15 13.56MHz CW Repetition Frequency

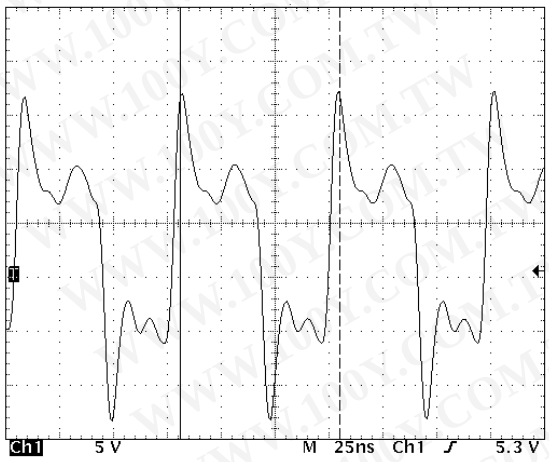


Figure 16 50MHz Burst Repetition Frequency

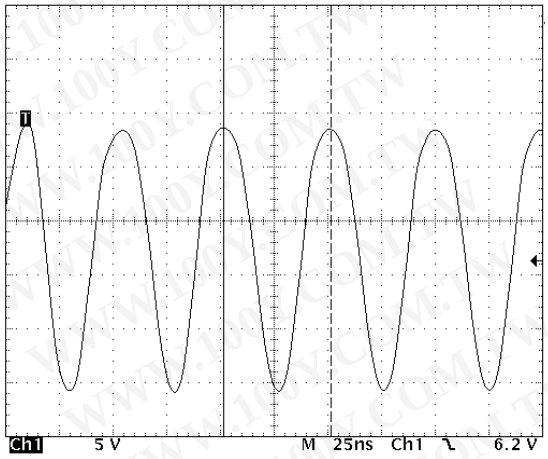
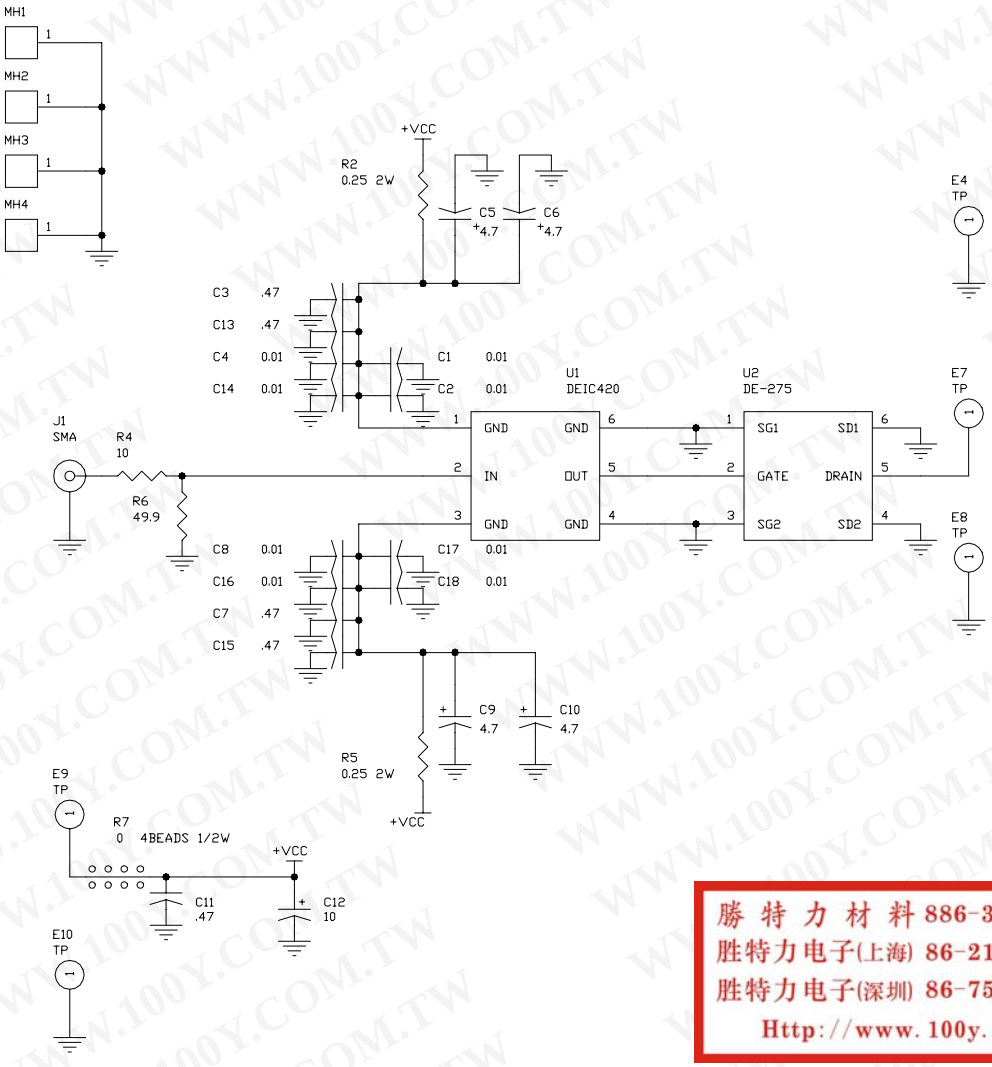


Figure 17 - High Frequency Gate Drive Circuit



APPLICATIONS INFORMATION

High Frequency Gate Drive Circuit

The circuit diagram in figure 17 is a circuit diagram for a very high switching speed, high frequency gate driver circuit using the DEIC420. This is the circuit used in the EVIC420 Evaluation Board,and is capable of driving a MOSFET at up to the maximum operating limits of the DEIC420. The circuit's very high switching speed and high frequency operation dictates the close attention to several important issues with respect to circuit design. The three key elements are circuit loop inductance, Vcc bypassing and grounding.

Circuit Loop Inductance
Referring to Figure 17, the Vcc to Vcc ground current path defines the loop which will generate the inductive term. This loop must be kept as short as possible. The output lead must be no further than 0.375 inches (9.5mm) from the gate of the MOSFET. Furthermore the output ground leads must provide a balanced symmetric coplanar ground return for optimum operation.

Vcc Bypassing
In order for the circuit to turn the MOSFET on properly, the DEIC420 must be able to draw up to 20A of current from the Vcc power supply in 2-6ns (depending upon the input capacitance of the MOSFET being driven). This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is at least two orders of magnitude larger than the load capacitance. Usually, this is achieved by placing two or three different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Care should be taken to keep the lengths of the leads between these bypass capacitors and the DEIC420 to an absolute minimum.

The bypassing should be comprised of several values of chip capacitors symmetrically placed on ether side of the IC. Recommended values are .01uF, .47uF chips and at least two 4.7uF tantalums.

Grounding
In order for the design to turn the load off properly, the DEIC420 must be able to drain this 20A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the DEIC420 and its load. Path #2 is between the DEIC420 and its power supply. Path #3 is between the DEIC420 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical.

Output Lead Inductance
Of equal importance to supply bypassing and grounding are issues related to the output lead inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible, and treated as coplanar transmission lines.

In configurations where the optimum configuration of circuit layout and bypassing cannot be used, a series resistance of a few Ohms in the gate lead may be necessary to prevent ringing.

Heat Sinking

For high power operation, the bottom side metalized substrate should be placed in compression against an appropriate heat sink. The substrate is metalized for improved heat dissipation, and is not electrically connected to the device or to ground.

See the DEI technical note "DE-Series MOSFET and IC Mounting Instructions" on the DEI web site at www.directedenergy.com/apptech.htm for detailed mounting instructions. The package dimensions of the DEIC420 are identical to those of the DE-275 MOSFET.

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