GENERAL DESCRIPTION

The XR33032/35/38 family of high performance half duplex RS-485 transceivers are optimized to operate over a wide range of supply voltage, from +2.8V to +5.5V. The analog bus pins can withstand direct shorts up to ±18V, and are protected against ESD events up to ±15kV.

In an isolated application it may be more efficient to use a remote power supply rather than generating an isolated supply at every node. The XR33032/35/38 transceivers can operate with more than 2V IR drop in the cable when utilizing a remote 5V power supply. The transceivers draw less than 600µA, and typically only 300µA when idling with the receivers active.

The receivers include full fail-safe circuitry, guaranteeing a logic-high receiver output when the receiver inputs are open, shorted, or undriven. The receiver input impedance is 96kΩ (1/8 unit load), allowing up to 256 devices on the bus while preserving the full signal margin.

The drivers are protected by short circuit detection as well as thermal shutdown, and maintain high impedance in shutdown or when powered off. The XR33032 and XR33035 drivers are slew limited for reduced EMI and error-free communication over long or unterminated data cables.

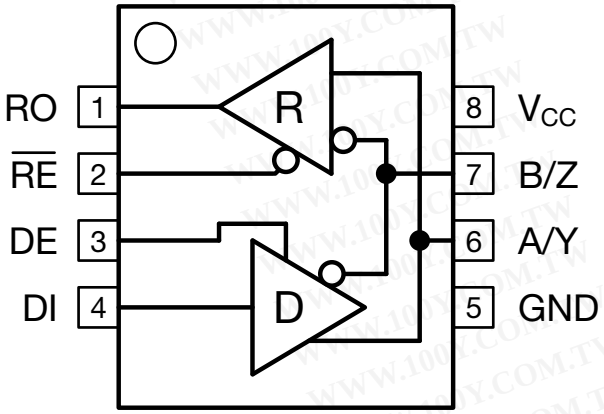
The DE and RE pins include hot swap circuitry to prevent false transitions on the bus during power-up or live insertion, and can enter a low current shutdown mode (40nA typically) for extreme power savings.

FEATURES

- **+2.8V to +5.5V Operating Range**
- **±18V Fault Tolerance** on Analog Bus pins
- Robust ESD (ElectroStatic Discharge) Protection:
  - **±15kV IEC 61000-4-2 Air Gap Discharge**
  - **± 8kV IEC 61000-4-2 Contact Discharge**
  - ±15kV Human Body Model
  - ± 4kV Human Body Model on non-bus pins
- **300µA Idle Current**, 40nA Shutdown Current
- Enhanced Receiver Fail-Safe Protection for Open, Shorted, or Terminated but Idle Data Lines
- Hot-Swap Glitch Protection on DE and $\overline{RE}$ Pins
- Driver Short Circuit Current Limit and Thermal Shutdown for Overload Protection
- 1/8th Unit Load Allows up to 256 Devices on Bus
- Industry Standard 8 NSOIC Half Duplex Package

TYPICAL APPLICATIONS

- Isolated Multipoint RS-485 Data Buses
- Remote Nodes Powered by the Host
- Building Automation and HVAC
- Industrial Process Control Networks
- Remote Utility Meter Reading
- Energy Monitoring and Control



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections to the specifications below is not implied.

V_{CC}	-0.3V to +7.0V
Input Voltage at Control and Driver Input ($\overline{RE}$, DE, and DI)	-0.3V to +7.0V
Receiver Output Voltage (RO)	-0.3V to (V_{CC} + 0.3V)
Driver Output Voltage (A and B)	±18V
Receiver Input Voltage (A and B)	±18V
Transient Voltage Pulse, through 100Ω Figure 5	±70V
Driver Output Current	±250mA
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Package Power Dissipation 8-Pin SO Θ_{JA} = 128.4°C/W 14-Pin SO Θ_{JA} = 86°C/W	Maximum Junction Temperature = +150°C

ORDERING INFORMATION

PART NUMBER	DUPLEX	DATA RATE	PACKAGE	TEMPERATURE RANGE
XR33032ID-F	Half	250kbps	8-pin Narrow SOIC	-40°C to +85°C
XR33032IDTR-F	Half	250kbps	8-pin Narrow SOIC	-40°C to +85°C
XR33035ID-F	Half	1Mbps	8-pin Narrow SOIC	-40°C to +85°C
XR33035IDTR-F	Half	1Mbps	8-pin Narrow SOIC	-40°C to +85°C
XR33038ID-F	Half	10Mbps	8-pin Narrow SOIC	-40°C to +85°C
XR33038IDTR-F	Half	10Mbps	8-pin Narrow SOIC	-40°C to +85°C

NOTE: *TR = Tape and Reel part numbers, -F = Green / RoHS Compliant*

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = +2.8V to +5.5V, T_A = -40C to +85C. Typical values are at V_{CC} = 3.3V, T_A = +25°C.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DC CHARACTERISTICS						
V_{CC}	Supply Voltage Range	2.8		5.5	V	
V_{OD}	Differential Driver Output, +3.0V ≤ V_{CC} ≤ +5.5V	2		V_{CC}	V	R_L = 100Ω (RS-422), Figure 2
		1.5		V_{CC}	V	R_L = 54Ω (RS-485), Figure 2
		1.5		V_{CC}	V	-7V ≤ V_{CM} ≤ +12V, Figure 3
V_{OD}	Differential Driver Output, +2.8V ≤ V_{CC} ≤ +3.0V	1.8		V_{CC}	V	R_L = 100Ω (RS-422), Figure 2
		1.4		V_{CC}	V	R_L = 54Ω (RS-485), Figure 2
		1.1		V_{CC}	V	-7V ≤ V_{CM} ≤ +12V, Figure 3
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	-0.2		+0.2	V	R_L = 100Ω (RS-422), or R_L = 54Ω (RS-485), Figure 2, Note 1
V_{CM}	Driver Common-Mode Output Voltage (Steady State)		V_{CC} / 2	3	V	
ΔV_{CM}	Change in Magnitude of Common-Mode Output Voltage	-0.2		+0.2	V	
V_{IH}	Logic High Threshold (DI, DE, $\overline{RE}$)	2.8			V	+4.5V ≤ V_{CC} ≤ +5.5V
		2.3			V	+4.0V ≤ V_{CC} ≤ +4.5V
		2.0			V	+2.8V ≤ V_{CC} ≤ +4.0V
V_{IL}	Logic Low Threshold (DI, DE, $\overline{RE}$)			0.8	V	
V_{HYS}	Input Hysteresis (DI, DE, $\overline{RE}$)		100		mV	
I_{IN}	Logic Input Current (DI, DE, $\overline{RE}$)	-1		+1	µA	0V ≤ V_{IN} ≤ V_{CC}, After first transition, Note 2
	Logic Input Current (DE and $\overline{RE}$)	-200	100	+200	µA	Until first transition, Note 2
$I_{A, B}$	Input Current (A and B)			125	µA	V_{OUT} = +12V, DE = 0V, V_{CC} = 0V or +5.5V
		-100			µA	V_{OUT} = -7V, DE = 0V, V_{CC} = 0V or +5.5V
I_{OL}	Output Leakage (Y and Z) Full Duplex (Note 2)			125	µA	V_{OUT} = +12V, DE = 0V, V_{CC} = 0V or +5.5V
		-100			µA	V_{OUT} = -7V, DE = 0V, V_{CC} = 0V or +5.5V
I_{OSD}	Driver Short-Circuit Output Current	-250		+250	mA	-7V ≤ V_{OUT} ≤ +12V, Figure 4

Unless otherwise noted: V_{CC} = +2.8V to +5.5V, T_A = -40C to +85C. Typical values are at V_{CC} = 3.3V, T_A = +25°C.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER THERMAL CHARACTERISTICS						
T_{TS}	Thermal Shutdown Temperature		175		°C	Junction temperature
T_{TSH}	Thermal Shutdown Hysteresis		15		°C	
RECEIVER DC CHARACTERISTICS						
V_{TH}	Receiver Differential Input Threshold Voltage (V_A - V_B)	-200	-125	-50	mV	-7V ≤ V_{CM} ≤ +12V
ΔV_{OH}	Receiver Input Hysteresis		25		mV	V_{CM} = 0V
V_{OH}	Receiver Output High Voltage (RO)	V_{CC}-0.6			V	I_{OUT} = -1mA
V_{OL}	Receiver Output Low Voltage (RO)			0.4	V	I_{OUT} = 1mA
I_{OZR}	High-Z Receiver Output Current			±1	µA	0V ≤ V_{OUT} ≤ V_{CC}
R_{IN}	Receiver Input Resistance	96			kΩ	-7V ≤ V_{CM} ≤ +12V
I_{OSC}	Receiver Output Short-Circuit Current			±120	mA	0V ≤ V_{RO} ≤ V_{CC}
SUPPLY CURRENT						
I_{CC}	Supply Current		400	600	µA	No Load, $\overline{RE}$ = 0V, DE = V_{CC} DI = 0V
			300	600	µA	No Load, $\overline{RE}$ = V_{CC}, DE = V_{CC} DI = 0V
			300	500	µA	No Load, $\overline{RE}$ = 0V, DE = 0V Receiver A and B inputs open
I_{SHDN}	Supply Current in Shutdown Mode		0.040	1	µA	$\overline{RE}$ = V_{CC}, DE = 0V
ESD PROTECTION						
	ESD Protection for A, B, Y, and Z	±15			kV	Human Body Model
		±15			kV	IEC 61000-4-2 Airgap
		±8			kV	IEC 61000-4-2 Contact
	ESD Protection for all other pins	±4			kV	Human Body Model

Unless otherwise noted: V_{CC} = +2.8V to +5.5V, T_A = -40C to +85C. Typical values are at V_{CC} = 3.3V, T_A = +25°C.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER AC CHARACTERISTICS						**XR33032 (250kbps)**
t_{DPLH}	Driver Prop. Delay (Low to High)	250		1500	ns	C_L = 50pF, R_L = 54Ω, Figure 6
t_{DPHL}	Driver Prop. Delay (High to Low)	250		1500	ns	
$\lvert t_{DPLH}-t_{DPHL}\rvert$	Differential Driver Output Skew		20	200	ns	
t_{DR}, t_{DF}	Driver Differential Output Rise or Fall Time	350		1600	ns	
	Maximum Data Rate	250			kbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{DZH}	Driver Enable to Output High		200	2500	ns	C_L = 50pF, R_L = 500Ω, Figure 7
t_{DZL}	Driver Enable to Output Low		200	2500	ns	
t_{DHZ}	Driver Disable from Output High		6	100	ns	
t_{DLZ}	Driver Disable from Output Low		6	100	ns	
$t_{DZH(SHDN)}$	Driver Enable from Shutdown to Output High			5500	ns	C_L = 50pF, R_L = 500Ω, Figure 7
$t_{DZL(SHDN)}$	Driver Enable from Shutdown to Output Low			5500	ns	
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 3
RECEIVER AC CHARACTERISTICS						**XR33032 (250kbps)**
t_{RPLH}	Receiver Prop. Delay (Low to High)			200	ns	C_L = 15pF, V_{ID} = ±2V, V_{ID} Rise and Fall times < 15ns Figure 8
t_{RPHL}	Receiver Prop. Delay (High to Low)			200	ns	
$\lvert t_{RPLH}-t_{RPHL}\rvert$	Receiver Propagation Delay Skew			30	ns	
	Maximum Data Rate	250			kbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{RZH}	Receiver Enable to Output High			50	ns	C_L = 15pF, R_L = 1kΩ, Figure 9
t_{RZL}	Receiver Enable to Output Low			50	ns	
t_{RHZ}	Receiver Disable from Output High			50	ns	
t_{RLZ}	Receiver Disable from Output Low			50	ns	
$t_{RZH(SHDN)}$	Receiver Enable from Shutdown to Output High			3500	ns	C_L = 15pF, R_L = 1kΩ, Figure 9
$t_{RZL(SHDN)}$	Receiver Enable from Shutdown to Output Low			3500	ns	
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 3

Unless otherwise noted: V_{CC} = +2.8V to +5.5V, T_A = -40C to +85C. Typical values are at V_{CC} = 3.3V, T_A = +25°C.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER AC CHARACTERISTICS						**XR33035 (1Mbps)**
t_{DPLH}	Driver Prop. Delay (Low to High)		150	300	ns	C_L = 50pF, R_L = 54Ω, Figure 6
t_{DPHL}	Driver Prop. Delay (High to Low)		150	300	ns	
$\lvert t_{DPLH}-t_{DPHL}\rvert$	Differential Driver Output Skew		5	50	ns	
t_{DR}, t_{DF}	Driver Differential Output Rise or Fall Time	100	200	350	ns	
	Maximum Data Rate	1			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{DZH}	Driver Enable to Output High		1000	2500	ns	C_L = 50pF, R_L = 500Ω, Figure 7
t_{DZL}	Driver Enable to Output Low		1000	2500	ns	
t_{DHZ}	Driver Disable from Output High		60	100	ns	
t_{DLZ}	Driver Disable from Output Low		60	100	ns	
$t_{DZH(SHDN)}$	Driver Enable from Shutdown to Output High			3500	ns	C_L = 50pF, R_L = 500Ω, Figure 7
$t_{DZL(SHDN)}$	Driver Enable from Shutdown to Output Low			3500	ns	
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 3
RECEIVER AC CHARACTERISTICS						**XR33035 (1Mbps)**
t_{RPLH}	Receiver Prop. Delay (Low to High)			200	ns	C_L = 15pF, V_{ID} = ±2V, V_{ID} Rise and Fall times < 15ns Figure 8
t_{RPHL}	Receiver Prop. Delay (High to Low)			200	ns	
$\lvert t_{RPLH}-t_{RPHL}\rvert$	Receiver Propagation Delay Skew			30	ns	
	Maximum Data Rate	1			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{RZH}	Receiver Enable to Output High			50	ns	C_L = 15pF, R_L = 1kΩ, Figure 9
t_{RZL}	Receiver Enable to Output Low			50	ns	
t_{RHZ}	Receiver Disable from Output High			50	ns	
t_{RLZ}	Receiver Disable from Output Low			50	ns	
$t_{RZH(SHDN)}$	Receiver Enable from Shutdown to Output High			3500	ns	C_L = 15pF, R_L = 1kΩ, Figure 9
$t_{RZL(SHDN)}$	Receiver Enable from Shutdown to Output Low			3500	ns	
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 3

Unless otherwise noted: V_{CC} = +2.8V to +5.5V, T_A = -40C to +85C. Typical values are at V_{CC} = 3.3V, T_A = +25°C.

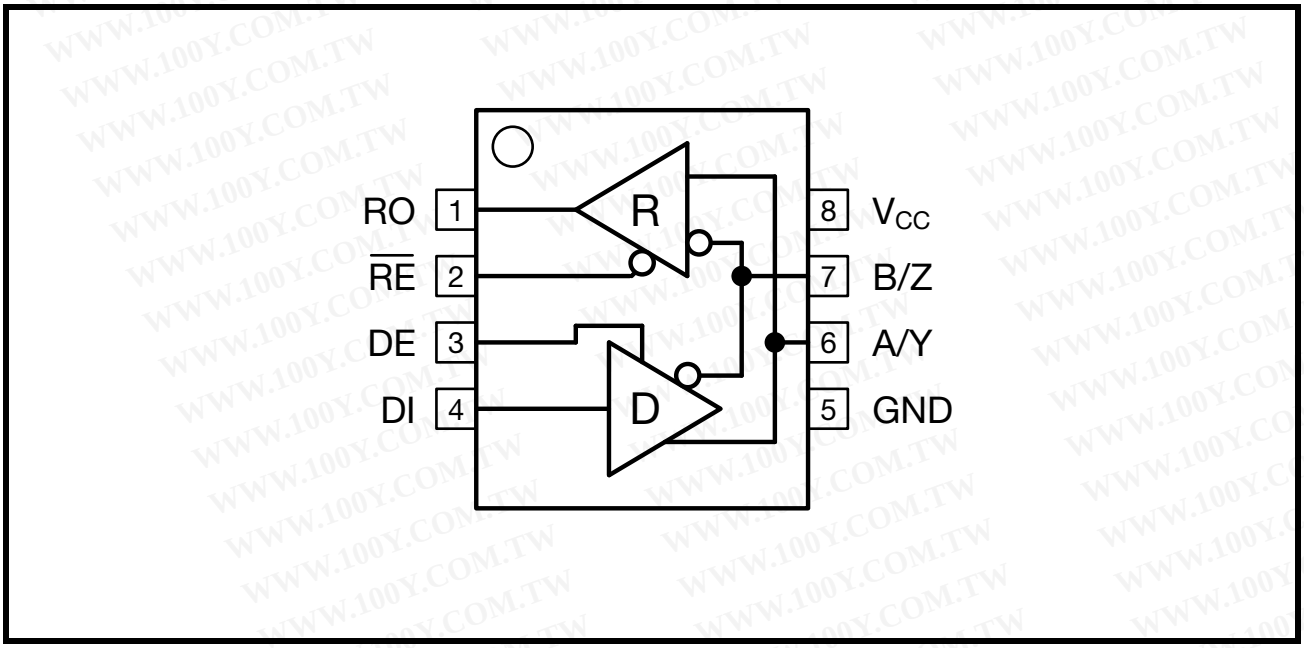
SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER AC CHARACTERISTICS						**XR33038 (10Mbps)**
t_{DPLH}	Driver Prop. Delay (Low to High)			30	ns	C_L = 50pF, R_L = 54Ω, Figure 6
t_{DPHL}	Driver Prop. Delay (High to Low)			30	ns	
$\lvert t_{DPLH}-t_{DPHL}\rvert$	Differential Driver Output Skew			5	ns	
t_{DR}, t_{DF}	Driver Differential Output Rise or Fall Time			25	ns	
	Maximum Data Rate	10			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{DZH}	Driver Enable to Output High			50	ns	C_L = 50pF, R_L = 500Ω, Figure 7
t_{DZL}	Driver Enable to Output Low			50	ns	
t_{DHZ}	Driver Disable from Output High			50	ns	
t_{DLZ}	Driver Disable from Output Low			50	ns	
$t_{DZH(SHDN)}$	Driver Enable from Shutdown to Output High			250	ns	C_L = 50pF, R_L = 500Ω, Figure 7
$t_{DZL(SHDN)}$	Driver Enable from Shutdown to Output Low			250	ns	
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 3
RECEIVER AC CHARACTERISTICS						**XR33038 (10Mbps)**
t_{RPLH}	Receiver Prop. Delay (Low to High)			50	ns	C_L = 15pF, V_{ID} = ±2V, V_{ID} Rise and Fall times < 15ns Figure 8
t_{RPHL}	Receiver Prop. Delay (High to Low)			50	ns	
$\lvert t_{RPLH}-t_{RPHL}\rvert$	Receiver Propagation Delay Skew			5	ns	
	Maximum Data Rate	10			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{RZH}	Receiver Enable to Output High			50	ns	C_L = 15pF, R_L = 1kΩ, Figure 9
t_{RZL}	Receiver Enable to Output Low			50	ns	
t_{RHZ}	Receiver Disable from Output High			50	ns	
t_{RLZ}	Receiver Disable from Output Low			50	ns	
$t_{RZH(SHDN)}$	Receiver Enable from Shutdown to Output High			2200	ns	C_L = 15pF, R_L = 1kΩ, Figure 9
$t_{RZL(SHDN)}$	Receiver Enable from Shutdown to Output Low			2200	ns	
t_{SHDN}	Time to Shutdown	50	200	600	ns	Notes 3

NOTE:

1. *Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.*
2. *The hot swap feature disables the DE and $\overline{RE}$ inputs for the first 10µs after power is applied. Following this time period these inputs are weakly pulled to their disabled state (low for DE, high for $\overline{RE}$) until the first transition, after which they become high impedance inputs.*
3. *The transceivers are put into shutdown by bringing $\overline{RE}$ High and DE Low simultaneously for at least 600ns. If the control inputs are in this state for less than 50ns, the device is guaranteed to not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. Note that the receiver and driver enable times increase significantly when coming out of shutdown.*

BLOCK DIAGRAMS

FIGURE 1. HALF DUPLEX 8 NSOIC



TEST FIGURES

FIGURE 2. DIFFERENTIAL DRIVER OUTPUT VOLTAGE

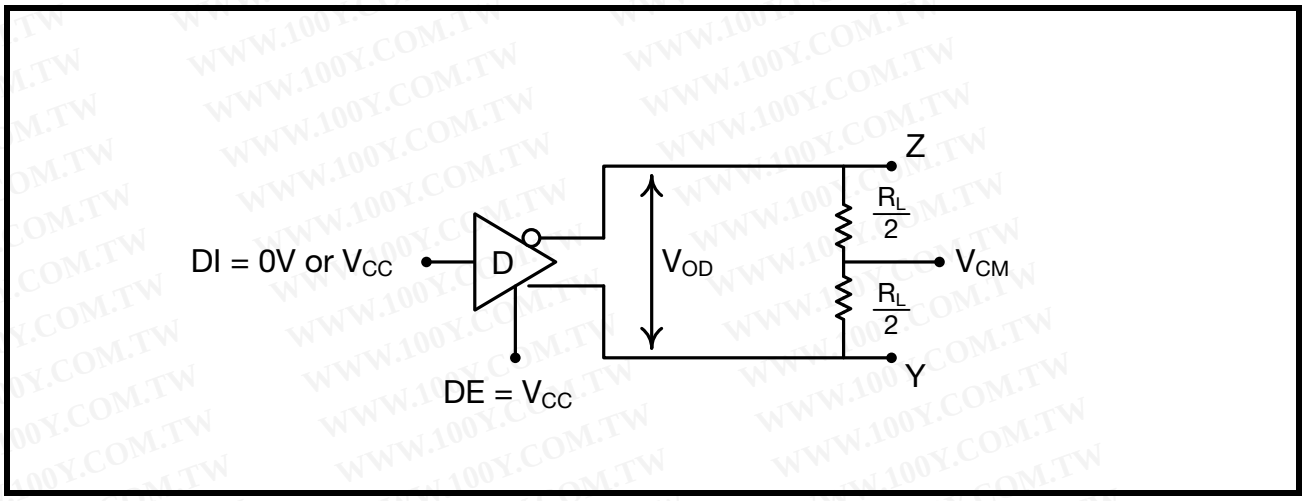


FIGURE 3. DIFFERENTIAL DRIVER OUTPUT VOLTAGE OVER COMMON MODE

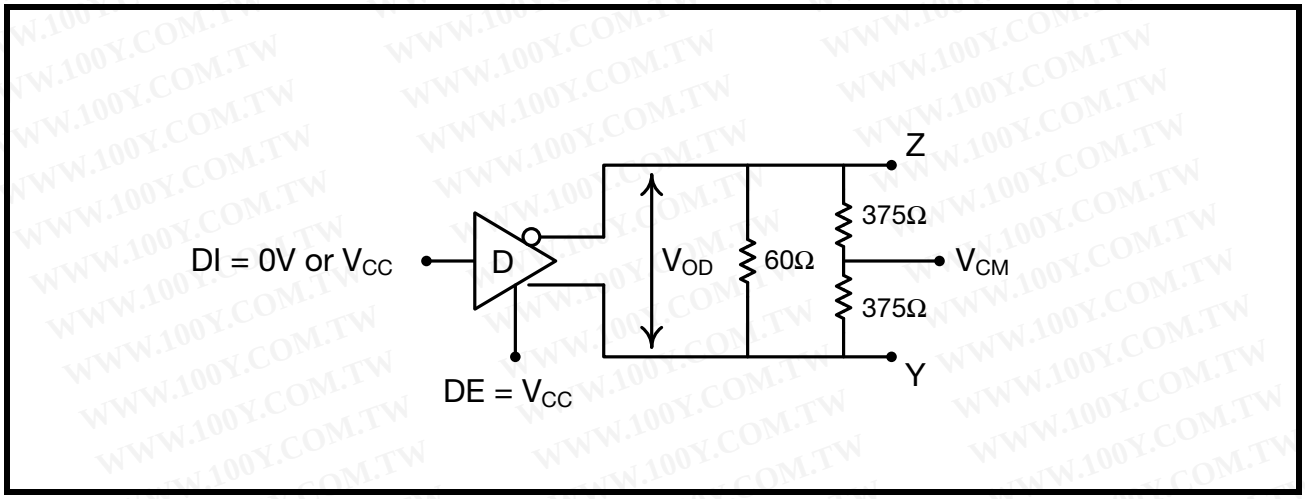


FIGURE 4. DRIVER OUTPUT SHORT CIRCUIT CURRENT

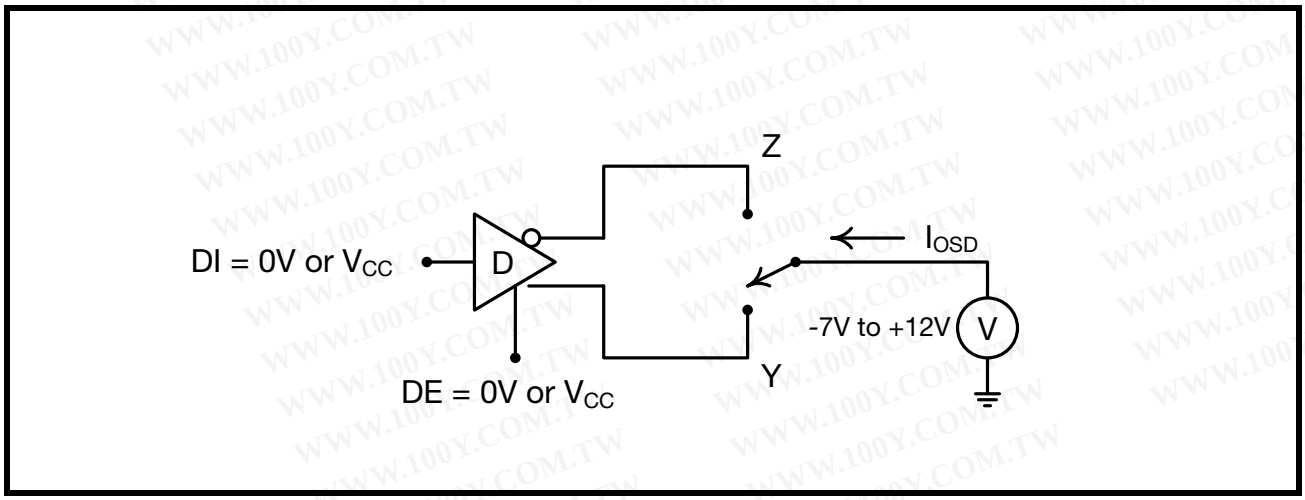


FIGURE 5. TRANSIENT OVER-VOLTAGE TEST CIRCUIT

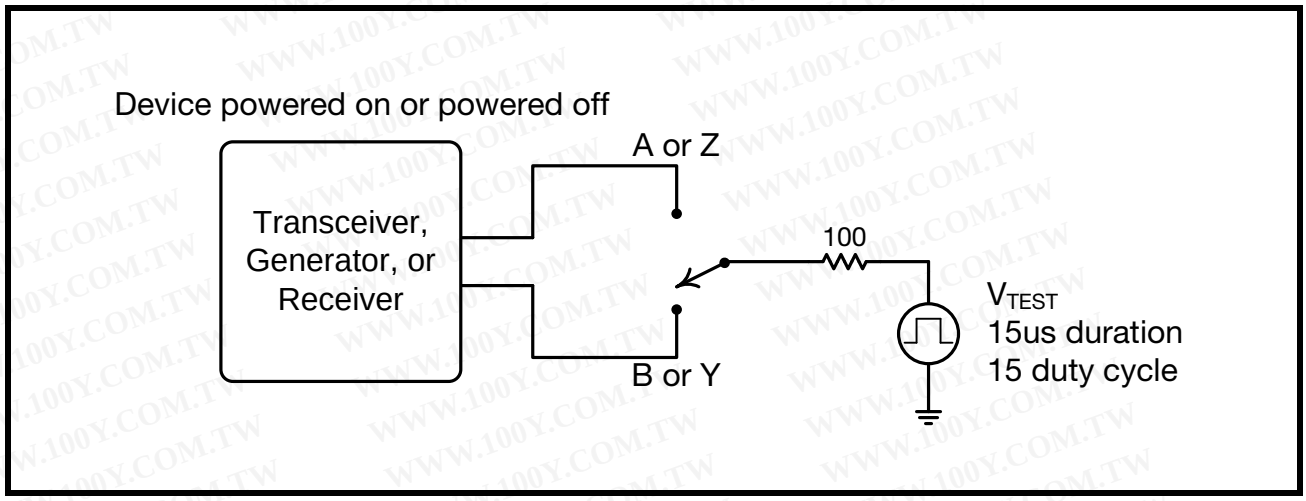


FIGURE 6. DRIVER PROPAGATION DELAY TEST CIRCUIT & TIMING DIAGRAM

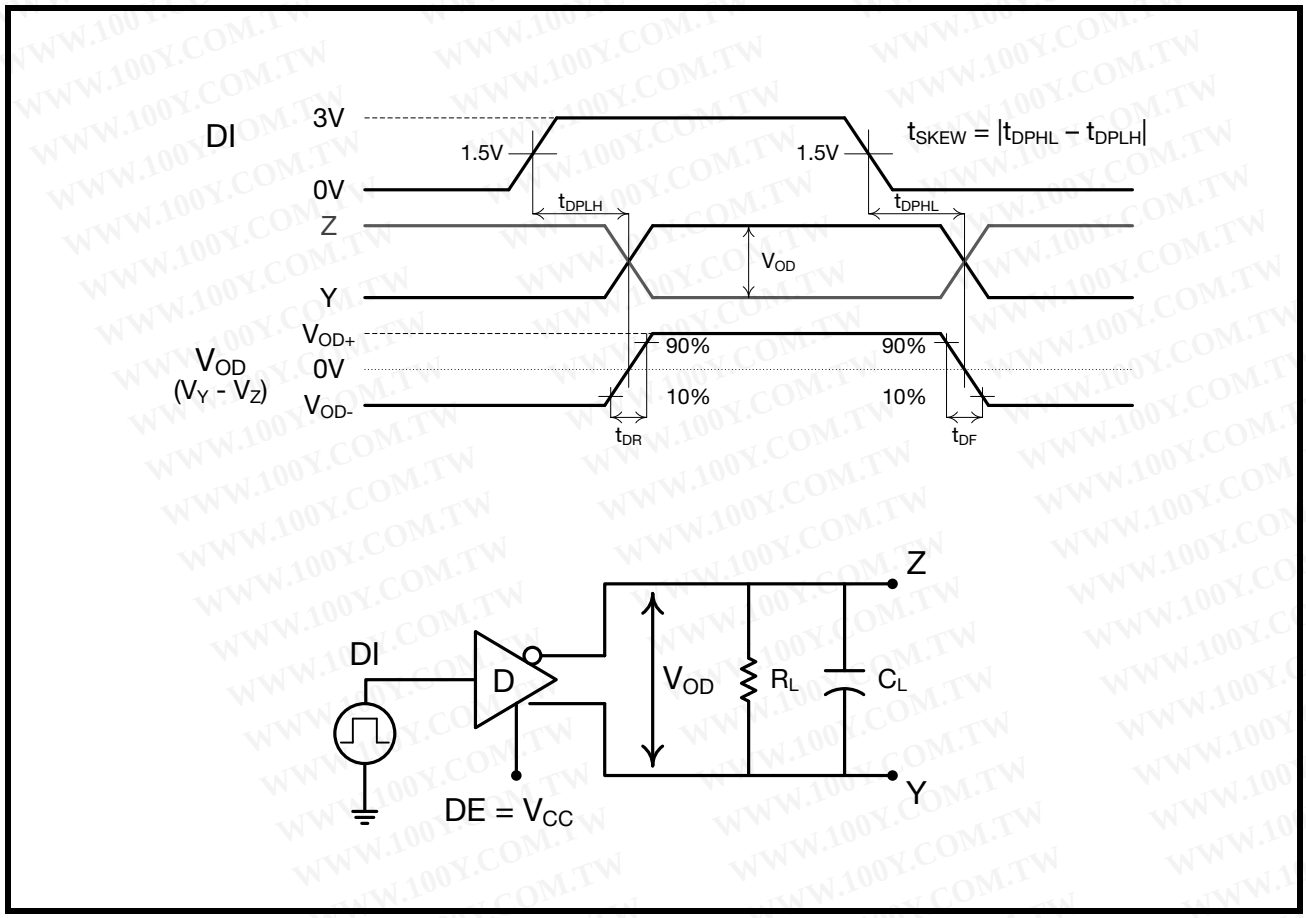


FIGURE 7. DRIVER ENABLE AND DISABLE TIMING TEST CIRCUITS & TIMING DIAGRAMS

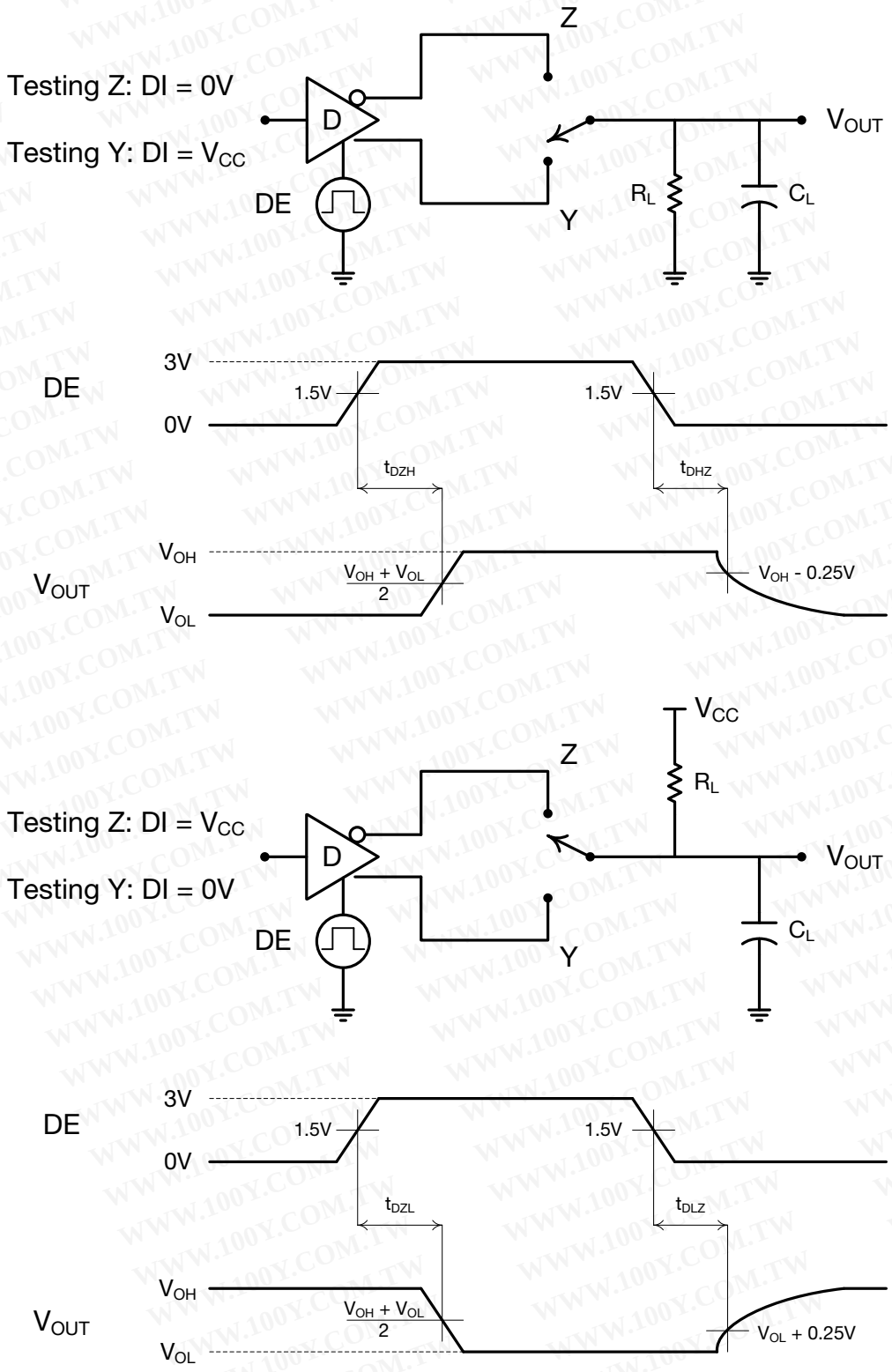


FIGURE 8. RECEIVER PROPAGATION DELAY TEST CIRCUIT & TIMING DIAGRAM

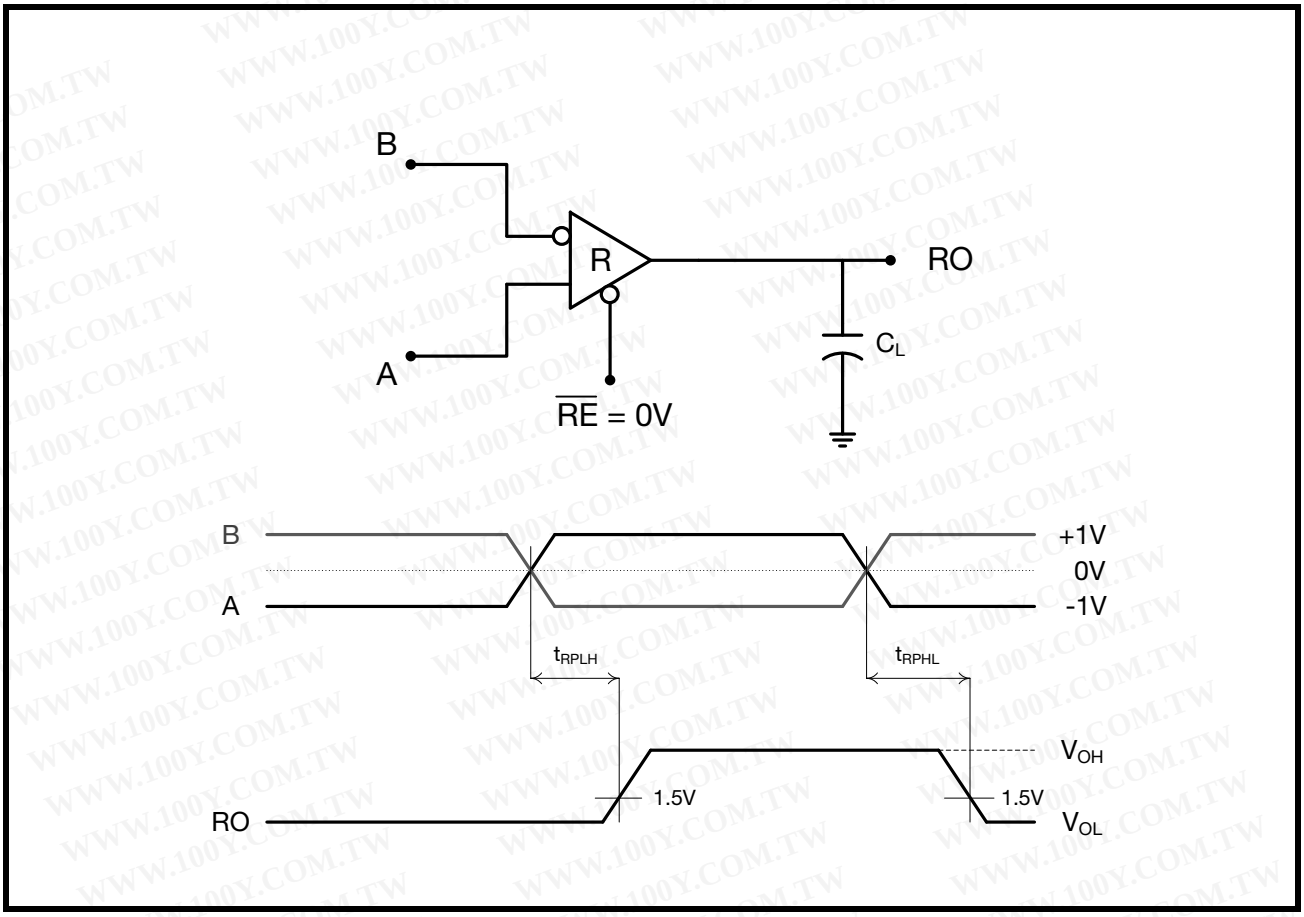
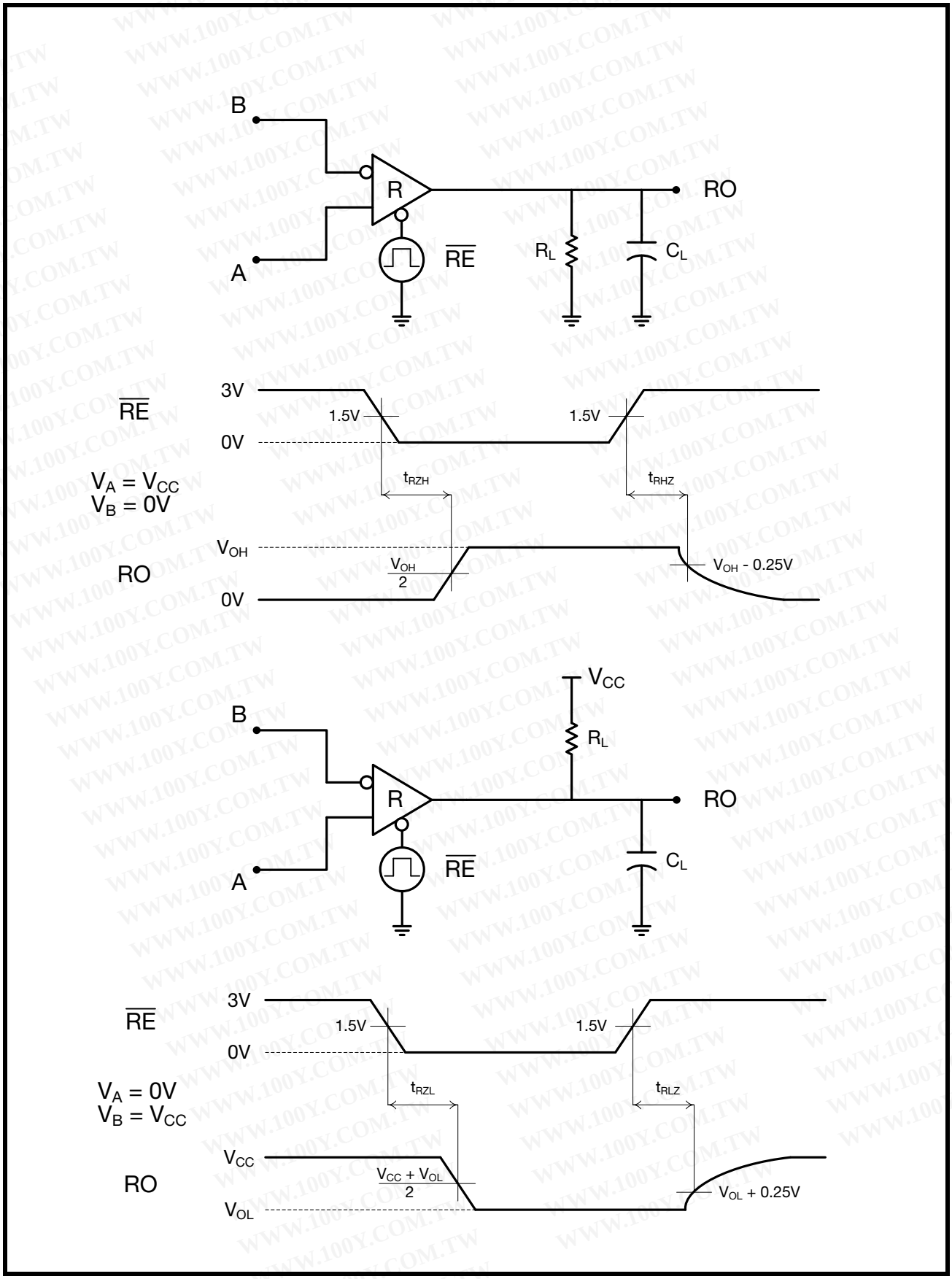


FIGURE 9. RECEIVER ENABLE AND DISABLE TEST CIRCUITS & TIMING DIAGRAMS



PIN DESCRIPTIONS

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	RO	Out	Receiver Output. When $\overline{RE}$ is low and if (A-B) ≥ -50mV, RO is high. If (A-B) ≤ -200mV, RO is Low.
2	$\overline{RE}$	In	Receiver Output Enable (Hot Swap). When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is High, RO is high impedance. When $\overline{RE}$ is high and DE is low, shutdown mode is enabled.
3	DE	In	Driver Output Enable (Hot Swap). When DE is high, outputs are enabled. When DE is low, outputs are high impedance. When DE is low and $\overline{RE}$ is high, shutdown mode is enabled.
4	DI	In	Driver Input. With DE high, a low level on DI forces non-Inverting output low and inverting output high. Similarly, a high level on DI forces non-Inverting output high and inverting output low.
5	GND	Pwr	Ground.
6	A	I/O	Non-Inverting Receiver Input and Non-Inverting Driver Output.
7	B	I/O	Inverting Receiver Input and Inverting Driver Output.
8	V_{CC}	Pwr	Power Supply Input. Bypass to ground with 0.1 µF capacitor.

PRODUCT DESCRIPTION

The XR33032/35/38 RS-485/422 devices are part of Exar's high performance serial interface product line. The analog bus pins can survive direct shorts up to ±18V, and are protected against ESD events up to ±15kV.

ENHANCED FAILSAFE

Standard RS-485 differential receivers will be in an indeterminate state whenever the analog bus pins are not being driven. The enhanced failsafe feature of the XR33032/35/38 family guarantees a logic-high receiver output when the receiver inputs are open, shorted, or when they are connected to a terminated transmission line with all drivers disabled. In a terminated bus with all transmitters disabled, the receivers' differential input voltage is pulled to 0V by the termination. The XR33032/35/38 family interprets 0V differential as a logic high with a minimum 50mV noise margin while maintaining compliance with the EIA/TIA-485 standard of ±200mV. Although the XR33032/35/38 family does not need failsafe biasing resistors, it can operate without issue if biasing is used.

RECEIVER INPUT FILTERING

XR33032 and XR33035 receivers incorporate internal filtering in addition to input hysteresis. This filtering enhances noise immunity by ignoring signals that do not meet a minimum pulse width of 30ns. Receiver propagation delay increases slightly due to this filtering. The high speed XR33038 device does not have this input filtering.

HOT-SWAP CAPABILITY

When V_{CC} is first applied the driver enable and receiver enable (DE and $\overline{RE}$) are held inactive for approximately 10 microseconds. During power ramp-up other system ICs may drive unpredictable values, or tristated lines may be influenced by stray capacitance. The hot-swap feature prevents these devices from driving any output signal until power has stabilized. After the initial 10µs, the driver and receiver enable pins are weakly pulled to their disabled states (low for DE, high for $\overline{RE}$) until the first transition. After the first transition, the DE and $\overline{RE}$ pins operate as high impedance inputs.

If circuit boards are inserted into an energized backplane (commonly called "live insertion" or "hot-swap") power may suddenly be applied to all circuits. Without the hot-swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared busses and possibly causing driver contention or device damage.

DRIVER OUTPUT PROTECTION

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

LINE LENGTH and TERMINATIONS

The RS-485/RS-422 standard covers line lengths up to 4000ft. Maximum achievable line length is a function of the data rate, cable characteristics and environmental noise. Termination prevents signal reflections by eliminating the impedance mismatches on a transmission line. Line termination is generally used if rise and fall times are shorter than the round-trip signal propagation time. Higher supply voltage will allow longer cables to be used.

±15kV ESD PROTECTION

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling, assembly and operation. The driver outputs and receiver inputs of the XR33032/35/38 have extra protection against static electricity. Exar uses state of the art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown and powered down. After an ESD event, the XR33032/35/38 keep operating without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the XR33032/35/38 are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ± 8kV Contact Discharge Model
- ±15kV Air-gap Discharge Model

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The XR33032/35/38 family helps you design equipment to meet IEC 61000-4-2, without sacrificing board-space and cost for external ESD-protection components.

The major differences between tests done using the Human body model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that of human body model.

The air-gap test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized.

256 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12k Ohms (1 unit load). A standard driver can drive up to 32 unit loads. The XR33032/35/38 transceivers have a $1/8^{th}$ unit load receiver input impedance of 96kΩ, allowing up to 256 transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS-485 transceivers up to a total of 32 unit loads may be connected to the line.

LOW POWER SHUTDOWN MODE

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low simultaneously. While in shutdown devices draw less than 1µA of supply current. DE and $\overline{RE}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts will enter shutdown.

Enable times t_{ZH} and t_{ZL} apply when the part is not in low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ apply when the parts are shutdown. The drivers and receivers take longer to become enabled from low-power shutdown $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ than from driver / receiver disable mode (t_{ZH} and t_{ZL}).

FUNCTION TABLES

TABLE 1: HALF DUPLEX 8 PIN

TRANSMITTING				
Inputs			Outputs	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

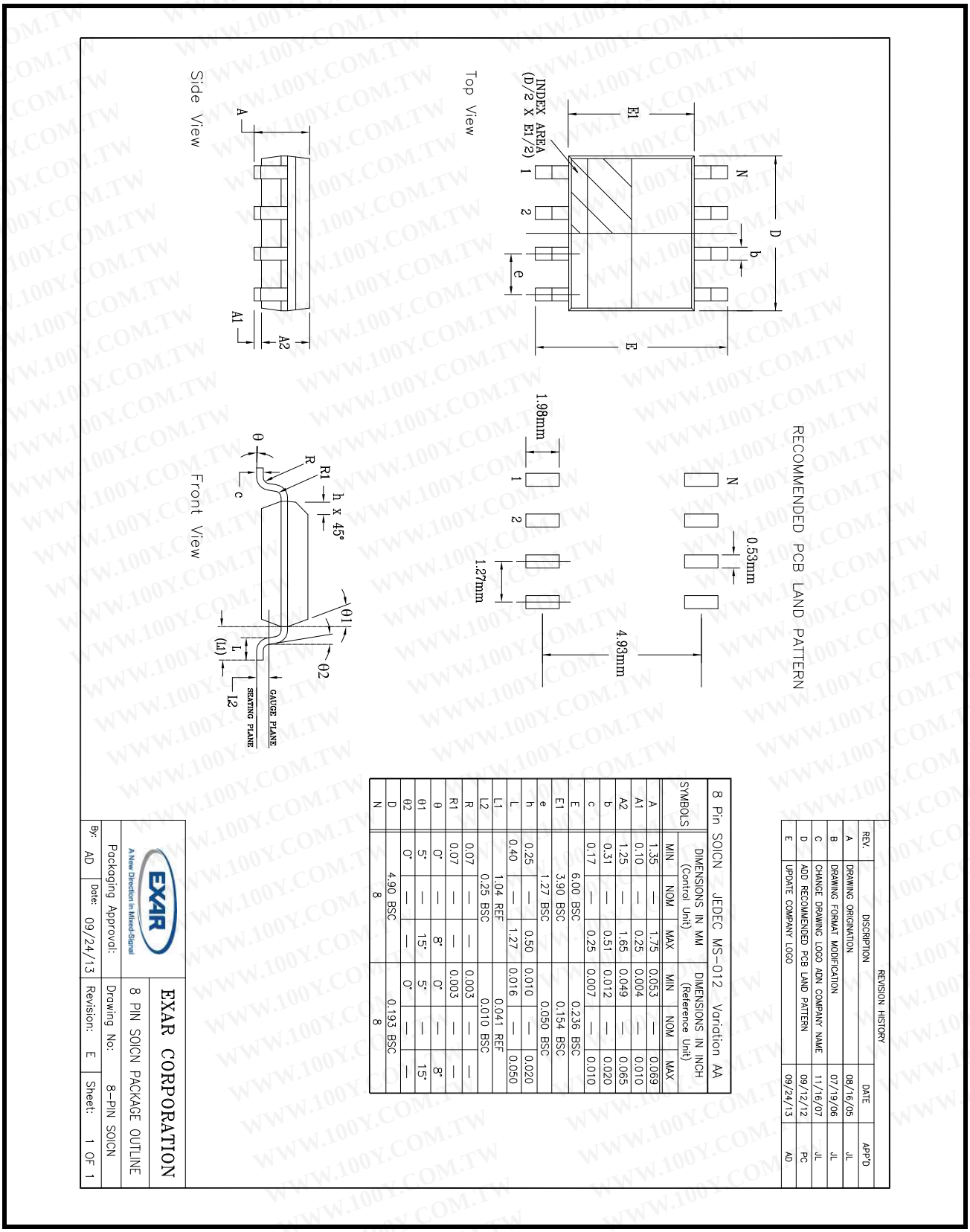
TABLE 2: HALF DUPLEX 8 PIN

RECEIVING			
Inputs			Output
$\overline{RE}$	DE	V_A - V_B	RO
0	X	≥ -50mV	1
0	X	≤ -200mV	0
0	X	Open/Shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Note: Receiver inputs -200mV ≤ V_A - V_B ≤ -50mV are considered indeterminate.

PACKAGE DRAWINGS

FIGURE 10. 8 NSOIC



REVISION HISTORY

REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO ADN COMPANY NAME	11/16/07	JL
D	ADD RECOMMENDED PCB LAND PATTERN	09/12/12	PC
E	UPDATE COMPANY LOGO	09/24/13	AD

8 Pin SOICN JEDEC MS-012 Variation AA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E		6.00 BSC			0.236 BSC	
E1		3.90 BSC			0.154 BSC	
e		1.27 BSC			0.050 BSC	
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1		1.04 REF			0.041 REF	
L2		0.25 BSC			0.010 BSC	
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	15°	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		

EXAR CORPORATION

8 PIN SOICN PACKAGE OUTLINE

Packaging Approval:	Drawing No: 8-PIN SOICN		
By: AD	Date: 09/24/13	Revision: E	Sheet: 1 OF 1

REVISION HISTORY

DATE	REVISION	DESCRIPTION
February 2014	1.0.0	Initial release [ECN 1411-03]

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Datasheet February 2014.

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