Single-Supply, Differential 18-Bit ADC Driver

ADA4941-1

FEATURES

- Single-ended-to-differential converter
- Excellent linearity
  - Distortion −110 dBc @100 KHz for V_O, dm = 2 V p-p
- Low noise: 10.2 nV/√Hz, output-referred, G = 2
- Extremely low power: 2.2 mA (3 V supply)
- High input impedance: 24 MΩ
- User-adjustable gain
- High speed: 31 MHz, −3 dB bandwidth (G = +2)
- Fast settling time: 300 ns to 0.005% for a 2 V step
- Low offset: 0.8 mV max, output-referred, G = 2
- Rail-to-rail output
- Disable feature
- Wide supply voltage range: 2.7 V to 12 V
- Available in space-saving, 3 mm × 3 mm LFCSP

APPLICATIONS

- Single-supply data acquisition systems
- Instrumentation
- Process control
- Battery-power systems
- Medical instrumentation

FUNCTIONAL BLOCK DIAGRAM

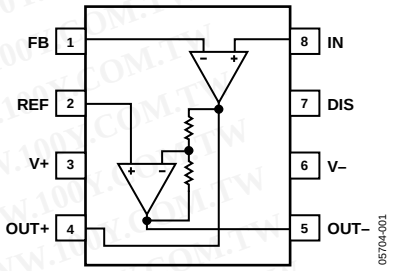

Figure 1.SOIC/LSCSP Pinout

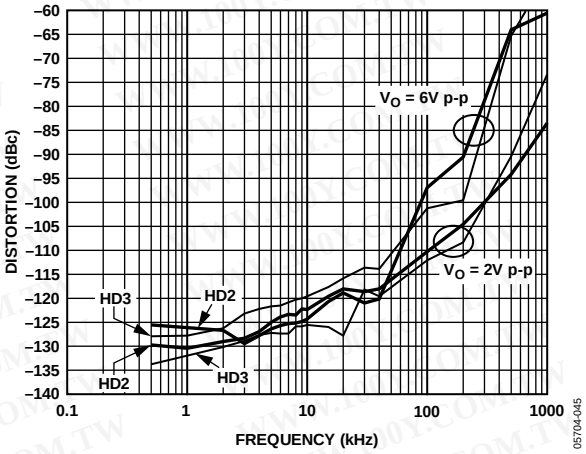

Figure 2. Distortion vs. Frequency at Various Output Amplitudes

GENERAL DESCRIPTION

The ADA4941-1 is a low power, low noise differential driver for ADCs up to 18 bits in systems that are sensitive to power. The ADA4941-1 is configured in an easy-to-use, single-ended-to-differential configuration and requires no external components for a gain of 2 configuration. A resistive feedback network can be added to achieve gains greater than 2. The ADA4941-1 provides essential benefits, such as low distortion and high SNR, that are required for driving high resolution ADCs.

With a wide input voltage range (0 V to 3.9 V on a single 5 V supply), rail-to-rail output, high input impedance, and a user-adjustable gain, the ADA4941-1 is designed to drive single-supply ADCs with differential inputs found in a variety of low power applications, including battery-operated devices and single-supply data acquisition systems.

The ADA4941-1 is ideal for driving the 16-bit and 18-bit PulSAR® ADCs such as the AD7687, AD7690, and AD7691.

The ADA4941-1 is manufactured on ADI's proprietary second-generation XFCB process, which enables the amplifier to achieve 18-bit performance on low supply currents.

The ADA4941-1 is available in a small 8-lead LFCSP as well as a standard 8-lead SOIC and is rated to work over the extended industrial temperature range, −40°C to +125°C.

Rev. B

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REVISION HISTORY

8/10—Rev. A to Rev. B

Added Caption to Figure 1 ... 1
Added Exposed Pad Notation to Figure 4 and Table 6 ... 7
Added Exposed Pad Notation to Outline Dimensions ... 23
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3/09—Rev. 0 to Rev. A

Change to Gain Error Drift Parameter, Table 1 ... 3
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Change to Gain Error Drift Parameter, Table 3 ... 5
Updated Outline Dimensions ... 23

4/06—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 3 V, OUT+ connected to FB (G = 2), $R_{L, dm}$ = 1 kΩ, REF = 1.5 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.1 V p-p	21	30		MHz
	V_O = 2.0 V p-p	4.6	6.5		MHz
Overdrive Recovery Time	+Recover/−Recovery		320/650		ns
Slew Rate	V_O = 2 V step		22		V/µs
Settling Time 0.005%	V_O = 2 V p-p step		300		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	f_C = 40 kHz, V_O = 2 V p-p, HD2/HD3		−116/−112		dBc
	f_C = 100 kHz, V_O = 2 V p-p, HD2/HD3		−101/−98		dBc
	f_C = 1 MHz, V_O = 2 V p-p, HD2/HD3		−75/−71		dBc
RTO Voltage Noise	f = 100 kHz		10.2		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
DC PERFORMANCE					
Differential Output Offset Voltage			0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		µV/°C
Single-Ended Input Offset Voltage	Amp A1 or Amp A2		0.1	0.4	mV
Single-Ended Input Offset Voltage Drift			0.3		µV/°C
Input Bias Current	IN and REF		3	4.5	µA
Input Offset Current	IN and REF		0.1		µA
Gain	(+OUT − −OUT)/(IN − REF)	1.98	2.00	2.01	V/V
Gain Error		−1		+1	%
Gain Error Drift			1	5	ppm
INPUT CHARACTERISTICS					
Input Resistance	IN and REF		24		MΩ
Input Capacitance	IN and REF		1.4		pF
Input Common-Mode Voltage Range		0.2		1.9	V
Common-Mode Rejection Ratio (CMRR)	CMRR = $V_{OS, dm}/V_{CM}$, VREF = VIN, V_{CM} = 0.2 V to 1.9 V, G = 4	81	105		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, G = 4	±2.90	±2.95		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, V_O, dm = 200 mV p-p		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.2	2.4	mA
Quiescent Current—Disable			10	16	µA
Power Supply Rejection Ratio (PSRR)					
+PSRR	PSRR = $V_{OS, dm}/\Delta V_S$, G = 4	86	100		dB
−PSRR		86	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = High		≥1.5		V
	Enabled, DIS = Low		≤1.0		V
DIS Input Current	Disabled, DIS = High		5.5	8	µA
	Enabled, DIS = Low		4	6	µA
Turn-On Time			0.7		µs
Turn-Off Time			30		µs

T_A = 25°C, V_S = 5 V, OUT+ connected to FB (G = 2), $R_{L, dm}$ = 1 kΩ, REF = 2.5 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.1 V p-p	22	31		MHz
	V_O = 2.0 V p-p	4.9	7		MHz
Overdrive Recovery Time	+Recover/−Recovery		200/600		ns
Slew Rate	V_O = 2 V step		24.5		V/µs
Settling Time 0.005%	V_O = 6 V p-p step		610		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	f_C = 40 kHz, V_O = 2 V p-p, HD2/HD3		−118/−119		dBc
	f_C = 100 kHz, V_O = 2 V p-p, HD2/HD3		−110/−112		dBc
	f_C = 1 MHz, V_O = 2 V p-p, HD2/HD3		−83/−73		dBc
RTO Voltage Noise	f = 100 kHz		10.2		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
DC PERFORMANCE					
Differential Output Offset Voltage			0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		µV/°C
Single-Ended Input Offset Voltage	Amp A1 or Amp A2		0.1	0.4	mV
Single-Ended Input Offset Voltage Drift			0.3		µV/°C
Input Bias Current	IN and REF		3	4.5	µA
Input Offset Current	IN and REF		0.1		µA
Gain	(+OUT − −OUT)/(IN − REF)	1.98	2	2.01	V/V
Gain Error		−1		+1	%
Gain Error Drift			1	5	ppm
INPUT CHARACTERISTICS					
Input Resistance	IN and REF		24		MΩ
Input Capacitance	IN and REF		1.4		pF
Input Common-Mode Voltage Range		0.2		3.9	V
Common-Mode Rejection Ratio (CMRR)	CMRR = $V_{OS, dm}/V_{CM}$, VREF = VIN, V_{CM} = 0.2 V to 3.9 V, G = 4	84	106		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, G = 4	±4.85	±4.93		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, V_O, dm = 200 mV p-p		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.3	2.6	mA
Quiescent Current—Disable			12	20	µA
Power Supply Rejection Ratio (PSRR)					
+PSRR	PSRR = $V_{OS, dm}/\Delta V_S$, G = 4	87	100		dB
−PSRR		87	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = High		≥1.5		V
	Enabled, DIS = Low		≤1.0		V
DIS Input Current	Disabled, DIS = High		5.5	8	µA
	Enabled, DIS = Low		4	6	µA
Turn-On Time			0.7		µs
Turn-Off Time			30		µs

T_A = 25°C, V_S = ±5 V, OUT+ connected to FB (G = 2), $R_{L, dm}$ = 1 kΩ, REF = 0 V, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.1 V p-p	23	32		MHz
	V_O = 2.0 V p-p	5.2	7.5		MHz
Overdrive Recovery Time	+Recover/−Recovery		200/650		ns
Slew Rate	V_O = 2 V step		26		V/µs
Settling Time 0.005%	V_O = 12 V p-p step		980		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	f_C = 40 kHz, V_O = 2 V p-p, HD2/HD3		−118/−119		dBc
	f_C = 100 kHz, V_O = 2 V p-p, HD2/HD3		−109/−112		dBc
	f_C = 1 MHz, V_O = 2 V p-p, HD2/HD3		−84/−75		dBc
RTO Voltage Noise	f = 100 kHz		10.2		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
DC PERFORMANCE					
Differential Output Offset Voltage			0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		µV/°C
Single-Ended Input Offset Voltage	Amp A1 or Amp A2		0.1	0.4	mV
Single-Ended Input Offset Voltage Drift			0.3		µV/°C
Input Bias Current	IN and REF		3	4.5	µA
Input Offset Current	IN and REF		0.1		µA
Gain	(+OUT − −OUT)/(IN − REF)	1.98	2	2.01	V/V
Gain Error		−1		+1	%
Gain Error Drift			1	5	ppm
INPUT CHARACTERISTICS					
Input Resistance	IN and REF		24		MΩ
Input Capacitance	IN and REF		1.4		pF
Input Common-Mode Voltage Range		−4.8		+3.9	V
Common-Mode Rejection Ratio (CMRR)	CMRR = $V_{OS, dm}/V_{CM}$, VREF = VIN, V_{CM} = −4.8 V to +3.9 V, G = 4	85	105		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, G = 4	V_S − 0.25	V_S ± 0.14		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, V_O, dm = 200 mV p-p		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.5	2.7	mA
Quiescent Current—Disable			15	26	µA
Power Supply Rejection Ratio (PSRR)					
+PSRR	PSRR = $V_{OS, dm}/\Delta V_S$, G = 4	87	100		dB
−PSRR		87	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = High		≥ −3		V
	Enabled, DIS = Low		≤ −4		V
DIS Input Current	Disabled, DIS = High		7	10	µA
	Enabled, DIS = Low		4	6	µA
Turn-On Time			0.7		µs
Turn-Off Time			30		µs

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12 V
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad (if applicable) on the PCB surface that is thermally connected to a copper plane, with zero airflow.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC on 4-Layer Board	126	28	°C/W
8-Lead LFCSP with EP on 4-Layer Board	83	19	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4941-1 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4941-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipation due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane to achieve the specified θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the packages vs. the ambient temperature for the 8-lead SOIC (126°C/W) and for the 8-lead LFCSP (83°C/W) on a JEDEC standard 4-layer board. The LFCSP must have its underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

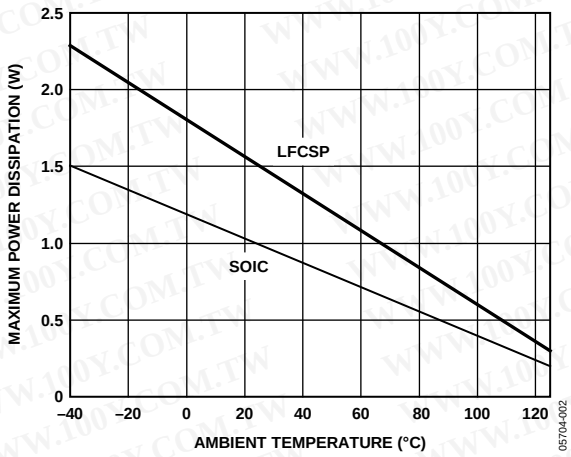
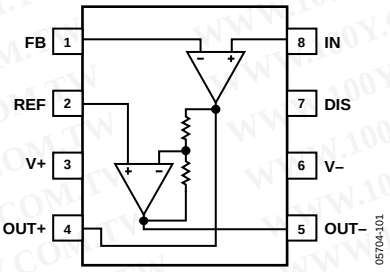


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS NOT ELECTRICALLY CONNECTED TO THE DEVICE. IT IS TYPICALLY SOLDERED TO GROUND OR A POWER PLANE ON THE PCB THAT IS THERMALLY CONDUCTIVE.

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB	Feedback Input
2	REF	Reference Input
3	V+	Positive Power Supply
4	OUT+	Noninverting Output
5	OUT–	Inverting Output
6	V–	Negative Power Supply
7	DIS	Disable
8	IN	Input
EP (For LFCSP Only)		Exposed Paddle. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the PCB that is thermally conductive.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, V_S = 5 V, $R_{L, dm}$ = 1 kΩ, REF = 2.5 V, DIS = LOW, OUT+ directly connected to FB (G = 2), T_A = 25°C.

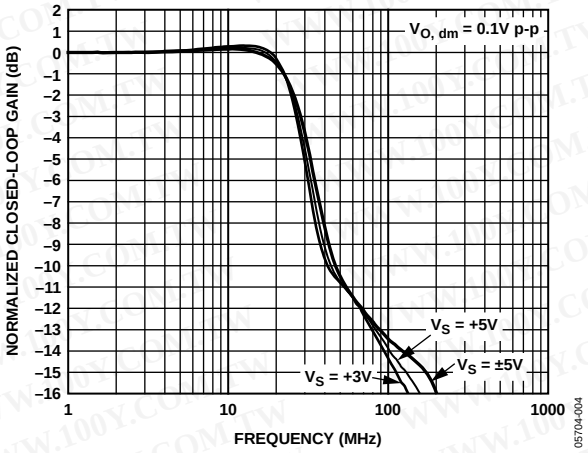


Figure 5. Small Signal Frequency Response for Various Power Supplies

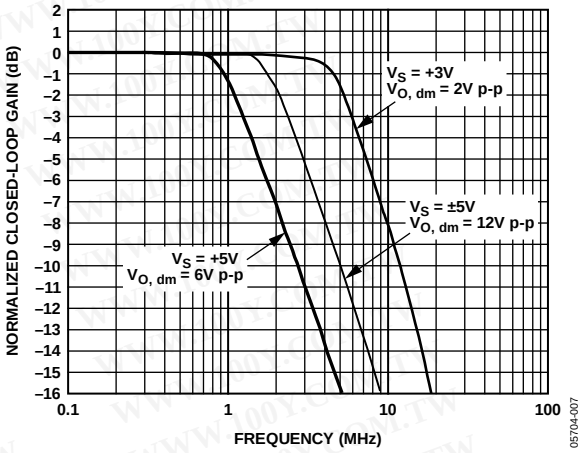


Figure 8. Large Signal Frequency Response for Various Power Supplies

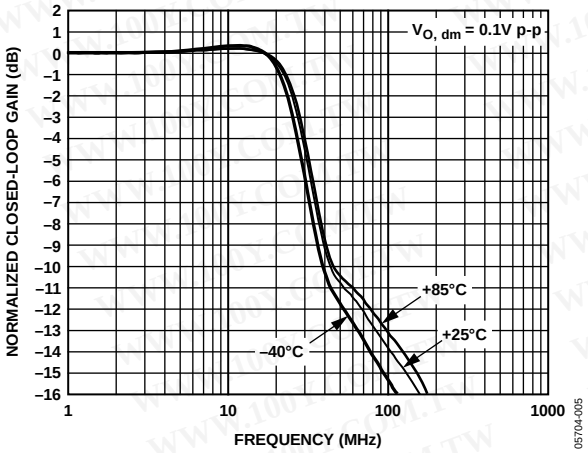


Figure 6. Small Signal Frequency Response at Various Temperatures

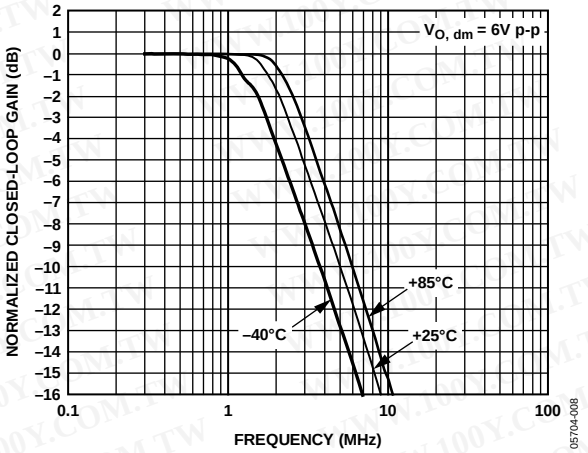


Figure 9. Large Signal Frequency Response at Various Temperatures

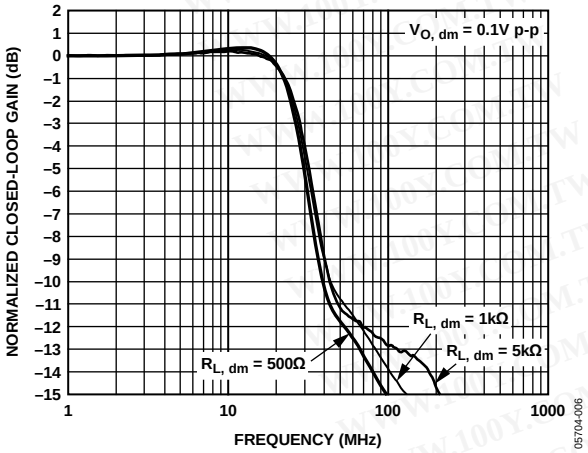


Figure 7. Small Signal Frequency Response for Various Resistive Loads

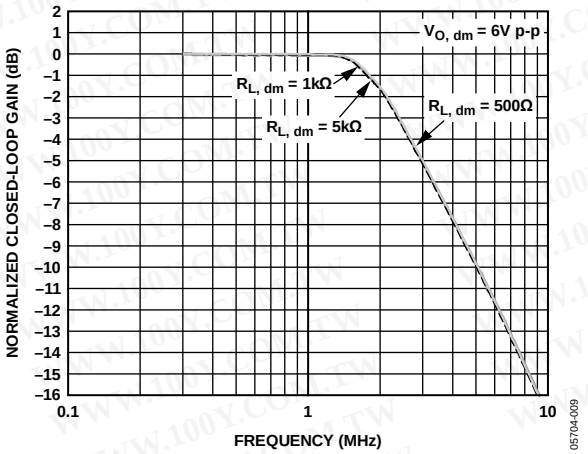


Figure 10. Large Signal Frequency Response for Various Resistive Loads

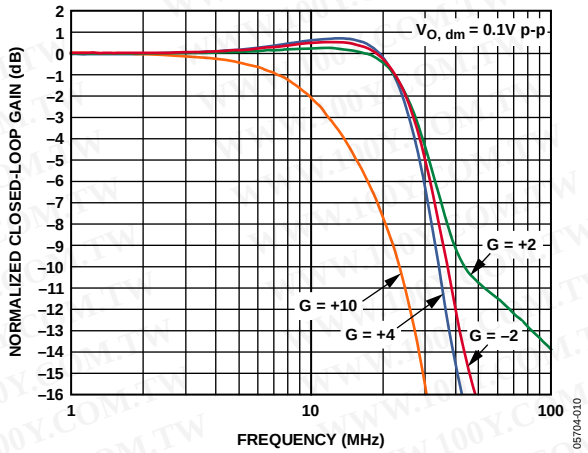


Figure 11. Small Signal Frequency Response for Various Gains

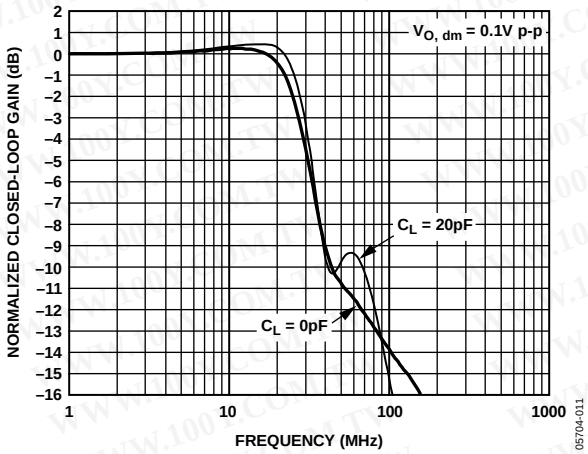


Figure 12. Small Signal Frequency Response for Various Capacitive Loads

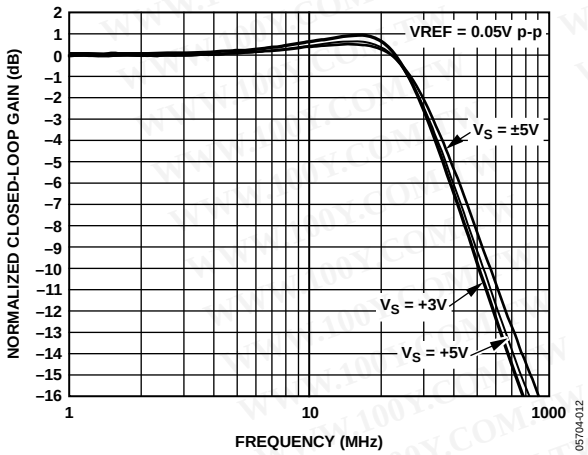


Figure 13. REF Input Small Signal Frequency Response for Various Supplies

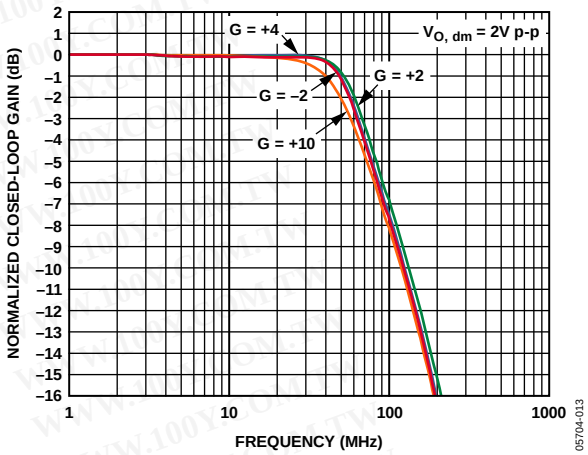


Figure 14. Large Signal Frequency Response for Various Gains

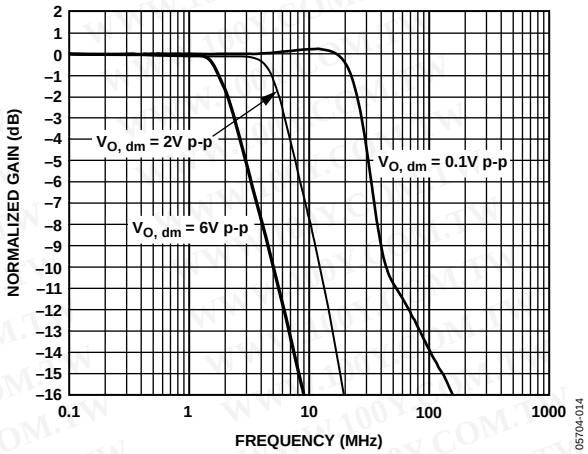


Figure 15. Frequency Response for Various Output Amplitudes

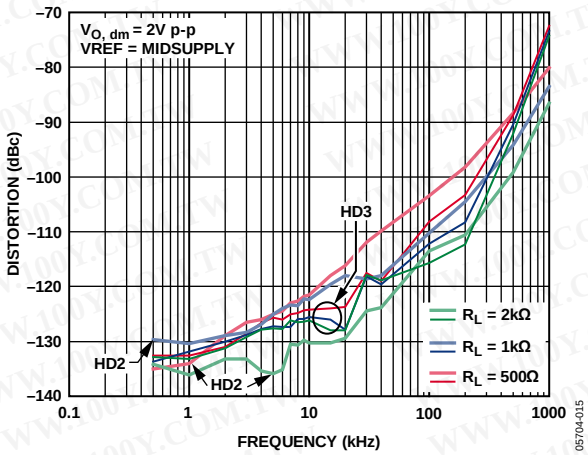


Figure 16. Distortion vs. Frequency for Various Loads

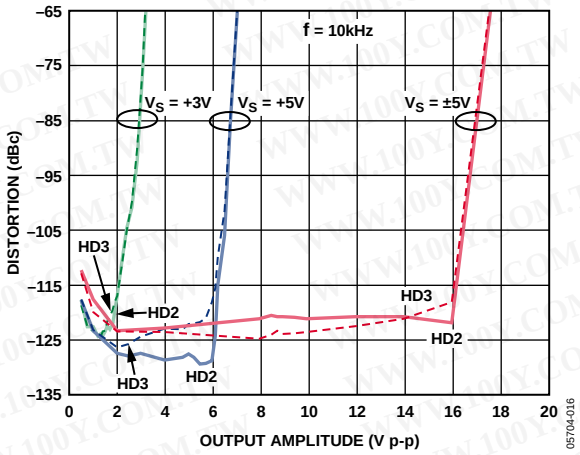


Figure 17. Distortion vs. Output Amplitude for Various Supplies (G = +2)

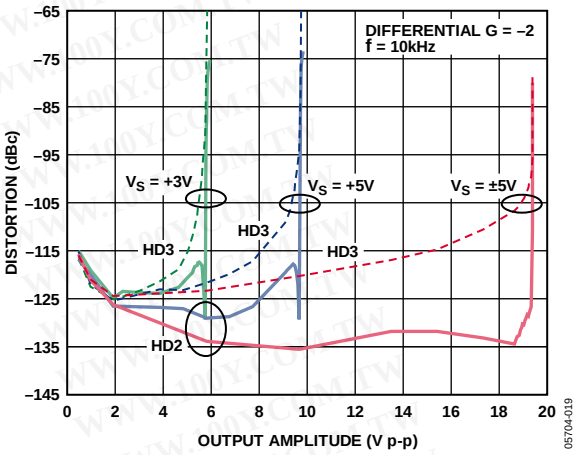


Figure 20. Distortion vs. Output Amplitude for Various Supplies (G = –2)

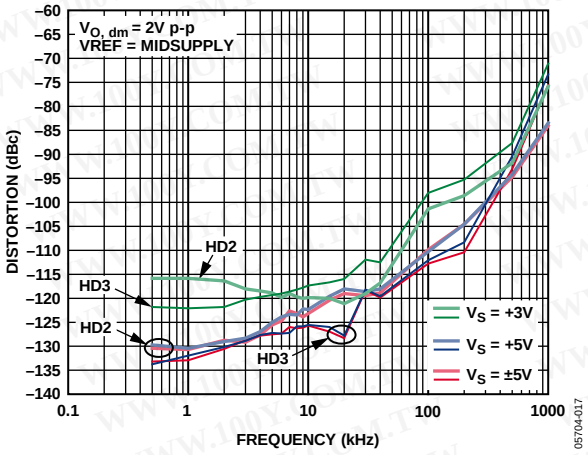


Figure 18. Distortion vs. Frequency for Various Supplies

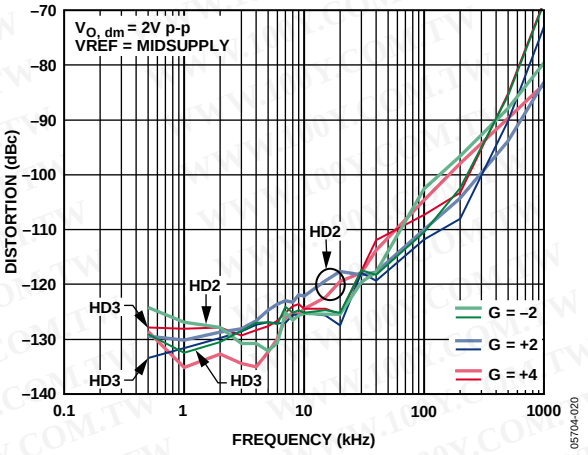


Figure 21. Distortion vs. Frequency for Various Gains

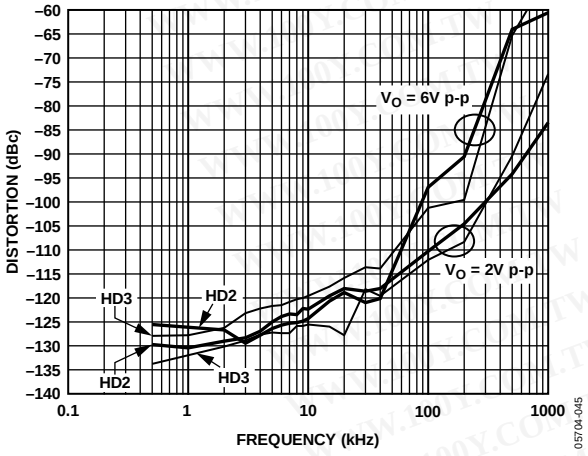


Figure 19. Distortion vs. Frequency at Various Output Amplitudes

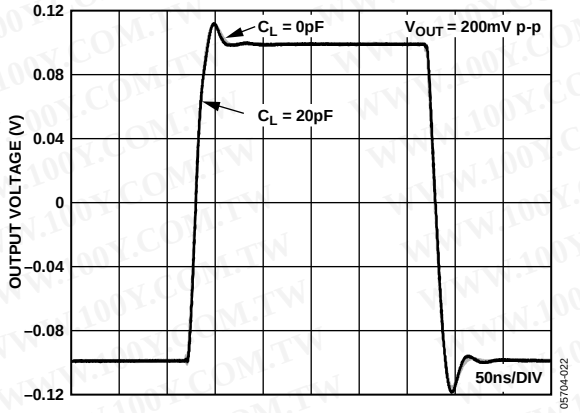


Figure 22. Small Signal Transient Response for Various Capacitive Loads

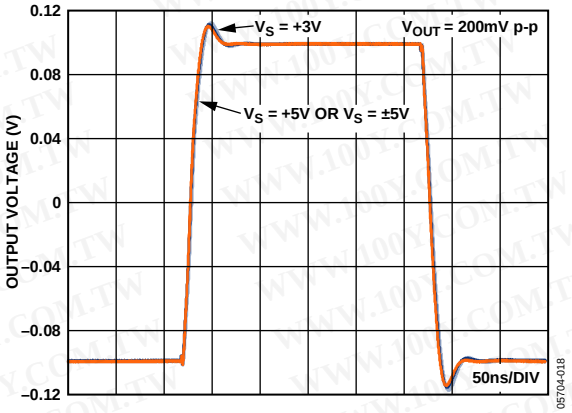


Figure 23. Small Signal Transient Response for Various Supplies

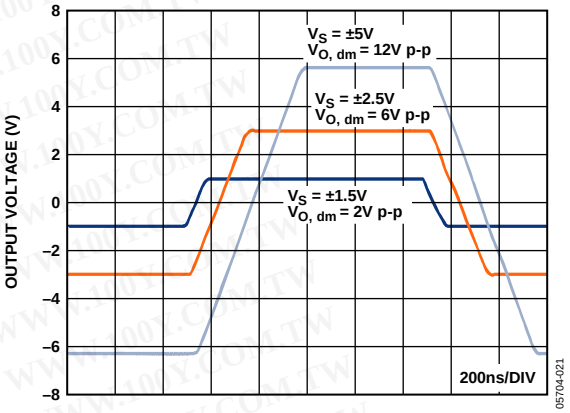


Figure 26. Large Signal Transient Response for Various Supplies

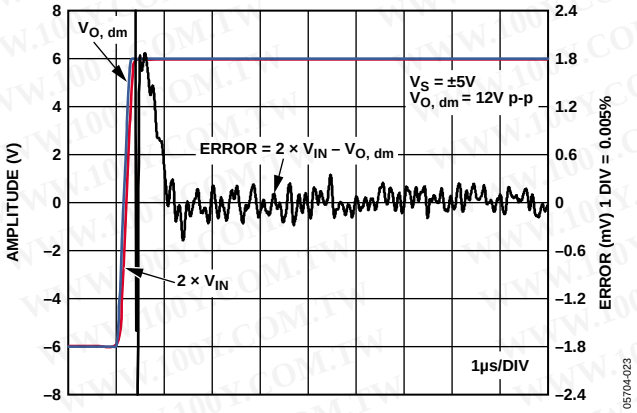


Figure 24. Settling Time (0.005%), V_S = ±5 V

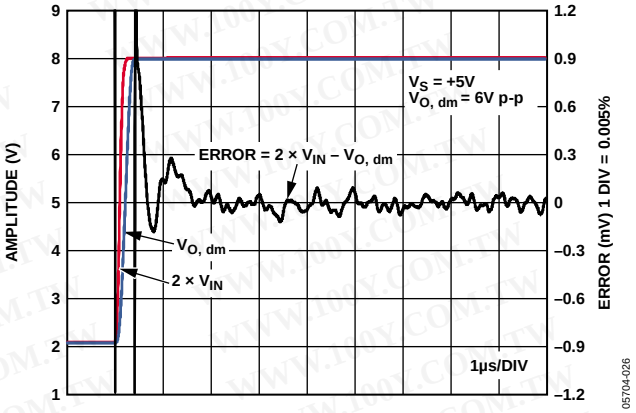


Figure 27. Settling Time (0.005%), V_S = +5 V

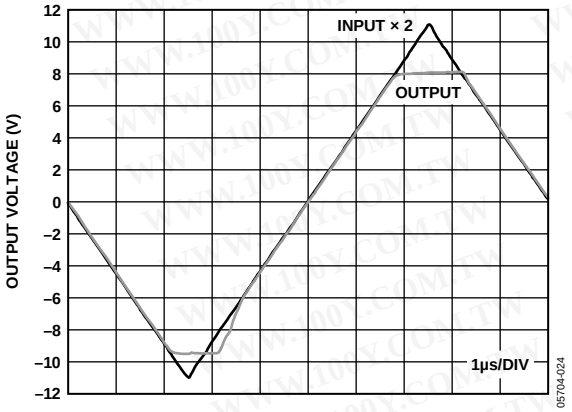


Figure 25. Input Overdrive Recovery, V_S = ±5 V

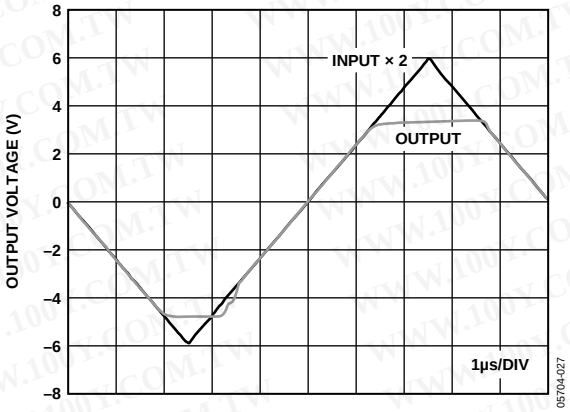


Figure 28. Input Overdrive Recovery, V_S = +5 V

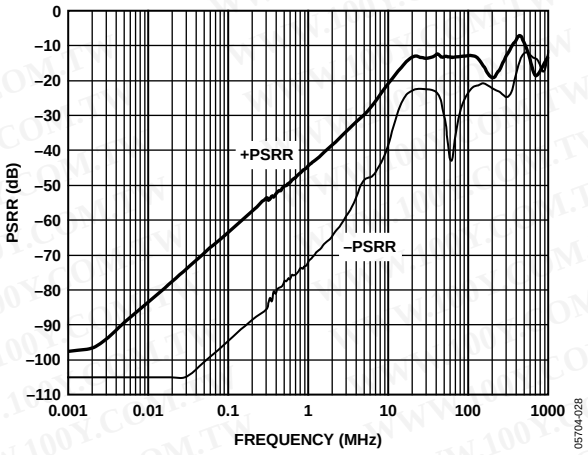


Figure 29. Power Supply Rejection Ratio vs. Frequency

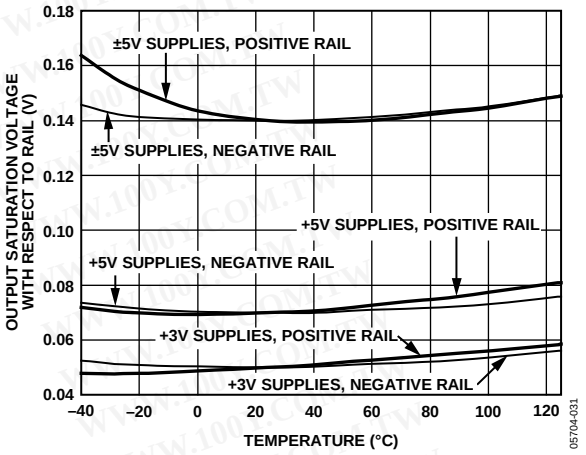


Figure 32. Output Saturation Voltage vs. Temperature

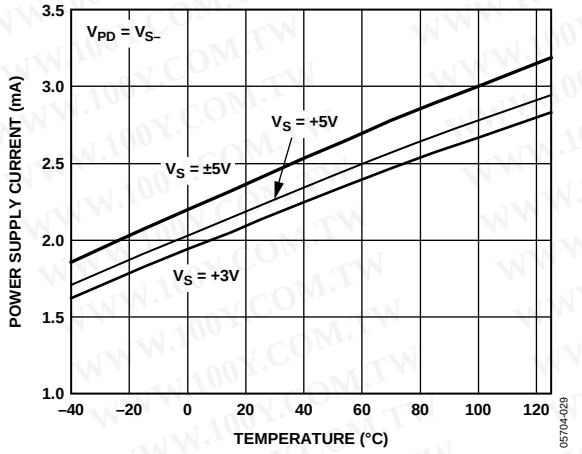


Figure 30. Power Supply Current vs. Temperature

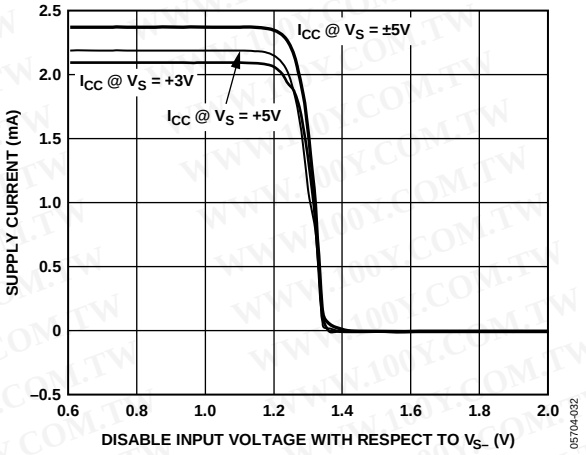


Figure 33. Power Supply Current vs. Disable Voltage

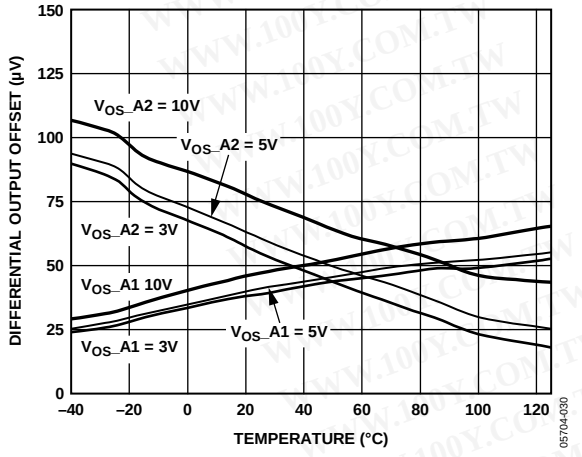


Figure 31. Differential Output Offset Voltage vs. Temperature

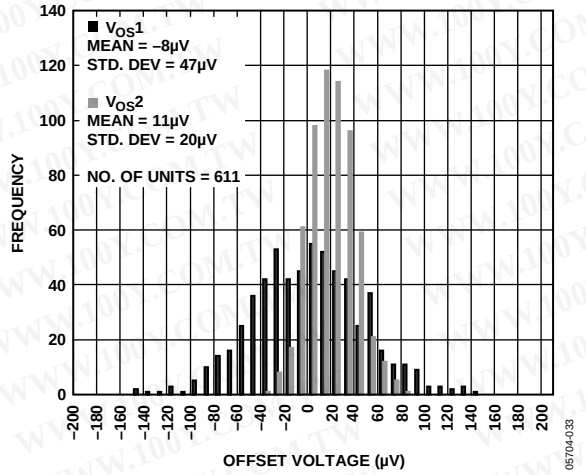


Figure 34. Differential Output Offset Distribution

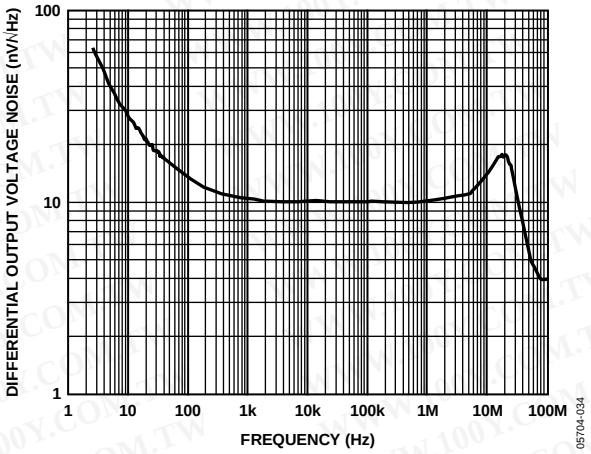


Figure 35. Differential Output Voltage Noise vs. Frequency

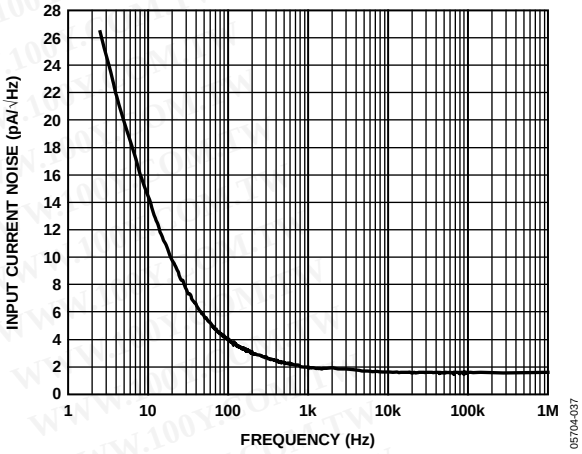


Figure 38. Input Current Noise vs. Frequency

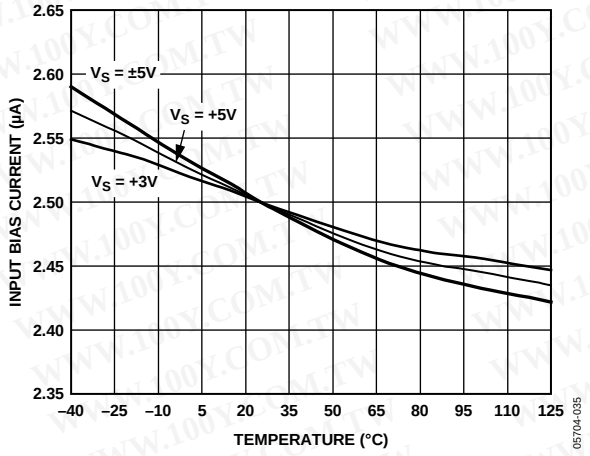


Figure 36. Input Bias Current vs. Temperature for Various Supplies

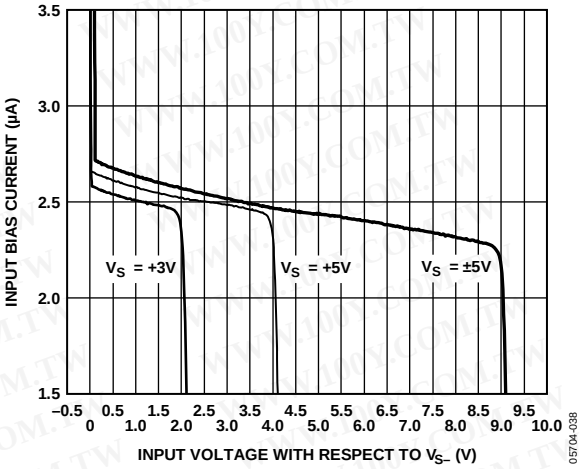


Figure 39. Input Bias Current vs. Input Voltage

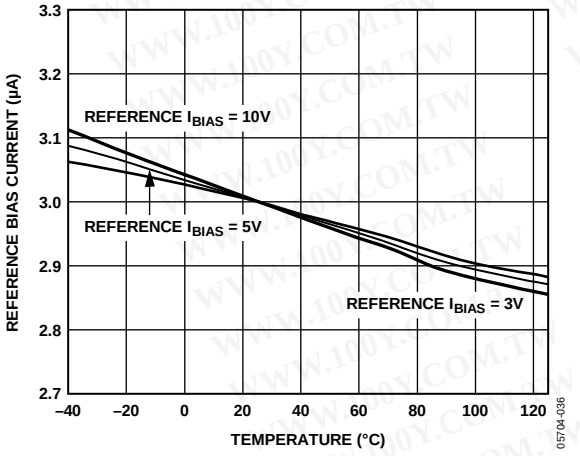


Figure 37. REF Input Bias Current vs. Temperature

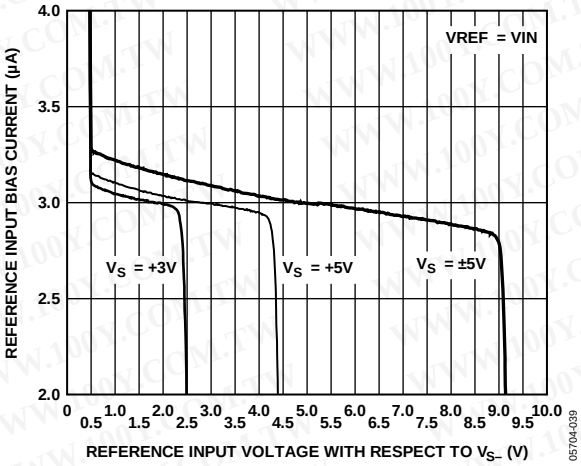


Figure 40. REF Input Bias Current vs. REF Input Voltage

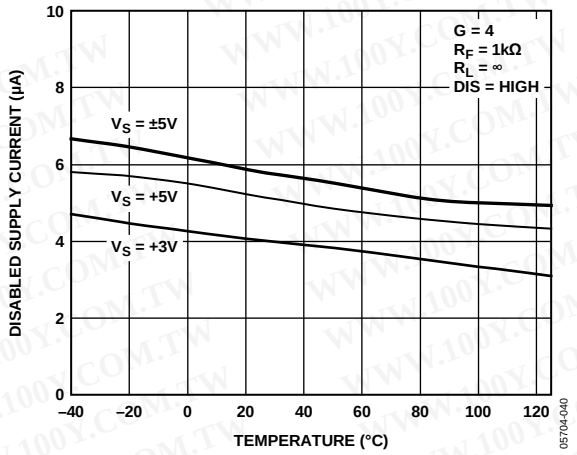


Figure 41. Disable Supply Current vs. Temperature for Various Supplies

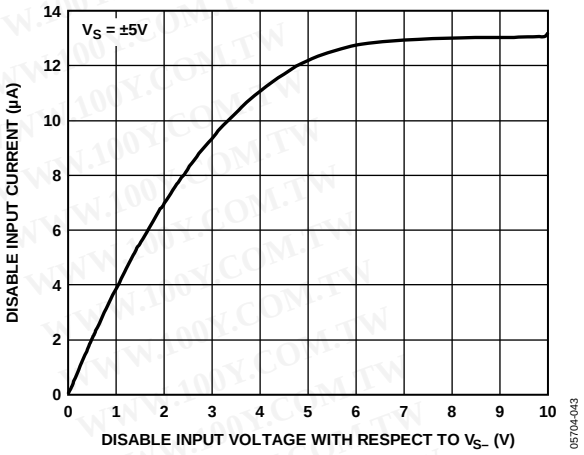


Figure 44. Disable Input Current vs. Disable Input Voltage

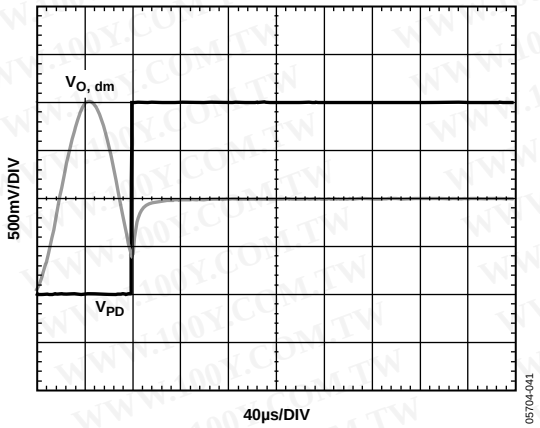


Figure 42. Disable Assert Time

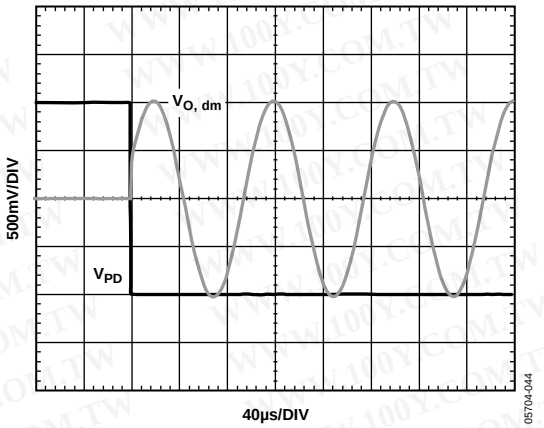


Figure 45. Disable Deassert Time

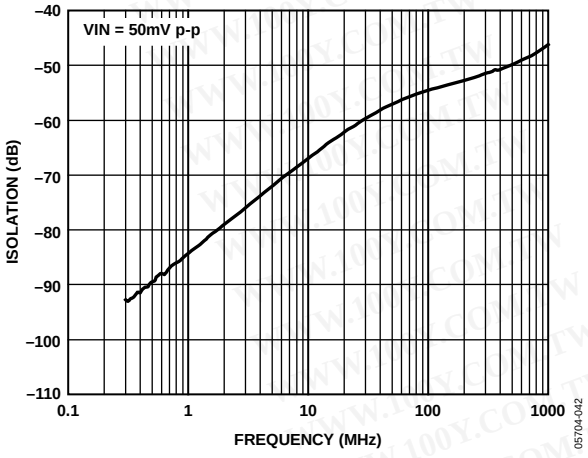


Figure 43. Disabled Input-to-Output Isolation vs. Frequency

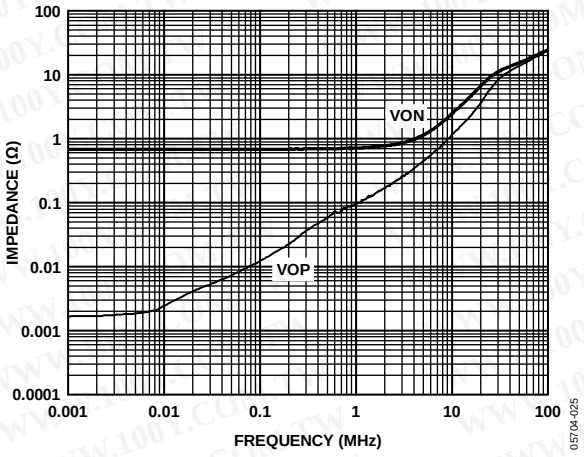


Figure 46. Single-Ended Output Impedance vs. Frequency

THEORY OF OPERATION

The ADA4941-1 is a low power, single-ended input, differential output amplifier optimized for driving high resolution ADCs. Figure 47 illustrates how the ADA4941-1 is typically connected. The amplifier is composed of an uncommitted amplifier, A1, driving a precision inverter, A2. The negative input of A1 is brought out to Pin 1 (FB), allowing for user-programmable gain. The inverting op amp, A2, provides accurate inversion of the output of A1, VOP, producing the output signal VON.

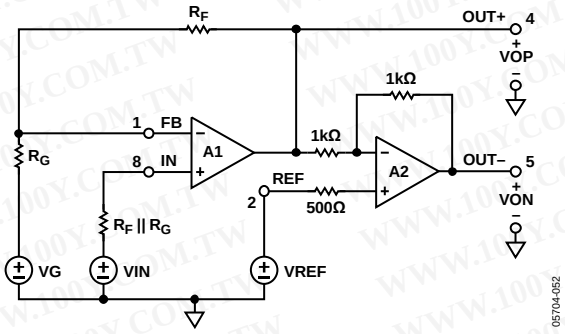


Figure 47. Basic Connections (Power Supplies Not Shown)

The voltage applied to the REF pin appears as the output common-mode voltage. Note that the voltage applied to the REF pin does not affect the voltage at the OUT+ pin. Because of this, a differential offset can exist between the outputs, while the desired output common-mode voltage is present. For example, when VOP = 3.5 V and VON = 1.5 V, the output common-mode voltage is equal to 2.5 V, just as it is when both outputs are at 2.5 V. In the first case, the differential voltage (or offset) is 2.0 V, and in the latter case, the differential voltage is 0 V. When calculating output voltages, both differential and common-mode voltages must be considered at the same time to avoid undesired differential offsets.

BASIC OPERATION

In Figure 47, R_G and R_F form the external gain-setting network. VG and VREF are externally applied voltages. V_O, cm is defined as the output common-mode voltage and V_O, dm is defined as the differential-mode output voltage. The following equations can be derived from Figure 47:

$$VOP = VIN\left(1+\frac{R_F}{R_G}\right) - VG\left(\frac{R_F}{R_G}\right) \quad (1)$$

$$VON = -VIN\left(1+\frac{R_F}{R_G}\right) + VG\left(\frac{R_F}{R_G}\right) + 2(VREF) \quad (2)$$

$$V_O, dm = VOP - VON = 2(VIN)\left(1+\frac{R_F}{R_G}\right) - 2VG\left(\frac{R_F}{R_G}\right) - 2(VREF) \quad (3)$$

$$V_O, cm = \left(\frac{VOP + VON}{2}\right) = VREF \quad (4)$$

When $R_F = 0$ and R_G is removed, Equation 3 simplifies to the following:

$$V_O, dm = 2(VIN) - 2(VREF) \quad (5)$$

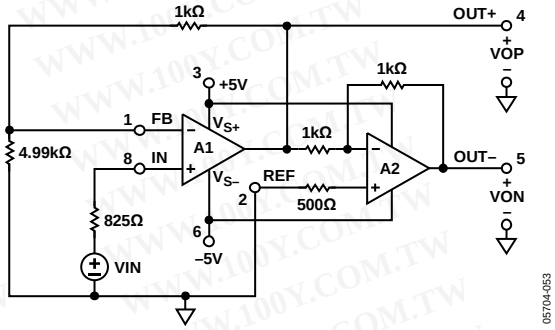


Figure 48. Dual Supply, G = 2.4, Single-Ended-to-Differential Amplifier

Figure 48 shows an example of a dual-supply connection. In this example, VG and VREF are set to 0 V, and the external R_F and R_G network provides a noninverting gain of 1.2 in A1. This example takes full advantage of the rail-to-rail output stage. The gain equation is

$$VOP - VON = 2.4(VIN) \quad (6)$$

The in-series, 825 Ω resistor combined with Pin 8 compensates for the voltage error generated by the input offset current of A1. The linear output range of both A1 and A2 extends to within 200 mV of each supply rail, which allows a peak-to-peak differential output voltage of 19.2 V on ±5 V supplies.

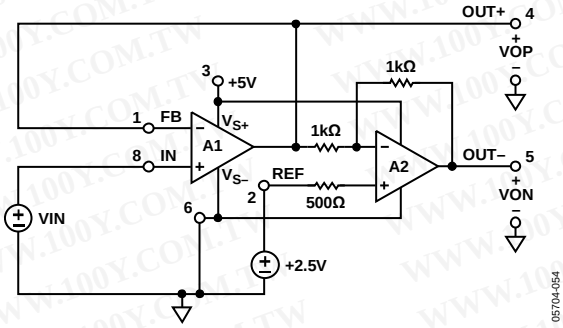


Figure 49. Single +5V Supply, G=2 Single-Ended-to-Differential Amplifier

Figure 49 shows a single 5 V supply connection with A1 used as a unity gain follower. The 2.5 V at the REF pin sets the output common-mode voltage to 2.5 V. The transfer function is then

$$VOP - VON = 2(VIN) - 5\ V \quad (7)$$

In this case, the linear output voltage is limited by A1. On the low end, the output of A1 starts to saturate and show degraded linearity when VOP approaches 200 mV. On the high end, the input of A1 becomes saturated and exhibits degraded linearity when VIN moves beyond 4 V (within 1 V of VCC). This limits the linear differential output voltage in the circuit shown in Figure 49 to about 7.6 V p-p.

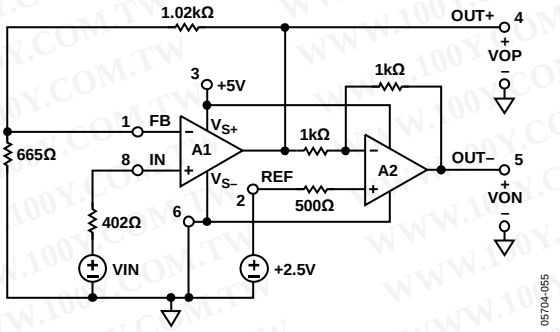


Figure 50. 5 V Supply, G = 5, Single-Ended-to-Differential Amplifier

Figure 50 shows a single 5 V supply connection for G = 5. The R_F and R_G network sets the gain of A1 to 2.5, and the 2.5 V at the REF input provides a centered 2.5 V output common-mode voltage. The transfer function is then

$$VOP - VON = 5(VIN) - 5\text{ V} \quad (8)$$

The output range limits of A1 and A2 limit the differential output voltage of the circuit shown in Figure 50 to approximately 8.4 V p-p.

DC ERROR CALCULATIONS

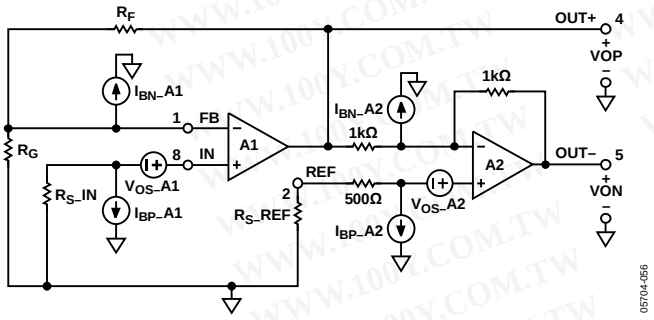


Figure 51. DC Error Sources

Figure 51 shows the major contributions to the dc output voltage error. For each output, the total error voltage can be calculated using familiar op amp concepts. Equation 9 expresses the dc voltage error present at the VOP output.

$$VOP\_error = \left(1+\frac{R_F}{R_G}\right)\left[V_{OS}\_A1-(I_{BP}\_A1)(R_S\_IN)\right]+(I_{BP}\_A1)R_F \quad (9)$$

When using data from the Specifications tables, it is often more expedient to use input offset current in place of the individual input bias currents when calculating errors. Input offset current is defined as the magnitude of the difference between the two input bias currents. Using this definition, each input bias current can be expressed in terms of the average of the two input bias currents, I_B, and the input offset current, I_{OS}, as $I_{BP,N} = I_B \pm I_{OS}/2$. DC errors are minimized when $R_S = R_F \,||\, R_G$. In this case, Equation 9 is reduced to

$$VOP\_error = \left(1+\frac{R_F}{R_G}\right)\left[V_{OS}\_A1\right]+(I_{OS})R_F \quad (R_S = R_F \,||\, R_G)$$

Equation 10 expresses the dc voltage error present at the VON output.

$$VON\_error = -(VOP\_error) + 2[V_{OS}\_A2 - (I_{BP}\_A2)(R_S\_REF + 500)] + 1000(I_{BN}\_A2) \quad (10)$$

The internal 500 Ω resistor is provided on-chip to minimize dc errors due to the input offset current in A2. The minimum error is achieved when R_S_REF = 0 Ω. In this case, Equation 10 is reduced to

$$VON\_error = -(VOP\_error) + 2[V_{OS}\_A2] + (I_{OS})1000 \quad (R_S\_REF = 0\ \Omega)$$

The differential output voltage error V_O_error, dm, is the difference between VOP_error and VON_error:

$$V_O\_error,\ dm = VOP\_error - VON\_error \quad (11)$$

The output offset voltage of each amplifier in the ADA4941-1 also includes the effects of finite common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and dc open-loop gain (A_{VOL}).

$$V_{OS} = V_{OS}\_nom + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_S}{PSRR} + \frac{\Delta VOUT}{A_{VOL}} \quad (12)$$

where:

V_{OS}_nom is the nominal output offset voltage without including the effects of CMRR, PSRR, and A_{VOL}.

Δ indicates the change in conditions from nominal.

V_{CM} is the input common-mode voltage (for A1, the voltage at IN, and for A2, the voltage at REF).

V_S is the power supply voltage.

VOUT is either op amp output.

Table 7, Table 8, and Table 9 show typical error budgets for the circuits shown in Figure 48, Figure 49, and Figure 50.

R_F = 1.0 kΩ, R_G = 4.99 kΩ, R_S_IN = 825 Ω, R_S_REF = 0 Ω

Table 7. Output Voltage Error Budget for G = 2.4 Amplifier Shown in Figure 48

Error Source	Typical Value	VOP_error	VON_error	V_O_dm_error
V_{OS}_A1	0.1 mV	+0.12 mV	−0.12 mV	+0.24 mV
I_{BP}_A1	3 µA	+2.48 mV	−2.48 mV	−4.96 mV
I_{BN}_A1	3 µA	−2.48 mV	+2.48 mV	+4.96 mV
V_{OS}_A2	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total V_O_error, dm = 0.44 mV

R_F = 0 Ω, R_G = ∞, R_S_IN = 0 Ω, R_S_REF = 0 Ω

Table 8. Output Voltage Error Budget for Amplifier Shown in Figure 49

Error Source	Typical Value	VOP_error	VON_error	V_O_dm_error
V_{OS}_A1	0.1 mV	+0.1 mV	−0.1 mV	+0.2 mV
I_{BP}_A1	3 µA	+2.48 mV	−2.48 mV	−4.96 mV
I_{BN}_A1	3 µA	−2.48 mV	+2.48 mV	+4.96 mV
V_{OS}_A2	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total V_O_error, dm = 0.4 mV

R_F = 1.02 kΩ, R_G = 665 Ω, R_S_IN = 402 Ω, R_S_REF = 0 Ω

Table 9. Output Voltage Error Budget for G = 5 Amplifier Shown in Figure 50

Error Source	Typical Value	VOP_error	VON_error	V_O_dm_error
V_{OS}_A1	0.1 mV	+0.25 mV	−0.25 mV	+0.5 mV
I_{BP}_A1	3 µA	+1.21 mV	−1.21 mV	−2.4 mV
I_{BN}_A1	3 µA	−1.21 mV	+1.21 mV	+2.4 mV
V_{OS}_A2	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total V_O_error, dm = 0.7 mV

OUTPUT VOLTAGE NOISE

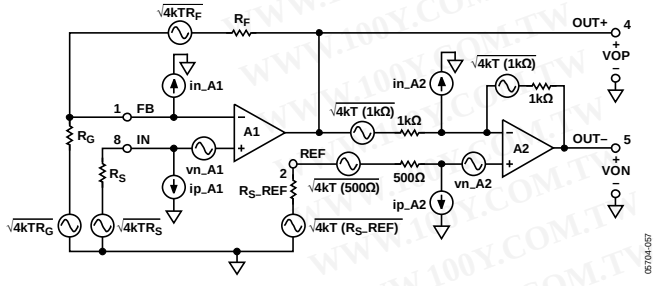


Figure 52. Noise Sources

Figure 52 shows the major contributors to the ADA4941-1 differential output voltage noise. The differential output noise mean-square voltage equals the sum of twice the noise mean-square voltage contributions from the noninverting channel (A1), plus the noise mean-square voltage terms associated with the inverting channel (A2).

$$\overline{V_O,dm\_n}^2 = 2\left[\left(1+\frac{R_F}{R_G}\right)\times(\overline{vn\_A1})\right]^2 + 2\times \left[\left(1+\frac{R_F}{R_G}\right)\times(\overline{ip\_A1}\times R_S)\right]^2 + 2\left[\overline{in\_A1}\times R_F\right]^2 + 2\left[\sqrt{4\,kTR_F}\right]^2 + 2\left[\sqrt{4\,kTR_G}\times\frac{R_F}{R_G}\right]^2 + 2\times \left[\left(1+\frac{R_F}{R_G}\right)\times\sqrt{4\,kTR_S}\right]^2 + \overline{VON\_n}^2 \quad (13)$$

where $\overline{VON\_n}^2$ is calculated as

$$\overline{VON\_n}^2 = 4\left(\overline{vn\_A2}^2\right) + 4\left[(\overline{ip\_A2})(500+R_S\_REF)\right]^2 + \left[1000(\overline{in\_A2})\right]^2 + 8\,kT(1000) + 16\,kT(500) + 16\,kT(R_S\_REF) \quad (14)$$

where:

$\overline{vn\_A1}$ and $\overline{vn\_A2}$ are the input voltage noises of A1 and A2, each equal to 2.1 nV/√Hz.

$\overline{in\_A1}$, $\overline{in\_A2}$, $\overline{ip\_A1}$, and $\overline{ip\_A2}$ are amplifier input current noise terms, each equal to 1 pA/√Hz.

R_S, R_F, and R_G are the external source, feedback, and gain resistors, respectively.

kT is Boltzmann's constant times absolute temperature, equal to 4.2 x 10^{-21} W-s at room temperature.

R_S_REF is any source resistance at the REF pin.

When A1 is used as a unity gain follower, the output voltage noise spectral density is at its minimum, 10 nV/√Hz. Higher voltage gains have higher output voltage noise.

Table 10, Table 11, and Table 12 show the noise contributions and output voltage noise for the circuits in Figure 48, Figure 49, and Figure 50.

Table 10. Output Voltage Noise, G = 2.4 Differential Amplifier Shown in Figure 48

Noise Source	Typical Value	VOP Contribution (nV√Hz)	VON Contribution (nV√Hz)	V_O, dm Contribution (nV√Hz)
$\overline{vn\_A1}$	2.1 nV/√Hz	2.5	2.5	5
$\overline{ip\_A1}$	1 pA/√Hz	1	1	2
$\overline{in\_A1}$	1 pA/√Hz	1	1	2
$\sqrt{4\ kTR_F}$	4 nV/√Hz	4	4	8
$\sqrt{4\ kTR_G}$	9 nV/√Hz	1.8	1.8	3.6
$\sqrt{4\ kTR_S}$	3.6 nV/√Hz	4.4	4.4	8.8
$\overline{vn\_inverter}$	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_S\_REF}$	0	0	0	0
$\overline{ip\_A2 \times R_S\_REF}$	0	0	0	0
	Totals	**6.8**	**11.4**	**16.5**

R_F = 1.0 kΩ, R_G = 4.99 kΩ, R_S = 825 Ω, R_S_REF = 0 Ω.

$\overline{vn\_inverter}$ = noise contributions from A2 and its associated internal 1 kΩ feedback resistors and 500 Ω offset current balancing resistor.

Table 11. Output Voltage Noise, G = 2 Differential Amplifier Shown in Figure 49

Noise Source	Typical Value	VOP Contribution (nV√Hz)	VON Contribution (nV√Hz)	V_O, dm Contribution (nV√Hz)
$\overline{vn\_A1}$	2.1 nV/√Hz	2.1	2.1	4.2
$\overline{ip\_A1}$	0	0	0	0
$\overline{in\_A1}$	0	0	0	0
$\sqrt{4\ kTR_F}$	0	0	0	0
$\sqrt{4\ kTR_G}$	0	0	0	0
$\sqrt{4\ kTR_S}$	0	0	0	0
$\overline{vn\_inverter}$	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_S\_REF}$	0	0	0	0
$\overline{ip\_A2 \times R_S\_REF}$	0	0	0	0
	Totals	**2.1**	**9.4**	**10**

R_F = 0 Ω, R_G = ∞, R_S = 0 Ω, R_S_REF = 0 Ω.

Table 12. Output Voltage Noise, G = 5 Differential Amplifier Shown in Figure 50

Noise Source	Typical Value	VOP Contribution (nV√Hz)	VON Contribution (nV√Hz)	V_O, dm Contribution (nV√Hz)
$\overline{vn\_A1}$	2.1 nV/√Hz	5.25	5.25	10.5
$\overline{ip\_A1}$	1 pA/√Hz	1	1	2
$\overline{in\_A1}$	1 pA/√Hz	1	1	2
$\sqrt{4\ kTR_F}$	4 nV/√Hz	4	4	8
$\sqrt{4\ kTR_G}$	3.26 nV/√Hz	4.9	4.9	9.8
$\sqrt{4\ kTR_S}$	2.54 nV/√Hz	6.54	6.54	13.1
$\overline{vn\_inverter}$	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_S\_REF}$	0	0	0	0
$\overline{ip\_A2 \times R_S\_REF}$	0	0	0	0
	Totals	**10.7**	**14.1**	**23.1**

R_F = 1.02 kΩ, R_G = 665 Ω, R_S = 402 Ω, R_S_REF = 0 Ω.

FREQUENCY RESPONSE VS. CLOSED-LOOP GAIN

The operational amplifiers used in the ADA4941-1 are voltage feedback with an open-loop frequency response that can be approximated with the integrator response, as shown in Figure 53.

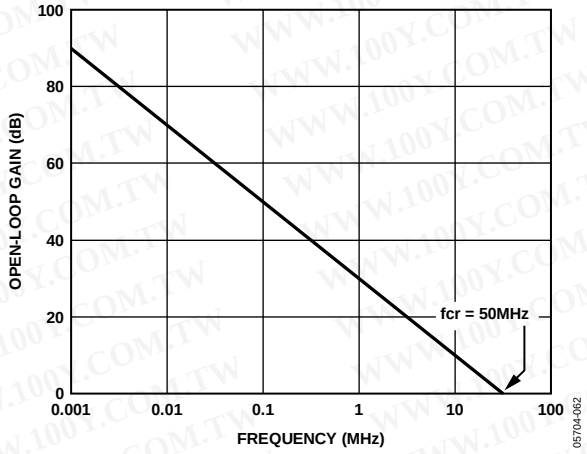


Figure 53. ADA4941-1 Op Amp Open-Loop Gain vs. Frequency

For each amplifier, the frequency response can be approximated by the following equations:

$$V_O\_A1 = VIN \times \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{R_G}\right] \times \frac{f}{fcr}}\right) \quad (15)$$

(Noninverting Response)

$$V_O\_A2 = VIN \times \left(\frac{-R_F}{R_G}\right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{R_G}\right] \times \frac{f}{fcr}}\right) \quad (16)$$

(Inverting Response)

f_{CR} is the gain-bandwidth frequency of the amplifier (where the open-loop gain shown in Figure 53 equals 1). f_{CR} for both amplifiers is about 50 MHz.

The inverting amplifier A2 has a fixed feedback network. The transfer function is approximately

$$V_O\_A2 = -VIN \times \left(\frac{1}{1 + \frac{2 \times f}{50\ \text{MHz}}}\right) = -VOP \times \left(\frac{1}{1 + \frac{f}{25\ \text{MHz}}}\right) \quad (17)$$

A1's frequency response depends on the external feedback network as indicated by Equation 15. The overall differential output voltage is therefore

$$V_O,\ dm = VOP - VON = VOP + VOP \times \left(\frac{1}{1 + \frac{f}{25\ \text{MHz}}}\right) \quad (18)$$

$$V_O,\ dm = VIN \times \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{R_G}\right] \times \frac{f}{50\ \text{MHz}}}\right) \times \left(1 + \frac{1}{1 + \frac{f}{25\ \text{MHz}}}\right) \quad (19)$$

Multiplying the terms and neglecting negligible terms leads to the following approximation:

$$V_O, dm = VIN\left(1 + \frac{R_F}{R_G}\right) \times \left[\frac{2}{\left(1 + \left[\frac{R_F + R_G}{R_G}\right] \times \frac{f}{50\ \text{MHz}}\right) \times \left(1 + \frac{f}{25\ \text{MHz}}\right)}\right] \quad (20)$$

There are two poles in this transfer function, and the lower frequency pole limits the bandwidth of the differential amplifier. If VOP is shorted to IN− (A1 is a unity gain follower), the 25 MHz closed-loop bandwidth of the inverting channel limits the overall bandwidth. When A1 is operating with higher noise gains, the bandwidth is limited by A1's closed-loop bandwidth, which is inversely proportional to the noise gain ($1 + R_F/R_G$). For instance, if the external feedback network provides a noise gain of 10, the bandwidth drops to 5 MHz.

APPLICATIONS

OVERVIEW

The ADA4941-1 is an adjustable-gain, single-ended-to-differential voltage amplifier, optimized for driving high resolution ADCs. Single-ended-to-differential gain is controlled by one feedback network, comprised of two external resistors: R_F and R_G.

USING THE REF PIN

The REF pin sets the output base line in the inverting path and is used as a reference for the input signal. In most applications, the REF pin is set to the input signal midswing level, which in many cases is also midsupply. For bipolar signals and dual power supplies, REF is generally set to ground. In single-supply applications, setting REF to the input signal midswing level provides optimal output dynamic range performance with minimum differential offset. Note that the REF input only affects the inverting signal path or VON.

Most applications require a differential output signal with the same dc common-mode level on each output. It is possible for the signal measured across VOP and VON to have a common-mode voltage that is of the desired level but not common to both outputs. This type of signal is generally avoided because it does not allow for optimal use of the amplifier's output dynamic range.

Defining VIN as the voltage applied to the input pin, the equations that govern the two signal paths are given in Equation 21 and Equation 22.

$$VOP = VIN \quad (21)$$

$$VON = -VIN + 2\,(REF) \quad (22)$$

When the REF voltage is set to the midswing level of the input signal, the two output signals fall directly on top of each other with minimal offset. Setting the REF voltage elsewhere results in an offset between the two outputs.

The best use of the REF pin can be further illustrated by considering a single-supply case with a 10 V power supply and an input signal that varies between 2 V and 7 V. This is a case where the midswing level of the input signal is not at midsupply but is at 4.5 V. Setting the REF input at 4.5 V and neglecting offsets, Equation 21 and Equation 22 are used to calculate the results. When the input signal is at its midpoint of 4.5 V, OUT+ is at 4.5 V, as is VON. This can be considered as a base line state where the differential output voltage is 0. When the input increases to 7 V, VOP tracks the input to 7 V, and VON decreases to 2 V. This can be viewed as a positive peak signal where the differential output voltage equals 5 V. When the input signal decreases to 2 V, VOP again tracks to 2 V, and VON increases to 7 V. This can be viewed as a negative peak signal where the differential output voltage equals −5 V. The resulting differential output voltage is 10 V p-p.

The previous discussion reveals how the single-ended-to-differential gain of 2 is achieved.

INTERNAL FEEDBACK NETWORK POWER DISSIPATION

While traditional op amps do not have on-chip feedback elements, the ADA4941-1 contains two on-chip, 1 kΩ resistors that comprise an internal feedback loop. The power dissipated in these resistors must be included in the overall power dissipation calculations for the device. Under certain circumstances, the power dissipated in these resistors could be comparable to the device's quiescent dissipation. For example, on ±5 V supplies with the REF pin tied to ground and OUT− at +4 VDC, each 1 kΩ resistor carries 4 mA and dissipates 16 mW for a total of 32 mW. This is comparable to the quiescent power and must therefore be included in the overall device power dissipation calculations. For ac signals, rms analysis is required.

DISABLE FEATURE

The ADA4941-1 includes a disable feature that can be asserted to minimize power consumption in a device that is not needed at a particular time. When asserted, the disable feature does not place the device output in a high impedance or tristate condition. The disable feature is active high. See the Specifications tables for the high and low level voltage specifications.

ADDING A 3-POLE, SALLEN-KEY FILTER

The noninverting amplifier in the ADA4941-1 can be used as the buffer amplifier of a Sallen-Key filter. A 3-pole, low-pass filter can be designed to limit the signal bandwidth in front of an ADC. The input signal first passes through the noninverting stage where it is filtered. The filtered signal is then passed through the inverting stage to obtain the complementary output.

Figure 54 illustrates a 3-pole, Sallen-Key, low-pass filter with a −3 dB cutoff frequency of 100 kHz. The 1.69 kΩ resistor is included to minimize dc errors due to the input offset current in A1. The passive RC filters on the outputs are generally required by the ADC converter that is being driven. The frequency response of the filter is shown in Figure 55.

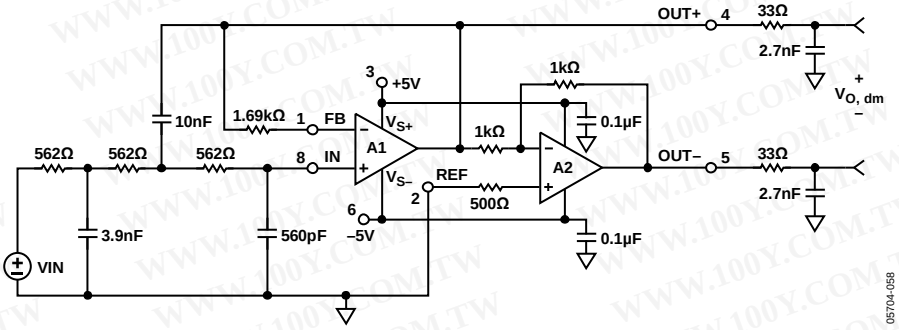


Figure 54. Sallen-Key, Low-Pass Filter with 100 kHz Cutoff Frequency

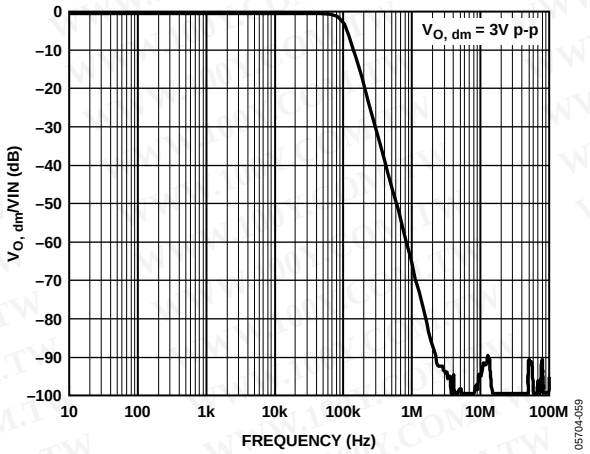


Figure 55. Frequency Response of the Circuit Shown in Figure 54

DRIVING THE AD7687 ADC

The ADA4941-1 is an excellent driver for high resolution ADCs, such as the AD7687, as shown in Figure 56. The Sallen-Key, low-pass filter shown in Figure 54 is included in this example but is not required. The circuit shown in Figure 56 accepts single-ended input signals that swing between 0 V and 3 V.

The ADR443 provides a stable, low noise, 3 V reference that is buffered by one of the AD8032 amplifiers and applied to the AD7687 REF input, providing a differential input full-scale level of 6 V. The reference voltage is also divided by two and buffered to supply the midsupply REF level of 1.5 V for the ADA4941-1.

GAIN OF −2 CONFIGURATION

The ADA4941-1 can be operated in a configuration referred to as gain of −2. Clearly, a gain of −2 can be achieved by simply swapping the outputs of a gain of +2 circuit, but the configuration described here is different. The configuration is referred to as having negative gain to emphasize that the input amplifier, A1, is operated as an inverting amplifier instead of in its usual noninverting mode. As implied in its name, the voltage gain from VIN to V_O, dm is −2 V/V. See Figure 57 for the gain of −2 configuration on ±5 V supplies.

The gain of −2 configuration is most useful in applications that have wide input swings because the input common-mode voltages are held at constant levels. The signal size is therefore constrained by the output swing limits. The gain of −2 has a low input resistance that is equal to R_G.

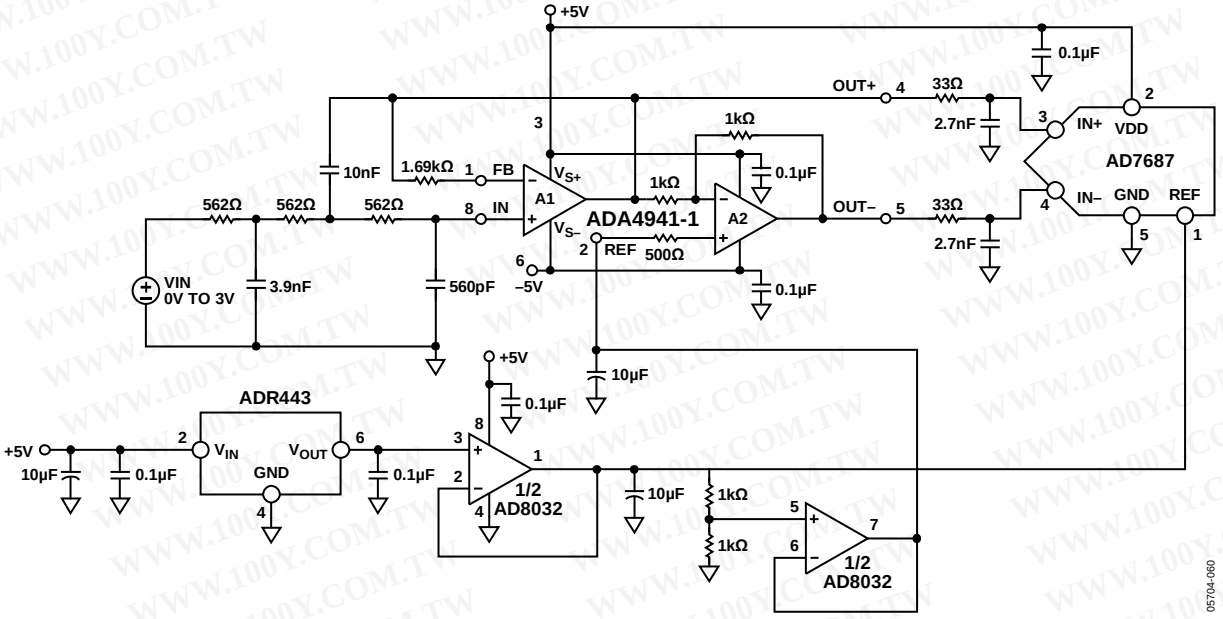


Figure 56. ADA4941-1 Driving the AD7687 ADC

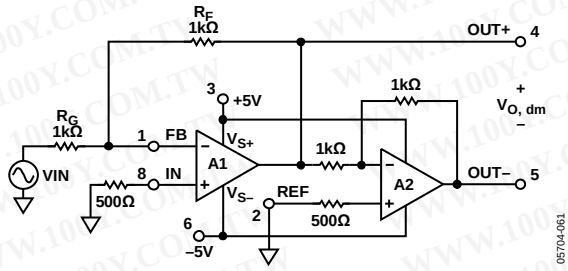


Figure 57. Gain of −2 Configuration

OUTLINE DIMENSIONS

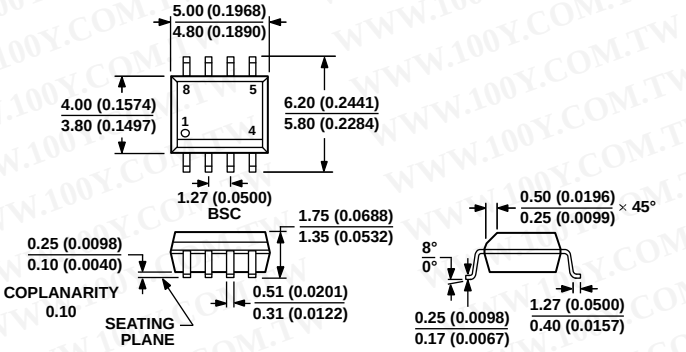


Figure 58. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

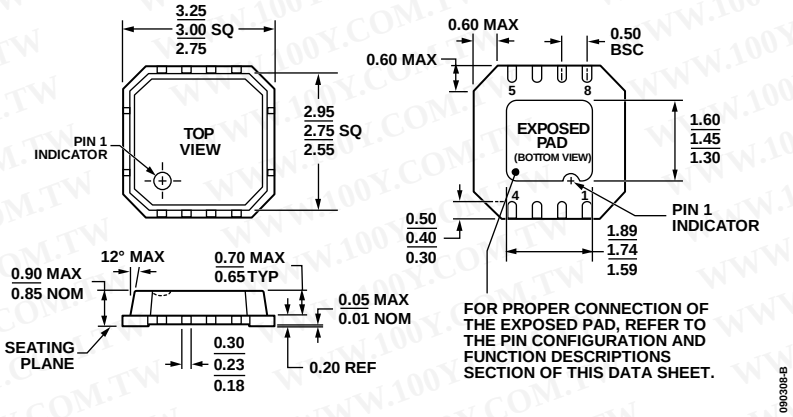


Figure 59. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead (CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4941-1YRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADA4941-1YRZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	2,500	
ADA4941-1YRZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADA4941-1YCPZ-R2	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	250	H0C
ADA4941-1YCPZ-RL	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	5,000	H0C
ADA4941-1YCPZ-R7	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	1,500	H0C
ADA4941-1YCP-EBZ		Evaluation Board			
ADA4941-1YR-EBZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

D05704-0-8/10(B)