Section 1 Overview

1.1 Features

The H8/532 is an original Hitachi CMOS microcomputer unit (MCU) comprising a high-performance CPU core plus a full range of supporting functions—an entire system integrated onto a single chip.

The CPU features a highly orthogonal instruction set that permits addressing modes and data sizes to be specified independently in each instruction. An internal 16-bit architecture and 16-bit access to on-chip memory enhance the CPU's data-processing capability and provide the speed needed for realtime control applications.

The on-chip supporting functions include RAM, ROM, timers, a serial communication interface (SCI), A/D conversion, and I/O ports. An on-chip data transfer controller (DTC) can transfer data in either direction between memory and I/O independently of the CPU.

For the on-chip ROM, a choice is offered between masked ROM and programmable ROM (PROM). The PROM version can be programmed by the user with a general-purpose PROM writer.

Table 1-1 lists the main features of the H8/532 chip.

Table 1-1 Features

Feature	Description
CPU	General-register machine • Eight 16-bit general registers • Five 8-bit and two 16-bit control registers High speed • Maximum clock rate: 10MHz (oscillator frequency: 20MHz) Expanded operating modes supporting external memory • Minimum mode: up to 64K-byte address space • Maximum mode: up to 1M-byte address space Highly orthogonal instruction set • Addressing modes and data size can be specified independently for each instruction 1.5 Addressing modes • Register-register operations • Register-memory operations Instruction set optimized for C language • Special short formats for frequently-used instructions and addressing modes
Memory	• 1K-Byte high-speed RAM on-chip • 32K-Byte programmable or masked ROM on-chip
16-Bit free-running timer (FRT) (3 channels)	Each channel provides: • 1 free-running counter (which can count external events) • 2 output-compare registers • 1 input capture register
8-Bit timer (1 channel)	• One 8-bit up-counter (which can count external events) • 2 time constant registers
PWM timer (3 channels)	• Generates pulses with any duty ratio from 0 to 100% • Resolution: 1/250
Watchdog timer (WDT) (1 channel)	• An overflow generates a nonmaskable interrupt • Can also be used as an interval timer

Table 1-1 Features (cont)

Feature	Description
Serial communication interface (SCI)	• Asynchronous or synchronous mode (selectable) • Full duplex: can send and receive simultaneously • Built-in baud rate generator
A/D converter	• 10-Bit resolution • 8 channels, controllable in single mode or scan mode (selectable) • Sample-and-hold function
I/O ports	• 57 Input/output pins (six 8-bit ports, one 5-bit port, one 4-bit port) • 8 Input-only pins (one 8-bit port) • Memory-mapped I/O
Interrupt controller (INTC)	• 3 external interrupt pins (NMI, $\overline{IRQ_0}$, $\overline{IRQ_1}$) • 19 internal interrupts • 8 priority levels
Data transfer controller (DTC)	Performs bidirectional data transfer between memory and I/O independently of the CPU
Wait-state controller (WSC)	Can insert wait states in access to external memory or I/O
Operating modes	5 MCU operating modes • Expanded minimum modes, supporting up to 64k bytes external memory with or without using on-chip ROM (Modes 1 and 2) • Expanded maximum modes, supporting up to 1M byte external memory with or without using on-chip ROM (Modes 3 and 4) • Single-chip mode (Mode 7) 3 power-down modes • Sleep mode • Software standby mode • Hardware standby mode
Other features	• E clock output available • Clock generator on-chip

Model Name	Package Options	ROM
HD6475328CG	84-Pin windowed LCC (CG-84)	PROM
HD6475328CP	84-Pin PLCC (CP-84)	
HD6475328F	80-Pin QFP (FP-80A)	
HD6435328CP	84-Pin PLCC (CP-84)	Mask
HD6435328F	80-Pin QFP (FP-80A)	ROM

1.2 Block Diagram

Figure 1-1 shows a block diagram of the H8/532 chip.

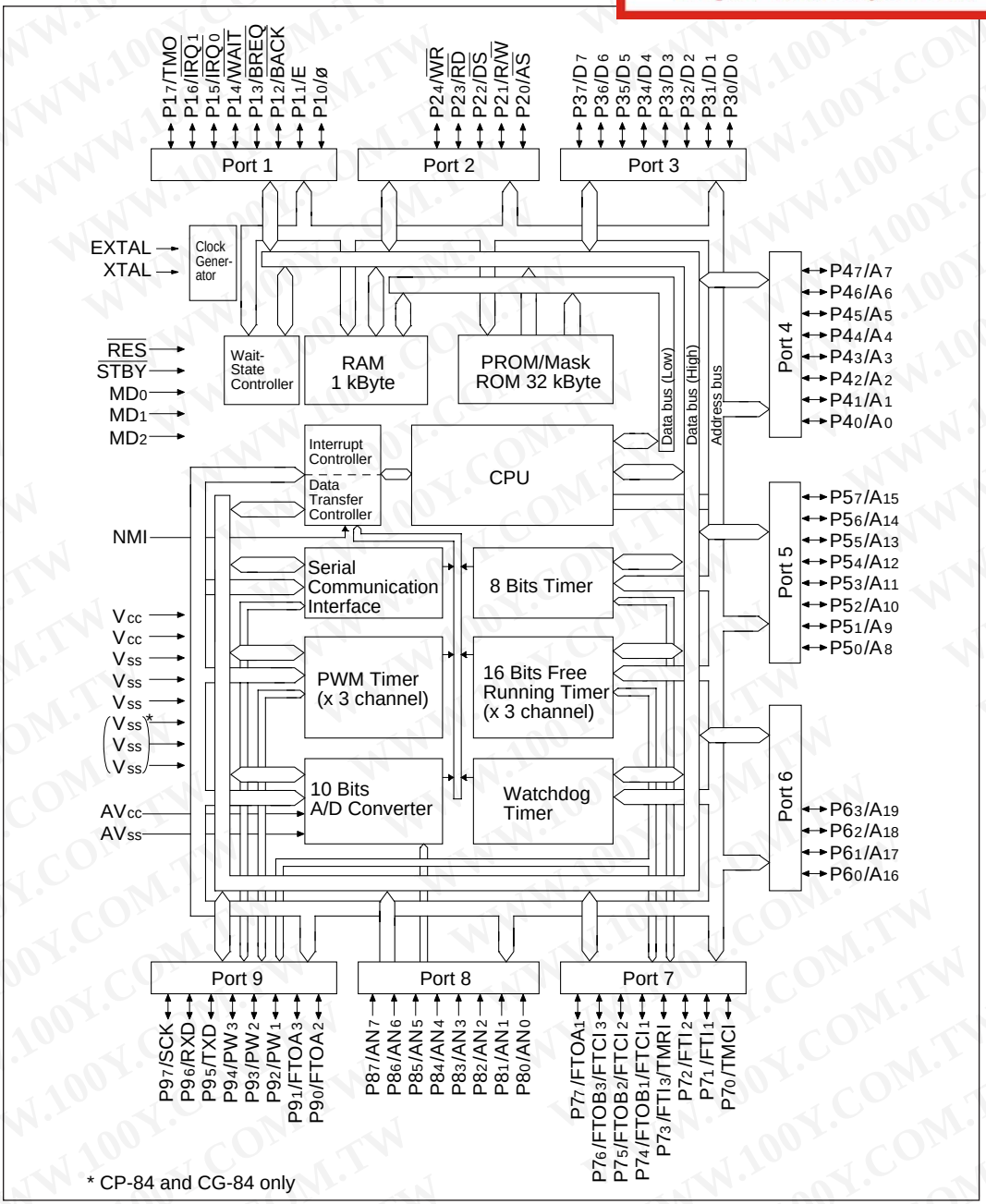

Figure 1-1 Block Diagram

1.3 Pin Arrangements and Functions

1.3.1 Pin Arrangement

Figure 1-2 shows the pin arrangement of the CP-84 package. Figure 1-3 shows the pin arrangement of the CG-84 package. Figure 1-4 shows the pin arrangement of the FP-80A package.

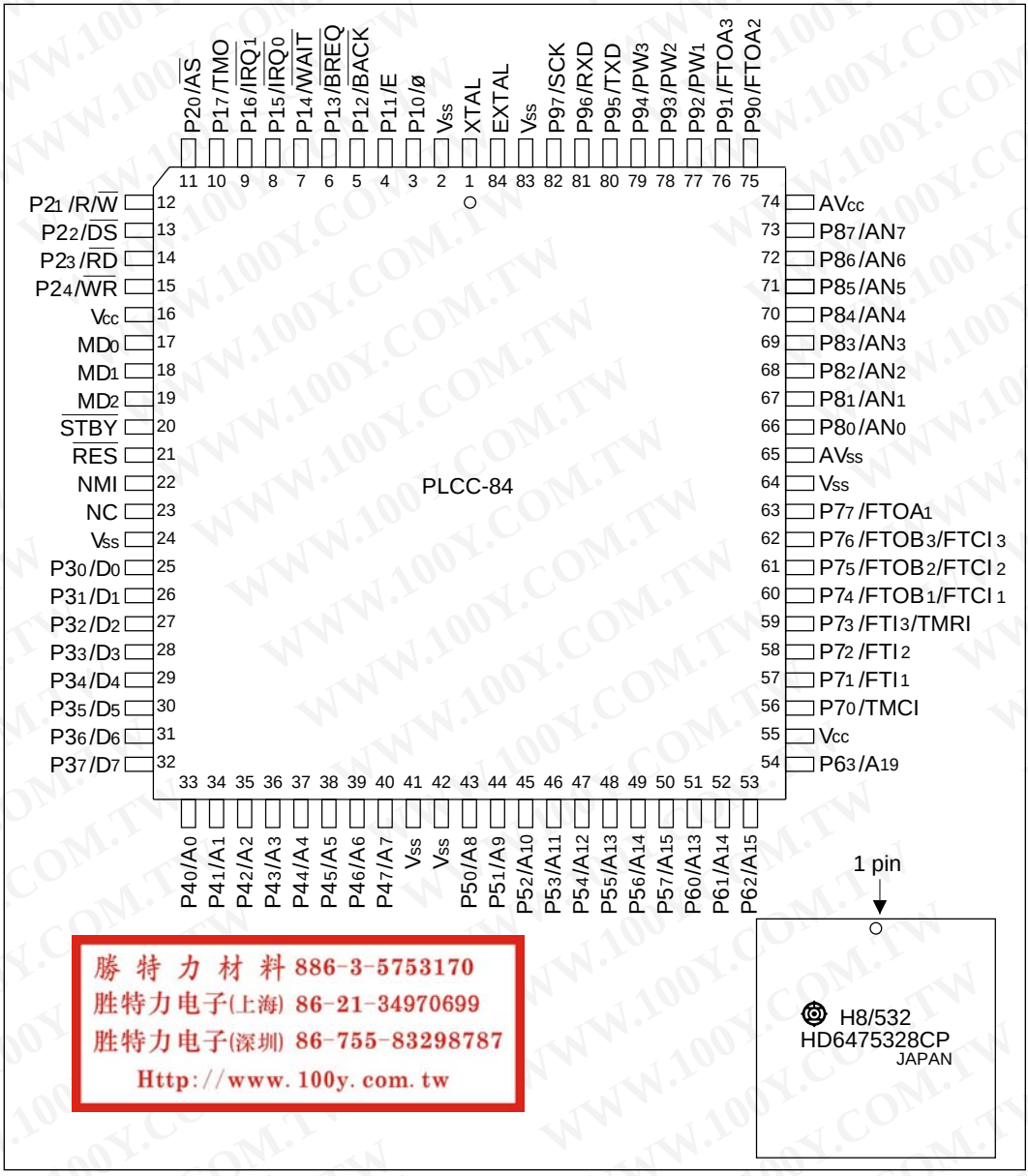

Figure 1-2 Pin Arrangement (CP-84, Top View)