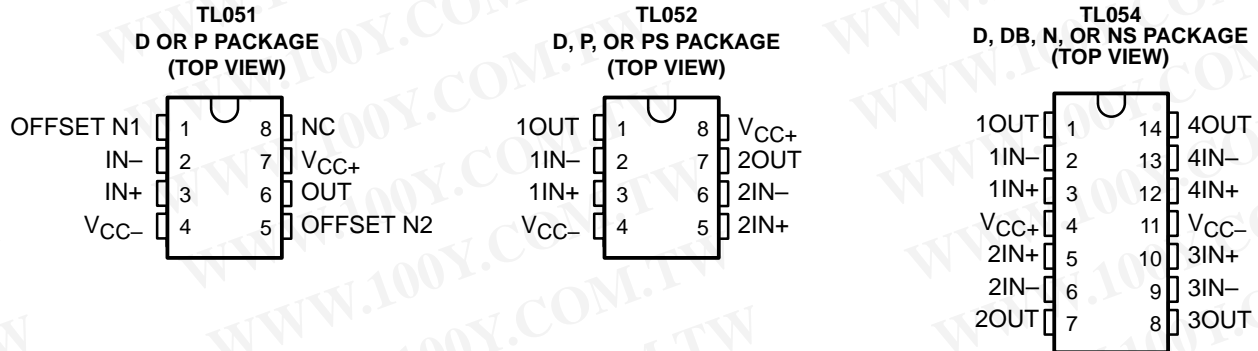


# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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- Direct Upgrades to TL07x and TL08x BiFET Operational Amplifiers
- Faster Slew Rate (20 V/ $\mu$ s Typ) Without Increased Power Consumption
- On-Chip Offset-Voltage Trimming for Improved DC Performance and Precision Grades Are Available (1.5 mV, TL051A)



## description/ordering information

The TL05x series of JFET-input operational amplifiers offers improved dc and ac characteristics over the TL07x and TL08x families of BiFET operational amplifiers. On-chip Zener trimming of offset voltage yields precision grades as low as 1.5 mV (TL051A) for greater accuracy in dc-coupled applications. Texas Instruments improved BiFET process and optimized designs also yield improved bandwidth and slew rate without increased power consumption. The TL05x devices are pin-compatible with the TL07x and TL08x and can be used to upgrade existing circuits or for optimal performance in new designs.

BiFET operational amplifiers offer the inherently higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. This makes them better suited for interfacing with high-impedance sensors or very low-level ac signals. They also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption.

The TL05x family was designed to offer higher precision and better ac response than the TL08x, with the low noise floor of the TL07x. Designers requiring significantly faster ac response or ensured lower noise should consider the Excalibur TLE208x and TLE207x families of BiFET operational amplifiers.

Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required, and loads should be terminated to a virtual-ground node at mid-supply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

The TL05x are fully specified at  $\pm 15$  V and  $\pm 5$  V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC-prefix) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to the slew rate and bandwidth requirements, and also the output loading.

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## ORDERING INFORMATION

TA	V <sub>IO</sub> max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	800 μV	PDIP (P)	Tube of 50	TL051ACP	TL051ACP	
				TL052ACP	TL052ACP	
		SOIC (D)	Tube of 75	TL051ACD	051AC	
				Tube of 75	TL052ACD	052AC
	Reel of 2500				TL052ACDR	
	1.5 mV	PDIP (P)	Tube of 50	TL051CP	TL051CP	
				TL052CP	TL052CP	
		PDIP (N)	Tube of 25	TL054ACN	TL054ACN	
				SOIC (D)	Tube of 75	TL051CD
		Reel of 2500	TL051CDR			
			Tube of 75			TL052CD
		Reel of 2500		TL052CDR		
			Tube of 50	TL054ACD	TL054C	
		Reel of 2500		TL054ACDR		
		SOP (PS)	Reel of 2000	TL052CPSR	TL052	
	SSOP (DB)	Reel of 2000	TL054CDBR	TL054		
	4 mV	PDIP (N)	Tube of 25	TL054CN	TL054CN	
				SOIC (D)	Tube of 50	TL054CD
Reel of 2500		TL054CDR				
		SOP (NS)	Reel of 2000			TL054CNSR
-40°C to 85°C	800 μV	PDIP (P)	Tube of 50	TL052AIP	TL052AI	
				SOIC (D)	Tube of 75	TL052AID
		Reel of 2500	TL052AIDR			
	1.5 mV	PDIP (N)	Tube of 25	TL054AIN	TL054AIN	
				PDIP (P)	Tube of 50	TL051IP
		TL052IP	TL052IP			
		SOIC (D)	Tube of 75			TL051ID
				Tube of 75	TL052ID	TL052I
					Reel of 2500	
	Tube of 50	TL054AID	TL054AI			
		Reel of 2500		TL054AIDR		
	4 mV	PDIP (N)	Tube of 25	TL054IN	TL054IN	
SOIC (D)				Tube of 50	TL054ID	TL054I
		Reel of 2500	TL054IDR			

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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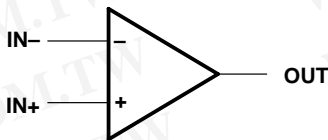


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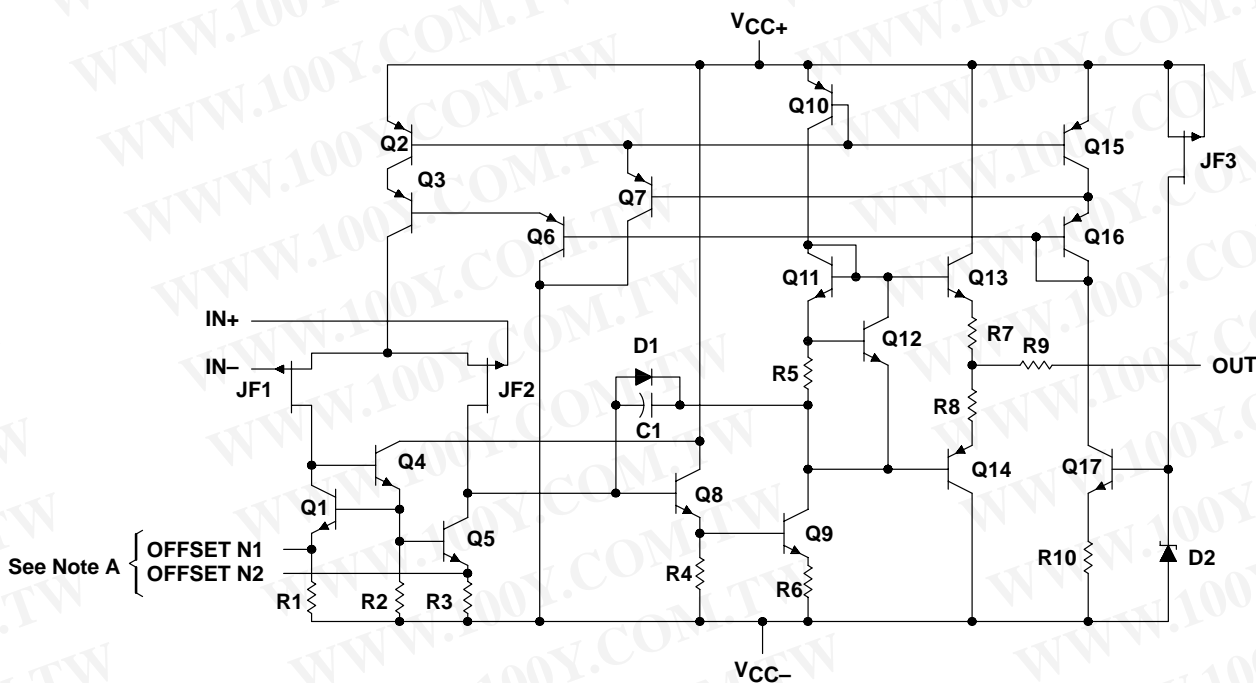
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symbol (each amplifier)



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equivalent schematic (each amplifier)



NOTE A: OFFSET N1 and OFFSET N2 are available only on the TL051x.

ACTUAL DEVICE COMPONENT COUNT†			
COMPONENT	TL051	TL052	TL054
Transistors	20	34	62
Resistors	10	19	37
Diodes	2	3	5
Capacitors	1	2	4

† These figures include all four amplifiers and all ESD, bias, and trim circuitry.

# TL05x, TL05xA

## ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (see Note 1)	18 V
Supply voltage, $V_{CC-}$ (see Note 1)	-18 V
Differential input voltage (see Note 2)	$\pm 30$ V
Input voltage range, $V_I$ (any input, see Notes 1 and 3)	$\pm 15$ V
Input current, $I_I$ (each input)	$\pm 1$ mA
Output current, $I_O$ (each output)	$\pm 80$ mA
Total current into $V_{CC+}$	160 mA
Total current out of $V_{CC-}$	160 mA
Duration of short-circuit current at (or below) 25°C	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 4 and 5):	
D package (8 pin)	97°C/W
D package (14 pin)	86°C/W
DB package (14 pin)	96°C/W
N package (14 pin)	80°C/W
NS package (14 pin)	76°C/W
P package (8 pin)	85°C/W
PS package (8 pin)	95°C/W
Operating virtual junction temperature, $T_J$	150°C
Lead temperature 1,6 mm (1/16inch) from case for 10 seconds	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at  $IN+$  with respect to  $IN-$ .
  3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
  4. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

		C SUFFIX		I SUFFIX		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC\pm}$	Supply voltage	$\pm 5$	$\pm 15$	$\pm 5$	$\pm 15$	V
$V_{IC}$	Common-mode input voltage	$V_{CC\pm} = \pm 5$ V		-1	4	V
		$V_{CC\pm} = \pm 15$ V		-11	11	
$T_A$	Operating free-air temperature	0	70	-40	85	°C

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL051C and TL051AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL051C, TL051AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage		TL051C	25°C	0.75 3.5		0.59 1.5		mV	
			Full range	4.5		2.5			
		TL051AC	25°C	0.55 2.8		0.35 0.8			
			Full range	3.8		1.8			
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage‡	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL051C	25°C to 70°C		8		8	μV/°C	
		TL051AC	25°C to 70°C		8		25		
Input offset-voltage long-term drift§		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5	25°C	4 100		5 100		pA		
		70°C	0.02 1		0.025 1		nA		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5	25°C	20 200		30 200		pA		
		70°C	0.15 4		0.2 4		nA		
V <sub>ICR</sub> Common-mode input voltage range		25°C	-1 to 4 -2.3 to 5.6		-11 to 11 -12.3 to 15.6		V		
		Full range	-1 to 4		-11 to 11				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	3 4.2		13 13.9		V		
		Full range	3		13				
	R <sub>L</sub> = 2 kΩ	25°C	2.5 3.8		11.5 12.7				
		Full range	2.5		11.5				
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	-2.5 -3.5		-12 -13.2		V		
		Full range	-2.5		-12				
	R <sub>L</sub> = 2 kΩ	25°C	-2.3 -3.2		-11 -12				
		Full range	-2.3		-11				
A <sub>VD</sub> Large-signal differential voltage amplification¶	R <sub>L</sub> = 2 kΩ	25°C	25 59		50 105		V/mV		
		0°C	30 65		60 129				
		70°C	20 46		30 85				
r <sub>i</sub> Input resistance		25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance		25°C	10		12		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	65 85		75 93		dB		
		0°C	65 84		75 92				
		70°C	65 84		75 91				
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	75 99		75 99		dB		
		0°C	75 98		75 98				
		70°C	75 97		75 97				
I <sub>CC</sub> Supply current	V <sub>O</sub> = 0, No load	25°C	2.6 3.2		2.7 3.2		mA		
		0°C	2.7 3.2		2.8 3.2				
		70°C	2.6 3.2		2.7 3.2				

† Full range is 0°C to 70°C.

‡ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset-voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C, extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V, or for V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL051C and TL051AC operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL051C, TL051AC			UNIT			
			V <sub>CC±</sub> = ±5 V		V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX		MIN	TYP	MAX
SR+	Positive slew rate at unity gain‡	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figure 1	25°C	16		13	20	V/μs	
			Full range	16.4		11	22.6		
SR-	Negative slew rate at unity gain‡	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figure 1	25°C	15		13	18		
			Full range	16		11	19.3		
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figures 1 and 2	25°C	55		56		ns	
			0°C	54		55			
			70°C	63		63			
t <sub>f</sub>	Fall time		25°C	55		57			
			0°C	54		56			
			70°C	62		64			
Overshoot factor		V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figures 1 and 2	25°C	24		19		%	
			0°C	24		19			
			70°C	24		19			
V <sub>n</sub>	Equivalent input noise voltage§		R <sub>S</sub> = 20 Ω, See Figure 3	f = 10 Hz	25°C		75		nV/√Hz
				f = 1 kHz	25°C		18	30	
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage			f = 10 Hz to 10 kHz	25°C		4		μV
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C	0.01		0.01		pA/√Hz	
THD	Total harmonic distortion¶	R <sub>S</sub> = 1 kΩ, f = 1 kHz, R <sub>L</sub> = 2 kΩ	25°C	0.003		0.003		%	
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, C <sub>L</sub> = 25 pF, R <sub>L</sub> = 2 kΩ, See Figure 4	25°C	3		3.1		MHz	
			0°C	3.2		3.3			
			70°C	2.7		2.8			
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, C <sub>L</sub> = 25 pF, R <sub>L</sub> = 2 kΩ, See Figure 4	25°C	59		62		deg	
			0°C	58		62			
			70°C	59		62			

† Full range is 0°C to 70°C.

‡ For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V.

§ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O(RMS)</sub> = 1 V; for V<sub>CC±</sub> = ±15 V, V<sub>O(RMS)</sub> = 6 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL051I and TL051AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub> †	TL051I, TL051AI						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage		TL051I	25°C	0.75 3.5		0.59 1.5		mV		
			Full range	5.3		3.3				
			TL051AI	25°C	0.55 2.8		0.35 0.8			
				Full range	4.6		2.6			
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage‡		TL051I	25°C to 85°C	7		8		μV/°C		
			TL051AI	25°C to 85°C	8		8 25			
Input offset-voltage long-term drift§			25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5		25°C	4 100		5 100		pA		
			85°C	0.06 10		0.07 10		nA		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5		25°C	20 200		30 200		pA		
			85°C	0.6 20		0.7 20		nA		
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1 to 4 -2.3 to 5.6		-11 to 11 -12.3 to 15.6		V		
			Full range	-1 to 4		-11 to 11				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3 4.2		13 13.9		V		
			Full range	3		13				
	R <sub>L</sub> = 2 kΩ	25°C	2.5 3.8		11.5 12.7					
		Full range	2.5		11.5					
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-2.5 -3.5		-12 -13.2		V		
			Full range	-2.5		-12				
	R <sub>L</sub> = 2 kΩ	25°C	-2.3 -3.2		-11 -12					
		Full range	-2.3		-11					
A <sub>VD</sub> Large-signal differential voltage amplification¶	R <sub>L</sub> = 2 kΩ		25°C	25 59		50 105		V/mV		
			-40°C	30 74		60 145				
			85°C	20 43		30 76				
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	10		12		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	65 85		75 93		dB		
			-40°C	65 83		75 90				
			85°C	65 84		75 93				
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	75 99		75 99		dB		
			-40°C	75 98		75 98				
			85°C	75 99		75 99				
I <sub>CC</sub> Supply current	V <sub>O</sub> = 0, No load		25°C	2.6 3.2		2.7 3.2		mA		
			-40°C	2.4 3.2		2.6 3.2				
			85°C	2.5 3.2		2.6 3.2				

† Full range is -40°C to 85°C

‡ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

§ Typical values are based on the input offset-voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C, extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V, or for V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL051I and TL051AI operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL051I, TL051AI			UNIT			
			V <sub>CC±</sub> = ±5 V		V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX				
SR+	Positive slew rate at unity gain‡	25°C	16		13	20	V/μs		
			Full range			11			
SR-	Negative slew rate at unity gain‡	25°C		15		13		18	
			Full range			11			
t <sub>r</sub>	Rise time	25°C		55		56		ns	
		-40°C	52		53				
		85°C	64		65				
t <sub>f</sub>	Fall time	25°C	55		57				
		-40°C	51		53				
		85°C	64		65				
Overshoot factor		25°C	24		19		%		
		-40°C	24		19				
		85°C	24		19				
V <sub>n</sub>	Equivalent input noise voltage§	R <sub>S</sub> = 20 Ω, See Figure 3	f = 10 Hz	25°C		75		nV/√Hz	
			f = 1 kHz	25°C		18			30
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4		μV	
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C	0.01		0.01		pA/√Hz	
THD	Total harmonic distortion¶	R <sub>S</sub> = 1 kΩ, f = 1 kHz	R <sub>L</sub> = 2 kΩ, 25°C	0.003		0.003		%	
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, C <sub>L</sub> = 25 pF,	R <sub>L</sub> = 2 kΩ, See Figure 4	25°C	3		3.1		MHz
				-40°C	3.5		3.6		
				85°C	2.6		2.7		
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, C <sub>L</sub> = 25 pF,	R <sub>L</sub> = 2 kΩ, See Figure 4	25°C	59		62		deg
				-40°C	58		61		
				85°C	59		62		

† Full range is -40°C to 85°C.

‡ For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V.

§ This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O(RMS)</sub> = 1 V; for V<sub>CC±</sub> = ±15 V, V<sub>O(RMS)</sub> = 6 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS178A – FEBRUARY 1997 - REVISED FEBRUARY 2003

## TL052C and TL052AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub> †	TL052C, TL052AC						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL052C	25°C	0.73 3.5		0.65 1.5		mV		
			Full range	4.5		2.5				
		TL052AC	25°C	0.51 2.8		0.4 0.8				
			Full range	3.8		1.8				
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage‡		TL052C	25°C to 70°C	8		8		μV/°C		
		TL052AC	25°C to 70°C	8		6 25				
Input offset-voltage long-term drift§	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	V <sub>IC</sub> = 0,	25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0,	25°C	4 100		5 100		pA		
			70°C	0.02 1		0.025 1		nA		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0,	25°C	20 200		30 200		pA		
			70°C	0.15 4		0.2 4		nA		
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1 to 4 -2.3 to 5.6		-11 to 11 -12.3 to 15.6		V		
			Full range	-1 to 4		-11 to 11				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C		3 4.2		13 13.9		V		
		Full range		3		13				
	R <sub>L</sub> = 2 kΩ	25°C		2.5 3.8		11.5 12.7				
		Full range		2.5		11.5				
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C		-2.5 -3.5		-12 -13.2		V		
		Full range		-2.5		-12				
	R <sub>L</sub> = 2 kΩ	25°C		-2.3 -3.2		-11 -12				
		Full range		-2.3		-11				
A <sub>VD</sub> Large-signal differential voltage amplification¶	R <sub>L</sub> = 2 kΩ		25°C	25 59		50 105		V/mV		
			0°C	30 65		60 129				
			70°C	20 46		30 85				
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	10		12		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω		25°C	65 85		75 93		dB		
			0°C	65 84		75 92				
			70°C	65 84		75 91				

† Full range is 0°C to 70°C.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or non-testing of other parameters.

§ Typical values are based on the input offset-voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C, extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS178A – FEBRUARY 1997 - REVISED FEBRUARY 2003

## TL052C and TL052AC electrical characteristics at specified free-air temperature (continued)

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL052C, TL052AC						UNIT	
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	75	99		75	99	dB	
			0°C	75	98		75	98		
			70°C	75	97		75	97		
I <sub>CC</sub>	Supply current (two amplifiers)	V <sub>O</sub> = 0, No load	25°C		4.6	5.6		4.8	5.6	mA
			0°C		4.7	6.4		4.8	6.4	
			70°C		4.4	6.4		4.6	6.4	
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	A <sub>VD</sub> = 100	25°C		120			120	dB	

## TL052C and TL052AC operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL052C, TL052AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Slew rate at unity gain	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figure 1	25°C		17.8		9	20.7	V/μs
SR-	Negative slew rate at unity gain‡		Full range				8		
			25°C		15.4		9	17.8	
			Full range				8		
t <sub>r</sub>	Rise time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figures 1 and 2	25°C		55			56	ns
			0°C		54			55	
			70°C		63			63	
t <sub>f</sub>	Fall time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figures 1 and 2	25°C		55			57	ns
			0°C		54			56	
			70°C		62			64	
Overshoot factor			25°C		24			19	%
			0°C		24			19	
			70°C		24			19	
V <sub>n</sub>	Equivalent input noise voltage§	R <sub>S</sub> = 20 Ω, See Figure 3	f = 10 Hz	25°C		71		71	nV/√Hz
			f = 1 kHz	25°C		19		19	
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise current	f = 10 Hz to 10 kHz	25°C		4			4	μV
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz	25°C		0.01			0.01	pA/√Hz
THD	Total harmonic distortion¶	R <sub>S</sub> = 1 kΩ, R <sub>L</sub> = 2 kΩ, f = 1 kHz	25°C		0.003			0.003	%
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 25 pF, See Figure 4	25°C		3			3	MHz
			0°C		3.2			3.2	
			70°C		2.6			2.7	
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 25 pF, See Figure 4	25°C		60			63	deg
			0°C		59			63	
			70°C		60			63	

† Full range is 0°C to 70°C.

‡ For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V.

§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O(RMS)</sub> = 1 V; for V<sub>CC±</sub> = ±15 V, V<sub>O(RMS)</sub> = 6 V.



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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS178A – FEBRUARY 1997 - REVISED FEBRUARY 2003

## TL052I and TL052AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub> †	TL052I, TL052AI						UNIT
				V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage		TL052I	25°C	0.73 3.5		0.65 1.5		mV		
			Full range	5.3		3.3				
			TL052AI	25°C	0.51 2.8		0.4 0.8			
				Full range	4.6		2.6			
α <sub>V<sub>IO</sub></sub> Temperature coefficient‡		TL052I	25°C to 85°C	7		6		μV/°C		
			TL052AI	25°C to 85°C	6		6 25			
Input offset-voltage long-term drift§	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	V <sub>IC</sub> = 0,	25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0,	25°C	4 100		5 100		pA		
			85°C	0.06 10		0.07 10		nA		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, See Figure 5	V <sub>IC</sub> = 0,	25°C	20 200		30 200		pA		
			85°C	0.6 20		0.7 20		nA		
V <sub>ICR</sub> Common-mode input voltage range			25°C	-1 to 4	-2.3 to 5.6	-11 to 11	-12.3 to 15.6	V		
			Full range	-1 to 4		-11 to 11				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	3 4.2		13 13.9		V		
			Full range	3		13				
	R <sub>L</sub> = 2 kΩ	25°C	2.5 3.8		11.5 12.7					
		Full range	2.5		11.5					
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ		25°C	-2.5 -3.5		-12 -13.2		V		
			Full range	-2.5		-12				
	R <sub>L</sub> = 2 kΩ	25°C	-2.3 -3.2		-11 -12					
		Full range	-2.3		-11					
A <sub>VD</sub> Large-signal differential voltage amplification¶	R <sub>L</sub> = 2 kΩ		25°C	25 59		50 105		V/mV		
			-40°C	30 74		60 145				
			85°C	20 43		30 76				
r <sub>i</sub> Input resistance			25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance			25°C	10		12		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0,	R <sub>S</sub> = 50 Ω	25°C	65 85		75 93		dB		
			-40°C	65 83		75 90				
			85°C	65 84		75 93				

† Full range is -40°C to 85°C.

‡ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters

§ Typical values are based on the input offset-voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C, extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.

¶ At V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V; at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL052I and TL052AI electrical characteristics at specified free-air temperature (continued)

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	TL052I, TL052AI						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
k <sub>SVR</sub> Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	75	99		75	99	dB	
		-40°C	75	98		75	98		
		85°C	75	99		75	99		
I <sub>CC</sub> Supply current (two amplifiers)	V <sub>O</sub> = 0, No load	25°C		4.6	5.6		4.8	5.6	mA
		-40°C		4.5	6.4		4.7	6.4	
		85°C		4.4	6.4		4.6	6.4	
V <sub>O1</sub> /V <sub>O2</sub> Crosstalk attenuation	A <sub>V</sub> D = 100	25°C		120		120		dB	

## TL052I and TL052AI operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL052I, TL052AI						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR+ Slew rate at unity gain‡	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figure 1	25°C		17.8		9	20.7	V/μs	
SR- Negative slew rate at unity gain‡		Full range				8			
		25°C		15.4		9	17.8		
		Full range				8			
t <sub>r</sub> Rise time	V <sub>I(PP)</sub> = ±10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, See Figures 1 and 2	25°C		55		56	ns		
t <sub>f</sub> Fall time		-40°C		52		53			
		85°C		64		65			
		25°C		55		57			
Overshoot factor		-40°C		51		53		%	
		85°C		64		65			
		25°C		24%		19%			
V <sub>n</sub> Equivalent input noise voltage§		R <sub>S</sub> = 20 Ω, See Figure 3	f = 10 Hz	25°C		71		71	nV/√Hz
			f = 1 kHz	25°C		19		19	
V <sub>N(PP)</sub> Peak-to-peak equivalent input noise current		f = 10 Hz to 10 kHz	25°C		4		4	μV	
I <sub>n</sub> Equivalent input noise current	f = 1 kHz	25°C		0.01		0.01	pA/√Hz		
THD Total harmonic distortion¶	R <sub>S</sub> = 1 kΩ, R <sub>L</sub> = 2 kΩ, f = 1 kHz	25°C		0.003		0.003	%		
B <sub>1</sub> Unity-gain bandwidth	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 25 pF, See Figure 4	25°C		3		3	MHz		
		-40°C		3.5		3.6			
		85°C		2.5		2.6			
φ <sub>m</sub> Phase margin at unity gain	V <sub>I</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 25 pF, See Figure 4	25°C		60		63	deg		
		-40°C		58		61			
		85°C		60		63			

† Full range is -40°C to 85°C.

‡ For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V.

§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O(RMS)</sub> = 1 V; for V<sub>CC±</sub> = ±15 V, V<sub>O(RMS)</sub> = 6 V.



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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TL054C and TL054AC electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL054C, TL054AC						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL054C	25°C	0.64 5.5		0.56 4		mV	
			Full range	7.7		6.2			
		TL054AC	25°C	0.57 3.5		0.5 1.5			
			Full range	5.7		3.7			
α <sub>V<sub>IO</sub></sub> Temperature coefficient of input offset voltage	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, R <sub>S</sub> = 50 Ω	TL054C	25°C to 70°C	25		23		μV/°C	
		TL054AC	25°C to 70°C	24		23			
Input offset-voltage long-term drift‡		25°C	0.04		0.04		μV/mo		
I <sub>IO</sub> Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5	25°C	4 100		5 100		pA		
		70°C	0.02 1		0.025 1		nA		
I <sub>IB</sub> Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5	25°C	20 200		30 200		pA		
		70°C	0.15 4		0.2 4		nA		
V <sub>ICR</sub> Common-mode input voltage range		25°C	-1 to 4	-2.3 to 5.6	-11 to 11	-12.3 to 15.6	V		
		Full range	-1 to 4		-11 to 11				
V <sub>OM+</sub> Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	3 4.2		13 13.9		V		
		Full range	3		13				
	R <sub>L</sub> = 2 kΩ	25°C	2.5 3.8		11.5 12.7				
		Full range	2.5		11.5				
V <sub>OM-</sub> Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	-2.5 -3.5		-12 -13.2		V		
		Full range	-2.5		-12				
	R <sub>L</sub> = 2 kΩ	25°C	-2.3 -3.2		-11 -12				
		Full range	-2.3		-11				
A <sub>VD</sub> Large-signal differential voltage amplification§	R <sub>L</sub> = 2 kΩ	25°C	25 72		50 133		V/mV		
		0°C	30 88		60 173				
		70°C	20 57		30 85				
r <sub>i</sub> Input resistance		25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω		
c <sub>i</sub> Input capacitance		25°C	10		12		pF		
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	65 84		75 92		dB		
		0°C	65 84		75 92				
		70°C	65 84		75 93				
k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±5 V to ±15 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	75 99		75 99		dB		
		0°C	75 99		75 99				
		70°C	75 99		75 99				
I <sub>CC</sub> Supply current (four amplifiers)	V <sub>O</sub> = 0, No load	25°C	8.1 11.2		8.4 11.2		mA		
		0°C	8.2 12.8		8.5 12.8				
		70°C	7.9 11.2		8.2 11.2				
V <sub>O1</sub> /V <sub>O2</sub> Crosstalk attenuation	A <sub>VD</sub> = 100	25°C	120		120		dB		

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset-voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C, extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.

§ For V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V, at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V.B

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS178A – FEBRUARY 1997 - REVISED FEBRUARY 2003

## TL054C and TL054AC operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL054C, TL054C						UNIT	
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V				
			MIN	TYP	MAX	MIN	TYP	MAX		
SR+	Positive slew rate at unity gain		25°C	15.4			10 17.8			V/μs
		0°C	15.7			8 17.9				
		70°C	14.4			8 17.5				
SR-	Negative slew rate at unity gain‡		25°C	13.9			10 15.9			
		0°C	14.3			8 16.1				
		70°C	13.3			8 15.5				
t <sub>r</sub>	Rise time		25°C	55			56			ns
		0°C	54			55				
		70°C	63			63				
t <sub>f</sub>	Fall time		25°C	55			57			
		0°C	54			56				
		70°C	62			64				
	Overshoot factor		25°C	24%			19%			%
		0°C	24%			19%				
		70°C	24%			19				
V <sub>n</sub>	Equivalent input noise voltage§		f = 10 Hz	25°C			75			nV/√Hz
			f = 1 kHz	25°C			21 45			
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C			4			
I <sub>n</sub>	Equivalent input noise current		f = 1 kHz	25°C			0.01			pA/√Hz
THD	Total harmonic distortion¶		R <sub>S</sub> = 1 kΩ, R <sub>L</sub> = 2 kΩ, f = 1 kHz	25°C			0.003			%
B <sub>1</sub>	Unity-gain bandwidth		V <sub>I</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 25 pF, See Figure 4	25°C			2.7			MHz
				0°C			3			
				70°C			2.4			
φ <sub>m</sub>	Phase margin at unity gain		V <sub>I</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 25 pF, See Figure 4	25°C			61			deg
				0°C			60			
				70°C			61			

† Full range is 0°C to 70°C.

‡ For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V.

§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O(RMS)</sub> = 1 V; for V<sub>CC±</sub> = ±15 V, V<sub>O(RMS)</sub> = 6 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS178A – FEBRUARY 1997 - REVISED FEBRUARY 2003

## TL054I and TL054AI electrical characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL054I, TL054AI						UNIT
			V <sub>CC±</sub> = ±5 V			V <sub>CC±</sub> = ±15 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	TL054I	25°C	0.64 5.5		0.56 4		mV	
			Full range	8.8		7.3			
		TL054AI	25°C	0.57 3.5		0.5 1.5			
			Full range	6.8		4.8			
α <sub>V<sub>IO</sub></sub>	Temperature coefficient of input offset voltage	TL054I	25°C to 85°C	25		24		μV/°C	
		TL054AI	25°C to 85°C	25		23			
	Input offset voltage long-term drift‡		25°C	0.04		0.04		μV/mo	
I <sub>IO</sub>	Input offset current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5	25°C	4	100	5	100	pA	
			85°C	0.06	10	0.07	10	nA	
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 0, V <sub>IC</sub> = 0, See Figure 5	25°C	20	200	30	200	pA	
			85°C	0.6	20	0.7	20	nA	
V <sub>ICR</sub>	Common-mode input voltage range		25°C	-1 to 4	-2.3 to 5.6	-11 to 11	-12.3 to 15.6	V	
			Full range	-1 to 4		-11 to 11			
V <sub>OM+</sub>	Maximum positive peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	3	4.2	13	13.9	V	
			Full range	3		13			
		R <sub>L</sub> = 2 kΩ	25°C	2.5	3.8	11.5	12.7		
			Full range	2.5		11.5			
V <sub>OM-</sub>	Maximum negative peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	-2.5	-3.5	-12	-13.2	V	
			Full range	-2.5		-12			
		R <sub>L</sub> = 2 kΩ	25°C	-2.3	-3.2	-11	-12		
			Full range	-2.3		-11			
A <sub>VD</sub>	Large-signal differential voltage amplification§	R <sub>L</sub> = 2 kΩ	25°C	25	72	50	133	V/mV	
			-40°C	30	101	60	212		
			85°C	20	50	30	70		
r <sub>i</sub>	Input resistance		25°C	10 <sup>12</sup>		10 <sup>12</sup>		Ω	
c <sub>i</sub>	Input capacitance		25°C	10		12		pF	
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	65	84	75	92	dB	
			-40°C	65	83	75	92		
			85°C	65	84	75	93		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±5 V to ±15 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C	75	99	75	99	dB	
			-40°C	75	98	75	99		
			85°C	75	99	75	99		
I <sub>CC</sub>	Supply current (four amplifiers)	V <sub>O</sub> = 0, No load	25°C	8.1	11.2	8.4	11.2	mA	
			-40°C	7.9	12.8	8.2	12.8		
			85°C	7.6	11.2	7.9	11.2		
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	A <sub>VD</sub> = 100	25°C	120		120		dB	

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T<sub>A</sub> = 150°C, extrapolated to T<sub>A</sub> = 25°C using the Arrhenius equation, and assuming an activation energy of 0.96 eV.

§ For V<sub>CC±</sub> = ±5 V, V<sub>O</sub> = ±2.3 V, at V<sub>CC±</sub> = ±15 V, V<sub>O</sub> = ±10 V.

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS178A – FEBRUARY 1997 - REVISED FEBRUARY 2003

## TL054I and TL054AI operating characteristics at specified free-air temperature

PARAMETER	TEST CONDITIONS	T <sub>A</sub> †	TL054I, TL054AI			UNIT	
			V <sub>CC±</sub> = ±5 V		V <sub>CC±</sub> = ±15 V		
			MIN	TYP	MAX		
SR+	Positive slew rate at unity gain	25°C	15.4		10	17.8	V/μs
		-40°C	16.4		8	18	
		85°C	14		8	17.3	
SR-	Negative slew rate at unity gain‡	25°C	13.9		10	15.9	
		-40°C	14.7		8	16.1	
		85°C	13		8	15.3	
t <sub>r</sub>	Rise time	25°C	55		56		ns
		-40°C	52		53		
		85°C	64		65		
t <sub>f</sub>	Fall time	25°C	55		57		
		-40°C	51		53		
		85°C	64		65		
	Overshoot factor	25°C	24		19		%
		-40°C	24		19		
		85°C	24		19		
V <sub>n</sub>	Equivalent input noise voltage§	R <sub>S</sub> = 20 Ω, See Figure 3	f = 10 Hz	25°C	75		nV/√Hz
			f = 1 kHz	25°C	21	21	
V <sub>N(PP)</sub>	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C	4		μV
I <sub>n</sub>	Equivalent input noise current	f = 1 kHz		25°C	0.01		pA/√Hz
THD	Total harmonic distortion¶	R <sub>S</sub> = 1 kΩ, f = 1 kHz	R <sub>L</sub> = 2 kΩ,	25°C	0.003%		%
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, C <sub>L</sub> = 25 pF,	R <sub>L</sub> = 2 kΩ, See Figure 4	25°C	2.7		MHz
				-40°C	3.3		
				85°C	2.3		
φ <sub>m</sub>	Phase margin at unity gain	V <sub>I</sub> = 10 mV, C <sub>L</sub> = 25 pF,	R <sub>L</sub> = 2 kΩ, See Figure 4	25°C	61		deg
				-40°C	59		
				85°C	61		

† Full range is -40°C to 85°C.

‡ For V<sub>CC±</sub> = ±5 V, V<sub>I(PP)</sub> = ±1 V; for V<sub>CC±</sub> = ±15 V, V<sub>I(PP)</sub> = ±5 V.

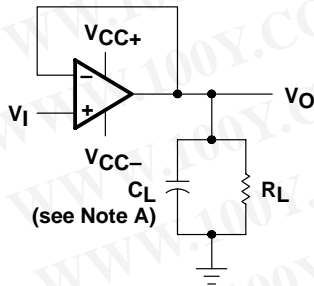
§ This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

¶ For V<sub>CC±</sub> = ±5 V, V<sub>O(RMS)</sub> = 1 V; for V<sub>CC±</sub> = ±15 V, V<sub>O(RMS)</sub> = 6 V.

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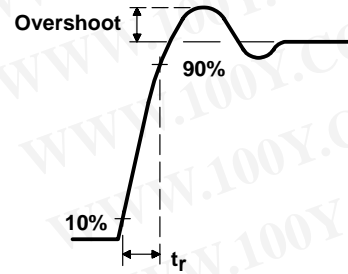


**PARAMETER MEASUREMENT INFORMATION**

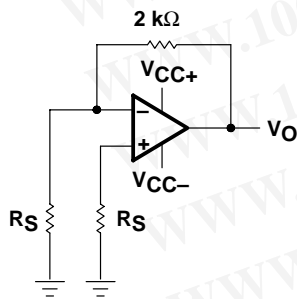


NOTE A:  $C_L$  includes fixture capacitance.

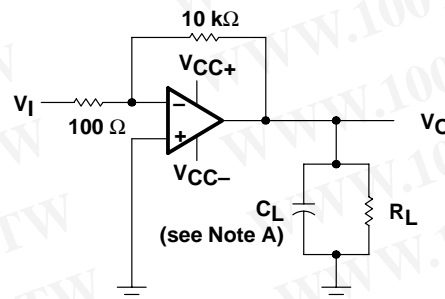
**Figure 1. Slew Rate, Rise/Fall Time, and Overshoot Test Circuit**



**Figure 2. Rise-Time and Overshoot Waveform**



**Figure 3. Noise-Voltage Test Circuit**



NOTE A:  $C_L$  includes fixture capacitance.

**Figure 4. Unity-Gain Bandwidth and Phase-Margin Test Circuit**

**typical values**

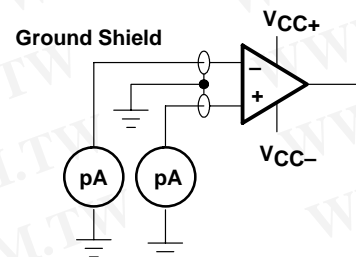
Typical values, as presented in this data sheet represent the median (50% point) of device parametric performance.

**input bias and offset current**

At the picoamp-bias-current level typical of the TL05x and TL05xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test-socket leakages easily can exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device then is inserted in the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements then are subtracted algebraically to determine the bias current of the device.

**noise**

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample tested at  $f = 1$  kHz. Texas Instruments also has additional noise-testing capability to meet specific application requirements. Please contact the factory for details.



**Figure 5. Input-Bias and Offset-Current Test Circuit**

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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

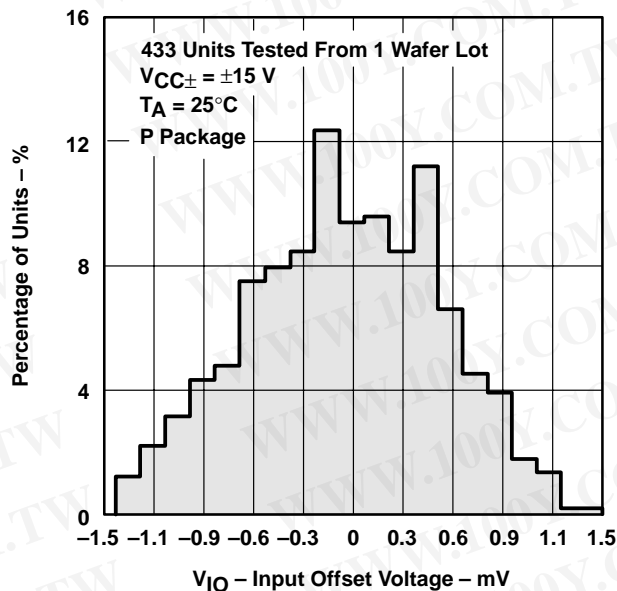
			<b>FIGURE</b>
$V_{IO}$	Input offset voltage	Distribution	6–11
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	Distribution	12, 13, 14
$I_{IB}$	Input bias current	vs Common-mode input voltage vs Free-air temperature	15 16
$I_{IO}$	Input offset current	vs Free-air temperature	16
$V_{IC}$	Common-mode input voltage range limits	vs Supply voltage vs Free-air temperature	17 18
$V_O$	Output voltage	vs Differential input voltage	19, 20
$V_{OM}$	Maximum peak output voltage	vs Supply voltage vs Output current vs Free-air temperature	21 25, 26 27, 28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	22, 23, 24
$A_{VD}$	Large-signal differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	29 30 31, 32, 33
$CMRR$	Common-mode rejection ratio	vs Frequency vs Free-air temperature	34, 35 36
$z_o$	Output impedance	vs Frequency	37
$k_{SVR}$	Supply-voltage rejection ratio	vs Free-air temperature	38
$I_{OS}$	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	39 40 41
$I_{CC}$	Supply current	vs Supply voltage vs Free-air temperature	42, 43, 44 45, 46, 47
$SR$	Slew rate	vs Load resistance vs Free-air temperature	48–53 54–59
	Overshoot factor	vs Load capacitance	60
$V_n$	Equivalent input noise voltage	vs Frequency	61, 62
$THD$	Total harmonic distortion	vs Frequency	63
$B_1$	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	64, 65, 66 67, 68, 69
$\phi_m$	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	70, 71, 72 73, 74, 75 76, 77, 78
	Phase shift	vs Frequency	30
	Voltage-follower small-signal pulse response	vs Time	79
	Voltage-follower large-signal pulse response	vs Time	80

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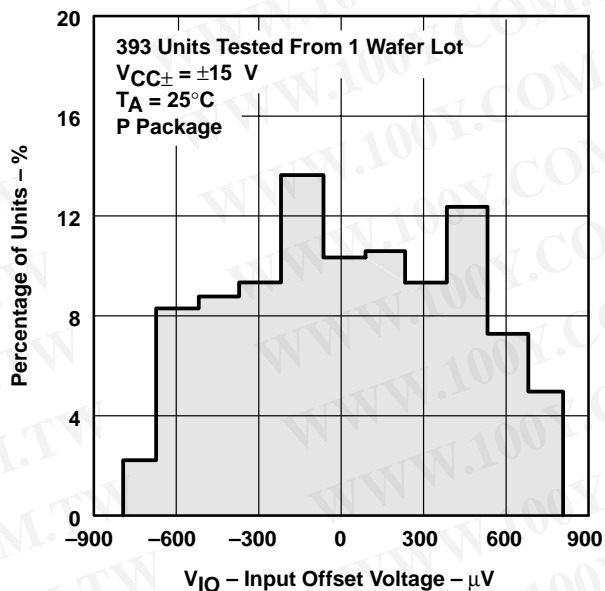
**TYPICAL CHARACTERISTICS**

**DISTRIBUTION OF TL051  
 INPUT OFFSET VOLTAGE**



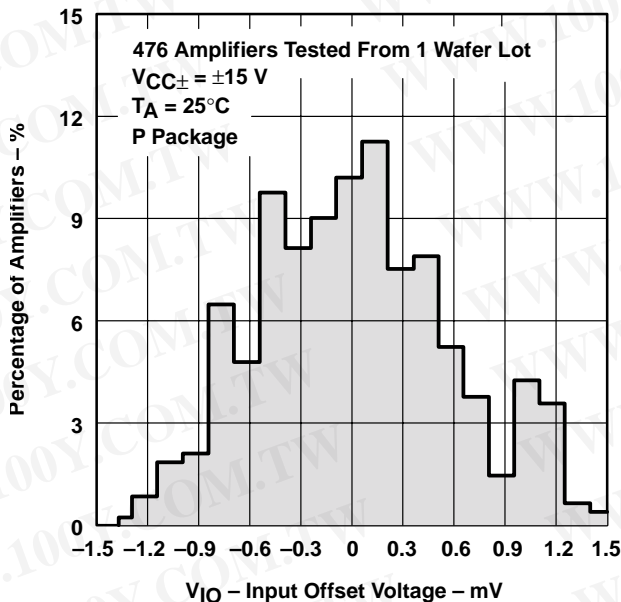
**Figure 6**

**DISTRIBUTION OF TL051A  
 INPUT OFFSET VOLTAGE**



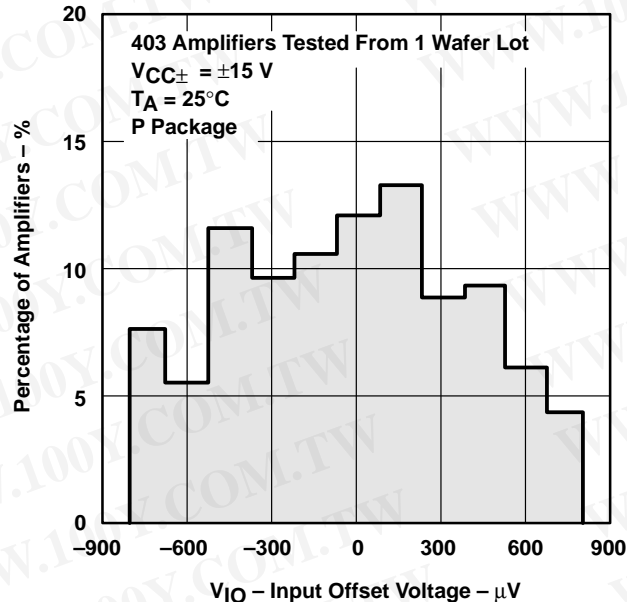
**Figure 7**

**DISTRIBUTION OF TL052  
 INPUT OFFSET VOLTAGE**



**Figure 8**

**DISTRIBUTION OF TL052A  
 INPUT OFFSET VOLTAGE**



**Figure 9**

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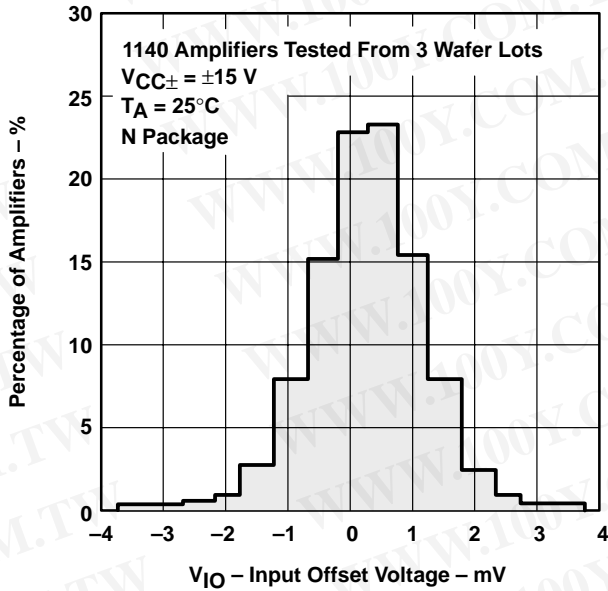
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**ENHANCED-JFET LOW-OFFSET**  
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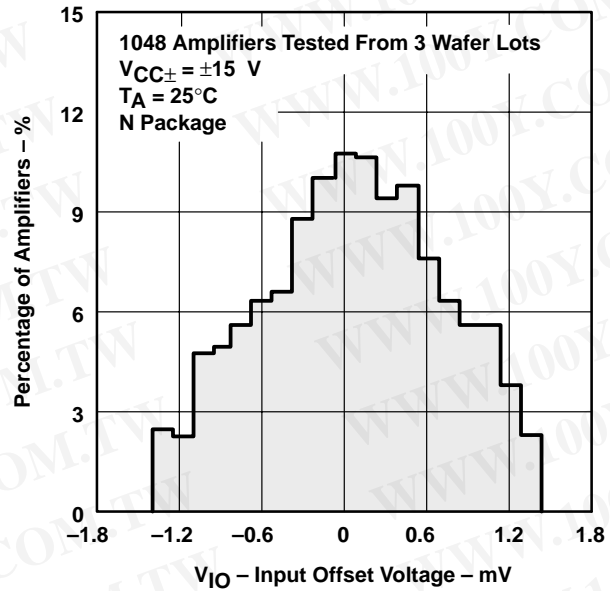
**TYPICAL CHARACTERISTICS**

**DISTRIBUTION OF TL054**  
**INPUT OFFSET VOLTAGE**



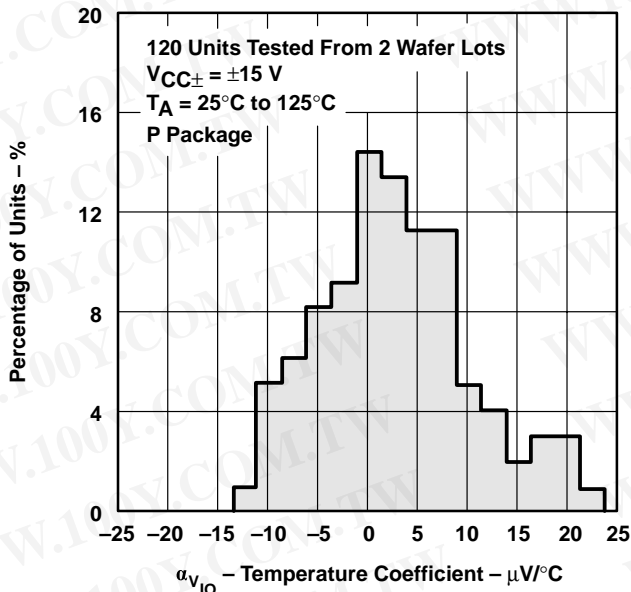
**Figure 10**

**DISTRIBUTION OF TL054A**  
**INPUT OFFSET VOLTAGE**



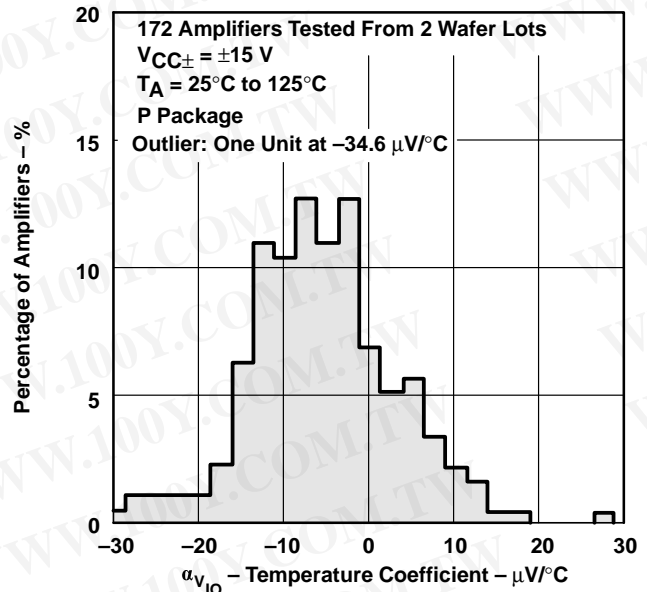
**Figure 11**

**DISTRIBUTION OF TL051**  
**INPUT OFFSET VOLTAGE**  
**TEMPERATURE COEFFICIENT**



**Figure 12**

**DISTRIBUTION OF TL052**  
**INPUT OFFSET VOLTAGE**  
**TEMPERATURE COEFFICIENT**

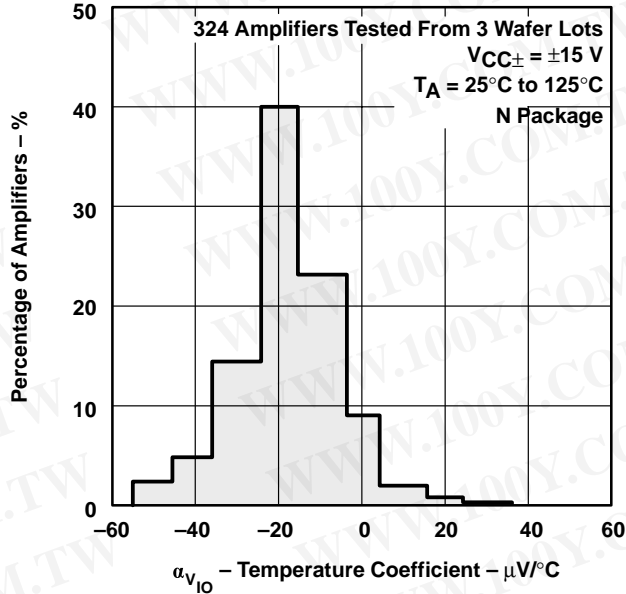


**Figure 13**



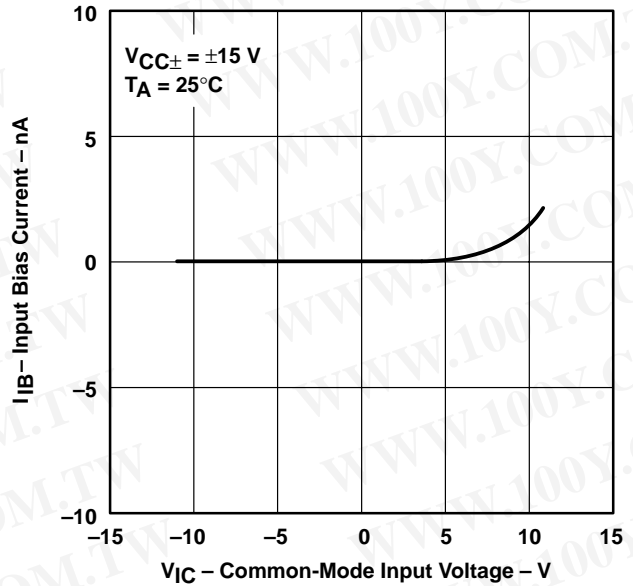
**TYPICAL CHARACTERISTICS**

**DISTRIBUTION OF TL054  
 INPUT OFFSET VOLTAGE  
 TEMPERATURE COEFFICIENT**



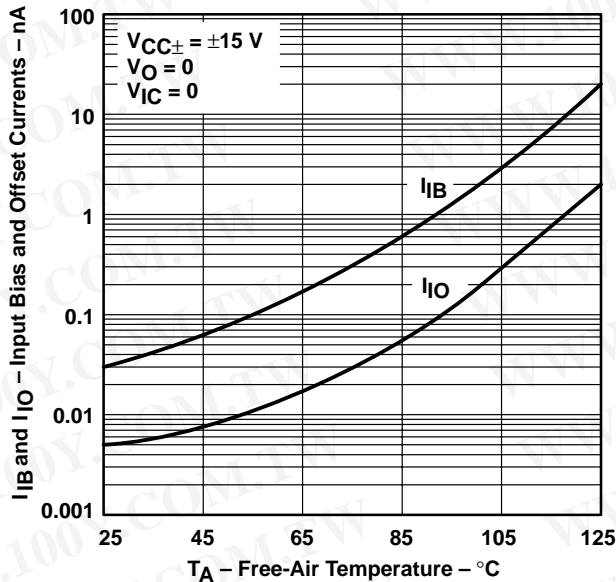
**Figure 14**

**INPUT BIAS CURRENT  
 vs  
 COMMON-MODE INPUT VOLTAGE**



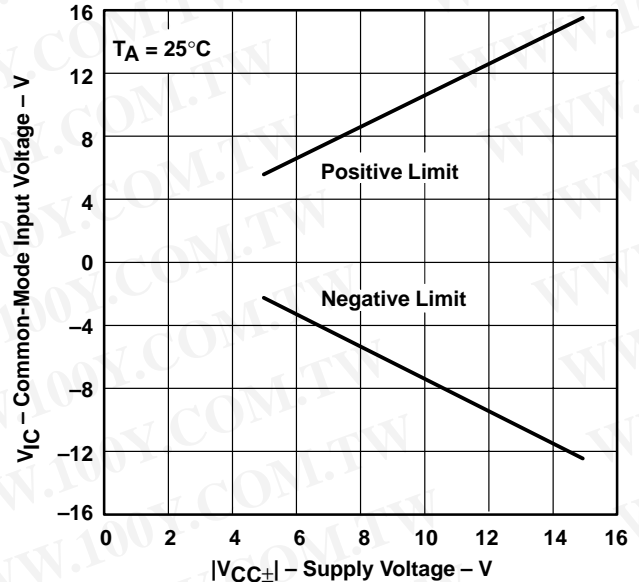
**Figure 15**

**INPUT BIAS CURRENT AND  
 INPUT OFFSET CURRENT†  
 vs  
 FREE-AIR TEMPERATURE**



**Figure 16**

**COMMON-MODE  
 INPUT VOLTAGE RANGE LIMITS  
 vs  
 SUPPLY VOLTAGE**



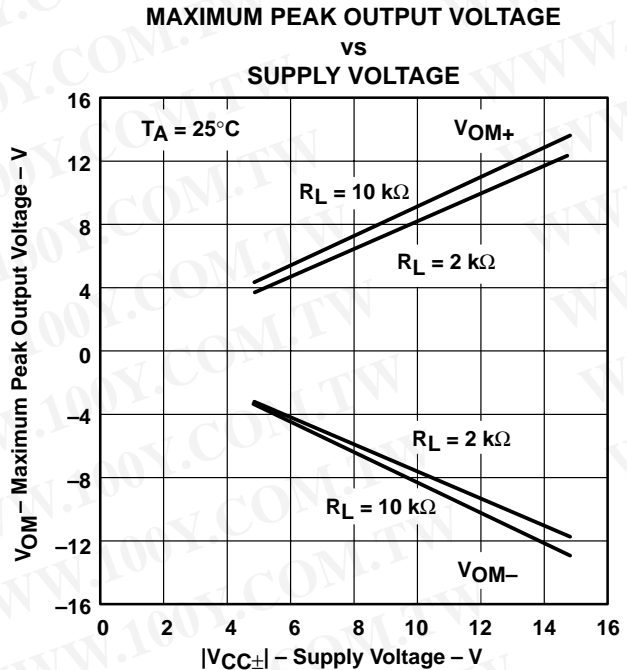
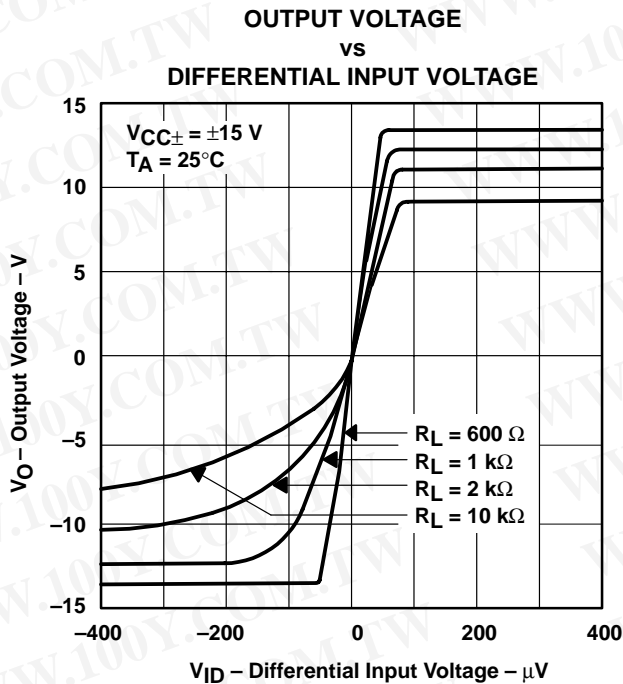
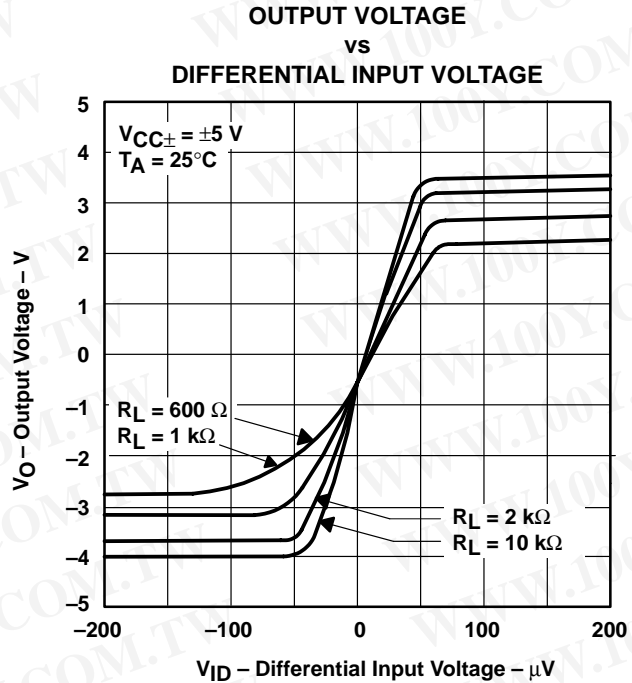
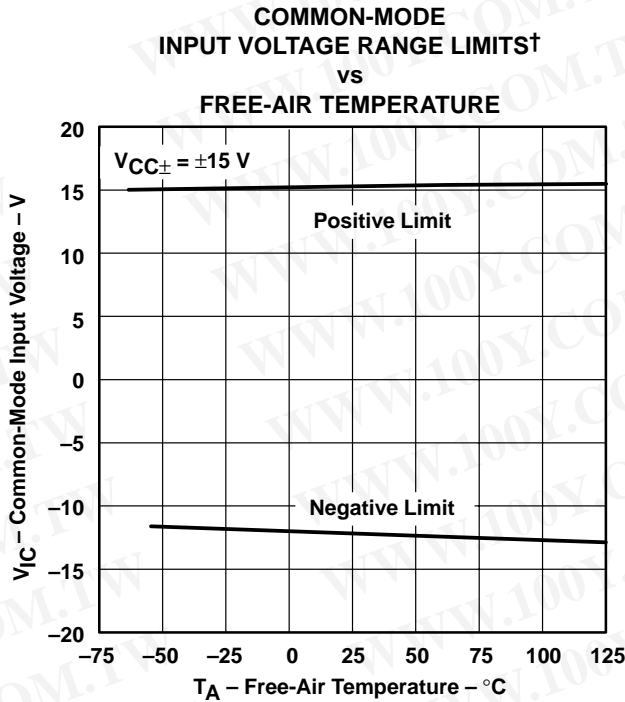
**Figure 17**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
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**TYPICAL CHARACTERISTICS**



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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**TYPICAL CHARACTERISTICS**

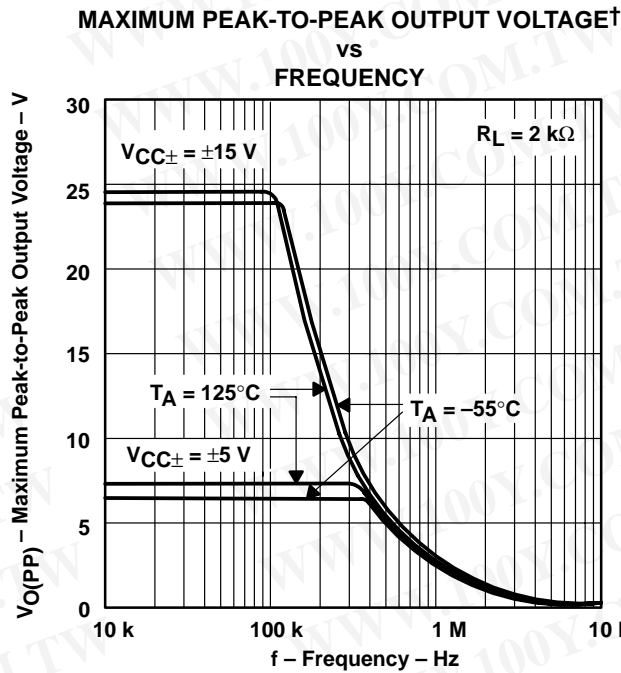


Figure 22

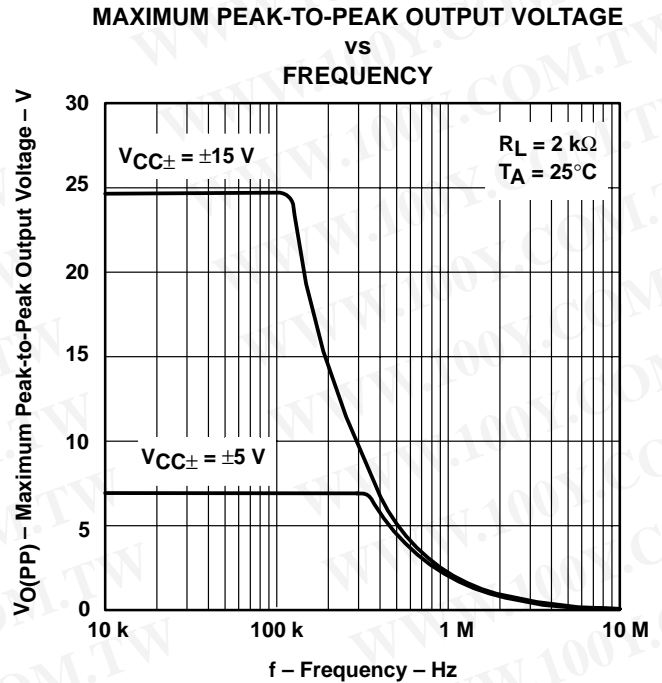


Figure 23

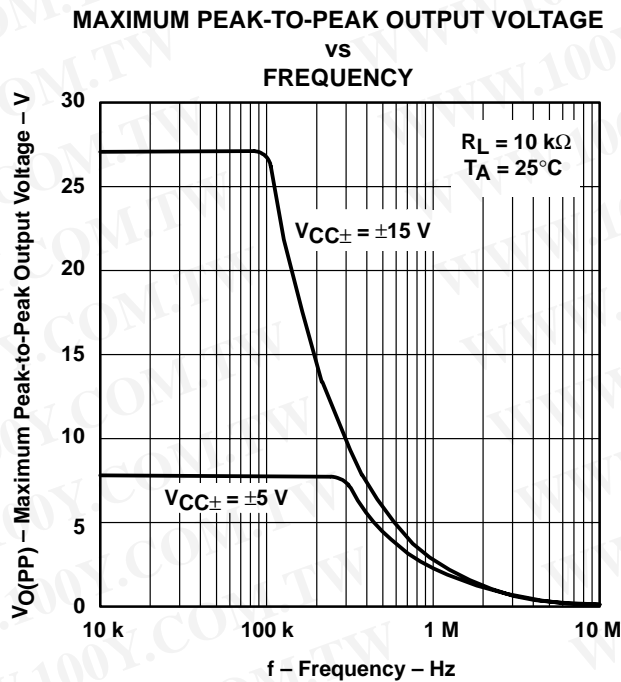


Figure 24

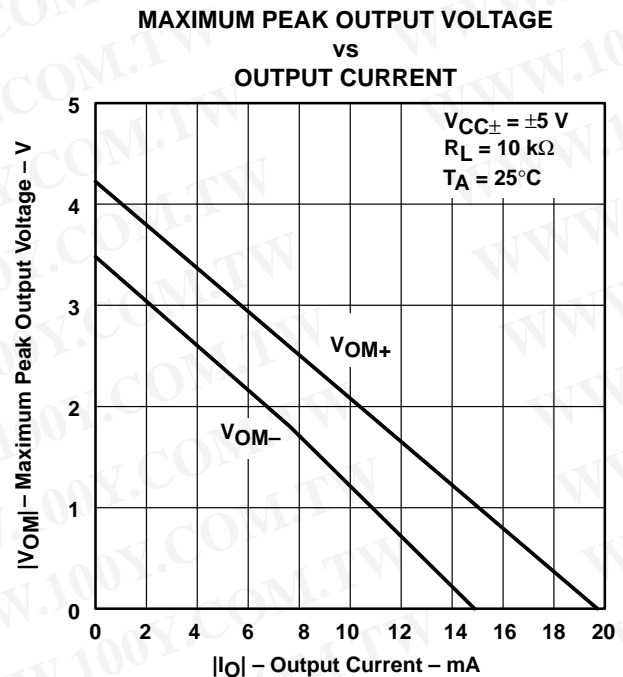


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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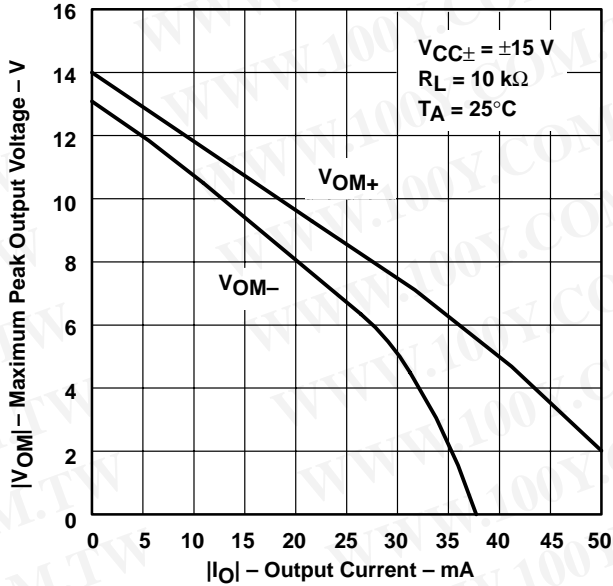


**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
**OPERATIONAL AMPLIFIERS**

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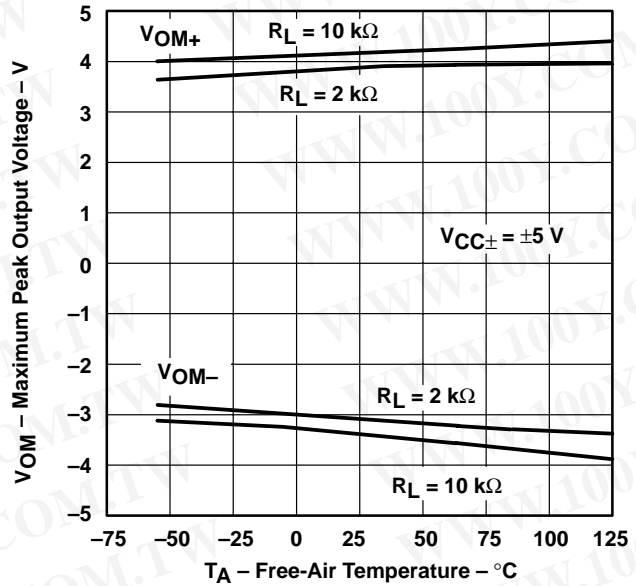
**TYPICAL CHARACTERISTICS**

**MAXIMUM PEAK OUTPUT VOLTAGE**  
**vs**  
**OUTPUT CURRENT**



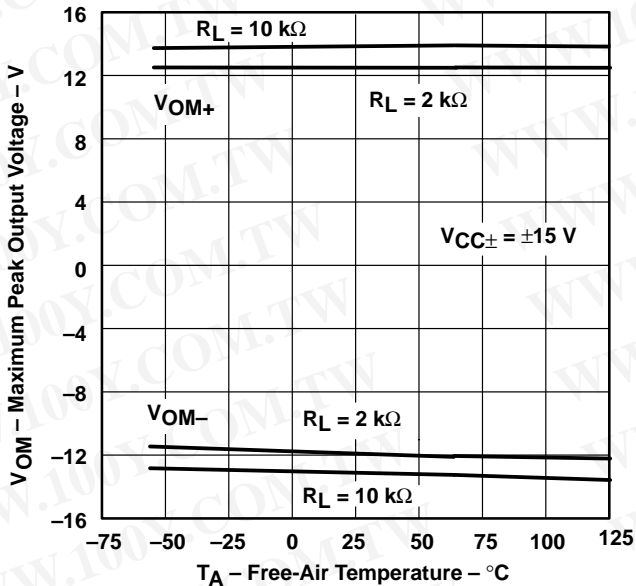
**Figure 26**

**MAXIMUM PEAK OUTPUT VOLTAGE†**  
**vs**  
**FREE-AIR TEMPERATURE**



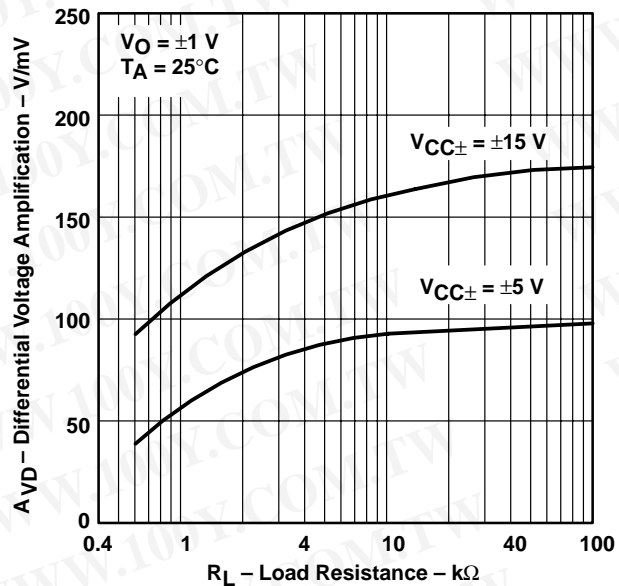
**Figure 27**

**MAXIMUM PEAK OUTPUT VOLTAGE†**  
**vs**  
**FREE-AIR TEMPERATURE**



**Figure 28**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE**  
**AMPLIFICATION**  
**vs**  
**LOAD RESISTANCE**



**Figure 29**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS  
 LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT  
 VS  
 FREQUENCY

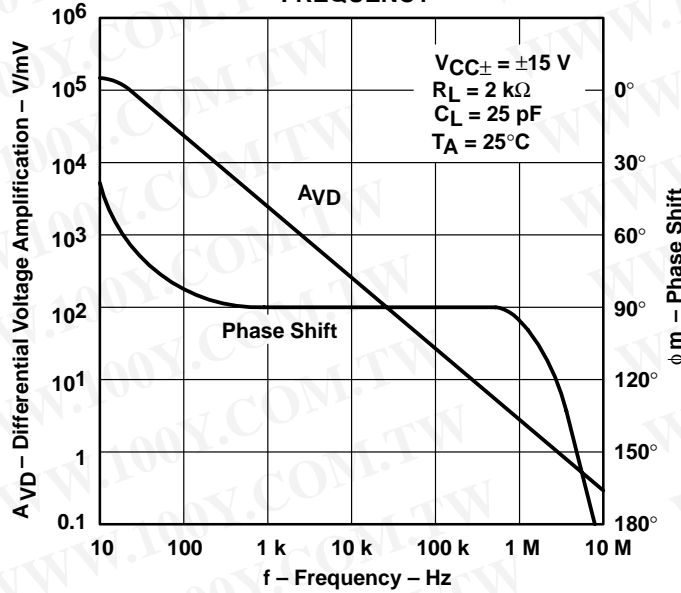


Figure 30

TL051 AND TL052  
 LARGE-SIGNAL DIFFERENTIAL  
 VOLTAGE AMPLIFICATION†  
 VS  
 FREE-AIR TEMPERATURE

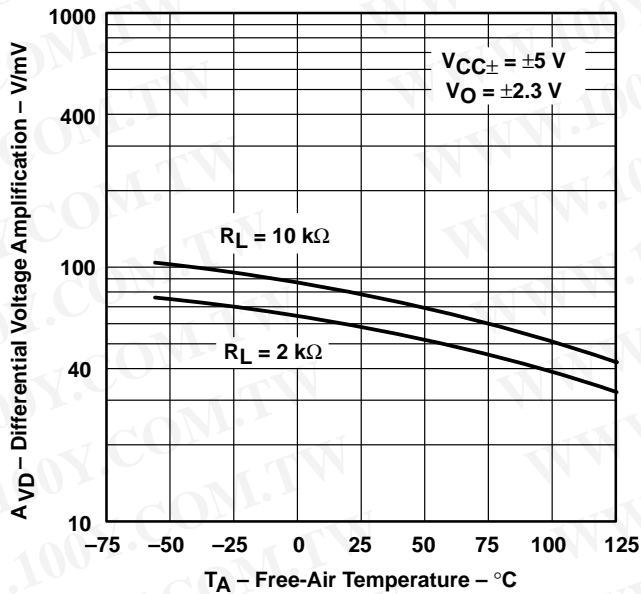


Figure 31

TL054  
 LARGE-SIGNAL DIFFERENTIAL  
 VOLTAGE AMPLIFICATION†  
 VS  
 FREE-AIR TEMPERATURE

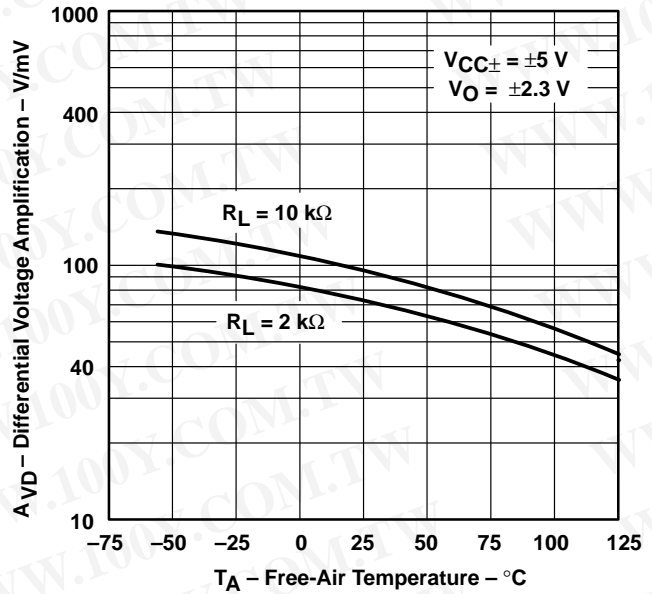


Figure 32

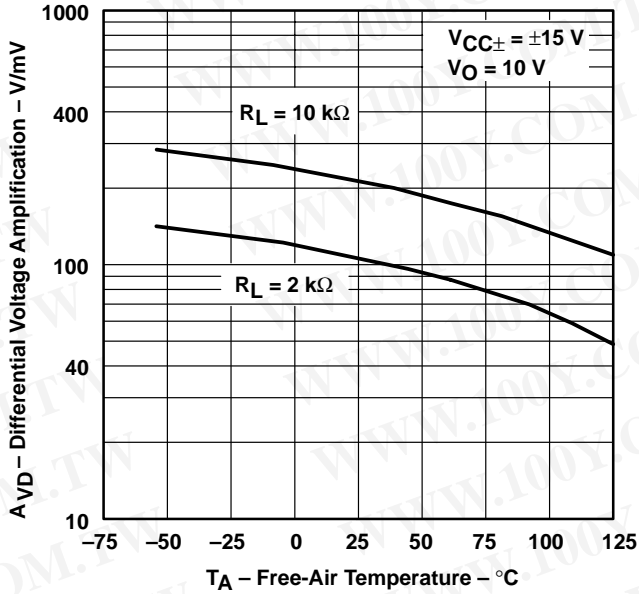
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
**OPERATIONAL AMPLIFIERS**

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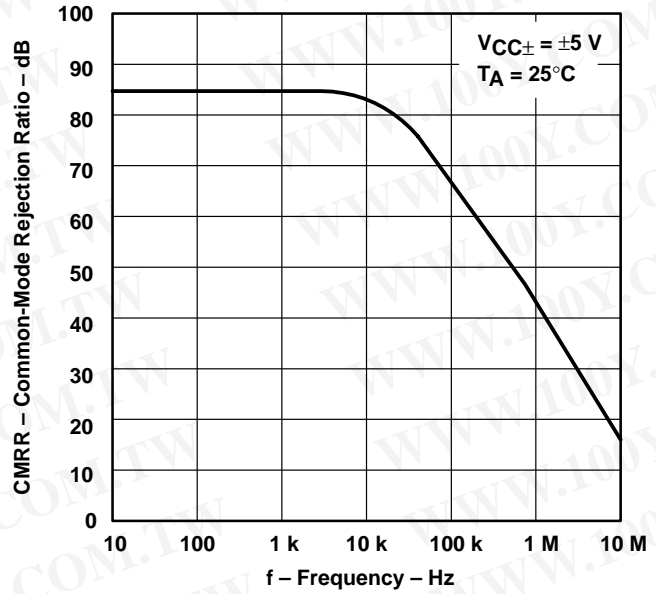
**TYPICAL CHARACTERISTICS**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†**  
**vs**  
**FREE-AIR TEMPERATURE**



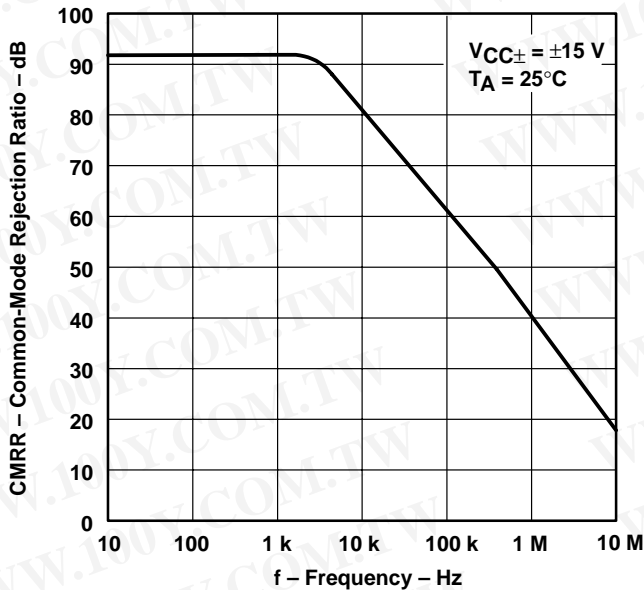
**Figure 33**

**COMMON-MODE REJECTION RATIO**  
**vs**  
**FREQUENCY**



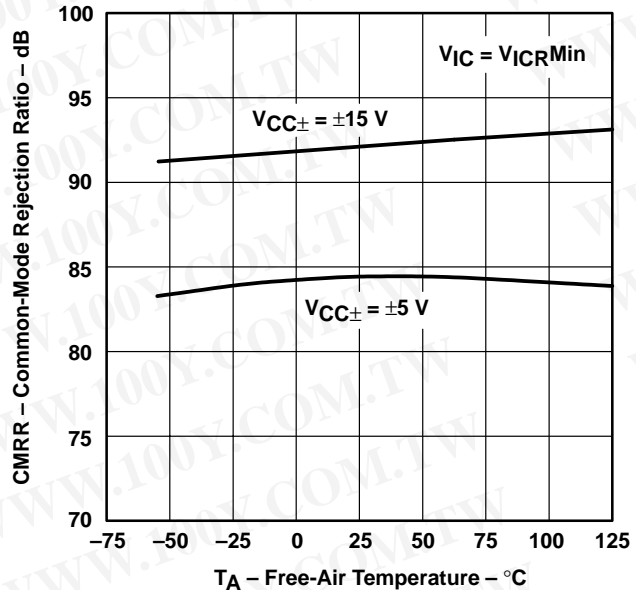
**Figure 34**

**COMMON-MODE REJECTION RATIO**  
**vs**  
**FREQUENCY**



**Figure 35**

**COMMON-MODE REJECTION RATIO†**  
**vs**  
**FREE-AIR TEMPERATURE**



**Figure 36**

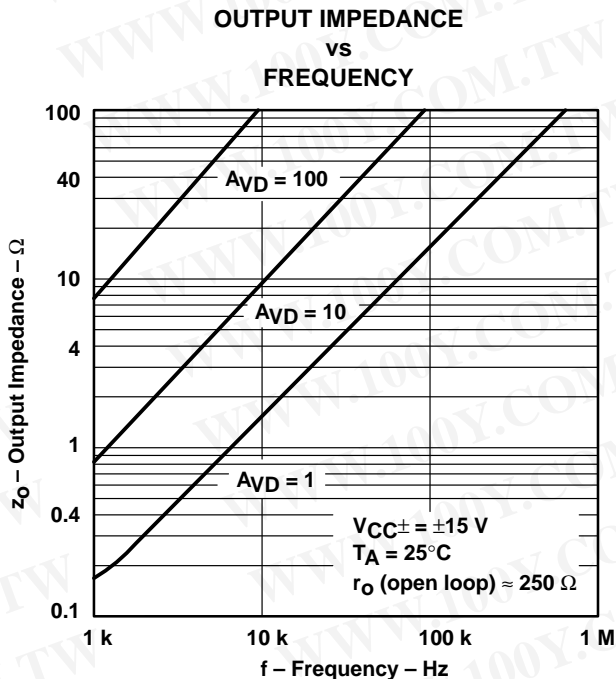
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



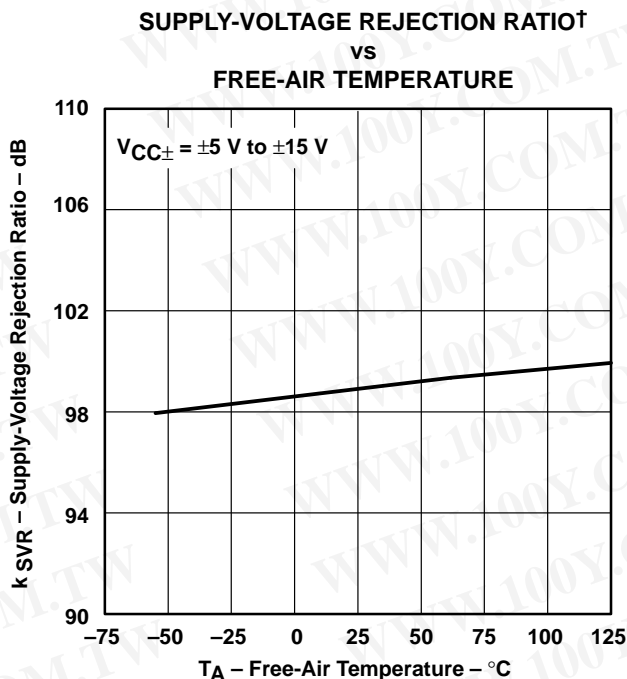
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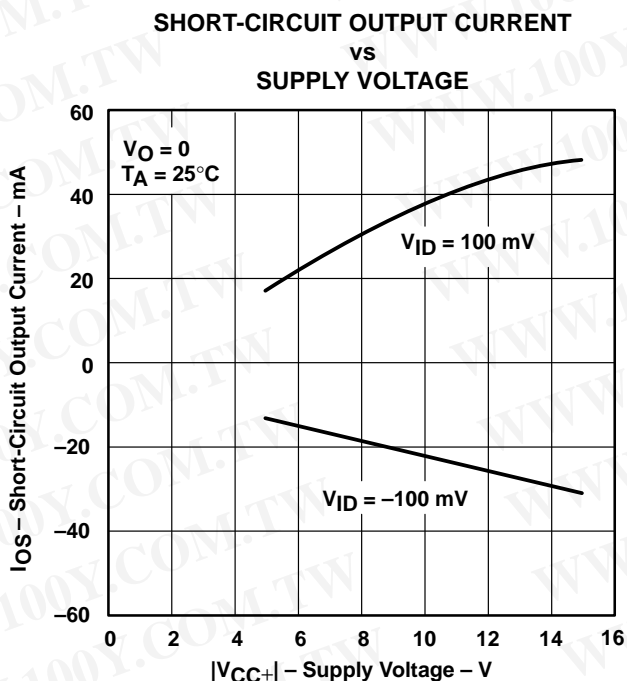
**TYPICAL CHARACTERISTICS**



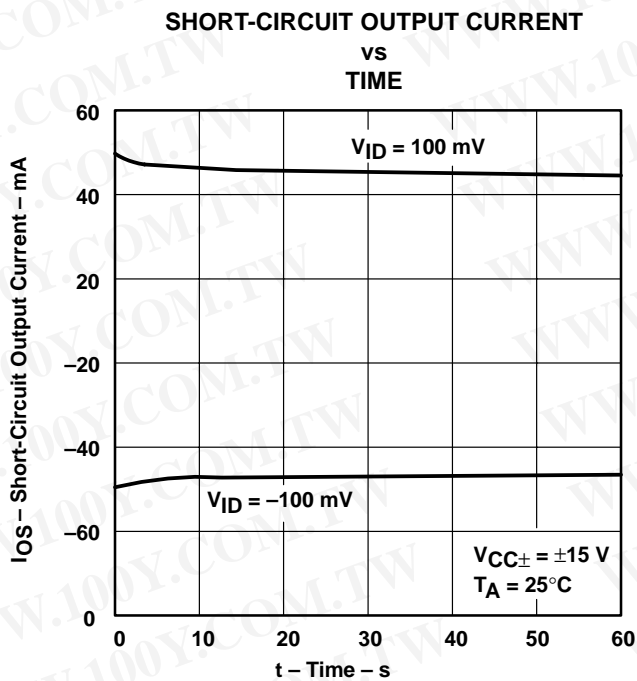
**Figure 37**



**Figure 38**



**Figure 39**



**Figure 40**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
**OPERATIONAL AMPLIFIERS**

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**TYPICAL CHARACTERISTICS**

**SHORT-CIRCUIT OUTPUT CURRENT†**  
**vs**  
**FREE-AIR TEMPERATURE**

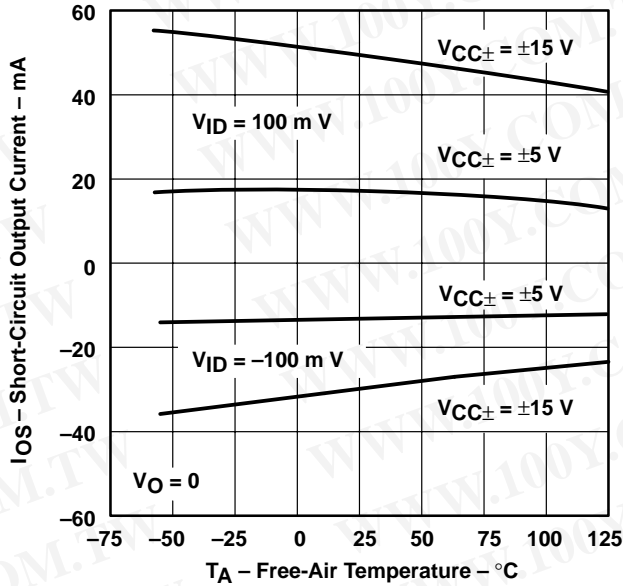


Figure 41

**TL051**  
**SUPPLY CURRENT†**  
**vs**  
**SUPPLY VOLTAGE**

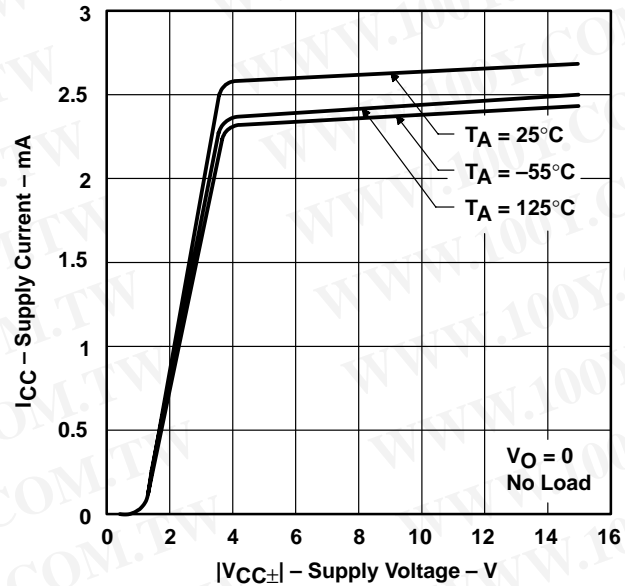


Figure 42

**TL052**  
**SUPPLY CURRENT†**  
**vs**  
**SUPPLY VOLTAGE**

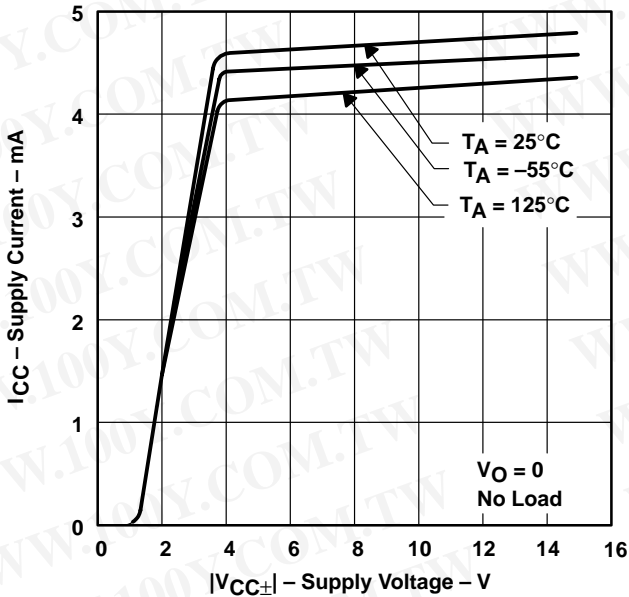


Figure 43

**TL054**  
**SUPPLY CURRENT†**  
**vs**  
**SUPPLY VOLTAGE**

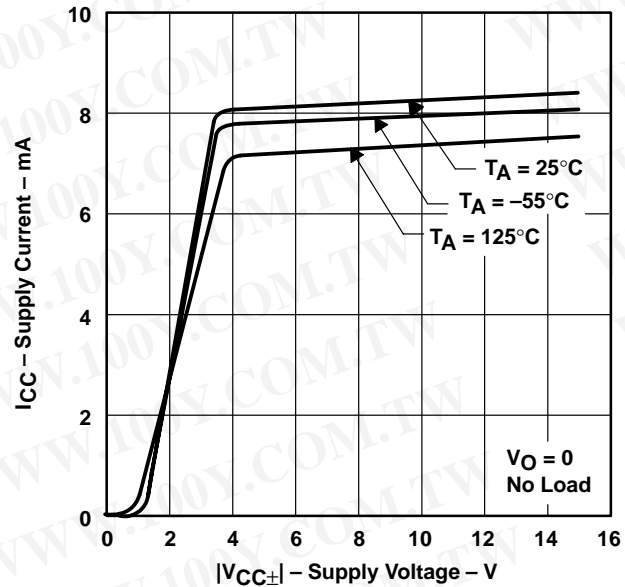


Figure 44

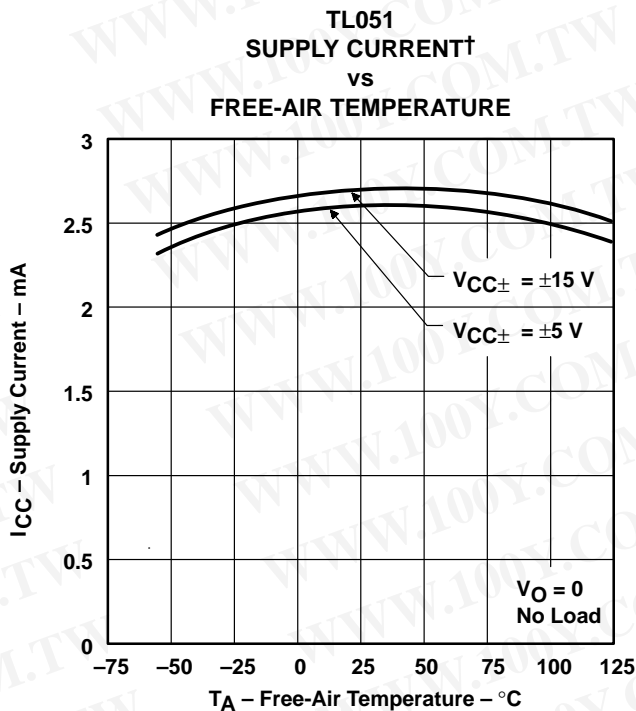
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



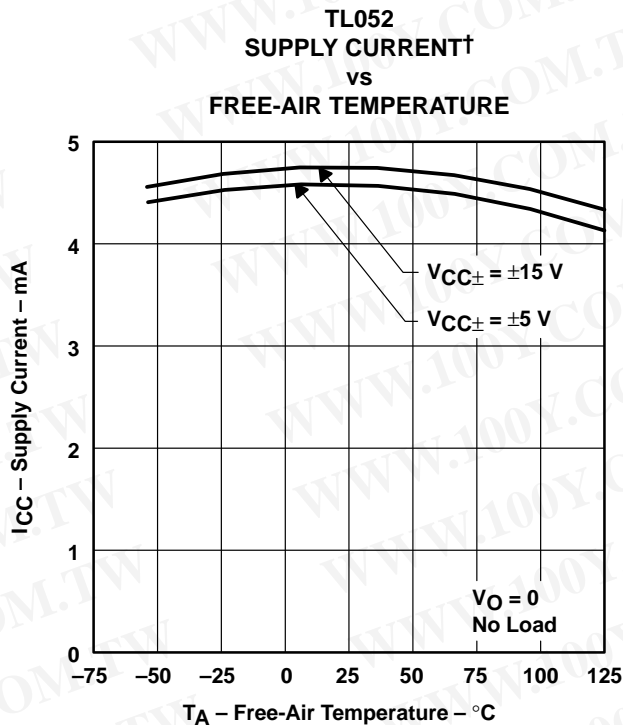
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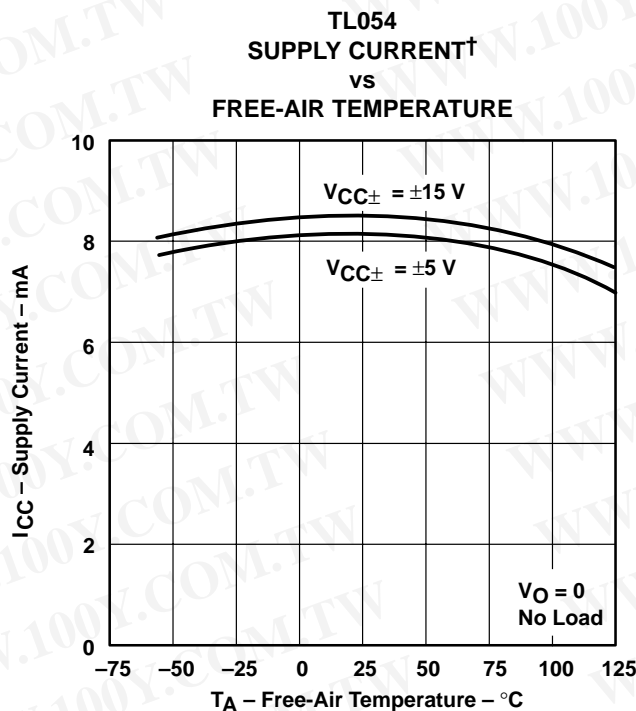
**TYPICAL CHARACTERISTICS**



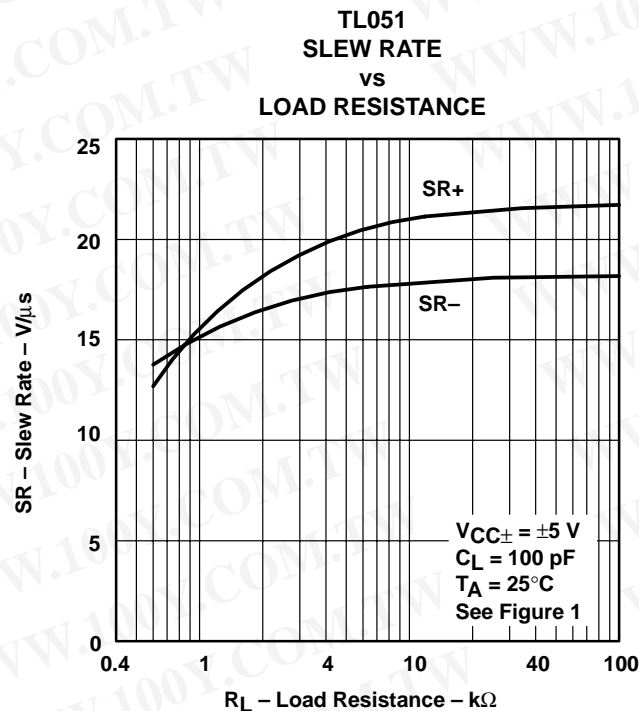
**Figure 45**



**Figure 46**



**Figure 47**



**Figure 48**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

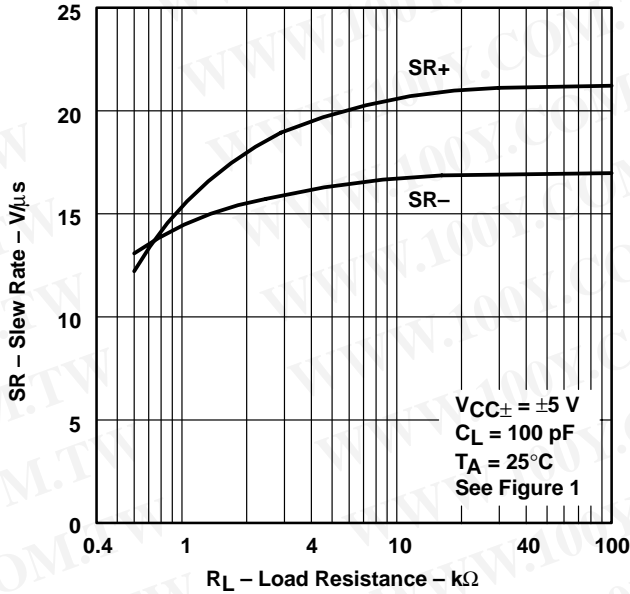
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**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
**OPERATIONAL AMPLIFIERS**

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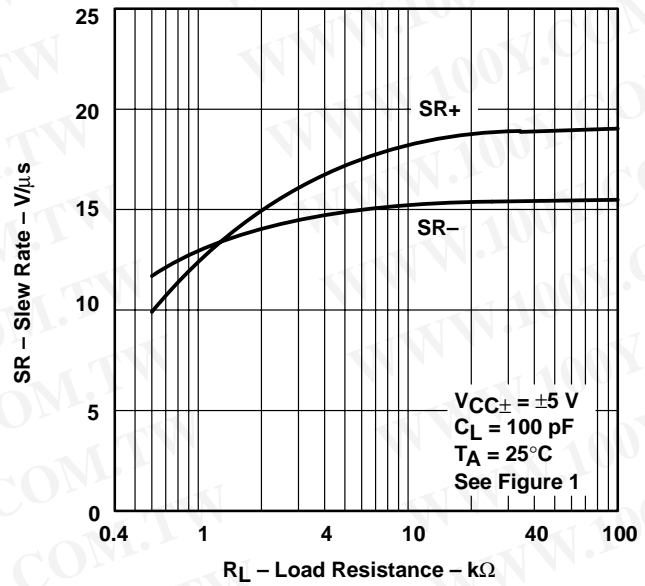
**TYPICAL CHARACTERISTICS**

**TL052**  
**SLEW RATE**  
**vs**  
**LOAD RESISTANCE**



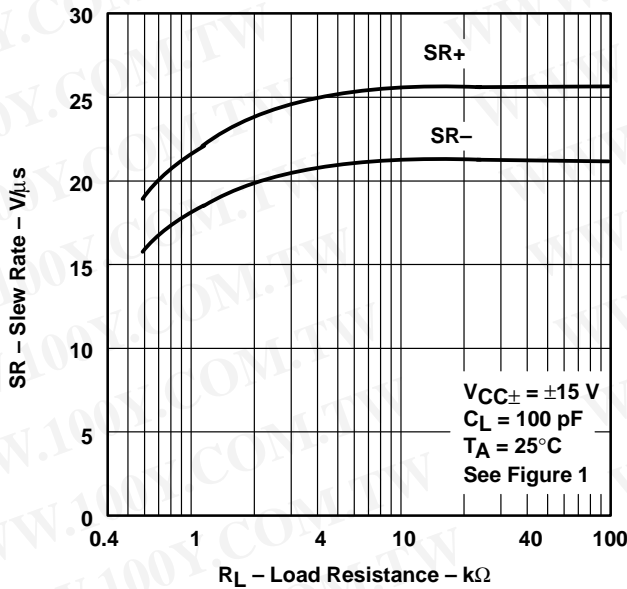
**Figure 49**

**TL054**  
**SLEW RATE**  
**vs**  
**LOAD RESISTANCE**



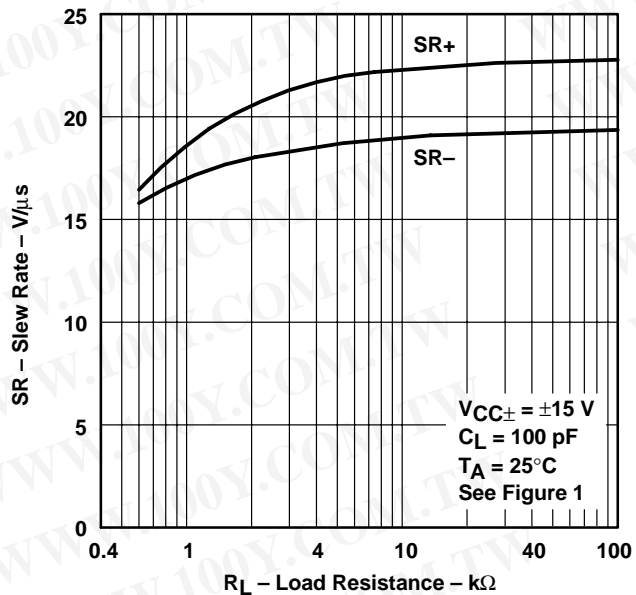
**Figure 50**

**TL051**  
**SLEW RATE**  
**vs**  
**LOAD RESISTANCE**



**Figure 51**

**TL052**  
**SLEW RATE**  
**vs**  
**LOAD RESISTANCE**



**Figure 52**

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**TYPICAL CHARACTERISTICS**

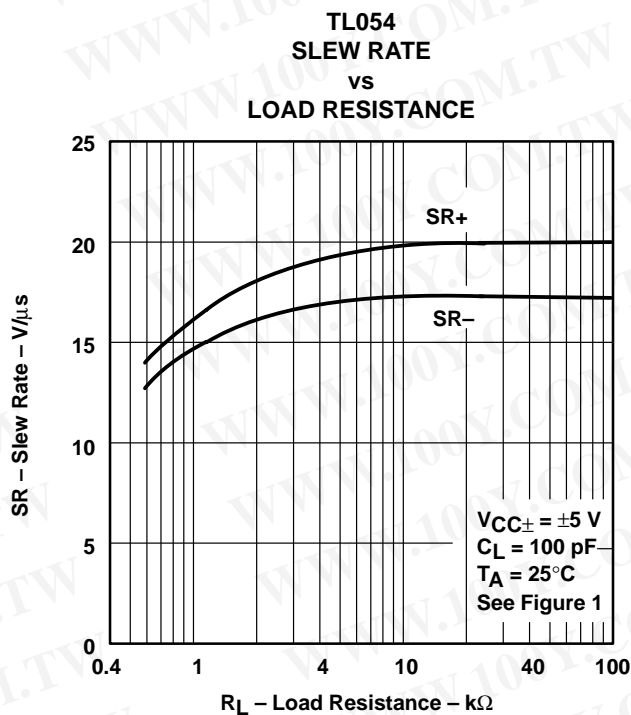


Figure 53

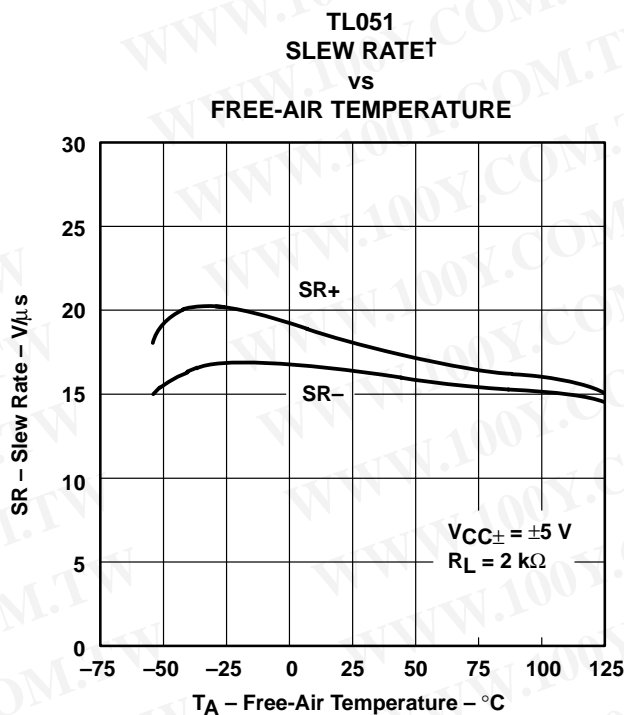


Figure 54

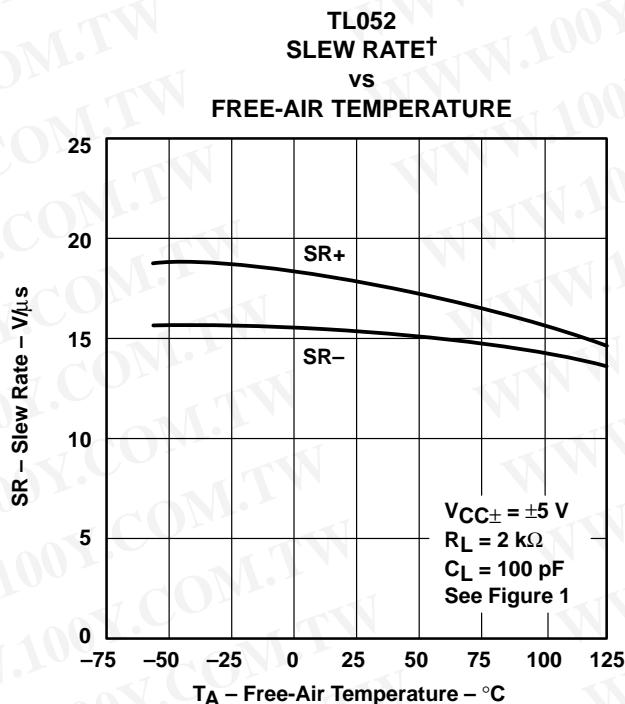


Figure 55

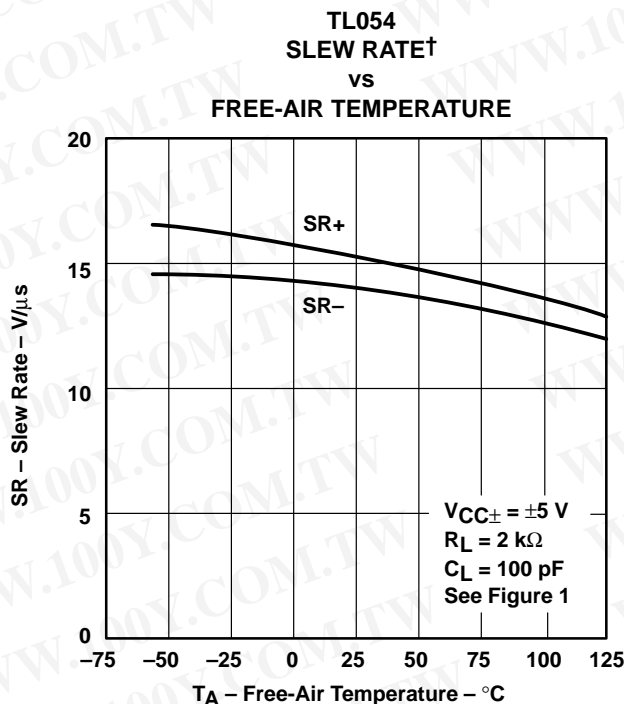


Figure 56

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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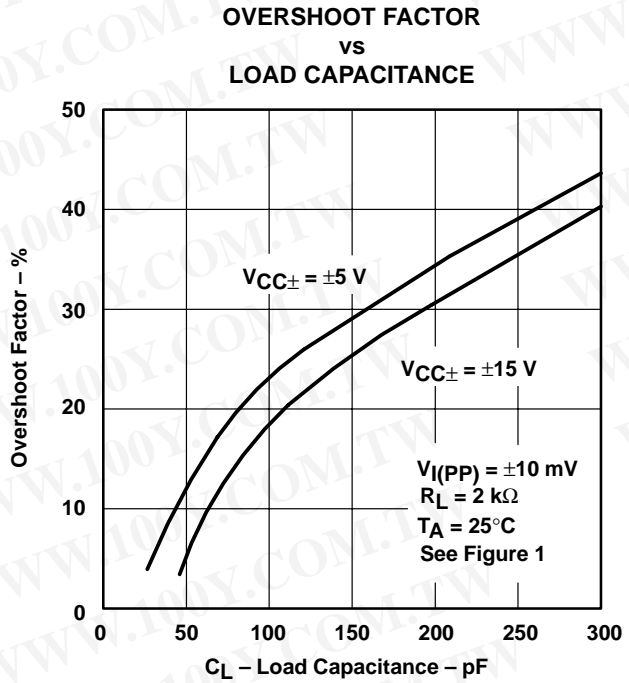
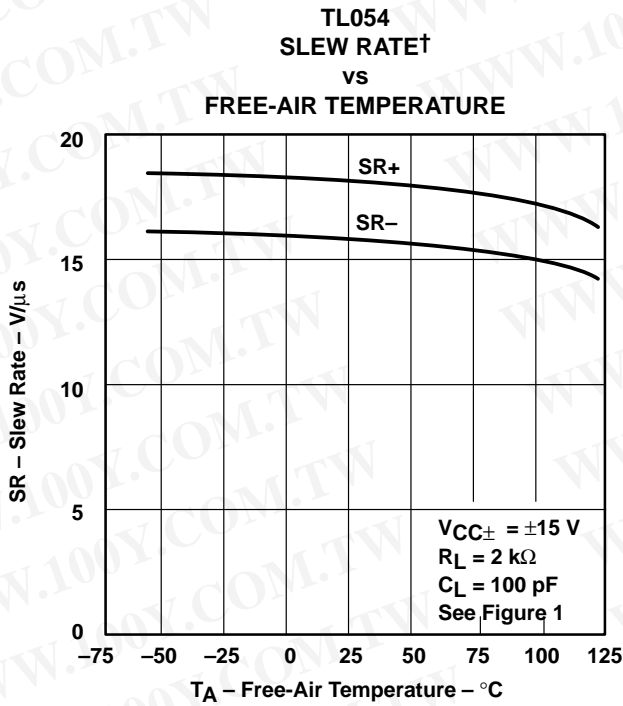
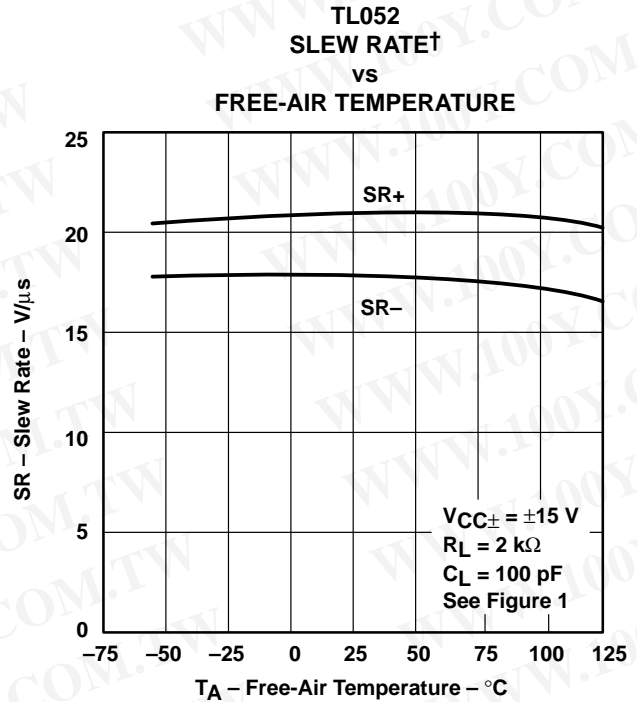
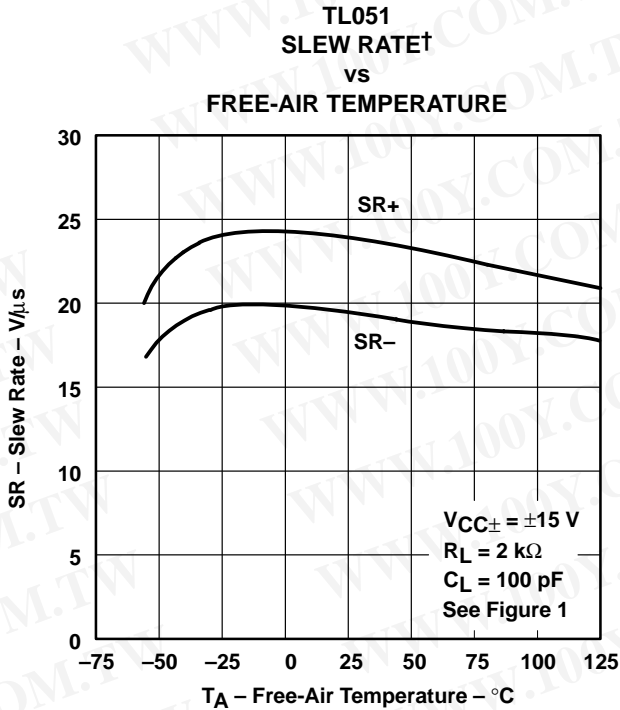


**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
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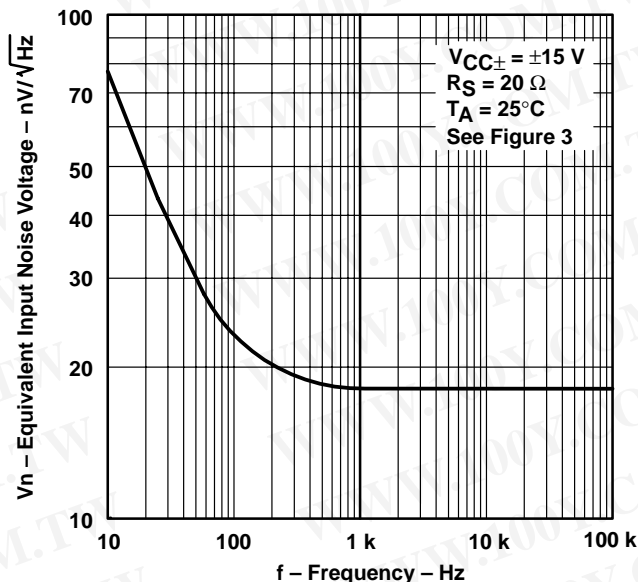
**TYPICAL CHARACTERISTICS**



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

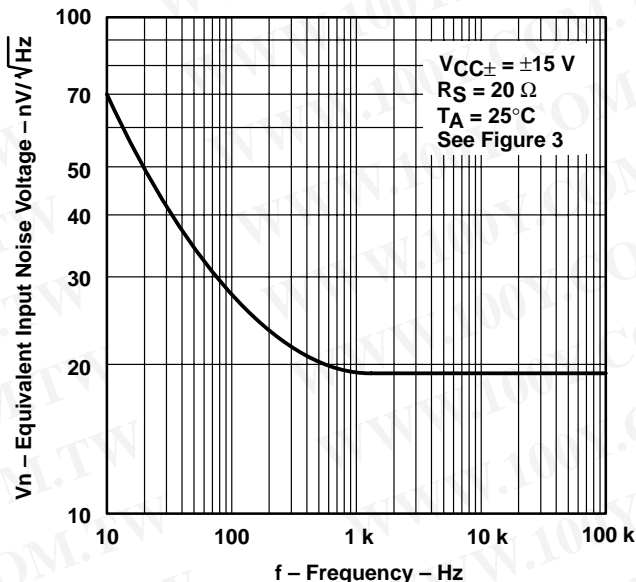
**TYPICAL CHARACTERISTICS**

**TL051  
 EQUIVALENT INPUT NOISE VOLTAGE  
 VS  
 FREQUENCY**



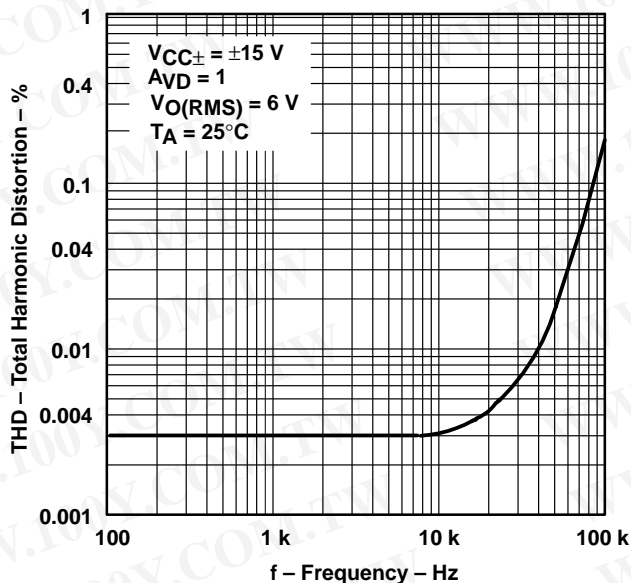
**Figure 61**

**TL052 AND TL054  
 EQUIVALENT INPUT NOISE VOLTAGE  
 VS  
 FREQUENCY**



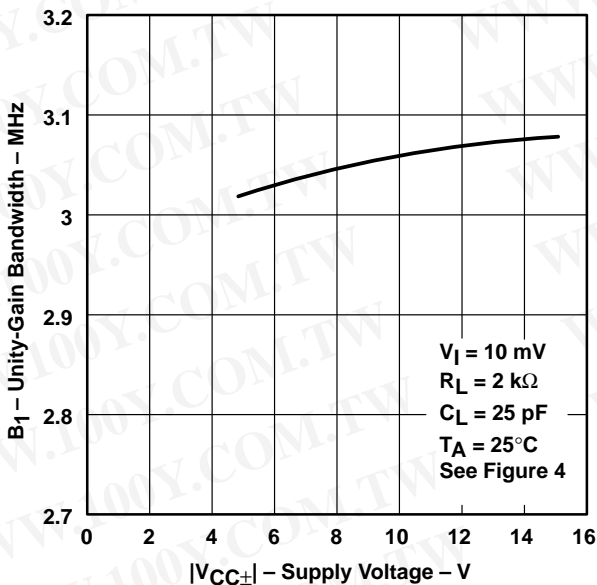
**Figure 62**

**TOTAL HARMONIC DISTORTION  
 VS  
 FREQUENCY**



**Figure 63**

**TL051  
 UNITY-GAIN BANDWIDTH  
 VS  
 SUPPLY VOLTAGE**



**Figure 64**

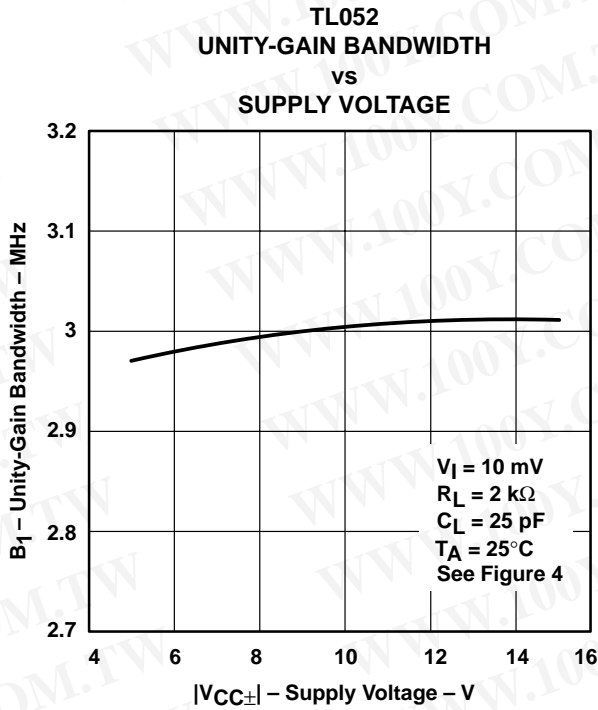
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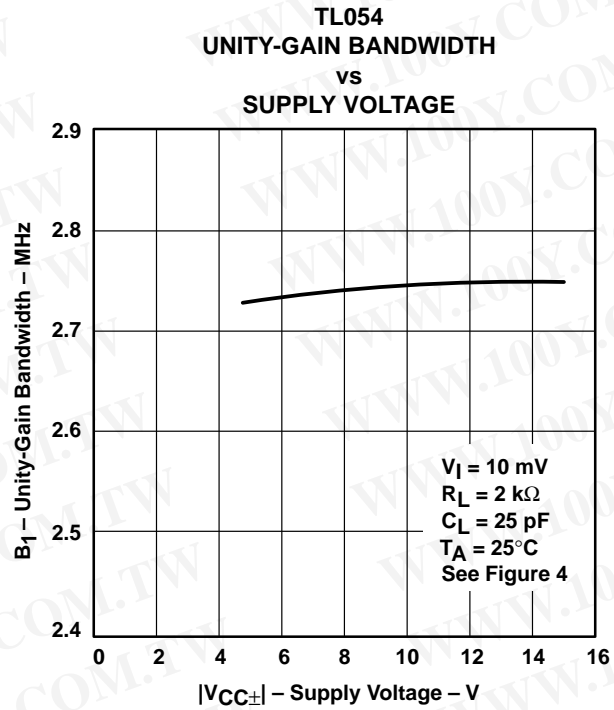
**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
**OPERATIONAL AMPLIFIERS**

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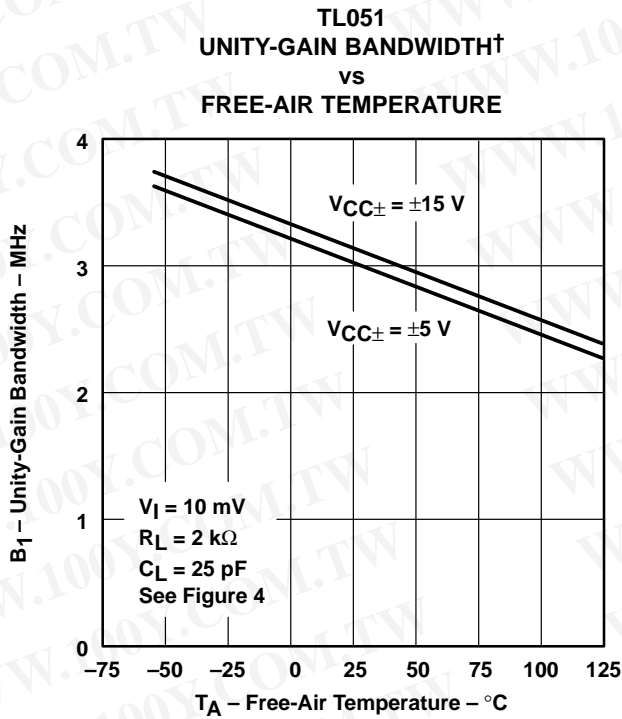
**TYPICAL CHARACTERISTICS**



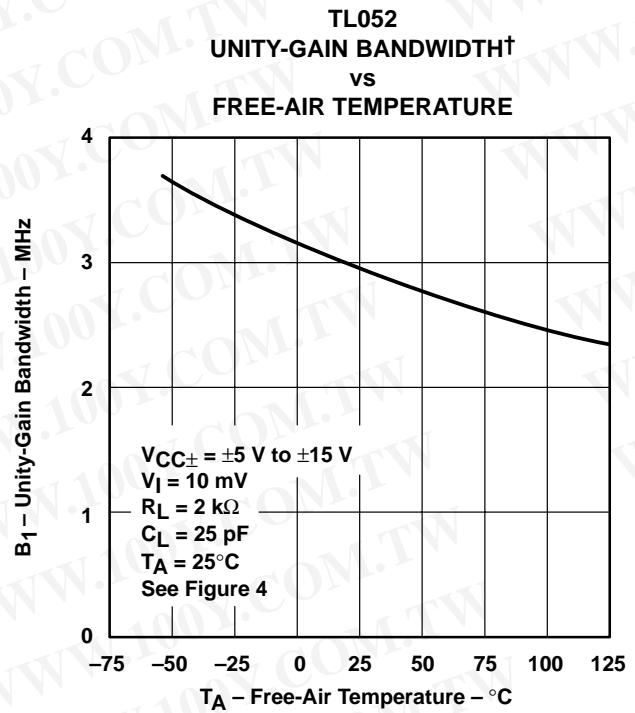
**Figure 65**



**Figure 66**



**Figure 67**



**Figure 68**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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**TYPICAL CHARACTERISTICS**

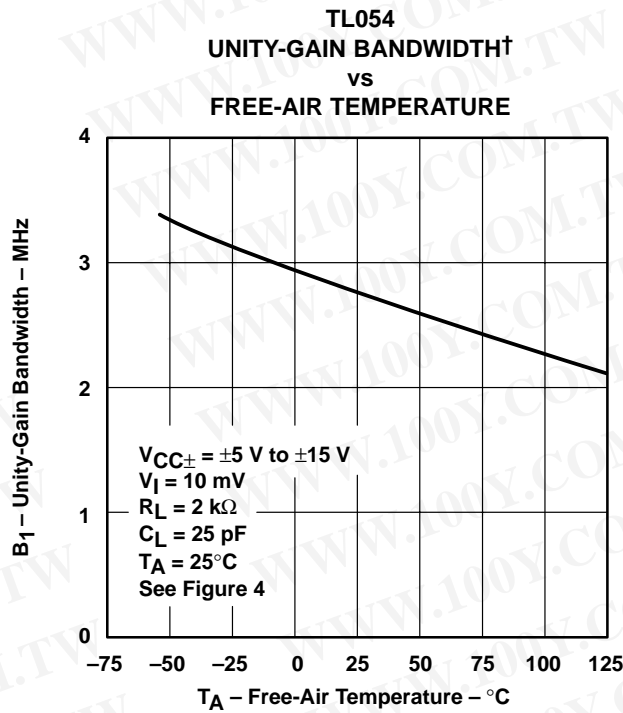


Figure 69

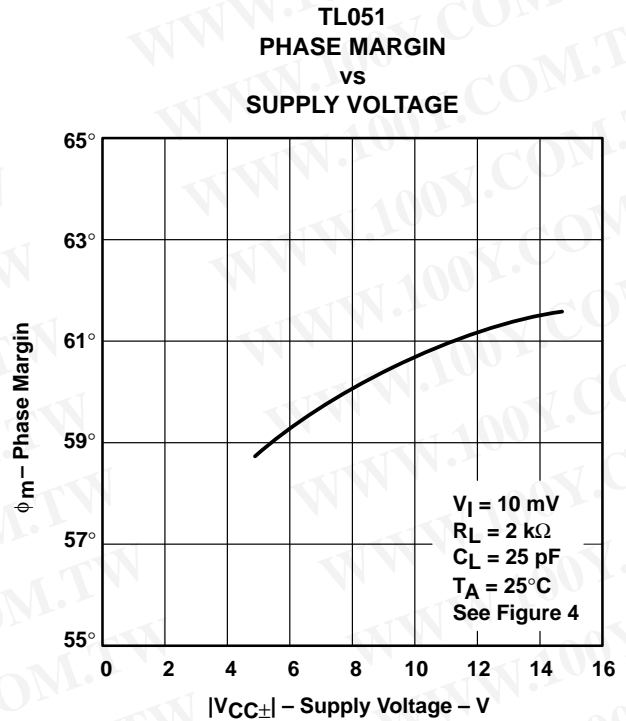


Figure 70

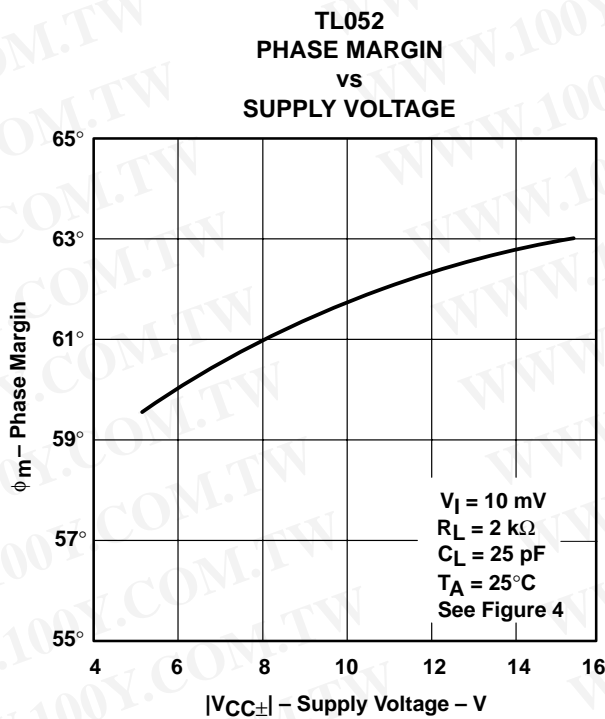


Figure 71

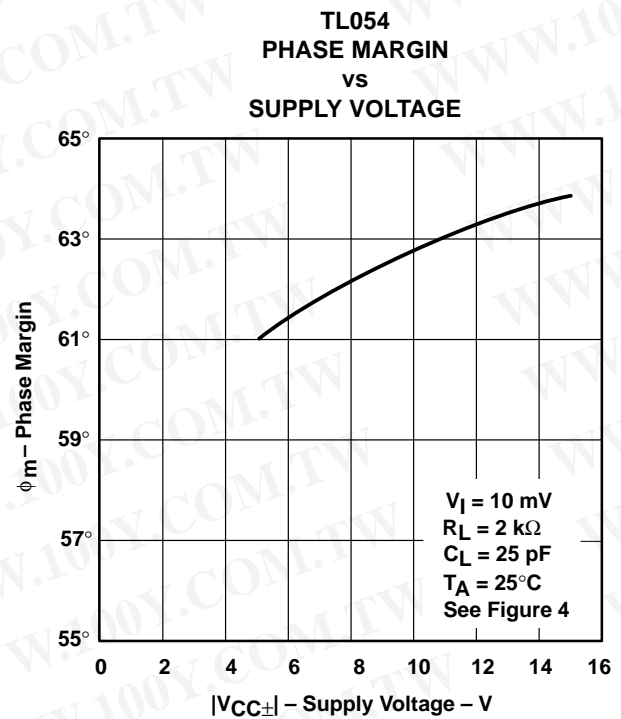


Figure 72

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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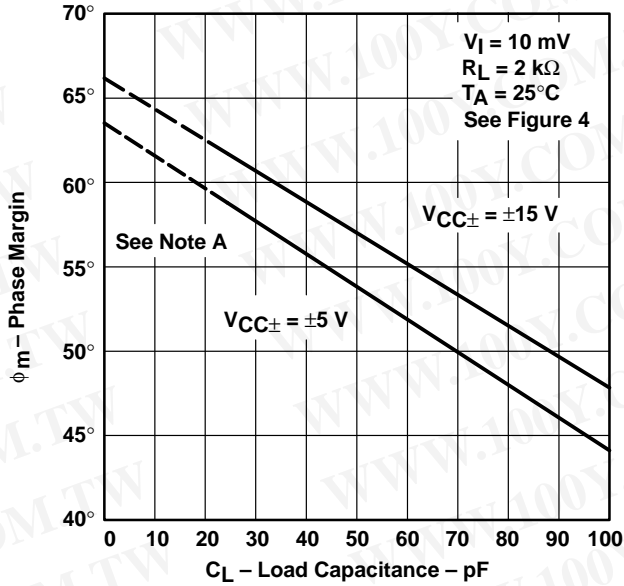


**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
**OPERATIONAL AMPLIFIERS**

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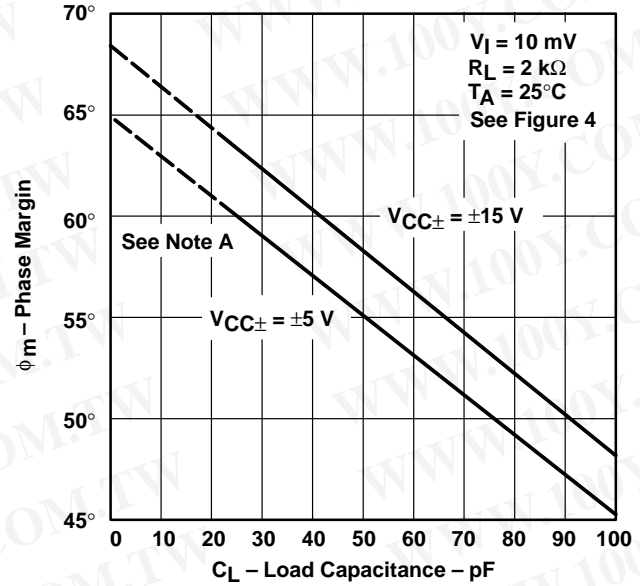
**TYPICAL CHARACTERISTICS**

**TL051**  
**PHASE MARGIN†**  
**vs**  
**LOAD CAPACITANCE**



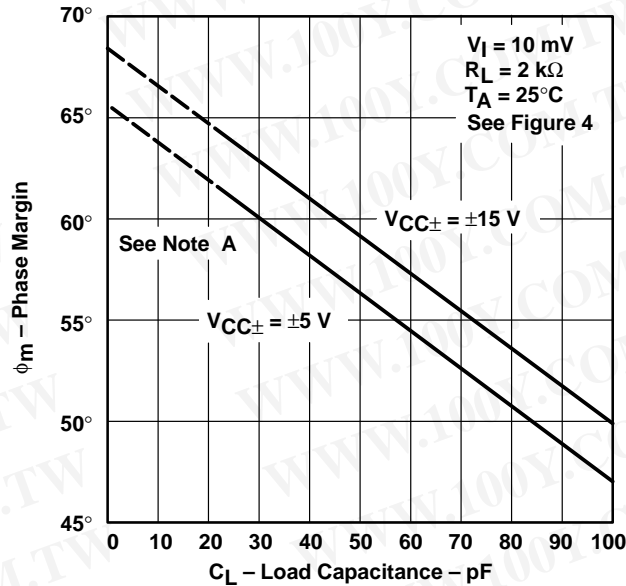
**Figure 73**

**TL052**  
**PHASE MARGIN†**  
**vs**  
**LOAD CAPACITANCE**



**Figure 74**

**TL054**  
**PHASE MARGIN†**  
**vs**  
**LOAD CAPACITANCE**

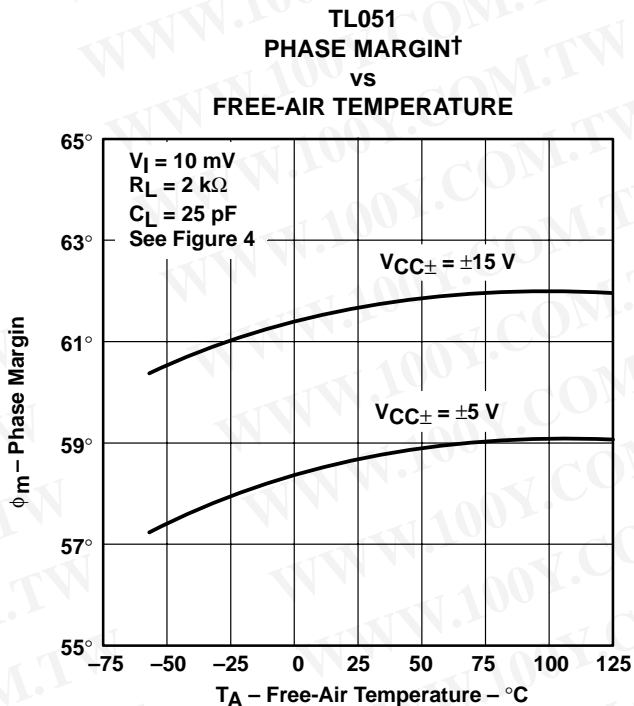


**Figure 75**

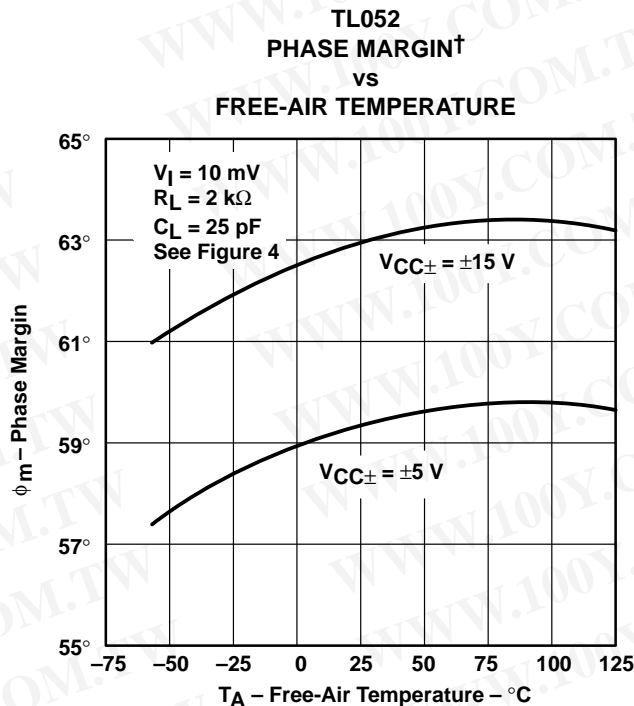
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† Values of phase margin below a load capacitance of 25 pF were estimated.

**TYPICAL CHARACTERISTICS**

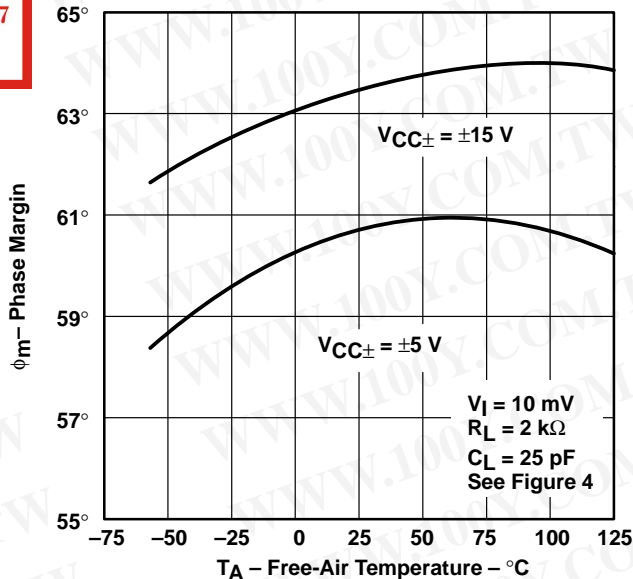


**Figure 76**



**Figure 77**

**TL054  
 PHASE MARGIN†  
 vs  
 FREE-AIR TEMPERATURE**



**Figure 78**

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

### VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

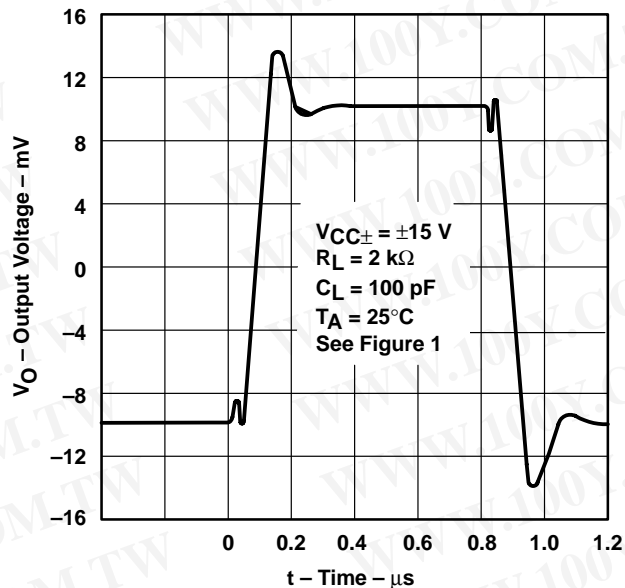


Figure 79

### VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

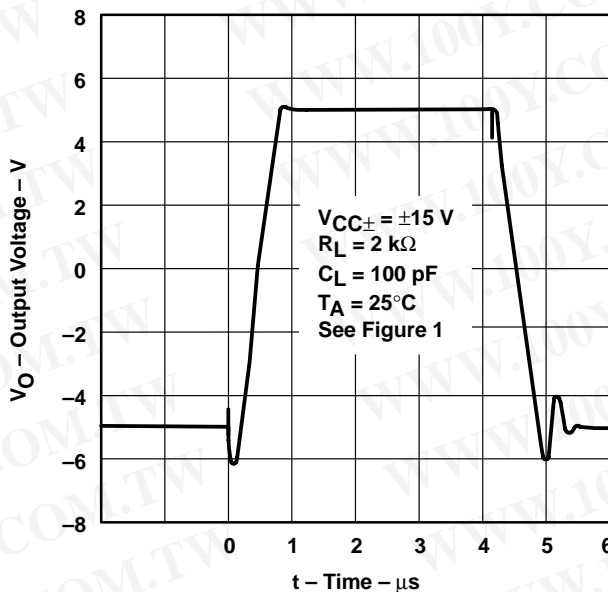


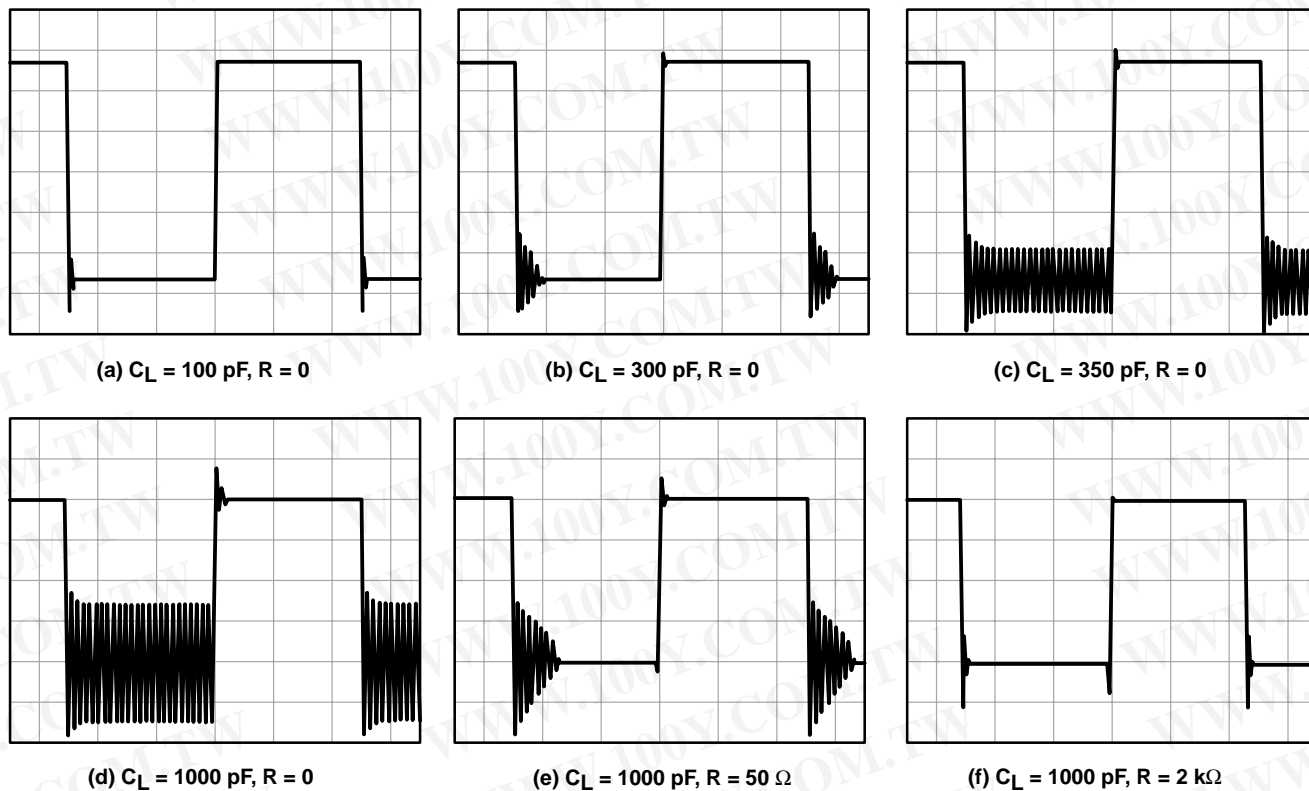
Figure 80

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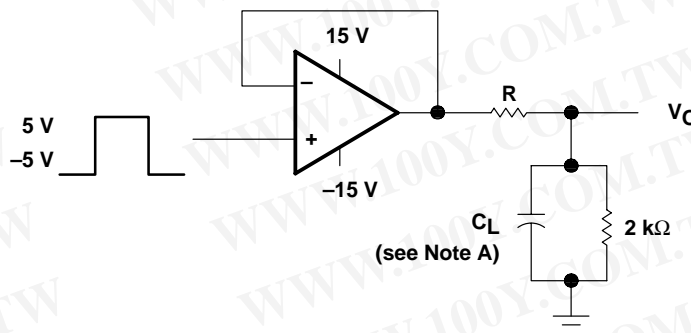
**APPLICATION INFORMATION**

**output characteristics**

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL05x and TL05xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF, and larger, may be driven if enough resistance is added in series with the output (see Figure 81 and Figure 82).



**Figure 81. Effect of Capacitive Loads**



NOTE A:  $C_L$  includes fixture capacitance.

**Figure 82. Test Circuit for Output Characteristics**

# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### input characteristics

The TL05x and TL05xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low-bias current requirements, the TL05x and TL05xA are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets easily can exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 83). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

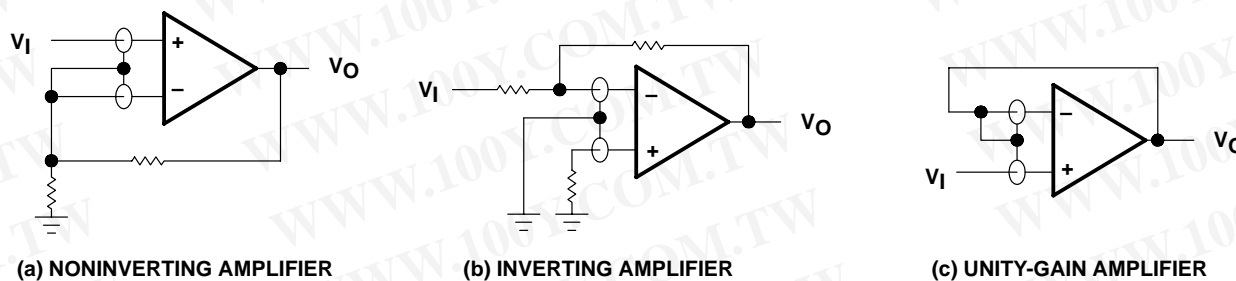


Figure 83. Use of Guard Rings

### noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input-bias current requirements of the TL05x and TL05xA result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k $\Omega$ .

**APPLICATION INFORMATION**

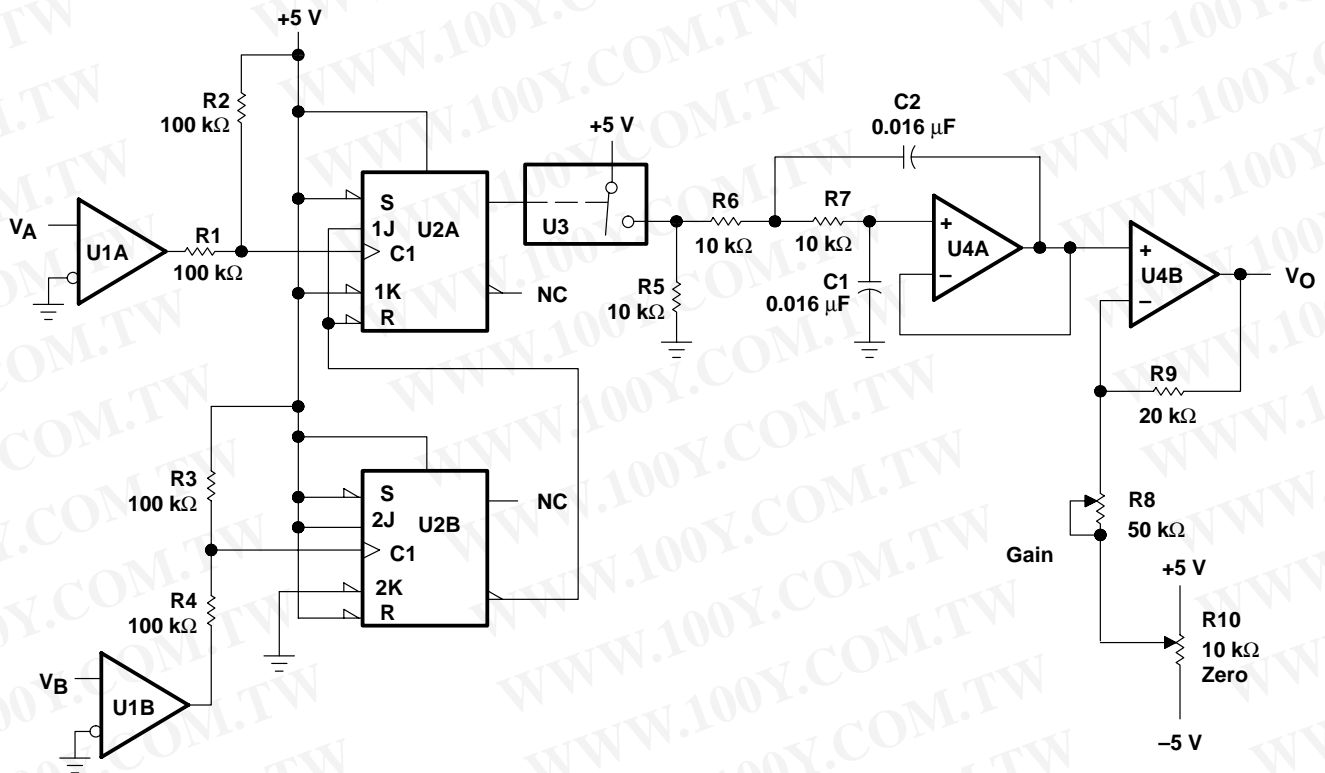
**phase meter**

The phase meter in Figure 84 produces an output voltage of 10 mV per degree of phase delay between the two input signals  $V_A$  and  $V_B$ . The reference signal  $V_A$  must be the same frequency as  $V_B$ . The TLC3702 comparators (U1) convert these two input sine waves into  $\pm 5$ -V square waves. Then, R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flops.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at one-half the frequency of  $V_B$ . Flip-flop U2A also produces a square wave at one-half the input frequency. The pulse duration of U2A varies from zero to one-half the period, where zero corresponds to zero phase delay between  $V_A$  and  $V_B$  and one-half the period corresponds to  $V_B$  lagging  $V_A$  by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL05x (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U4A approximates a square wave, and U2A has an output of almost 2.5 V. U4B acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0- to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTE A: U1 = TLC3702;  $V_{CC\pm} = \pm 5$  V  
 U2 = SN74HC109  
 U3 = TLC4066  
 U4, U5 = TL05x;  $V_{CC\pm} = \pm 5$  V

**Figure 84. Phase Meter**

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**TL05x, TL05xA**  
**ENHANCED-JFET LOW-OFFSET**  
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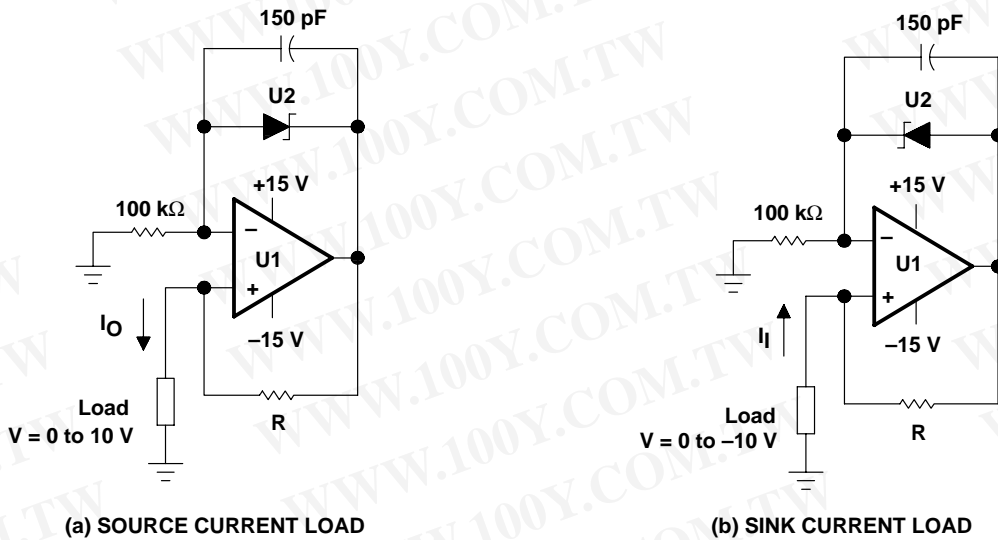
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**APPLICATION INFORMATION**

**precision constant-current source over temperature**

A precision current source (see Figure 85) benefits from the high input impedance and stability of Texas Instruments enhanced-JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL05x. The negative feedback then forces 2.5 V across the current-setting resistor R; therefore, the current to the load simply is 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. If the regulator's cathode connects to the operational amplifier output, this circuit sources load current. Similarly, if the cathode connects to the inverting input, the circuit sinks current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split-voltage supplies.



NOTE A: U1 = 1/2 TL05x  
 U2 = LM385, LT1004, or LT1009 voltage reference  
 $I = \frac{2.5 \text{ V}}{R}$ , R = Low-temperature-coefficient metal-film resistor

**Figure 85. Precision Constant-Current Source**

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**APPLICATION INFORMATION**

**instrumentation amplifier with adjustable gain/null**

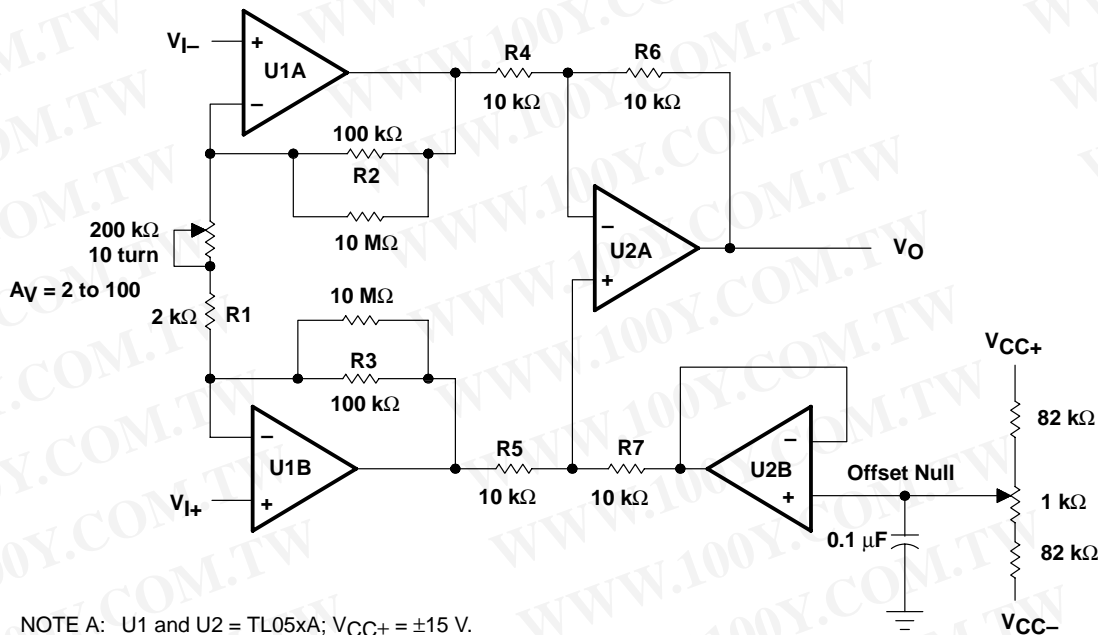
The instrumentation amplifier in Figure 86 benefits greatly from the high input impedance and stable input offset voltage of the TL05xA. Amplifiers U1A, U1B, and U2A form the actual instrumentation amplifier, while U2B provides offset null. Potentiometer R1 provides gain adjustment. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

$$A_v = 1 + \left( \frac{R_2 + R_3}{R_1} \right)$$

Readjusting the offset null is necessary when the circuit gain is changed. If U2B is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL05xA minimizes the dc error of the circuit. For best matching, all resistors should be one-percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets, rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V<sub>I</sub> equals zero, V<sub>O</sub> can be shown as a function of the offset voltage:

$$V_O = V_{IO2} \left[ \left( 1 + \frac{R_3}{R_1} \right) \left( \frac{R_7}{R_5 + R_7} \right) \left( 1 + \frac{R_6}{R_4} \right) + \frac{R_2}{R_1} \left( \frac{R_6}{R_4} \right) \right] - V_{IO1} \left[ \frac{R_3}{R_1} \left( \frac{R_7}{R_5 + R_7} \right) \left( 1 + \frac{R_6}{R_4} \right) + \frac{R_6}{R_4} \left( 1 + \frac{R_2}{R_1} \right) \right] + V_{IO3} \left( 1 + \frac{R_6}{R_4} \right)$$



**Figure 86. Instrumentation Amplifier**

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**APPLICATION INFORMATION**

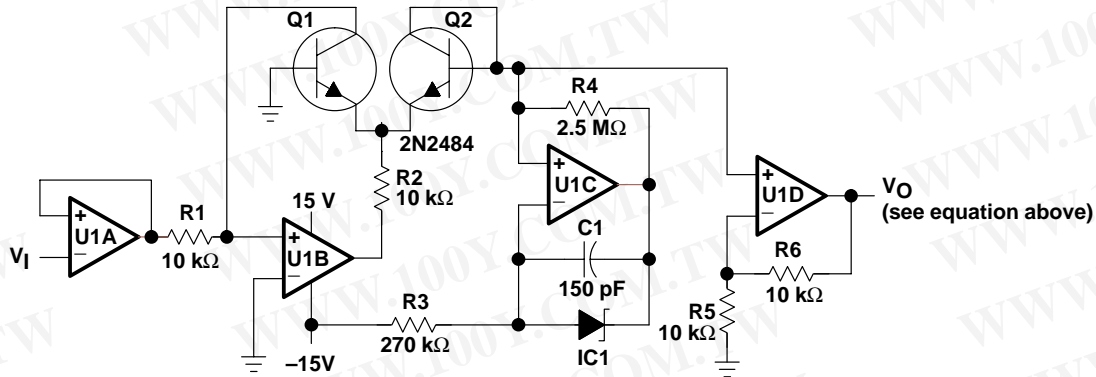
**high input impedance log amplifier**

The low input offset voltage and high input impedance of the TL05xA creates a precision log amplifier (see Figure 87). IC1 is a 2.5-V, low-current precision, shunt regulator. Transistors Q1 and Q2 must be a closely matched npn pair. For best performance over temperature, R4 should be a metal-film resistor with a low temperature coefficient.

In this circuit, U1A serves as a high-impedance unity-gain buffer. Amplifier U1B converts the input voltage to a current through R1 and Q1. Amplifier U1C, IC1, and R4 form a 1-μA temperature-stable current source that sets the base-emitter voltage of Q2. U1D amplifies the difference between the base-emitter voltage of Q1 and Q2 (see Figure 88). The output voltage is given by the following equation:

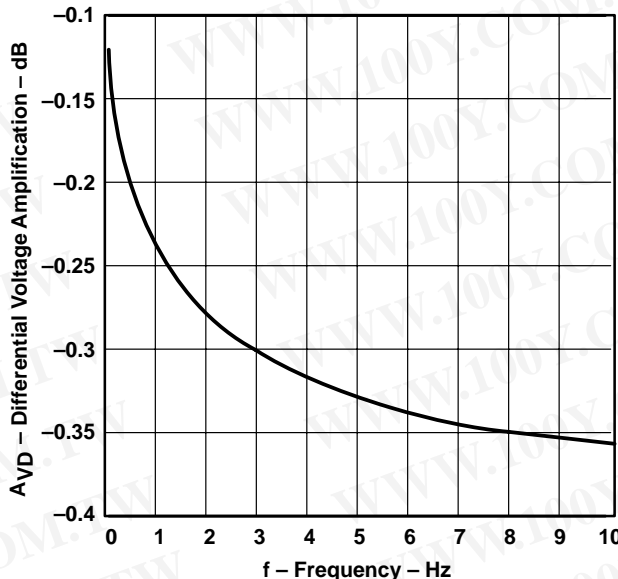
$$V_O = -\left[1 + \frac{R_6}{R_5}\right] \frac{kT}{q} \left[ \ln \frac{V_I}{(R_1 \times 1 \times 10^{-6})} \right]$$

where  $k = 1.38 \times 10^{-23}$ ,  $q = 1.602 \times 10^{-19}$ , and T is Kelvin temperature



NOTE A: U1A through U1D = TL05xA. IC1 = LM385, LT1004, or LT1009 voltage reference

**Figure 87. Log Amplifier**



**Figure 88. Output Voltage vs Input Voltage for Log Amplifier**

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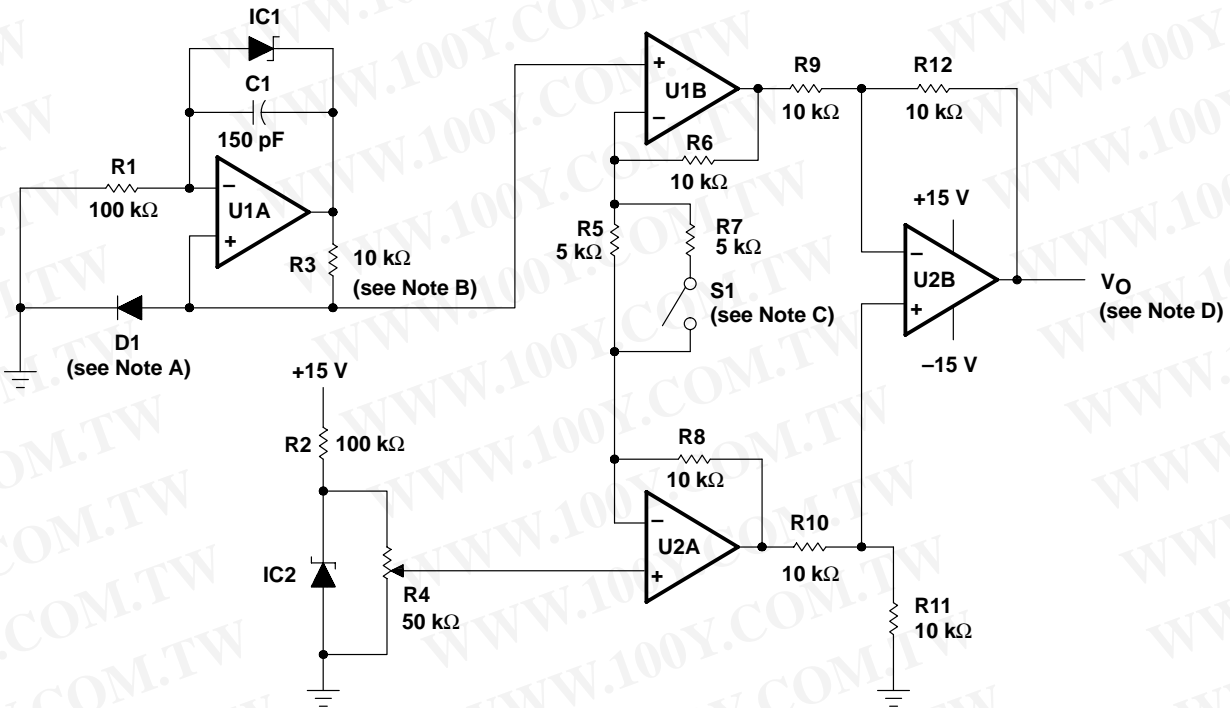
**APPLICATION INFORMATION**

**analog thermometer**

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 89). Amplifier U1A and IC1 establish a constant current through the temperature-sensing diode D1. For this section of the circuit to operate correctly, the TL05x must use split supplies, and R3 must be a metal-film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U2A, and U2B form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5 and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9 and the output is proportional to temperature in degrees Fahrenheit. Every time S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



- NOTES: A. Temperature-sensing diode  $\approx (-2 \text{ mV}/^\circ\text{C})$   
 B. Metal-film resistor (low temperature coefficient)  
 C. Switch open for  $^\circ\text{F}$  and closed for  $^\circ\text{C}$   
 D.  $V_O \propto$  temperature;  $10 \text{ mV}/^\circ\text{C}$  or  $10 \text{ mV}/^\circ\text{F}$   
 E. U1, U2 = TL05x. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference

**Figure 89. Analog Thermometer**

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# TL05x, TL05xA ENHANCED-JFET LOW-OFFSET OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### voltage-ratio-to-dB converter

The application in Figure 90 measures the amplitude ratio of two signals, then converts the ratio to decibels (see Figure 91). The output voltage provides a resolution of 100 mV/dB. The two inputs can be either dc or sinusoidal ac signals. When using ac signals, both signals should be the same frequency or output glitches will occur. For measuring two input signals of different frequencies, extra filtering should be added after the rectifiers.

The circuit contains three low-offset TL05xA devices. Two of these devices provide the rectification and logarithmic conversion of the inputs. The third TL05xA forms an instrumentation amplifier. The stage performing the logarithmic conversion also requires two well-matched npn transistors.

The input signal first passes through a high-impedance unity-gain buffer U1A (U2A). Then U1B (U2B) rectifies the input signal at a gain of 0.5, and U1C (U2C) provides a noninverting gain of 2, so that the system gain is still one. U1D (U2D), R6 (R13), and Q1 (Q2) perform the logarithmic conversion of the rectified input signal. The instrumentation amplifier formed by U3A, U3B, U3D scales the difference of the two logarithmic voltages by a gain of 33.6. As a result, the output voltage equals 100 mV/dB. The 1-k $\Omega$  potentiometer on the input of U3C calibrates the zero-dB reference level. The following equations are used to derive the relationship between the input voltage ratio, expressed in decibels, and the output voltage.

$$X \text{ dB} = 20 \log \left[ \frac{V_A}{V_B} \right] = 20 \left[ \frac{\ln(V_A) - \ln(V_B)}{\ln(10)} \right]$$

$$X \text{ dB} = 8.686 \left[ \ln(V_A) - \ln(V_B) \right]$$

$$V_{BE(Q1)} = \frac{kT}{q} \ln \left[ \frac{V_A}{R \times I_S} \right] \quad V_{BE(Q2)} = \frac{kT}{q} \ln \left[ \frac{V_B}{R \times I_S} \right]$$

$$\Delta V_{BE} = V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q} \left[ \ln(V_A) - \ln(V_B) \right]$$

$$X \text{ dB} = \frac{8.686}{kT/q} \left[ V_{BE(Q1)} - V_{BE(Q2)} \right] = 336 \left[ V_{BE(Q1)} - V_{BE(Q2)} \right] \text{ at } 25^\circ\text{C}$$

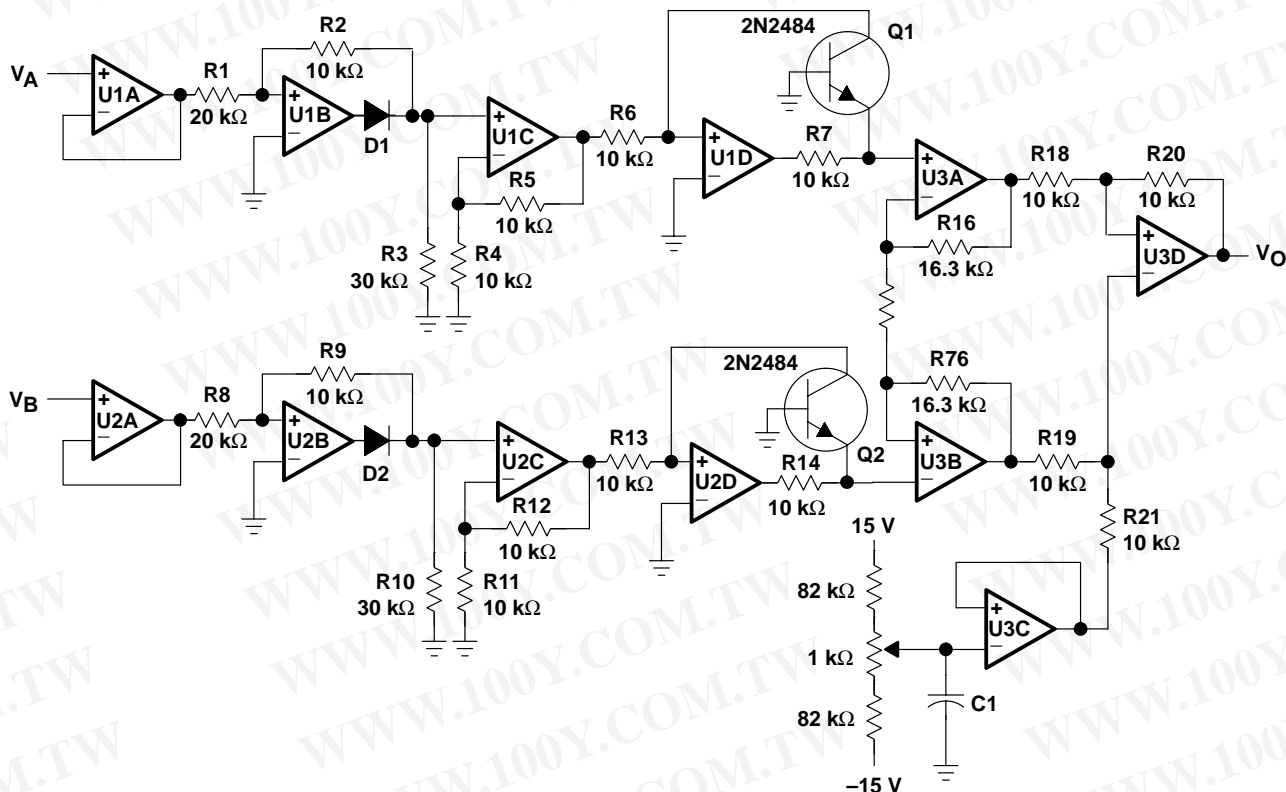
where

$$k = 1.38 \times 10^{-23}, \quad q = 1.602 \times 10^{-19}, \quad \text{and } T \text{ is Kelvin temperature}$$

This gives a resolution of 1 V/dB. Therefore, the gain of the instrumentation amplifier is set at 33.6 to obtain 100 mV/dB.

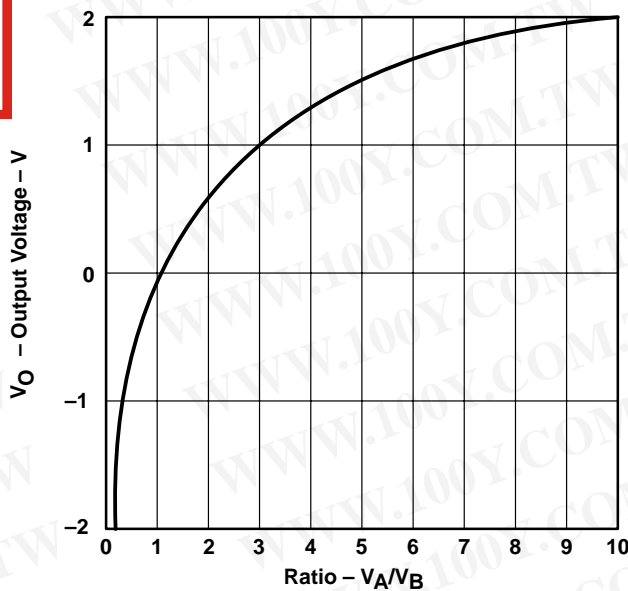
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**APPLICATION INFORMATION**



NOTE A: U1A through U3D = TL05xA,  $V_{CC\pm} = \pm 15$  V. D1 and D2 = 1N914.

**Figure 90. Voltage Ratio-to-dB Converter**



**Figure 91. Output Voltage vs the Ratio of the Input Voltages for Voltage-to-dB Converter**

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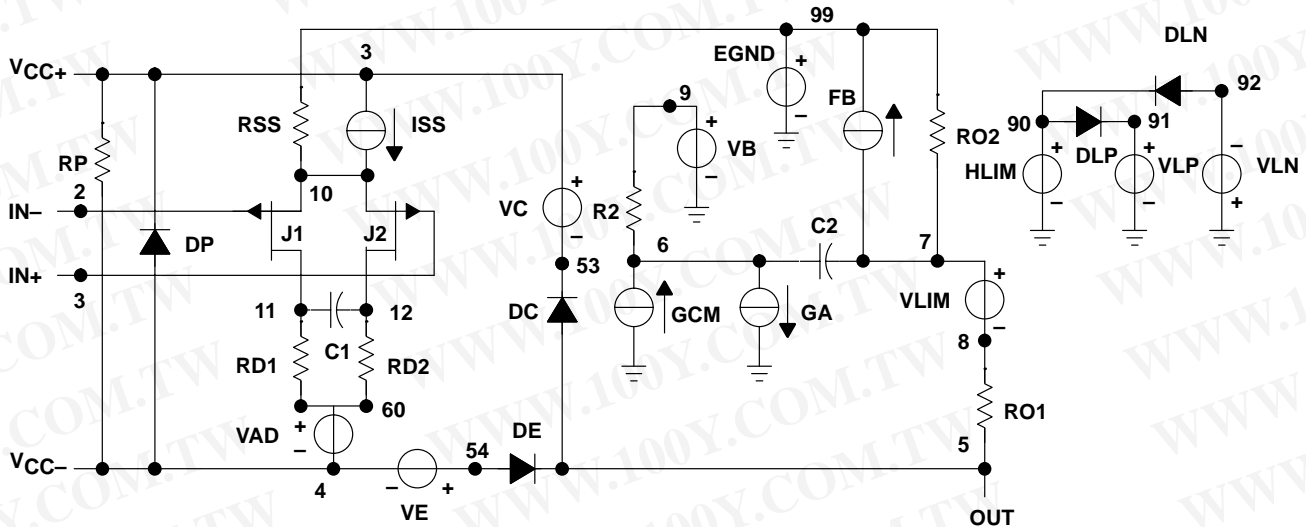
## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model-generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6 and subcircuit Figure 92) are generated using the TL05x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



```
.SUBCKT TL05x 1 2 3 4 5
C1 11 12 3.988E-12
C2 6 7 15.00E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY (2) (3,0) (4,0) 0 .5 .5
FB 7 99 POLY (5) VB VC VE VLP
+ VLN 0 2.875E6 -3E6 3E6 3E6 -3E6
GA 6 0 11 12 292.2E-6
GCM 0 6 10 99 6.542E-9
ISS 3 10 DC 300.0E-6
HLIM 90 0 VLIM 1K
J1 11 2 10 JX
J2 12 1 10 JX
R2 6 9 100.0E3
RD1 4 11 3.422E3
RD2 4 12 3.422E3
R01 8 5 125
R02 7 99 125
RSS 10 99 666.7E6
VB 9 0 DC 0
VC 3 53 DC 3
VE 54 4 DC 3.7
VLIM 7 8 DC 0
VLP 91 0 DC 28
VLN 0 92 DC 28
.MODEL DX D (IS=800.0E-18)
.MODEL JX PJF (IS=15.00E-12 BETA=185.2E-6
+ VTO=-.1)
.ENDS
```

Figure 92. Boyle Macromodel and Subcircuit

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TL051ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL051ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL051AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL051AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL051CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL051CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL051CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL051ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL051IDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL051IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL052ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TL052ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052AMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL052AMJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL052CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TL052CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL052IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL052MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL052MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL052MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL054ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TL054ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL054ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL054AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054AIDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054AIDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054AMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL054AMJB	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
TL054CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL054CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TL054CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL054IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL054INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL054MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL054MJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
TL054MJB	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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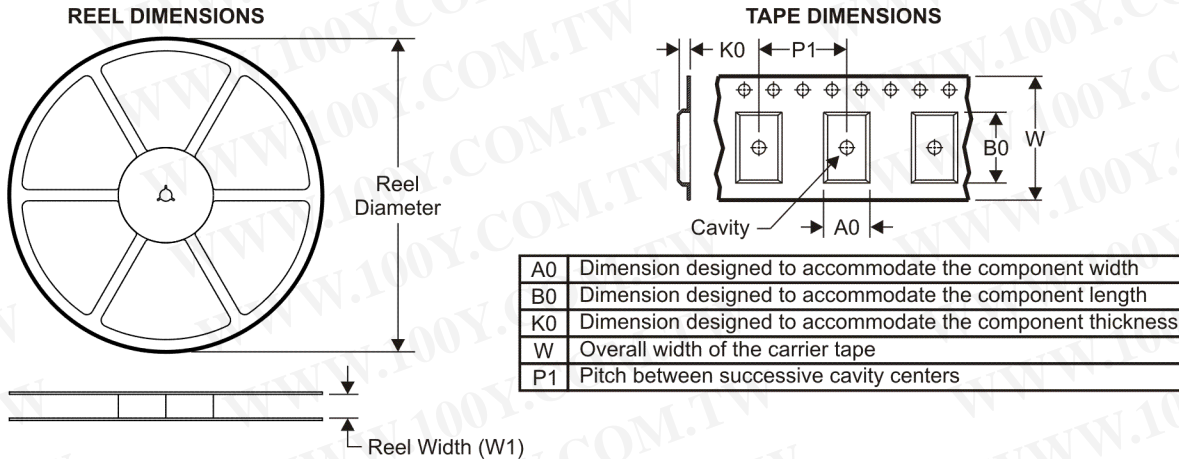
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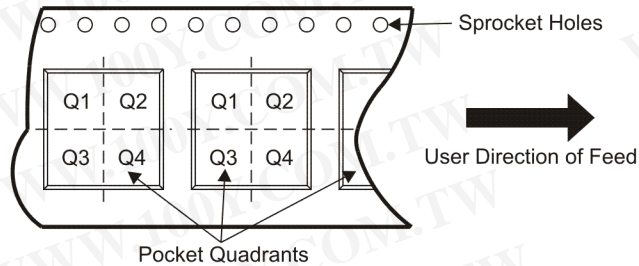
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## TAPE AND REEL INFORMATION



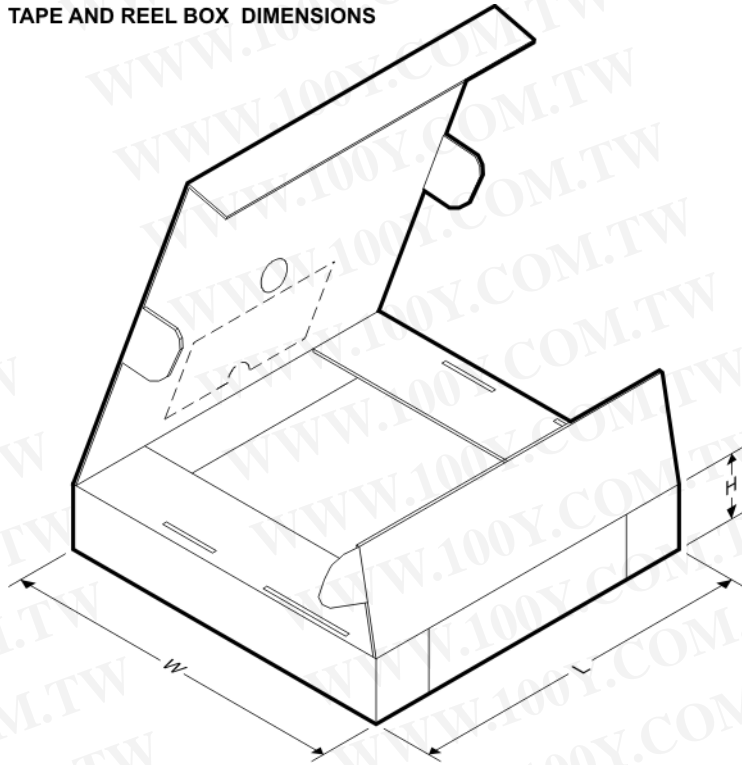
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL051CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL052CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL052IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL054ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL054AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL054CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL054CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL054IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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**TAPE AND REEL BOX DIMENSIONS**


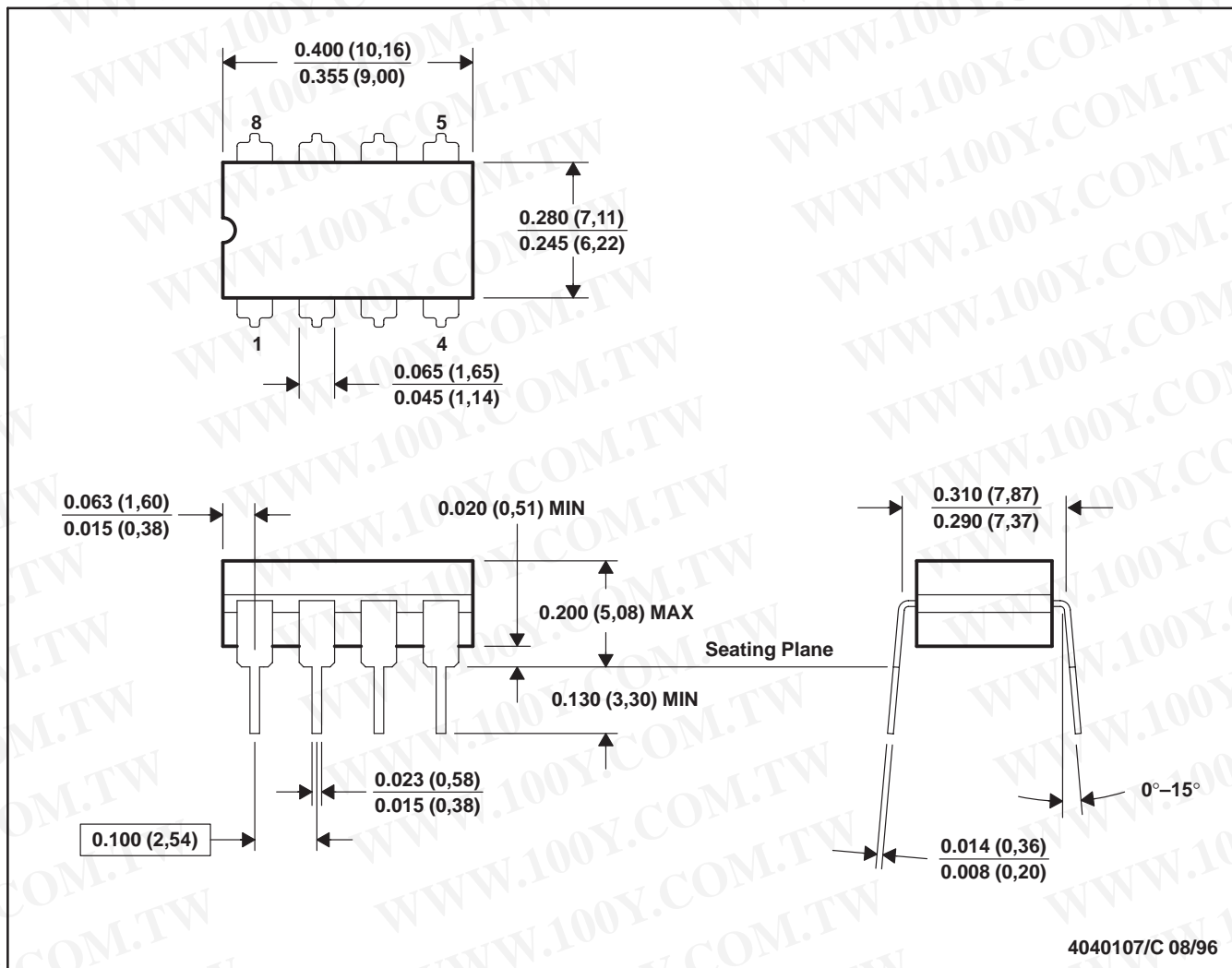
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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL051CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL052ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL052AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL052CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL052CPSR	SO	PS	8	2000	346.0	346.0	33.0
TL052IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL054ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL054AIDR	SOIC	D	14	2500	333.2	345.9	28.6
TL054CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL054CNSR	SO	NS	14	2000	346.0	346.0	33.0
TL054IDR	SOIC	D	14	2500	333.2	345.9	28.6

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

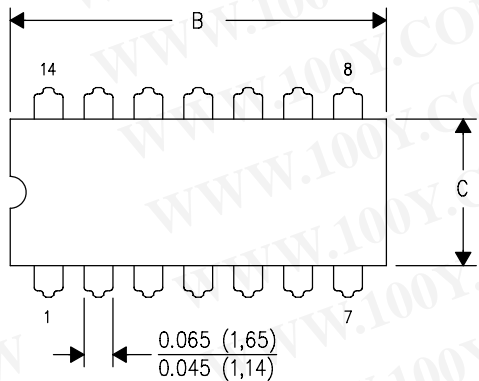


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

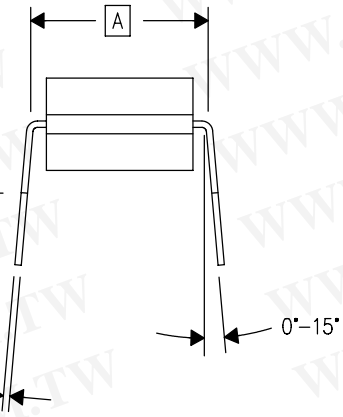
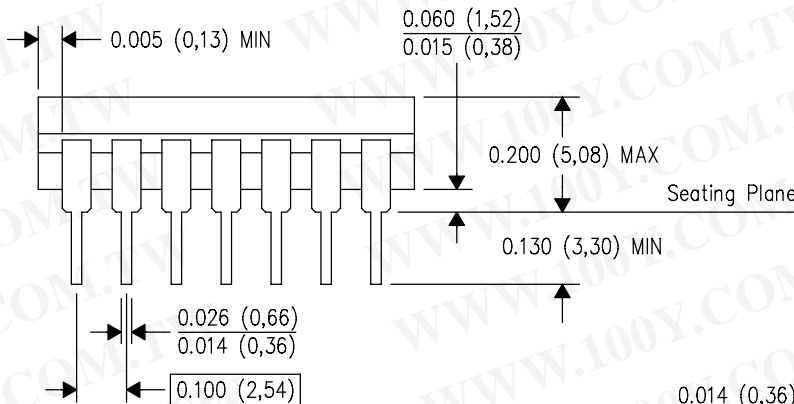
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J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
	A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

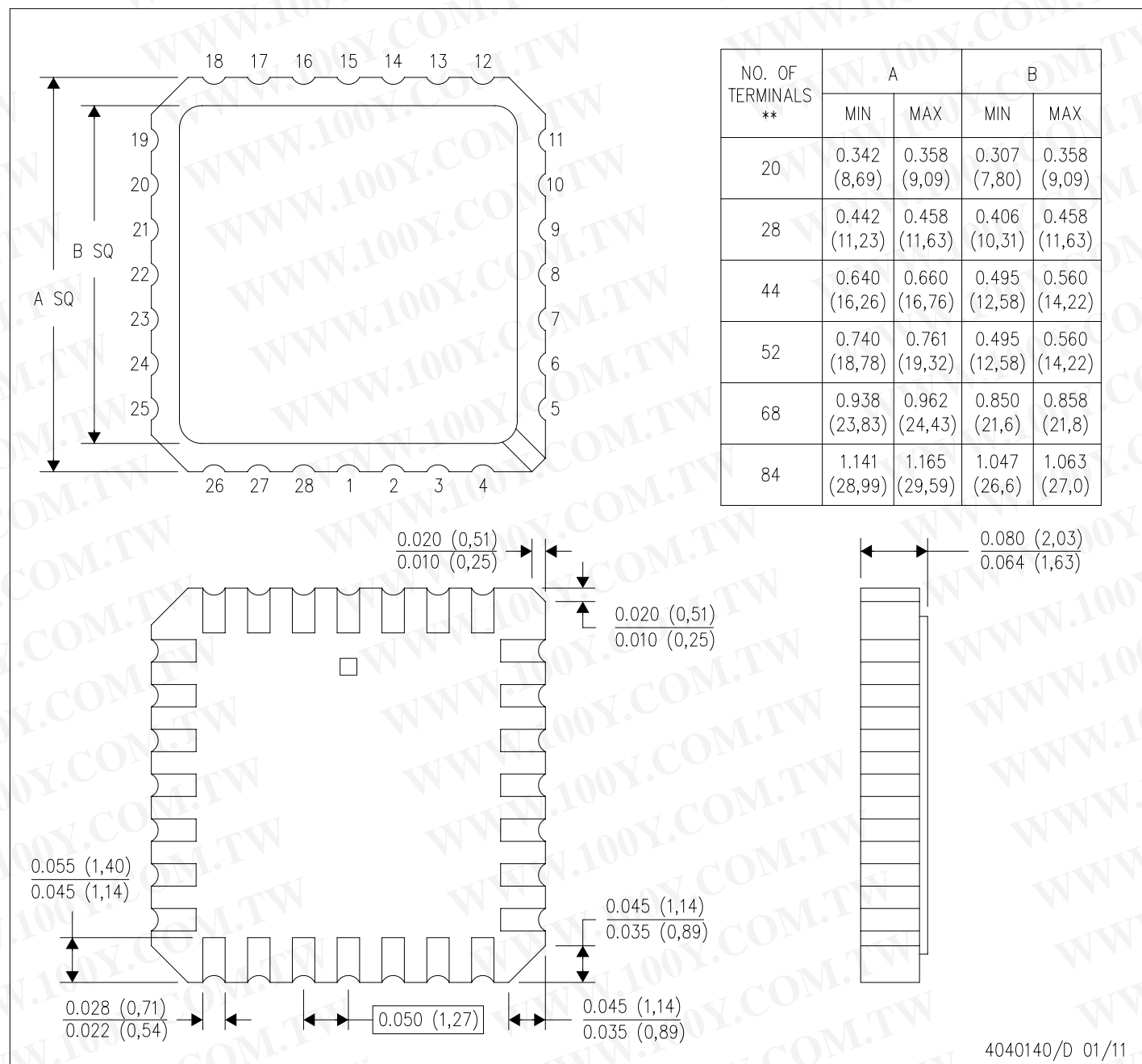
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



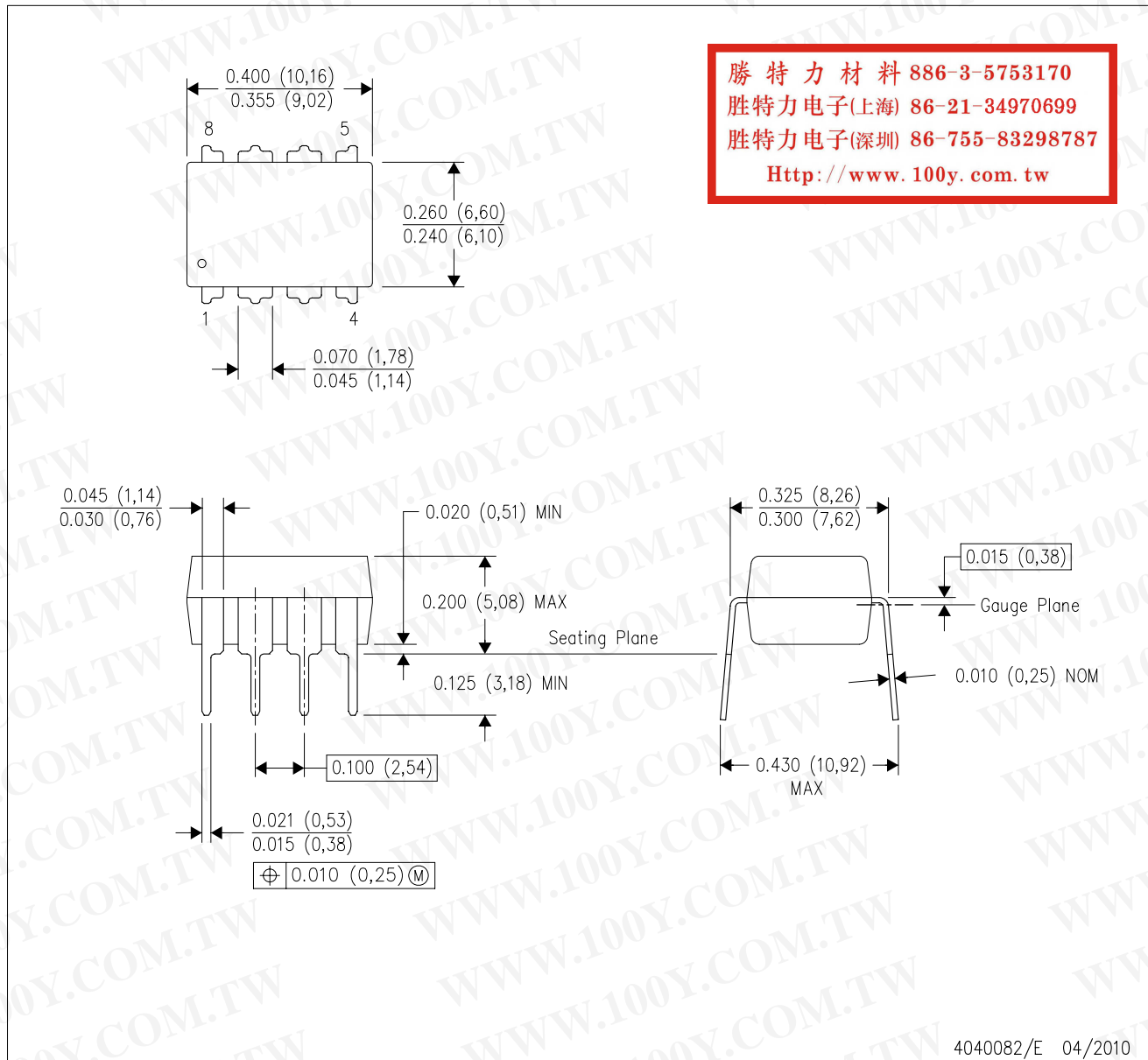
4040140/D 01/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. Falls within JEDEC MS-004

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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



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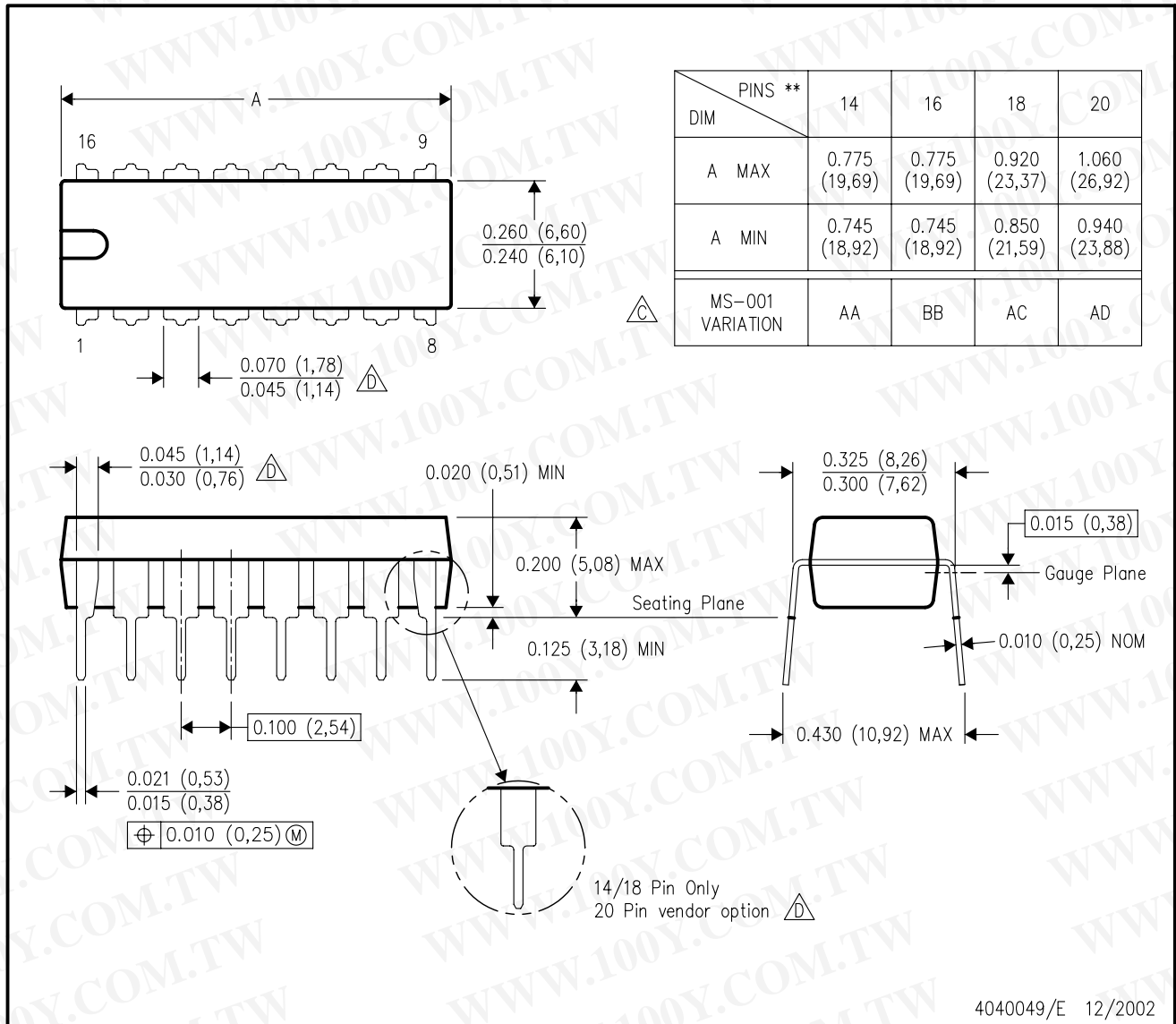
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

4040082/E 04/2010

N (R-PDIP-T\*\*)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

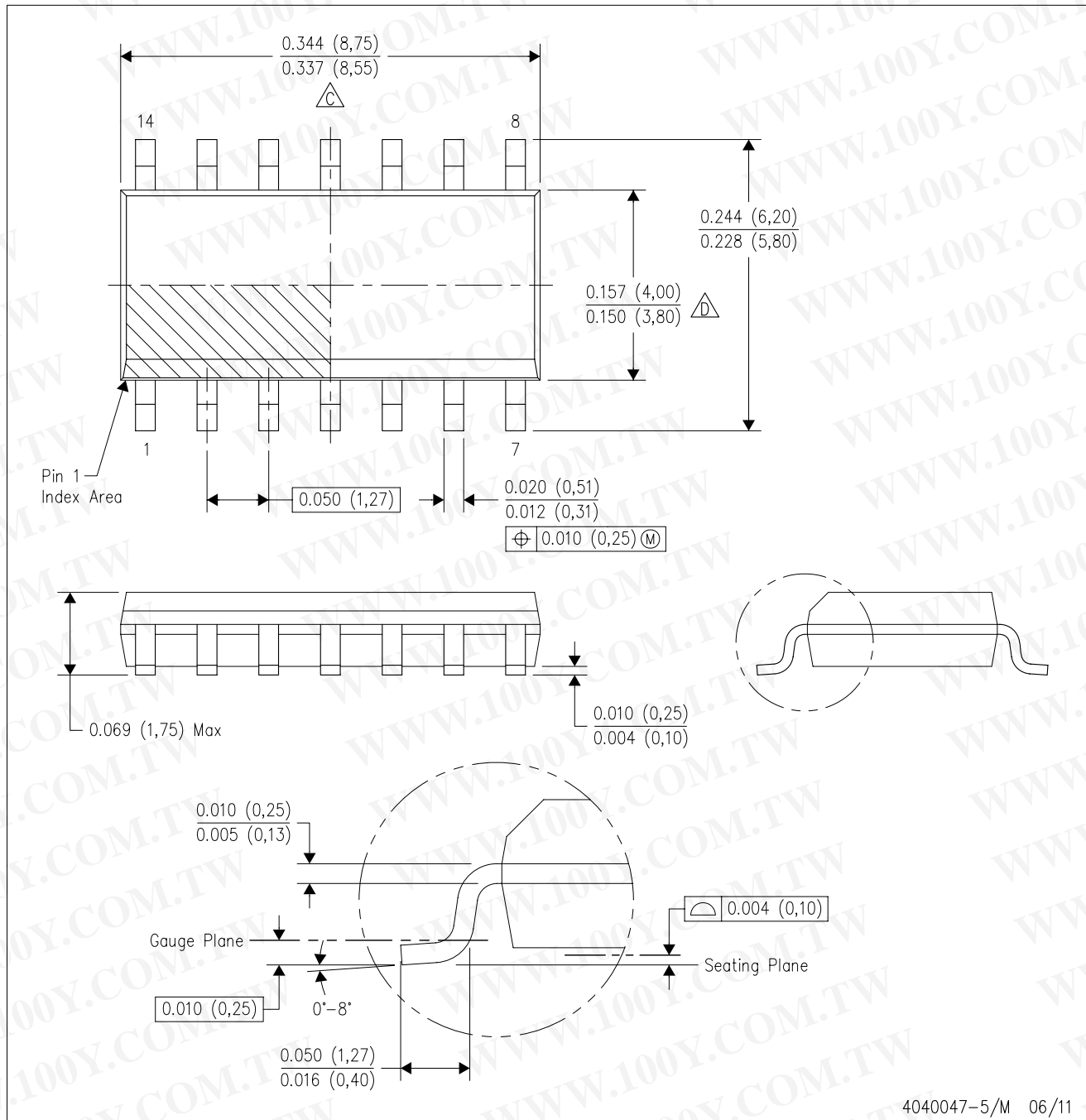


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

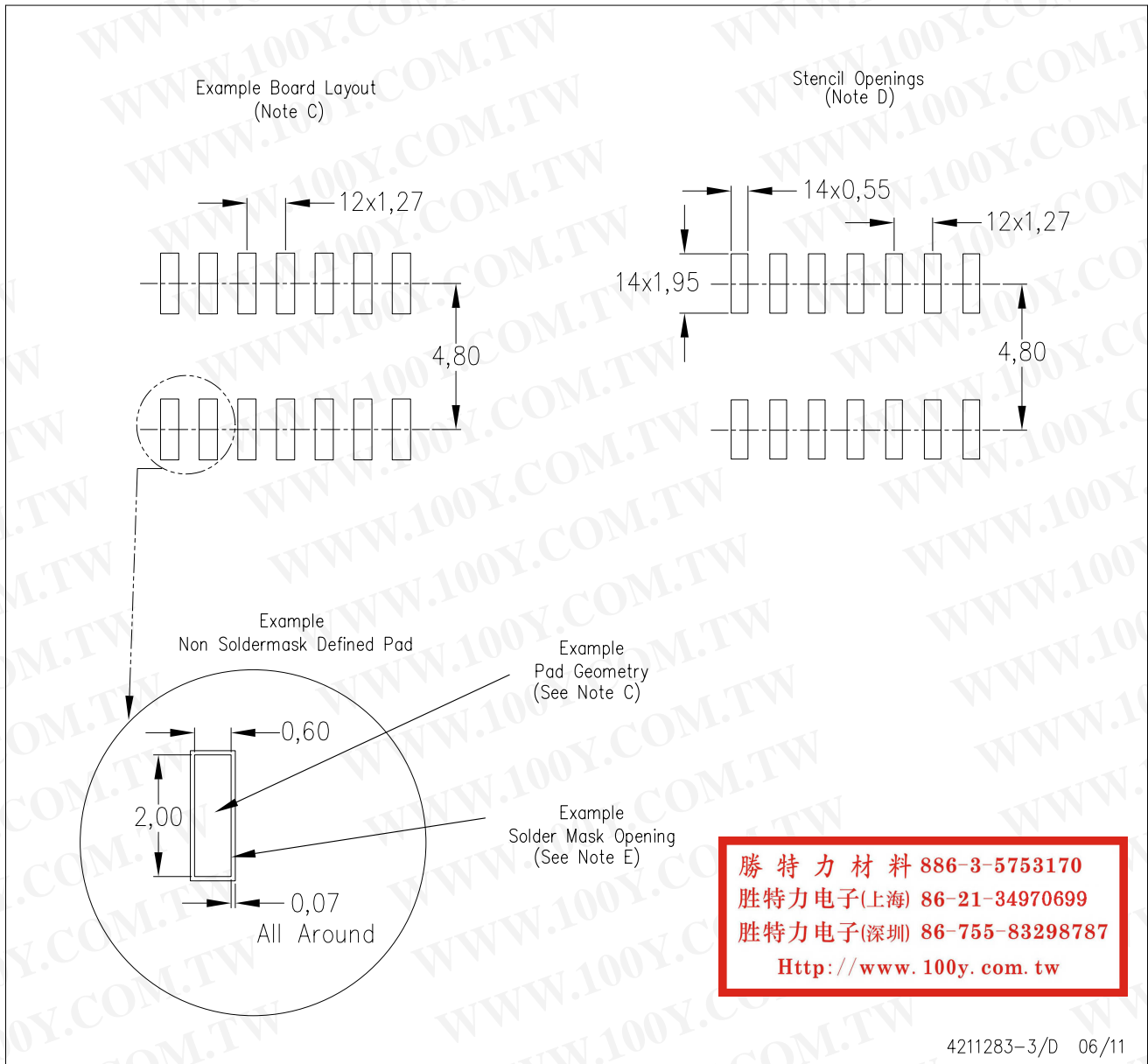


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

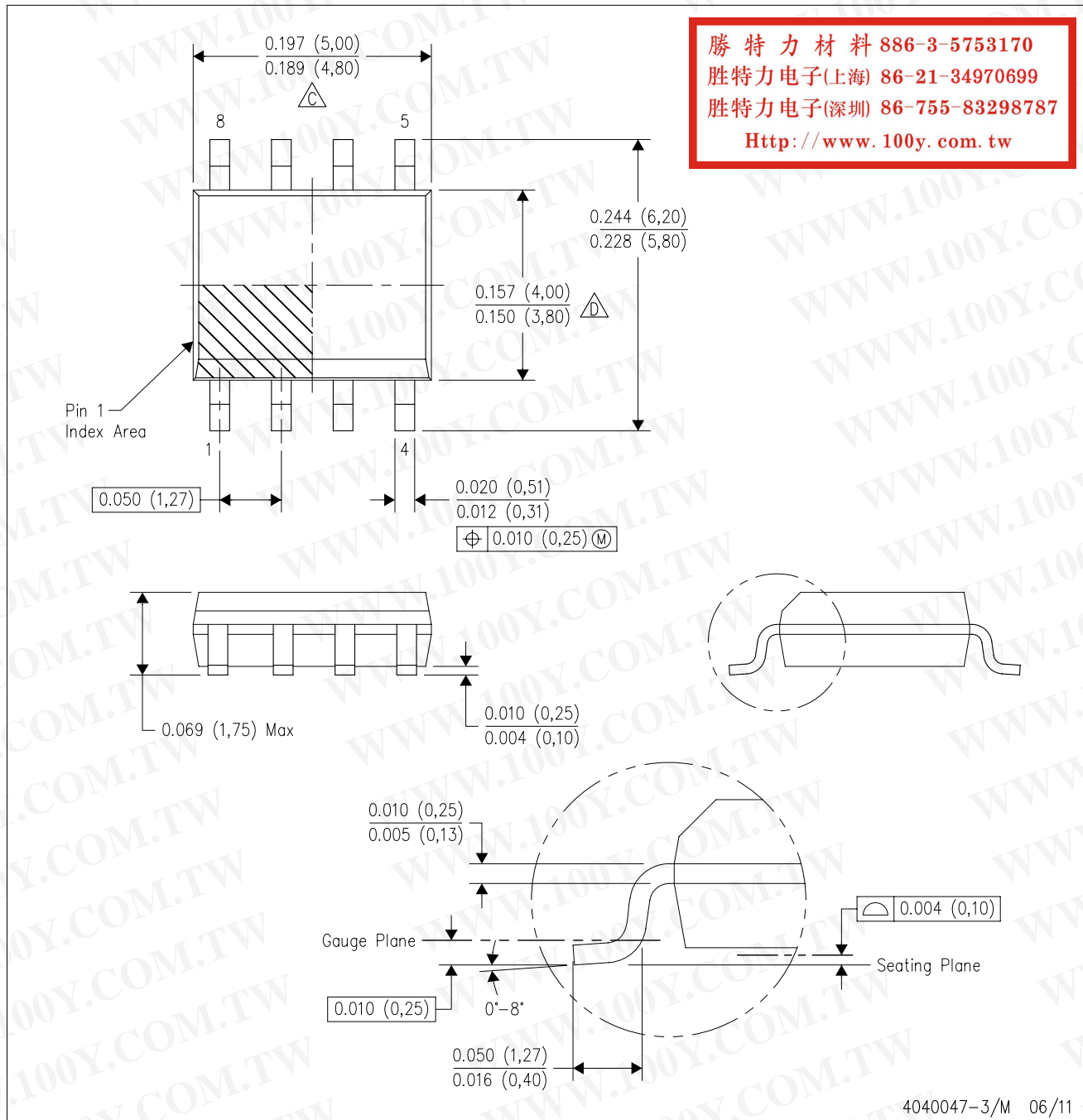
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

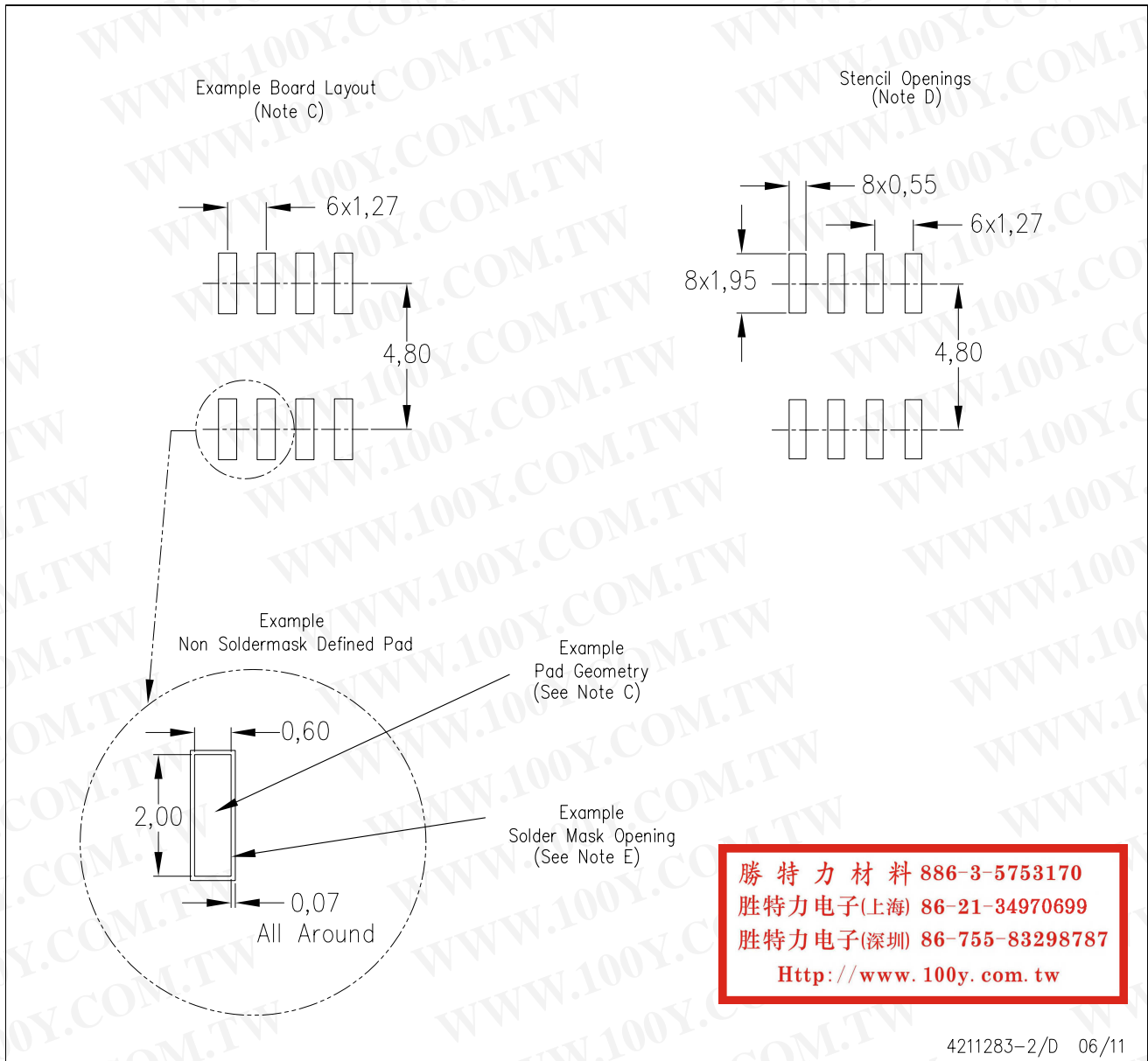
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

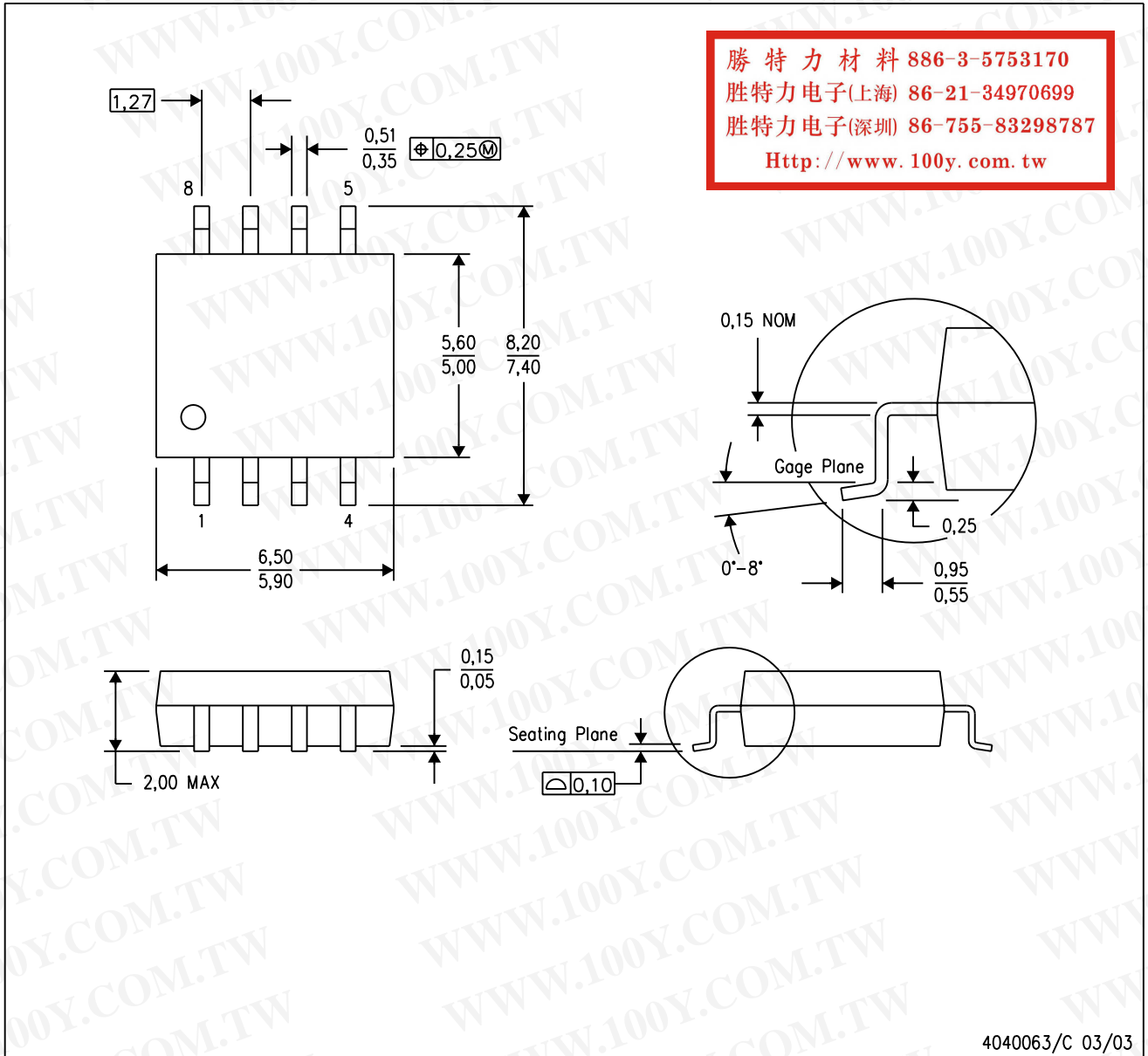


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



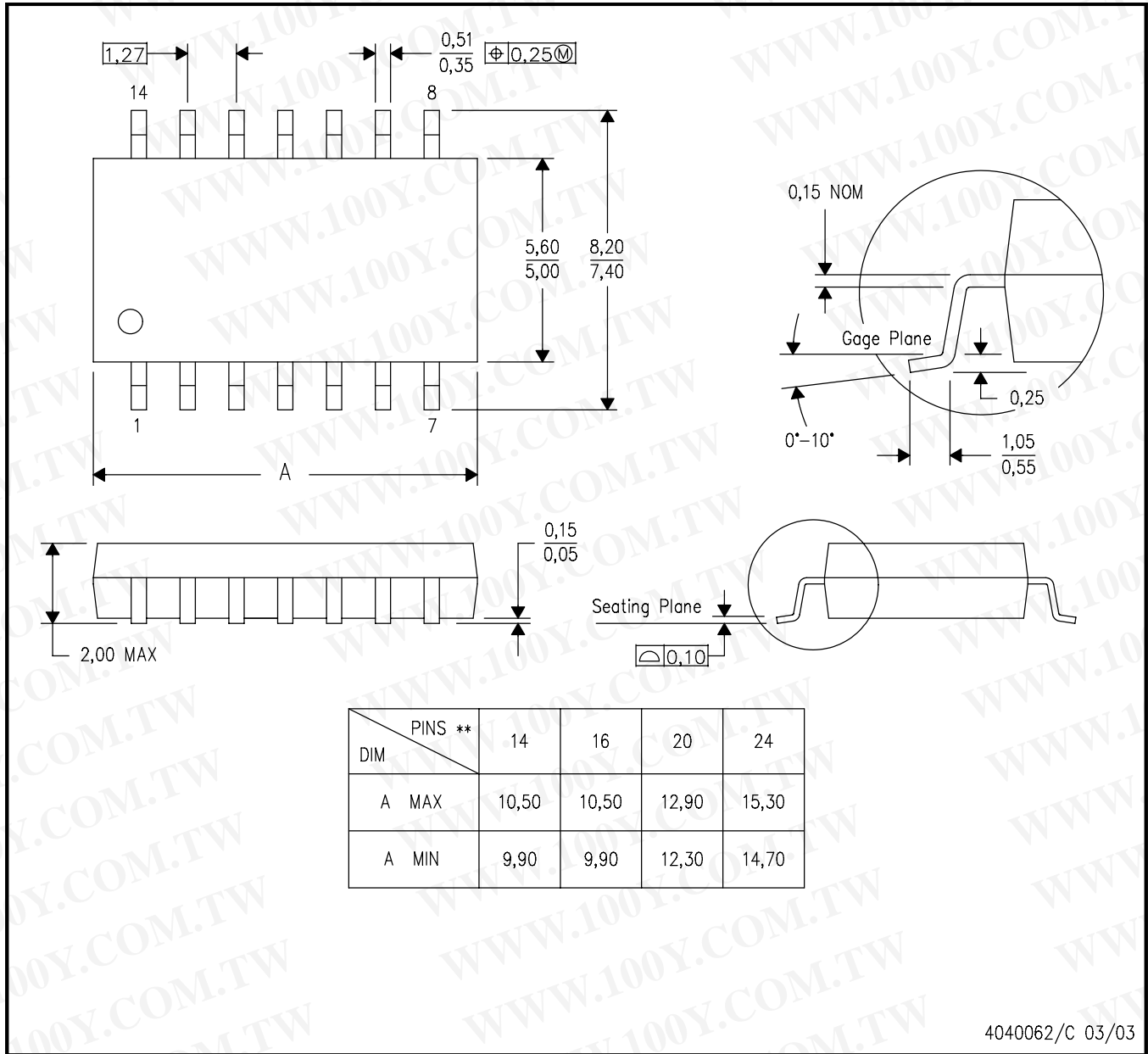
4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)  
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

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