VERY LOW-POWER, HIGH-SPEED, RAIL-TO-RAIL INPUT AND OUTPUT VOLTAGE-FEEDBACK OPERATIONAL AMPLIFIER

FEATURES

- **Very Low Quiescent Current: 750 µA (at 5 V)**
- **Rail-to-Rail Input and Output:**
  - **Common-Mode Input Voltage Extends 400 mV Beyond the Rails**
  - **Output Swings Within 150 mV From the Rails**
- **Wide -3 dB Bandwidth at 5 V:**
  - **90-MHz @ Gain = +1, 40 MHz @ Gain = +2**
- **High Slew Rate: 35 V/µs**
- **Fast Settling Time (2-V Step):**
  - **78 ns to 0.1%**
  - **150 ns to 0.01%**
- **Low Distortion @ Gain = +2, V_O = 2-Vpp, 5 V:**
  - **-91 dBc at 100 kHz, -67 dBc at 1 MHz**
- **Input Offset Voltage: 2.5 mV (Max at 25°C)**
- **Output Current >30 mA (10-Ω Load, 5 V)**
- **Low Voltage Noise of 12.5 nV/√Hz**
- **Supply Voltages: +2.7 V, 3 V, +5 V, ±5 V, +15 V**
- **Packages: SOT-23, MSOP, and SOIC**

APPLICATIONS

- **Portable/Battery-Powered Applications**
- **High Channel Count Systems**
- **ADC Buffer**
- **Active Filters**
- **Current Sensing**

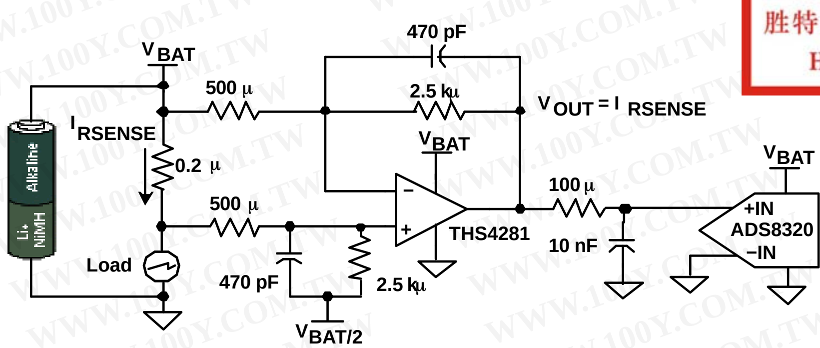
DESCRIPTION

Fabricated using the BiCom-II process, the THS4281 is a low-power, rail-to-rail input and output voltage-feedback operational amplifier designed to operate over a wide power supply range of 2.7-V to 15-V single supply, and ±1.35-V to ±7.5-V dual supply. Consuming only 750 µA with a unity gain bandwidth of 90 MHz and a high 35-V/µs slew rate, the THS4281 allows portable or other power-sensitive applications to realize high performance with minimal power. To ensure long battery life in portable applications, the quiescent current is trimmed to be less than 900 µA at 25°C, and 1 mA from –40°C to 85°C.

The THS4281 is a true single-supply amplifier with a specified common-mode input range of 400 mV beyond the rails. This allows for high-side current sensing applications without phase reversal concerns. Its output swings to within 40 mV from the rails with 10-kΩ loads, and 150 mV from the rails with 1-kΩ loads.

The THS4281 has a good 0.1% settling time of 78 ns, and 0.01% settling time of 150 ns. The low THD of -87 dBc at 100 kHz, coupled with a maximum offset voltage of less than 2.5 mV, makes the THS4281 a good match for high-resolution ADCs sampling less than 2 MSPS.

The THS4281 is offered in a space-saving SOT-23-5 package, a small MSOP-8 package, and the industry standard SOIC-8 package.



High-Side, Low Power Current-Sensing System

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FilterPro is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
Supply voltage, V_{S-} to V_{S+}		16.5 V
Input voltage, V_I		$\pm V_S \pm$ 0.5 V
Differential input voltage, V_{ID}		±2 V
Output current, I_O		±100 mA
Continuous power dissipation		See Dissipation Rating Table
Maximum junction temperature, any condition, (2) T_J		150°C
Maximum junction temperature, continuous operation, long term reliability(2) T_J		125°C
Storage temperature range, T_{stg}		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
ESD ratings	HBM	3500 V
	CDM	1500 V
	MM	100 V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device. recommended operating conditions.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±1.35	±8.25	V
	Single supply	2.7	16.5	

DISSIPATION RATINGS TABLE PER PACKAGE

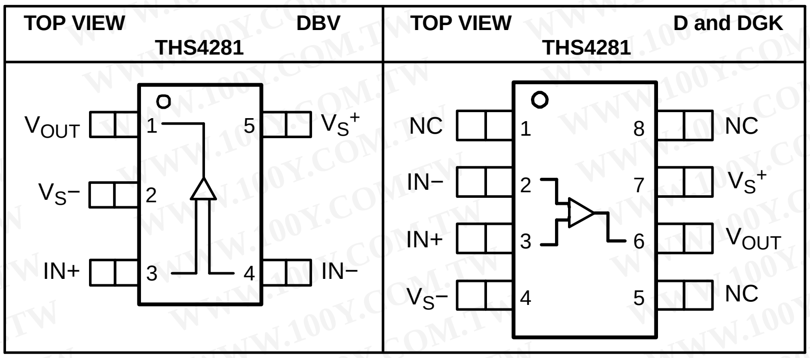
PACKAGE	θ_{JC} (°C/W)	θ_{JA}(1) (°C/W)	POWER RATING(2)	
			T_A < 25°C	T_A = 85°C
DBV (5)	55	255.4	391 mW	156 mW
D (8)	38.3	97.5	1.02 W	410 mW
DGK (8)	71.5	180.8	553 mW	221 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

PACKAGING/ORDERING INFORMATION

PACKAGED DEVICES	DEVICE MARKING	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS4281DBVT	AON	SOT-23 - 5	Tape and Reel, 250
THS4281DBVR			Tape and Reel, 3000
THS4281D	--	SOIC - 8	Rails, 75
THS4281DR			Tape and Reel, 2500
THS4281DGK	AOO	MSOP - 8	Rails, 75
THS4281DGKR			Tape and Reel, 2500

PIN CONFIGURATION



NOTE: NC indicates there is no internal connection to these pins.

TEXAS INSTRUMENTS
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ELECTRICAL CHARACTERISTICS, V_S = 3 V (V_{S+} = 3 V, V_{S-} = GND)

G = +2, R_F = 2.49 kΩ, R_L = 1 kΩ to 1.5 V, unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-Signal Bandwidth	G = +1, V_O = 100 mVpp, R_F = 34 Ω	83				MHz	Typ
	G = +2, V_O = 100 mVpp, R_F = 1.65 kΩ	40				MHz	Typ
	G = +5, V_O = 100 mVpp, R_F = 1.65 kΩ	8				MHz	Typ
	G = +10, V_O = 100 mVpp, R_F = 1.65 kΩ	3.8				MHz	Typ
0.1 dB Flat Bandwidth	G = +2, V_O = 100 mVpp, R_F = 1.65 kΩ	20				MHz	Typ
Full-Power Bandwidth	G = +2, V_O = 2 Vpp	8				MHz	Typ
Slew Rate	G = +1, V_O = 2-V Step	26				V/µs	Typ
	G = -1, V_O = 2-V Step	27				V/µs	Typ
Settling time to 0.1%	G = -1, V_O = 1-V Step	80				ns	Typ
Settling time to 0.01%	G = -1, V_O = 1-V Step	155				ns	Typ
Rise/Fall Times	G = +1, V_O = 2-V Step	55				ns	Typ
Harmonic Distortion	G = +2, V_O = 2 Vpp						
Second Harmonic Distortion	f = 1 MHz, R_L = 1 kΩ	-52				dBc	Typ
Third Harmonic Distortion		-52				dBc	Typ
Second Harmonic Distortion	f = 100 kHz, R_L = 1 kΩ	-69				dBc	Typ
Third Harmonic Distortion		-71				dBc	Typ
THD + N	V_O = 1 Vpp, f = 10 kHz	0.003				%	Typ
	V_O = 2 Vpp, f = 10 kHz	0.03				%	Typ
Differential Gain (NTSC/PAL)	G = +2, R_L = 150 Ω	0.05/0.08				%	Typ
Differential Phase (NTSC/PAL)		0.25/0.35				°	Typ
Input Voltage Noise	f = 100 kHz	12.5				nA/√Hz	Typ
Input Current Noise	f = 100 kHz	1.5				pA/√Hz	Typ
DC PERFORMANCE							
Open-Loop Voltage Gain (AOL)		95				dB	Typ
Input Offset Voltage	V_{CM} = 1.5 V	0.5	2.5	3.5	3.5	mV	Max
Average Offset Voltage Drift				±7	±7	µV/°C	Typ
Input Bias Current		0.5	0.8	1	1	µA	Max
Average Bias Current Drift				±2	±2	nA/°C	Typ
Input Offset Current		0.1	0.4	0.5	0.5	µA	Max
Average Offset Current Drift				±2	±2	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-Mode Input Range		-0.4/3.4	-0.3/3.3	-0.1/3.1	-0.1/3.1	V	Min
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3 V	92	75	70	70	dB	Min
Input Resistance	Common-mode	100				MΩ	Typ
Input Capacitance	Common-mode/Differential	0.8/1.2				pF	Typ

ELECTRICAL CHARACTERISTICS, V_S = 3 V (V_{S+} = 3 V, V_{S-} = GND) (continued)

G = +2, R_F = 2.49 kΩ, R_L = 1 kΩ to 1.5 V, unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ MAX
OUTPUT CHARACTERISTICS							
Output Voltage Swing	R_L = 10 kΩ	0.04/2.96				V	Typ
	R_L = 1 kΩ	0.1/2.9	0.14/2.86	0.2/2.8	0.2/2.8	V	Min
Output Current (Sourcing)	R_L = 10 Ω	23	18	15	15	mA	Min
Output Current (Sinking)	R_L = 10 Ω	29	22	19	19	mA	Min
Output Impedance	f = 1 MHz	1				Ω	Typ
POWER SUPPLY							
Maximum Operating Voltage		3	16.5	16.5	16.5	V	Max
Minimum Operating Voltage		3	2.7	2.7	2.7	V	Min
Maximum Quiescent Current		0.75	0.9	0.98	1.0	mA	Max
Minimum Quiescent Current		0.75	0.6	0.57	0.55	mA	Min
Power Supply Rejection (+PSRR)	V_{S+} = 3.25 V to 2.75 V, V_{S-} = 0 V	90	70	65	65	dB	Min
Power Supply Rejection (-PSRR)	V_{S+} = 3 V, V_{S-} = 0 V to 0.65 V	90	70	65	65	dB	Min

ELECTRICAL CHARACTERISTICS, V_S = 5 V (V_{S+} = 5 V, V_{S-} = GND)

G = +2, R_F = 2.49 kΩ, R_L = 1 kΩ to 2.5 V, unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-Signal Bandwidth	G = +1, V_O = 100 mVpp, R_F = 34 Ω	90				MHz	Typ
	G = +2, V_O = 100 mVpp, R_F = 2 kΩ	40				MHz	Typ
	G = +5, V_O = 100 mVpp, R_F = 2 kΩ	8				MHz	Typ
	G = +10, V_O = 100 mVpp, R_F = 2 kΩ	3.8				MHz	Typ
0.1-dB Flat Bandwidth	G = +2, V_O = 100 mVpp, R_F = 2 kΩ	20				MHz	Typ
Full-Power Bandwidth	G = +2, V_O = 2 Vpp	9				MHz	Typ
Slew Rate	G = +1, V_O = 2-V Step	31				V/µs	Typ
	G = -1, V_O = 2-V Step	34				V/µs	Typ
Settling Time to 0.1%	G = -1, V_O = 2-V Step	78				ns	Typ
Settling Time to 0.01%	G = -1, V_O = 2-V Step	150				ns	Typ
Rise/Fall Times	G = +1, V_O = 2-V Step	48				ns	Typ
Harmonic Distortion	G = +2, V_O = 2 Vpp						
Second Harmonic Distortion	f = 1 MHz, R_L = 1 kΩ	-67				dBc	Typ
Third Harmonic Distortion		-76				dBc	Typ
Second Harmonic Distortion	f = 100 kHz, R_L = 1 kΩ	-92				dBc	Typ
Third Harmonic Distortion		-106				dBc	Typ
THD + N	V_O = 2 Vpp, f = 10 kHz	0.0009				%	Typ
	V_O = 4 Vpp, f = 10 kHz	0.0005				%	Typ
Differential Gain (NTSC/PAL)	G = +2, R_L = 150 Ω	0.11/0.17				%	Typ
Differential Phase (NTSC/PAL)		0.11/0.14				°	Typ
Input Voltage Noise	f = 100 kHz	12.5				nV/√Hz	Typ
Input Current Noise	f = 100 kHz	1.5				pA/√Hz	Typ
DC PERFORMANCE							
Open-Loop Voltage Gain (AOL)		105	85	80	80	dB	Min
Input Offset Voltage	V_{CM} = 2.5 V	0.5	2.5	3.5	3.5	mV	Max
Average Offset Voltage Drift				±7	±7	µV/°C	Typ
Input Bias Current		0.5	0.8	1	1	µA	Max
Average Bias Current Drift				±2	±2	nA/°C	Typ
Input Offset Current		0.1	0.4	0.5	0.5	µA	Max
Average Offset Current Drift				±2	±2	nA/°C	Typ

ELECTRICAL CHARACTERISTICS, V_S = 5 V (V_{S+} = 5 V, V_{S-} = GND) (continued)

G = +2, R_F = 2.49 kΩ, R_L = 1 kΩ to 2.5 V, unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ MAX
INPUT CHARACTERISTICS							
Common-Mode Input Range		-0.4/5.4	-0.3/5.3	-0.1/5.1	-0.1/5.1	V	Min
Common-Mode Rejection Ratio	V_{CM} = 0 V to 5 V	100	85	80	80	dB	Min
Input Resistance	Common-mode	100				MΩ	Typ
Input Capacitance	Common-mode/Differential	0.8/1.2				pF	Typ
OUTPUT CHARACTERISTICS							
Output Voltage Swing	R_L = 10 kΩ	0.04/4.96				V	Typ
	R_L = 1 kΩ	0.15/4.85	0.2/4.8	0.25/4.75	0.25/4.75	V	Min
Output Current (Sourcing)	R_L = 10 Ω	33	24	20	20	mA	Min
Output Current (Sinking)	R_L = 10 Ω	44	30	25	25	mA	Min
Output Impedance	f = 1 MHz	1				Ω	Typ
POWER SUPPLY							
Maximum Operating Voltage		5	16.5	16.5	16.5	V	Max
Minimum Operating Voltage		5	2.7	2.7	2.7	V	Min
Maximum Quiescent Current		0.75	0.9	0.98	1.0	mA	Max
Minimum Quiescent Current		0.75	0.6	0.57	0.55	mA	Min
Power Supply Rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 0 V	100	80	75	75	dB	Min
Power Supply Rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = 0 V to 1.0 V	100	80	75	75	dB	Min

ELECTRICAL CHARACTERISTICS, V_S = ±5 V

G = +2, R_F = 2.49 kΩ, R_L = 1 kΩ, unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-Signal Bandwidth	G = +1, V_O = 100 mVpp, R_F = 34 Ω	95				MHz	Typ
	G = +2, V_O = 100 mVpp	40				MHz	Typ
	G = +5, V_O = 100 mVpp	8				MHz	Typ
	G = +10, V_O = 100 mVpp	3.8				MHz	Typ
0.1-dB Flat Bandwidth	G = +2, V_O = 100 mVpp	20				MHz	Typ
Full-Power Bandwidth	G = +1, V_O = 2 Vpp	9.5				MHz	Typ
Slew Rate	G = +1, V_O = 2-V Step	35				V/μs	Typ
	G = -1, V_O = 2-V Step	35				V/μs	Typ
Settling Time to 0.1%	G = -1, V_O = 2-V Step	78				ns	Typ
Settling Time to 0.01%	G = -1, V_O = 2-V Step	140				ns	Typ
Rise/Fall Times	G = +1, V_O = 2-V Step	45				ns	Typ
Harmonic Distortion	G = +2, V_O = 2 Vpp						
Second Harmonic Distortion	f = 1 MHz, R_L = 1 kΩ	-69				dBc	Typ
Third Harmonic Distortion		-76				dBc	Typ
Second Harmonic Distortion	f = 100 kHz, R_L = 1 kΩ	-93				dBc	Typ
Third Harmonic Distortion		-107				dBc	Typ
THD + N	V_O = 2 Vpp, f = 10 kHz	0.0009				%	Typ
	V_O = 8 Vpp, f = 10 kHz	0.0003				%	Typ
Differential Gain (NTSC/PAL)	G = +2, R_L = 150 Ω	0.03/0.03				%	Typ
Differential Phase (NTSC/PAL)		0.08/0.1				°	Typ
Input Voltage Noise	f = 100 kHz	12.5				nV/√Hz	Typ
Input Current Noise	f = 100 kHz	1.5				pA/√Hz	Typ
DC PERFORMANCE							
Open-Loop Voltage Gain (AOL)		108	90	85	85	dB	Min
Input Offset Voltage	V_{CM} = 0 V	0.5	2.5	3.5	3.5	mV	Max
Average Offset Voltage Drift				±7	±7	μV/°C	Typ
Input Bias Current		0.5	0.8	1	1	μA	Max
Average Bias Current Drift				±2	±2	nA/°C	Typ
Input Offset Current		0.1	0.4	0.5	0.5	μA	Max
Average Offset Current Drift				±2	±2	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-Mode Input Range		±5.4	±5.3	±5.1	±5.1	V	Min
Common-Mode Rejection Ratio	V_{CM} = -5 V to +5 V	107	90	85	85	dB	Min
Input Resistance	Common-mode	100				MΩ	Typ
Input Capacitance	Common-mode / Differential	0.8/1.2				pF	Typ
OUTPUT CHARACTERISTICS							
Output Voltage Swing	R_L = 10 kΩ	±4.93				V	Typ
	R_L = 1 kΩ	±4.8	±4.6	±4.5	±4.5	V	Min
Output Current (Sourcing)	R_L = 10 Ω	48	35	30	30	mA	Min
Output Current (Sinking)	R_L = 10 Ω	60	45	40	40	mA	Min
Output Impedance	f = 1 MHz	1				Ω	Typ

ELECTRICAL CHARACTERISTICS, V_S = ±5 V (continued)

G = +2, R_F = 2.49 kΩ, R_L = 1 kΩ, unless otherwise noted

PARAMETER	CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ MAX
POWER SUPPLY							
Maximum Operating Voltage		±5	±8.25	±8.25	±8.25	V	Max
Minimum Operating Voltage		±5	±1.35	±1.35	±1.35	V	Min
Maximum Quiescent Current		0.8	0.93	1.0	1.05	mA	Max
Minimum Quiescent Current		0.8	0.67	0.62	0.6	mA	Min
Power Supply Rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, V_{S-} = 5.0 V	100	80	75	75	dB	Min
Power Supply Rejection (-PSRR)	V_{S+} = 5 V, V_{S-} = -5.5 V to -4.5 V	100	80	75	75	dB	Min

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
SUPPLY VOLTAGE

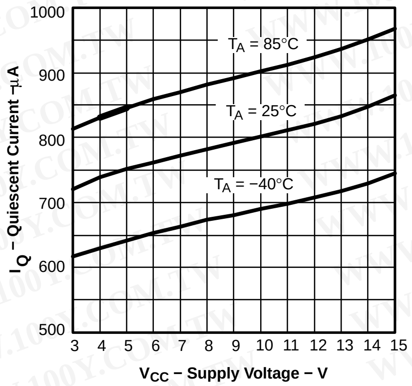

Figure 1.

(V_S = 3 V, V_S = 5 V)
INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

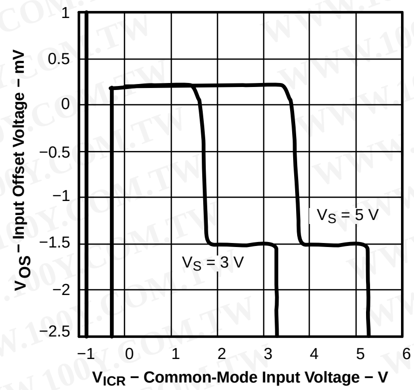

Figure 2.

(V_S = ±5 V)
INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

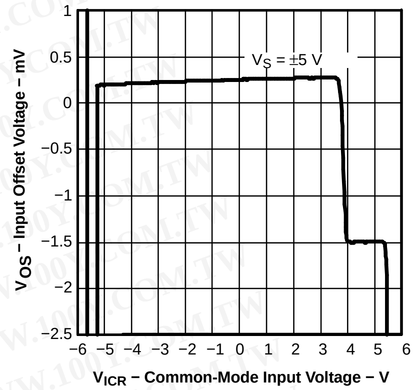

Figure 3.

(V_S = 15 V)
INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

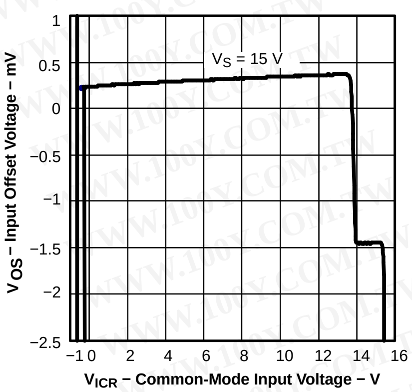

Figure 4.

POSITIVE VOLTAGE HEADROOM
vs
SOURCE CURRENT

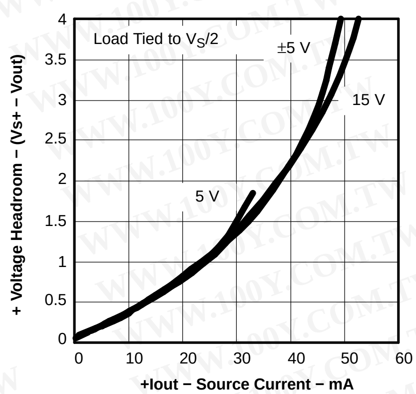

Figure 5.

NEGATIVE VOLTAGE HEADROOM
vs
SINK CURRENT

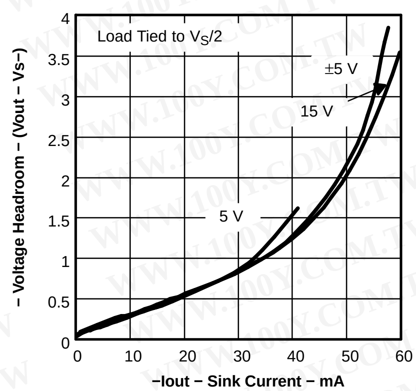

Figure 6.

(V_S = 5 V)
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

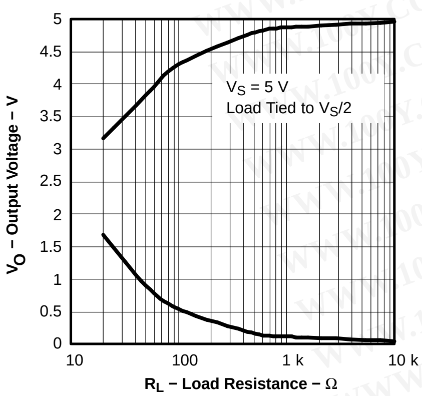

Figure 7.

(V_S = ±5 V)
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

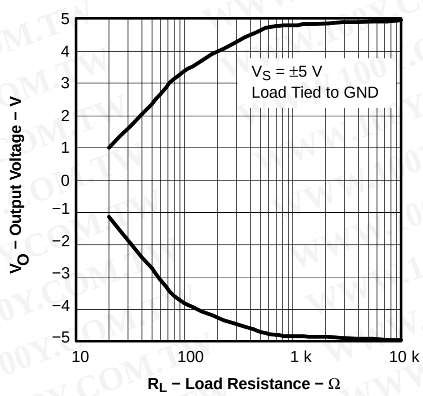

Figure 8.

(V_S = 15 V)
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

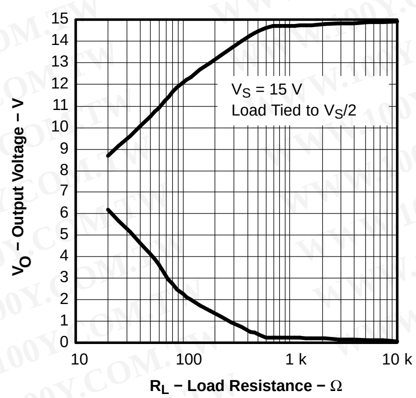

Figure 9.

TYPICAL CHARACTERISTICS (continued)

FREQUENCY RESPONSE

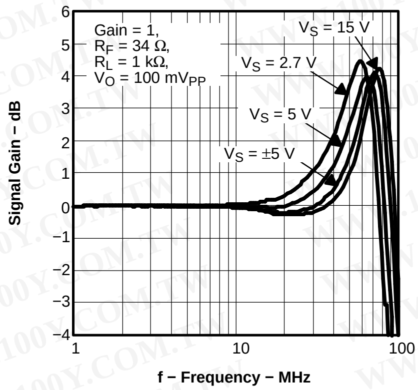

Figure 10.

(VS = 2.7 V) FREQUENCY RESPONSE

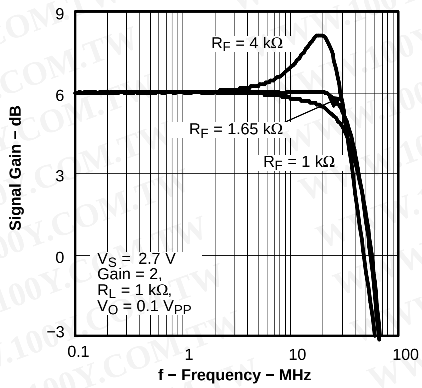

Figure 11.

(VS = 3 V) FREQUENCY RESPONSE

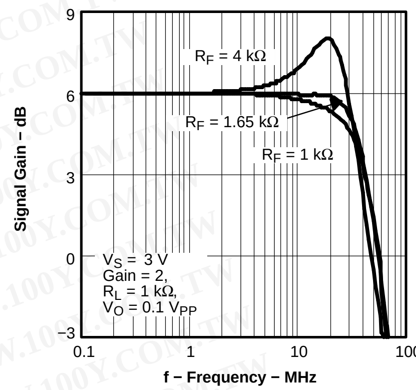

Figure 12.

(VS = 5 V) FREQUENCY RESPONSE

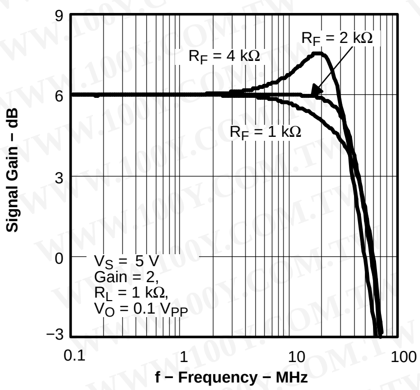

Figure 13.

(VS = ±5 V) FREQUENCY RESPONSE

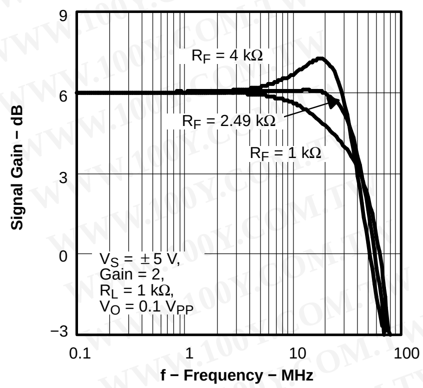

Figure 14.

(VS = 2.7 V, VS = 3 V) 0.1-dB FREQUENCY RESPONSE

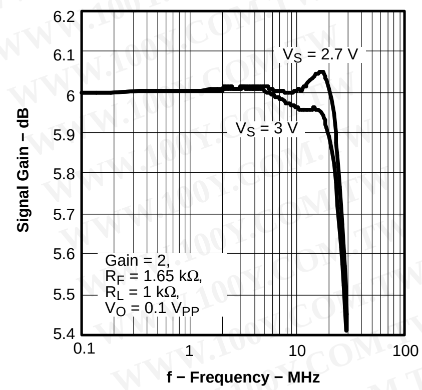

Figure 15.

(VS = 5 V, ±5 V, 15 V) 0.1-dB FREQUENCY RESPONSE

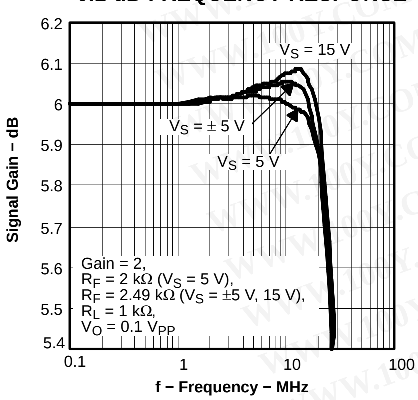

Figure 16.

(VS = 2.7 V) FREQUENCY RESPONSE

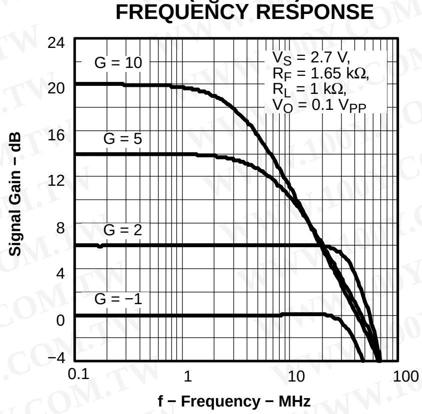

Figure 17.

(VS = 3 V) FREQUENCY RESPONSE

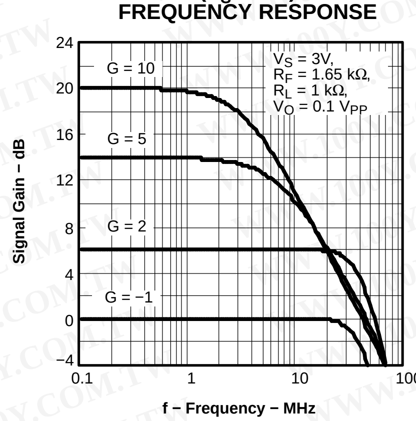

Figure 18.

TYPICAL CHARACTERISTICS (continued)

(V_S = 5 V) FREQUENCY RESPONSE

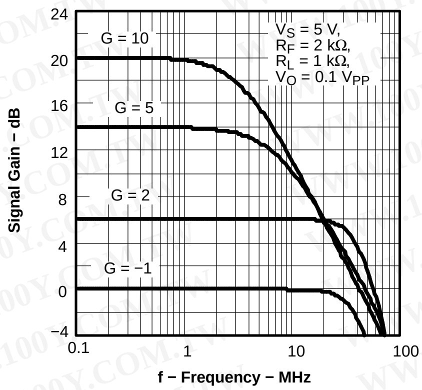

Figure 19.

(V_S = ±5 V) FREQUENCY RESPONSE

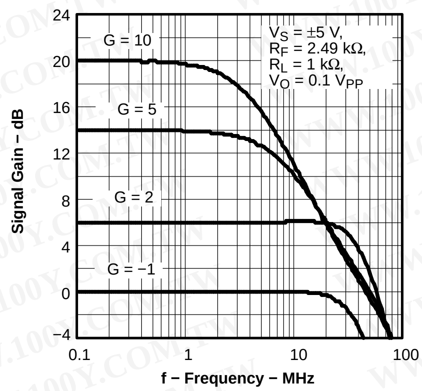

Figure 20.

(V_S = 15 V) FREQUENCY RESPONSE

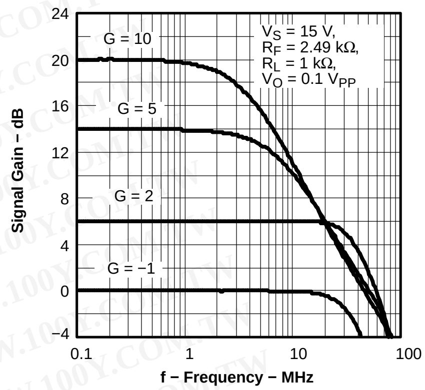

Figure 21.

(V_S = 2.7 V) LARGE-SIGNAL FREQUENCY RESPONSE

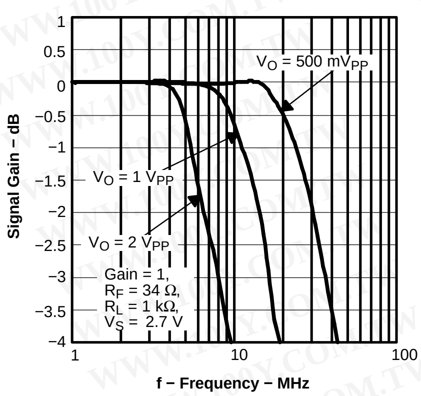

Figure 22.

(V_S = 5 V) LARGE-SIGNAL FREQUENCY RESPONSE

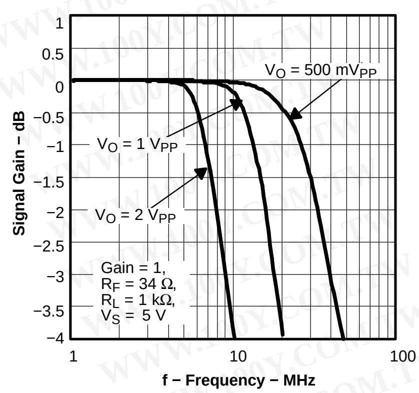

Figure 23.

(V_S = ±5 V) LARGE-SIGNAL FREQUENCY RESPONSE

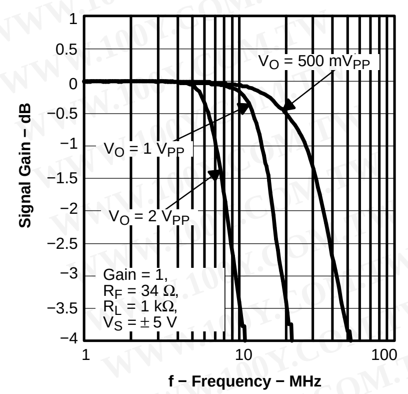

Figure 24.

OPEN-LOOP GAIN vs FREQUENCY

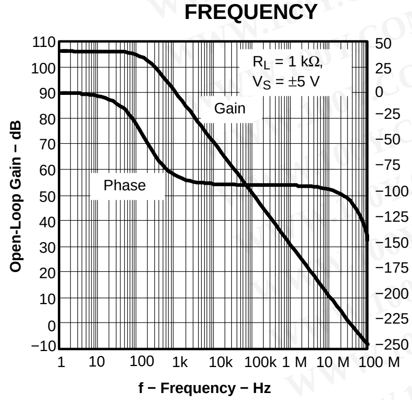

Figure 25.

OUTPUT IMPEDANCE vs FREQUENCY

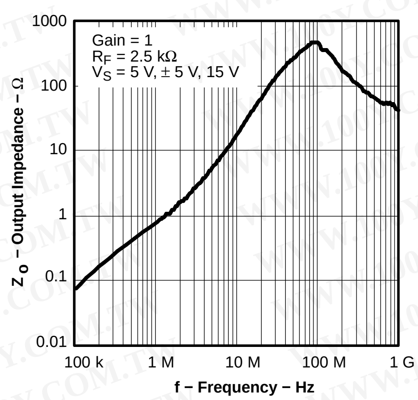

Figure 26.

REJECTION RATIO vs FREQUENCY

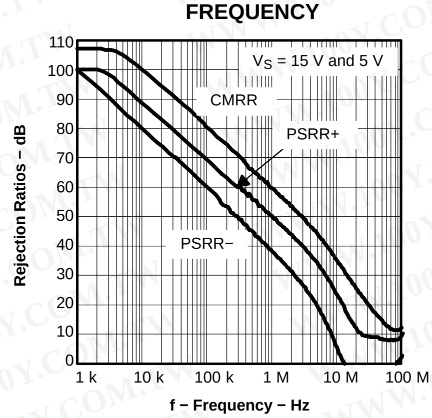

Figure 27.

TYPICAL CHARACTERISTICS (continued)

NOISE vs FREQUENCY

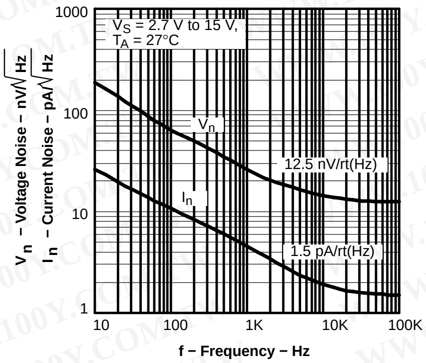

Figure 28.

(V_S = 2.7 V) SLEW RATE

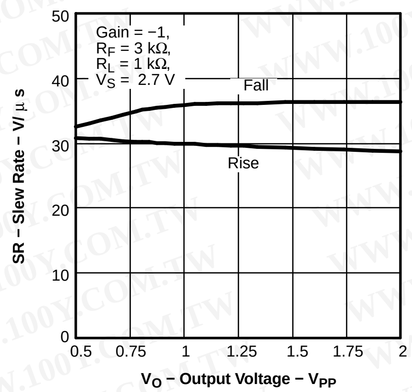

Figure 29.

(V_S = 5 V) SLEW RATE

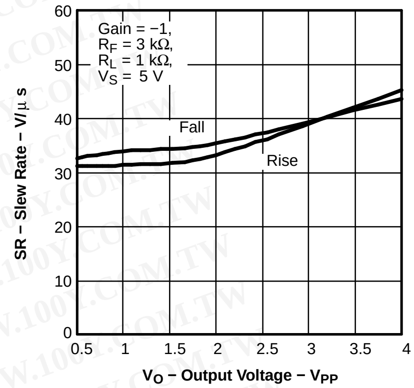

Figure 30.

(V_S = ±5 V) SLEW RATE

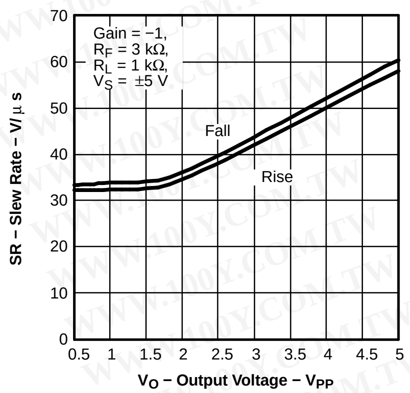

Figure 31.

(V_S = 15 V) SLEW RATE

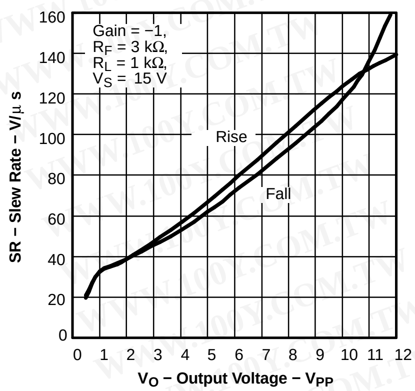

Figure 32.

(V_S = ±1.35 V) SETTLING TIME

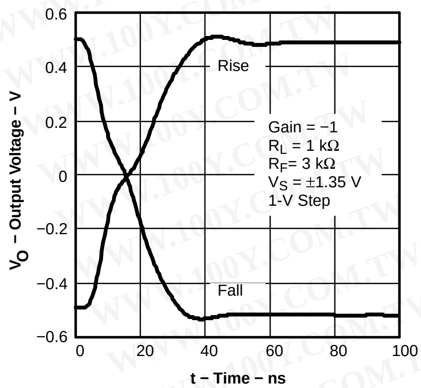

Figure 33.

(V_S = ±1.35 V) SETTLING TIME

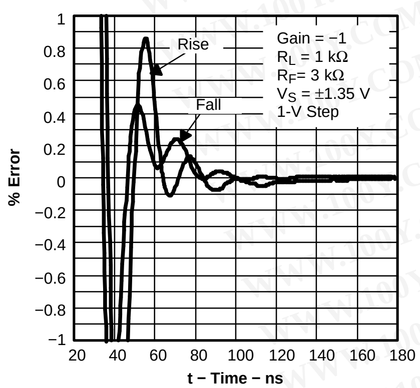

Figure 34.

(V_S = ±2.5 V) SETTLING TIME

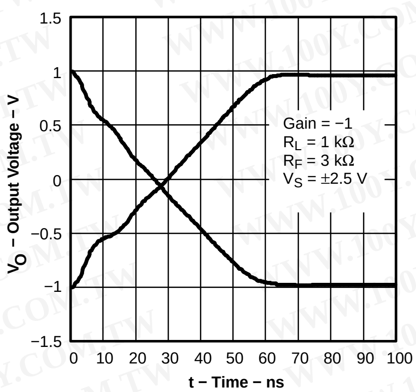

Figure 35.

(V_S = ±2.5 V) SETTLING TIME

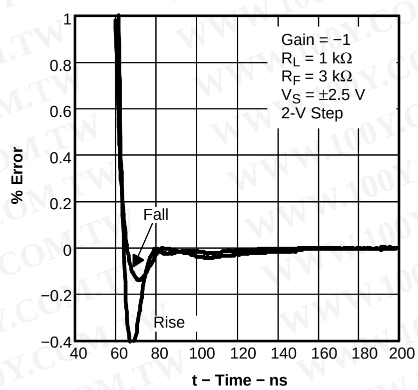

Figure 36.

TYPICAL CHARACTERISTICS (continued)

$(V_S = \pm 5\ V)$
SETTLING TIME

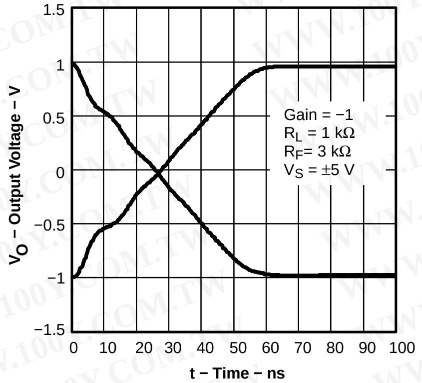

Figure 37.

$(V_S = \pm 5\ V)$
SETTLING TIME

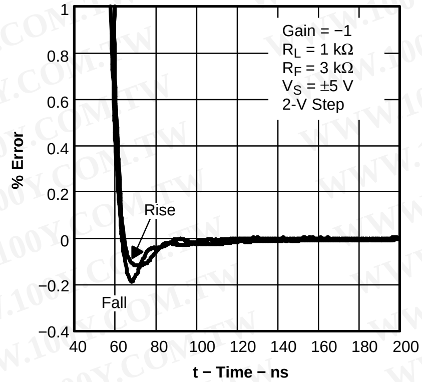

Figure 38.

(Gain = +1)
HARMONIC DISTORTION
vs
FREQUENCY

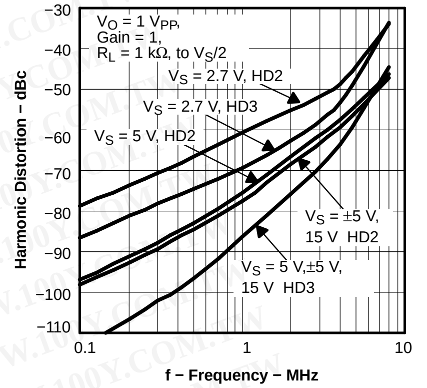

Figure 39.

(Gain = +1)
HARMONIC DISTORTION
vs
FREQUENCY

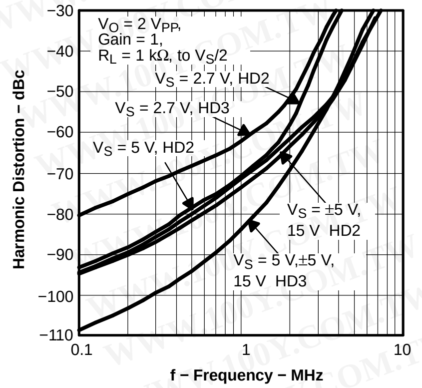

Figure 40.

$(V_S = 3\ V, 3.3\ V)$
HARMONIC DISTORTION
vs
FREQUENCY

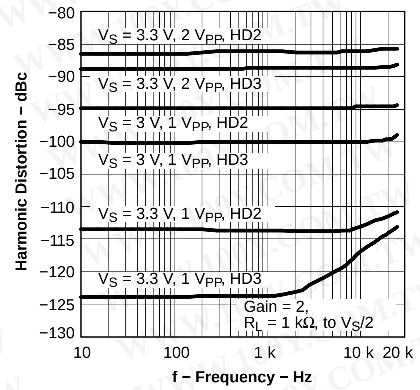

Figure 41.

(Gain = +2)
HARMONIC DISTORTION
vs
FREQUENCY

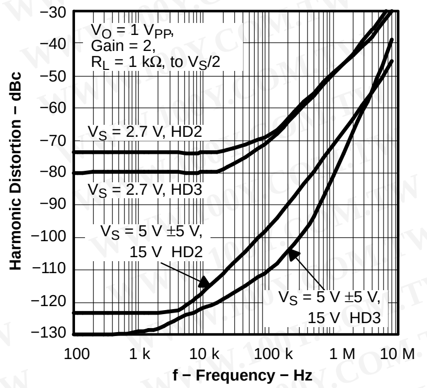

Figure 42.

(Gain = +2)
HARMONIC DISTORTION
vs
FREQUENCY

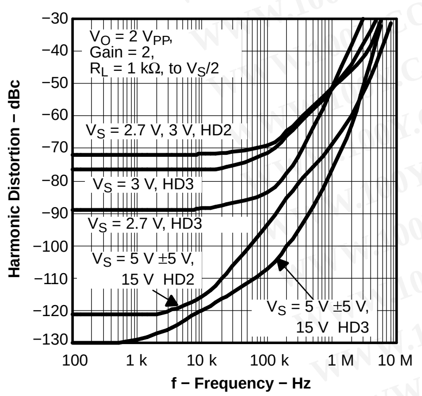

Figure 43.

HARMONIC DISTORTION
vs
LOAD RESISTANCE

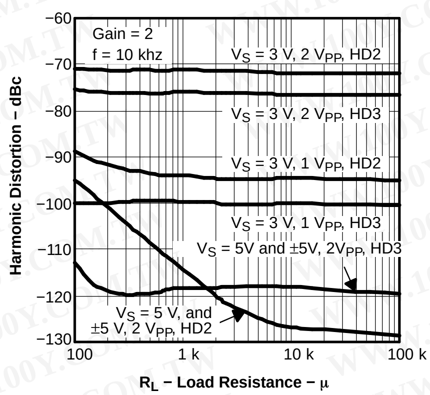

Figure 44.

$(V_S = 2.7\ V, 5\ V)$
HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

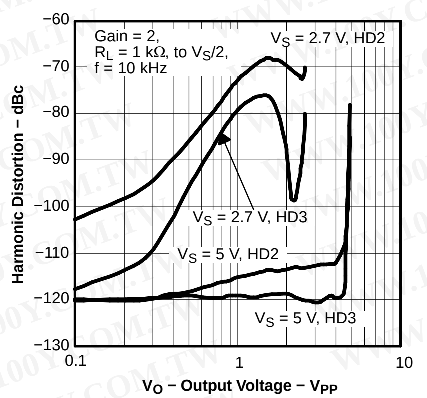

Figure 45.

TYPICAL CHARACTERISTICS (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE (V_S = 3 V, ±5 V)

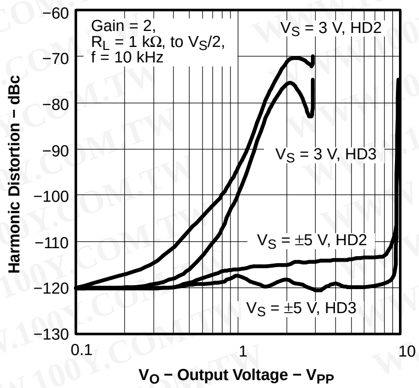

Figure 46.

HARMONIC DISTORTION vs OUTPUT VOLTAGE (V_S = 3.3 V, 15 V)

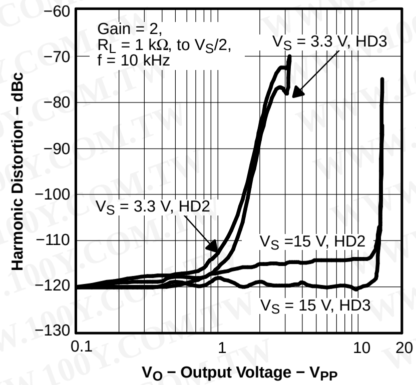

Figure 47.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (V_S = 2.7 V)

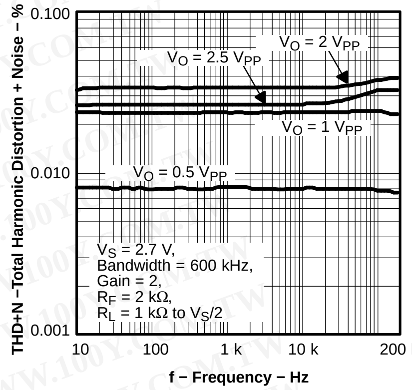

Figure 48.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (V_S = 3 V)

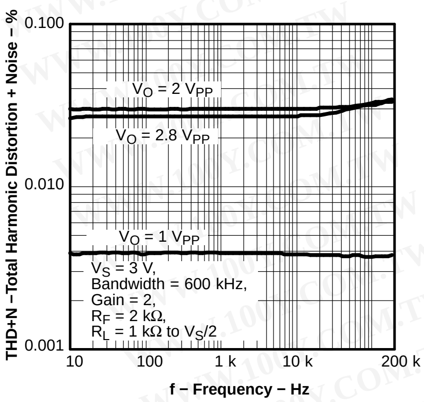

Figure 49.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (V_S = 5 V)

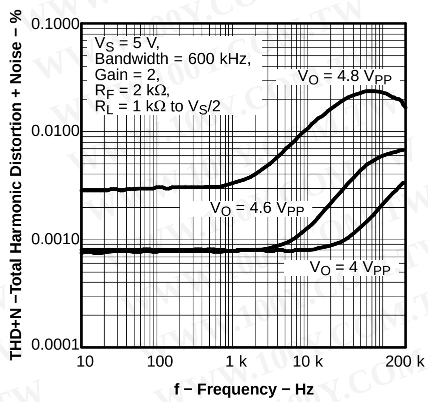

Figure 50.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (V_S = ±5 V)

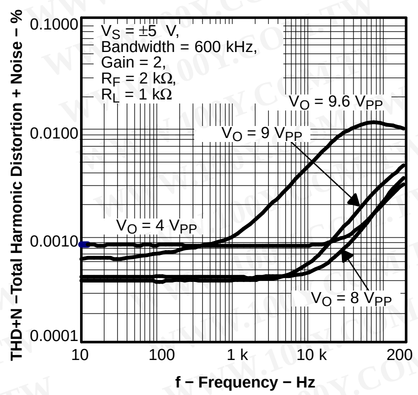

Figure 51.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (V_S = 15 V)

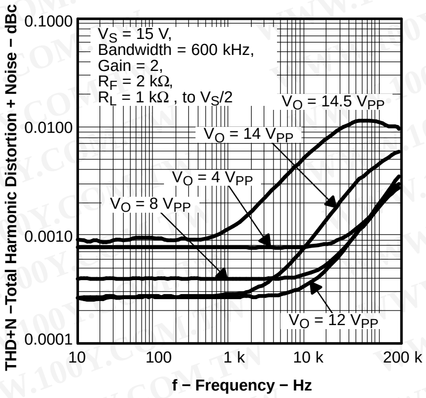

Figure 52.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE (f = 1 kHz)

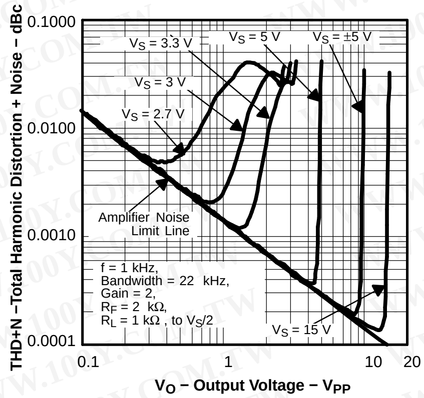

Figure 53.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE (f = 10 kHz)

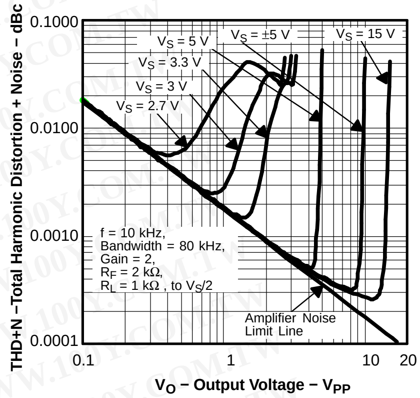

Figure 54.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE (f = 100 kHz)

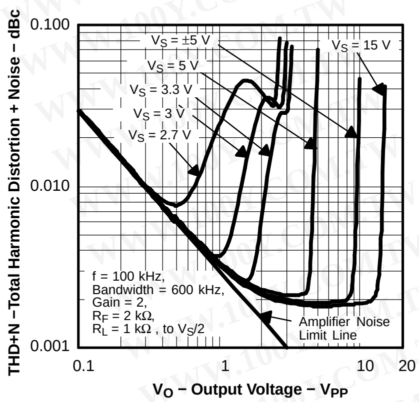

Figure 55.

DIFFERENTIAL GAIN vs NUMBER OF LOADS (V_S = 5 V)

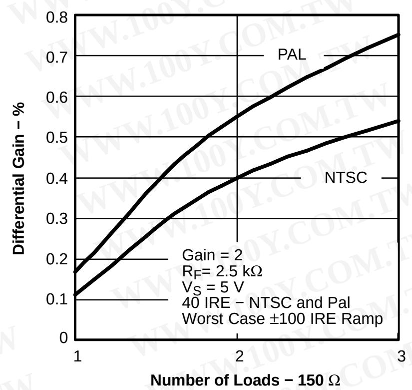

Figure 56.

DIFFERENTIAL PHASE vs NUMBER OF LOADS (V_S = 5 V)

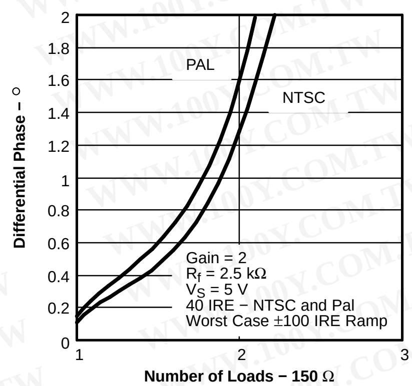

Figure 57.

TYPICAL CHARACTERISTICS (continued)

**(V_S = ±5 V)
DIFFERENTIAL GAIN
vs
NUMBER OF LOADS**

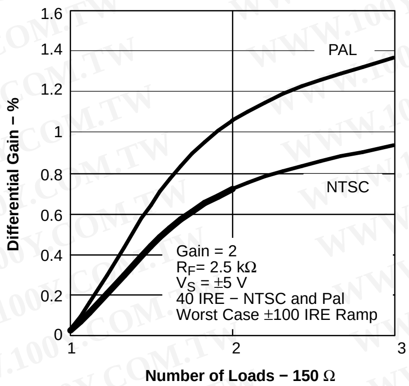

Figure 58.

**(V_S = ±5 V)
DIFFERENTIAL PHASE
vs
NUMBER OF LOADS**

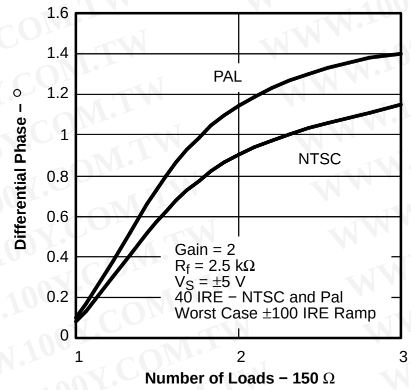

Figure 59.

**INPUT OFFSET VOLTAGE
vs
TEMPERATURE**

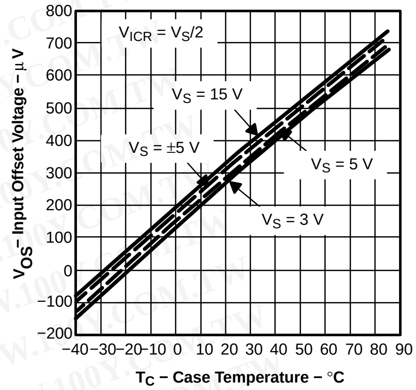

Figure 60.

**(V_S = 5 V)
INPUT BIAS AND OFFSET
CURRENT
vs
TEMPERATURE**

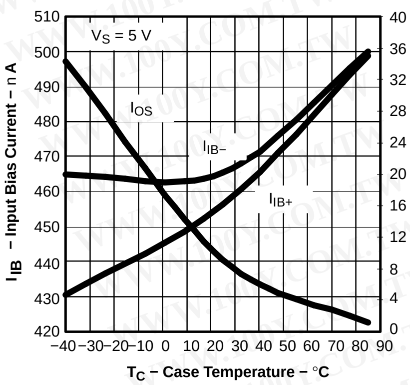

Figure 61.

**(V_S = 15 V)
INPUT BIAS AND
OFFSET CURRENT
vs
TEMPERATURE**

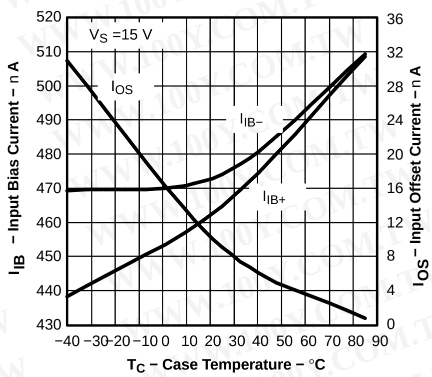

Figure 62.

**SMALL-SIGNAL
TRANSIENT RESPONSE**

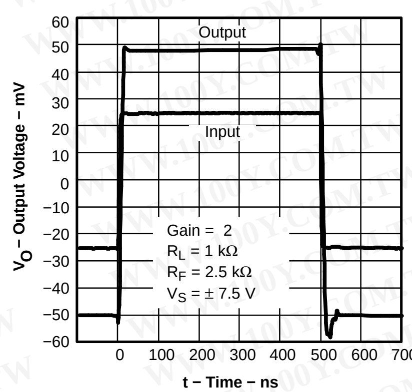

Figure 63.

**LARGE-SIGNAL
TRANSIENT RESPONSE**

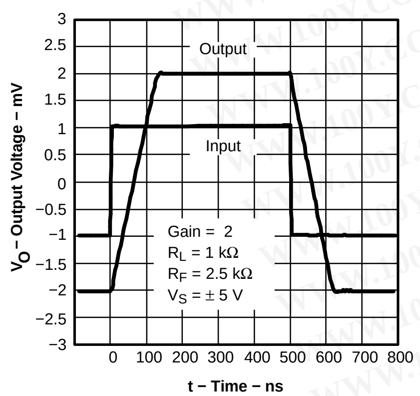

Figure 64.

**(V_S = 5 V)
OVERDRIVE RECOVERY TIME**

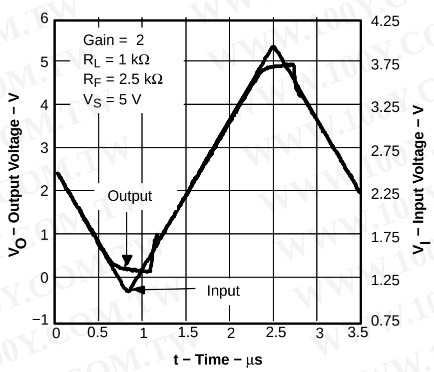

Figure 65.

**(V_S = ±5 V)
OVERDRIVE RECOVERY TIME**

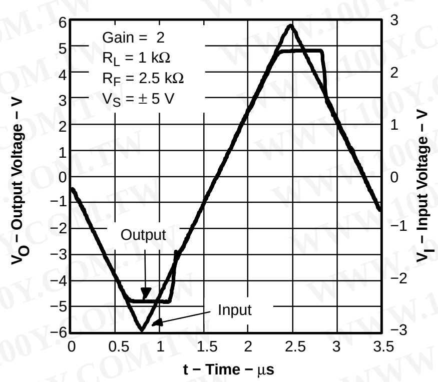

Figure 66.

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TYPICAL CHARACTERISTICS (continued)

OVERDRIVE RESPONSE
OUTPUT VOLTAGE
vs
TIME

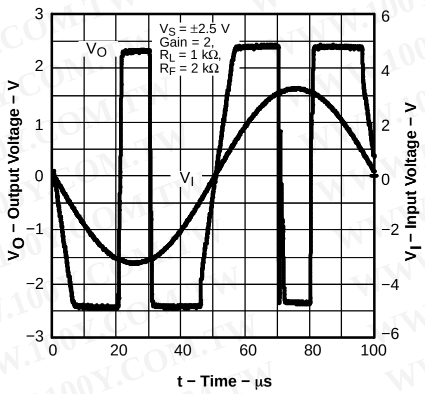


Figure 67.

APPLICATION INFORMATION

HIGH-SPEED OPERATIONAL AMPLIFIERS

The THS4281 is a unity gain stable rail-to-rail input and output voltage feedback operational amplifier designed to operate from a single 2.7-V to 16.5-V power supply.

Applications Section Contents

- Wideband, Noninverting Operation
- Wideband, Inverting Gain Operation
- Video Drive Circuits
- Single-Supply Operation
- Power Supply Decoupling Techniques and Recommendations
- Active Filtering With the THS4281
- Driving Capacitive Loads
- Board Layout
- Thermal Analysis
- Additional Reference Material
- Mechanical Package Drawings

WIDEBAND, NONINVERTING OPERATION

Figure 68 shows the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves.

Voltage feedback amplifiers can use a wide range of resistors values to set their gain with minimal impact on frequency response. Larger-valued resistors decrease loading of the feedback network on the output of the amplifier, but may cause peaking and instability. For a gain of +2, feedback resistor values between 1 kΩ and 4 kΩ are recommended for most applications. However, as the gain increases, the use of even higher feedback resistors can be used to conserve power. This is due to the inherent nature of amplifiers becoming more stable as the gain increases, at the expense of bandwidth. Figure 69 and Figure 70 show the THS4281 using feedback resistors of 10 kΩ and 100 kΩ. Be cautioned that using such high values with high-speed amplifiers is not typically recommended, but under certain conditions, such as high gain and good high-speed-PCB layout practices, such resistances can be used.

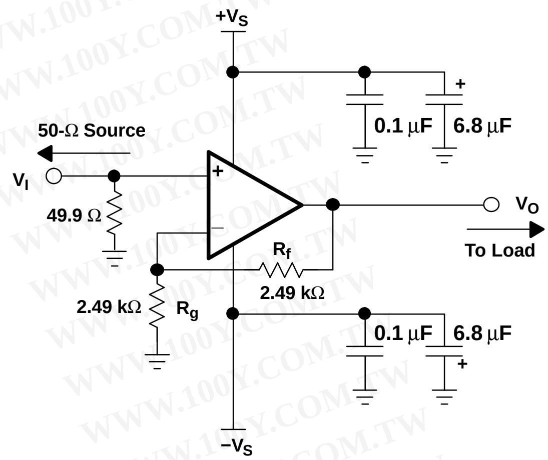


Figure 68. Wideband, Noninverting Gain Configuration

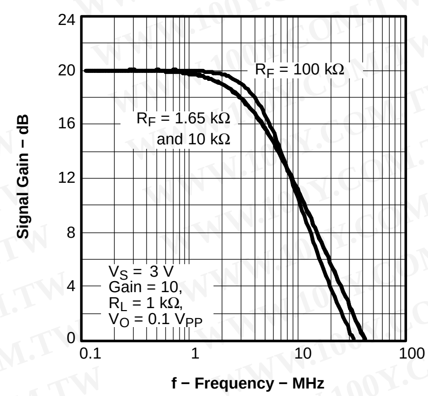


Figure 69. Signal Gain vs Frequency, V_S = 3 V

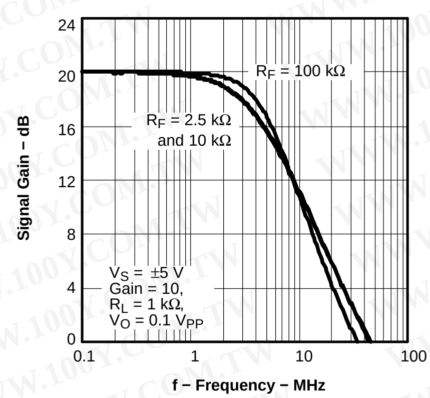


Figure 70. Signal Gain vs Frequency, V_S = ±5 V

WIDEBAND, INVERTING OPERATION

Figure 71 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 68 are retained with an inverting circuit gain of -1 V/V.

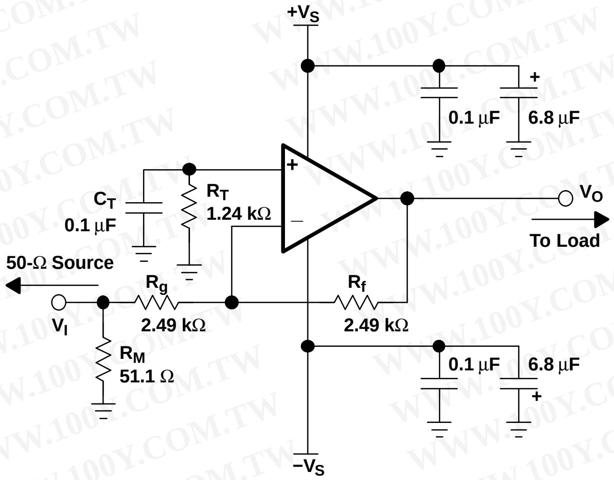


Figure 71. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resultant feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2, setting R_g to 49.9 Ω for input matching, eliminates the need for R_M but requires a 100-Ω feedback resistor. The 100-Ω feedback resistor, in parallel with the external load, causes excessive loading on the amplifier output. To eliminate this excessive loading, it is preferable to increase both R_g and R_f values, as shown in Figure 71, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance is the parallel combination of R_g and R_M.

Another consideration in inverting amplifier design is setting the bias current cancellation resistor (R_T) on the noninverting input. If the resistance is set equal to the total dc resistance presented to the device at the inverting terminal, the output dc error (due to the input bias currents) is reduced to the input offset current multiplied by R_T. In Figure 71, the dc source impedance presented at the inverting terminal is 2.49 kΩ || (2.49 kΩ + 25.3 Ω) ≅ 1.24 kΩ. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, R_T is bypassed with a 0.1-µF capacitor to ground (C_T).

SINGLE-SUPPLY OPERATION

The THS4281 is designed to operate from a single 2.7-V to 16.5-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing and not violate V_{ICR}. The circuits shown in Figure 72 shows inverting and noninverting amplifiers configured for single-supply operation.

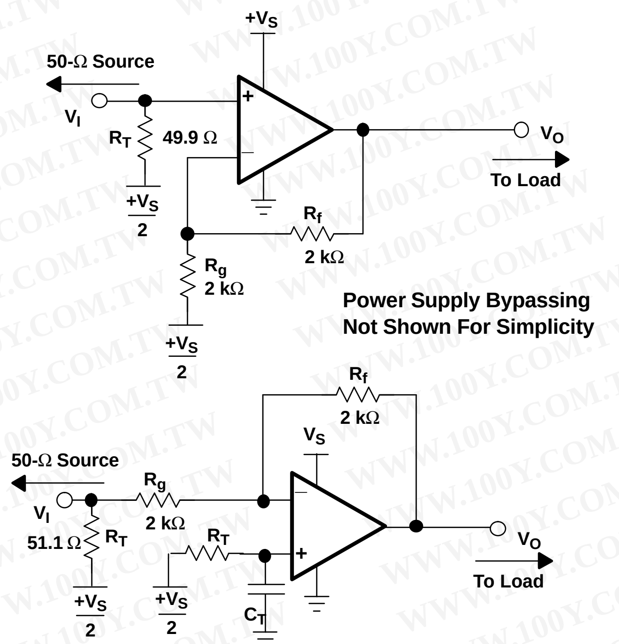


Figure 72. DC-Coupled Single Supply Operation

APPLICATION CIRCUITS

Active Filtering With the THS4281

High performance active filtering with the THS4281 is achievable due to the amplifier's good slew rate, wide bandwidth, and voltage feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. Filters can be quite complex and time consuming to design. Several books and application reports are available to help design active filters. But, to help simplify the process and minimize the chance of miscalculations, Texas Instruments has developed a filter design program called FilterPro™. FilterPro is available for download at no cost from TI's Web site (www.ti.com).

The two most common low-pass filter circuits used are the Sallen-Key filter and the Multiple Feedback (MFB)–aka Rauch filter. FilterPro was used to determine a 2-pole Butterworth response filter with a corner (-3 dB) frequency of 100 kHz which is shown in Figure 73 and Figure 74. One of the advantages of the MFB filter, a much better high frequency rejection, is clearly shown in the response shown in Figure 75. This is due to the inherent R-C filter to ground being the first elements in the design of the MFB filter. The Sallen-Key design also has an R-C filter, but the capacitor connects directly to the output. At very high frequencies, where the amplifier's access loop gain is decreasing, the ability of the amplifier to reject high frequencies is severely reduced and allows the high frequency signals to pass through the system. One other advantage of the MFB filter is the reduced sensitivity in component variation. This is important when using real-world components where capacitors can easily have ±10% variations.

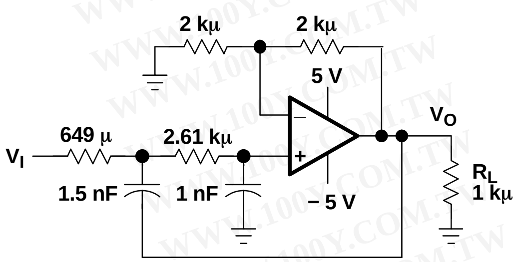


Figure 73. Second-Order Sallen-Key 100-kHz Butterworth Filter, Gain = 2 V/V

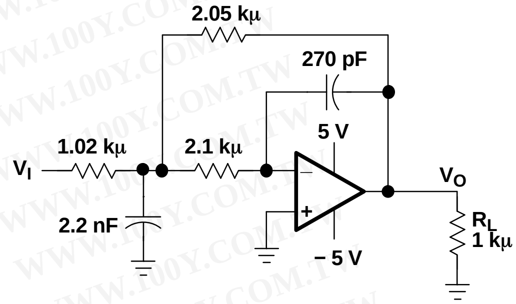


Figure 74. Second-Order MFB 100-kHz Butterworth Filter, Gain = 2 V/V

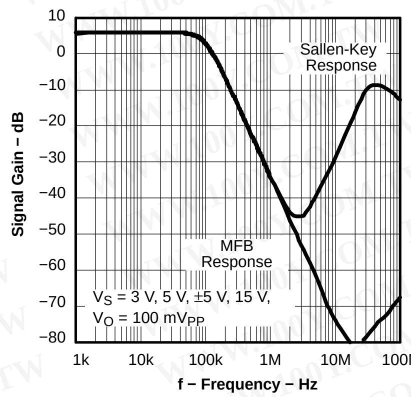


Figure 75. Second-Order 100-kHz Active Filter Response

Driving Capacitive Loads

One of the most demanding, and yet common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the THS4281 can be susceptible to instability and peaking when a capacitive load is placed directly on the output. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the feedback path that decreases the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, a simple and effective solution is to isolate the capacitive load from the feedback loop by inserting a small series isolation resistor (10 Ω to 25 Ω) between the amplifier output and the capacitive load.

Power Supply Decoupling Techniques and Recommendations

Power supply decoupling is a critical aspect of any high-performance amplifier design. Careful decoupling provides higher quality ac performance. The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance.
2. Placement priority should put the smallest valued capacitors closest to the device.
3. Use of solid power and ground planes is recommended to reduce the inductance along power supply return current paths (with the exception of the areas underneath the input and output pins as noted below).
4. A bulk decoupling capacitor is recommended (6.8 to 22 µF) within 1 inch, and a ceramic (0.1 µF) within 0.1 inch of the power input pins.

NOTE:

The bulk capacitor may be shared by other op amps.

BOARD LAYOUT

Achieving optimum performance with a high frequency amplifier like the THS4281 requires careful attention to board layout parasitics and external component types. See the EVM layout figures in the Design Tools Section.

Recommendations that optimize performance include:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability and on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
2. **Minimize the distance (< 0.1 inch) from the power supply pins to high frequency 0.1-µF decoupling capacitors.** Avoid narrow power and ground traces to minimize inductance. The power supply connections should always be decoupled as described above.
3. **Careful selection and placement of external components preserves the high frequency performance of the THS4281.** Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film, axial-lead resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire wound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Excessively high resistor values can create significant phase lag that can degrade performance. Keep resistor values as low as possible, consistent with load-driving considerations. It is suggested that a good starting point for design is to set the R_f to 2 kΩ for low-gain, noninverting applications. Doing this automatically keeps the resistor noise terms reasonable and minimizes the effect of parasitic capacitance.
4. **Connections to other wideband devices on the board should be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic capacitive loads (<4 pF) may not need an $R_{(ISO)}$, because the THS4281 is nominally compensated to operate at unity gain (+1 V/V) with a 2-pF capacitive load. Higher capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases. If a long trace is required, and the 6-dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A matching series resistor into the trace from the output of the THS4281 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of $R_{(ISO)}$ vs capacitive load. If the input impedance of the destination device is low, there is signal attenuation due to the voltage divider formed by $R_{(ISO)}$ into the terminating impedance.

A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots.

5. **Socketing a high speed part like the THS4281 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4281 onto the board.

THERMAL ANALYSIS

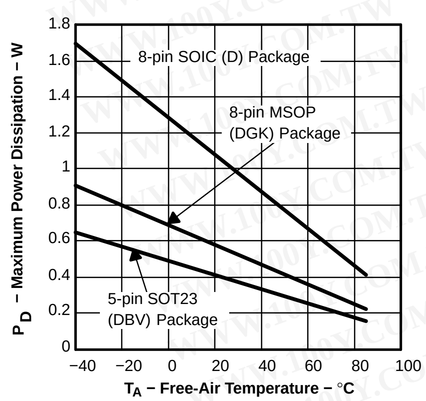
The THS4281 does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150° C is exceeded. For long-term dependability, the junction temperature should not exceed 125°C.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).



θ_{JA} = 97.5°C/W for 8-Pin SOIC (D)
θ_{JA} = 180.8°C/W for 8-Pin MSOP (DGK)
θ_{JA} = 255.4°C/W for 5-Pin SOT−23 (DBV)
T_J = 125°C, No Airflow

Figure 76. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS value can provide a reasonable analysis.

DESIGN TOOLS

Evaluation Fixtures and Application Support Information

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, an evaluation board has been developed for the THS4281 operational amplifier. The evaluation board is available and easy to use allowing for straight-forward evaluation of the device. These evaluation board can be obtained by ordering through the Texas Instruments Web site, www.ti.com, or through your local Texas Instruments Sales Representative. A schematic for the evaluation board is shown in Figure 77 with their default component values. Unpopulated footprints are shown to provide insight into design flexibility.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4281 device is available through either the Texas Instruments Web site (www.ti.com) or as one model on a disk from the Texas Instruments Product Information Center (1–800–548–6132). The PIC is also available for design assistance and detailed product information at this number. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

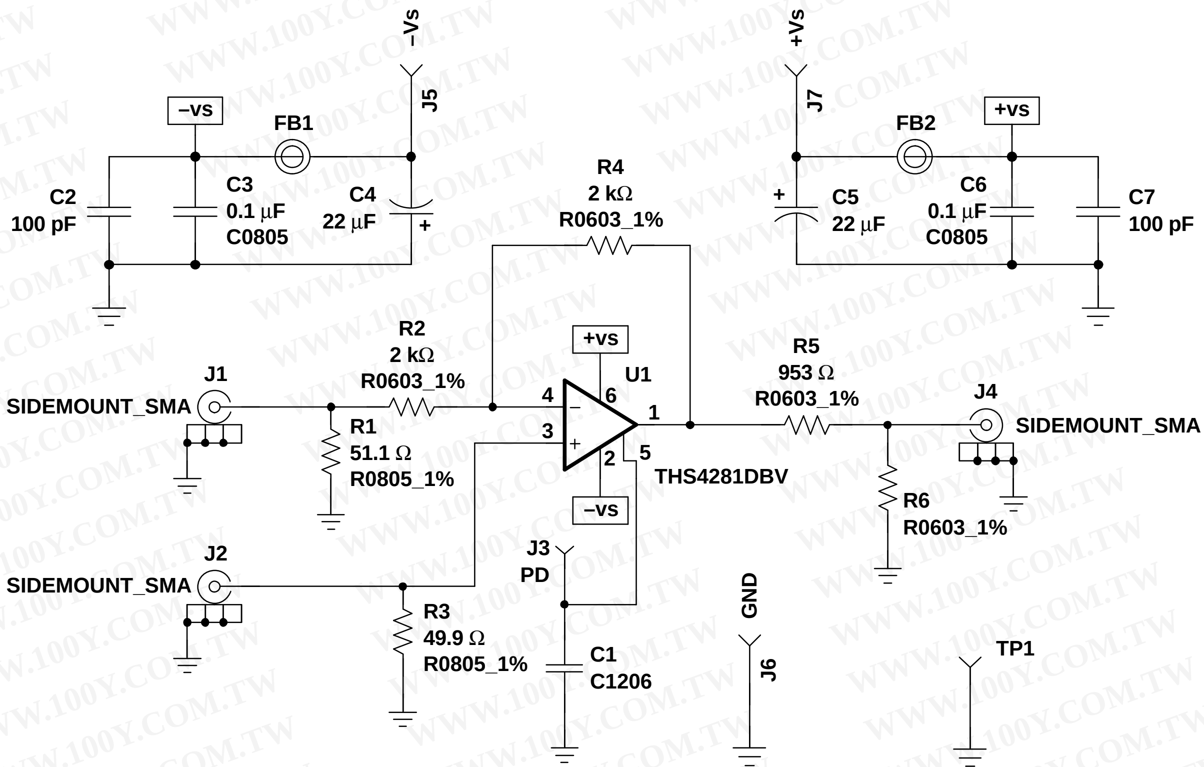
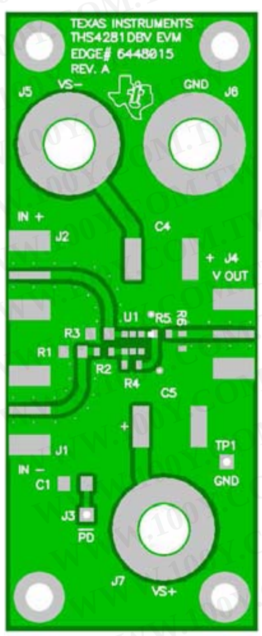
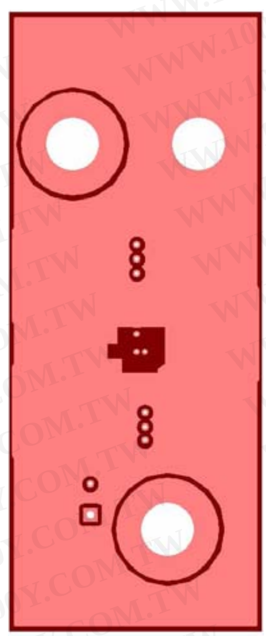


Figure 77. THS4281EVM Schematic



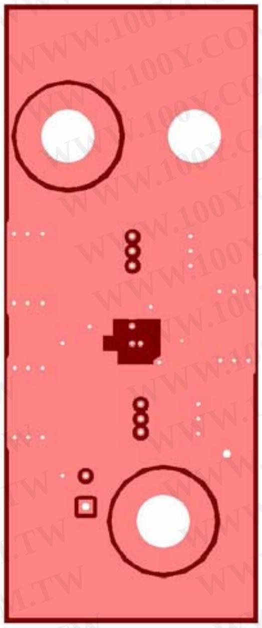
TOP

Figure 78. THS4281EVM Layout (Top Layer and Silkscreen Layer)



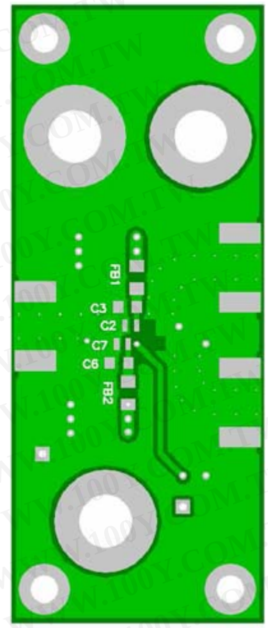
Layer 2 – GND

Figure 79. THS4281EVM Board Layout



Layer 3 − GND

Figure 80. THS4281EVM Board Layout



BOTTOM

Figure 81. THS4281EVM Board Layout

BILL OF MATERIALS

THS4281DBV EVM

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIG-NATOR	PCB QTY.	MANUFACTURER'S PART NUMBER(1)	DISTRIBUTOR'S PART NUMBER
1	Bead, Ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(STEWARD) HI1206N800R-00	(DIGI-KEY) 240-1010-1-ND
2	OPEN	1206	C1	1		
3	Cap, 22 µF, tanatalum, 25 V, 10%	D	C4, C5	2	(AVX) TAJD226K025R	(GARRETT) TAJD226K025R
4	Cap, 0.1 µF, ceramic, X7R, 50V	0805	C3, C6	2	(AVX) 08055C104KAT2A	(GARRETT) 08055C104KAT2A
5	Cap, 100 pF, ceramic, 5%, 150V	AQ12	C2, C7	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
6	OPEN	0603	R6	1		
7	Resistor, 2 KΩ, 1/10W, 1%	0603	R2, R4	2	(PHYCOMP) 9C06031A2001FKHFT	(GARRETT) 9C06031A2001FKHFT
8	Resistor, 953 Ω, 1/10W, 1%	0603	R5	1	(PHYCOMP) 9C06031A9530FKRFT	(GARRETT) 9C06031A9530FKRFT
9	Resistor, 51.1 Ω, 1/8W, 1%	0805	R1	1	(PHYCOMP) 9C08052A51R1FKHFT	(GARRETT) 9C08052A51R1FKHFT
10	Resistor, 49.9 Ω, 1/8W, 1%	0805	R3	1	(PHYCOMP) 9C08052A49R9FKHFT	(GARRETT) 9C08052A49R9FKHFT
11	Jack, banana receptance, 0.25" diameter hole		J5, J6, J7	3	(HH SMITH) 101	(NEWARK) 35F865
12	OPEN		J3	1		
13	Test point, black		TP1	1	(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
14	Connector, edge, SMA PCB JACK		J1, J2, J4	3	(JOHNSON) 142-0701-801	(NEWARK) 90F2624
15	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1804	(NEWARK) 89F1934
16	Screw, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN	
17	IC, THS4281		U1	1	(TI) THS4281DBV	
18	Board, printed circuit			1	(TI) EDGE # 6448015 Rev.A	

(1) The manufacturer's part numbers are used for test purposes only.

ADDITIONAL REFERENCE MATERIALS

- *PowerPAD Made Easy*, application brief, (SLMA004)
- *PowerPAD Thermally Enhanced Package*, technical brief (SLMA002)
- *Active Low-Pass Filter Design*, application report (SLOA049)
- *FilterPro MFB and Sallen-Key Low-Pass Filter Design Program*, application report (SBFA001)

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
THS4281D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS4281DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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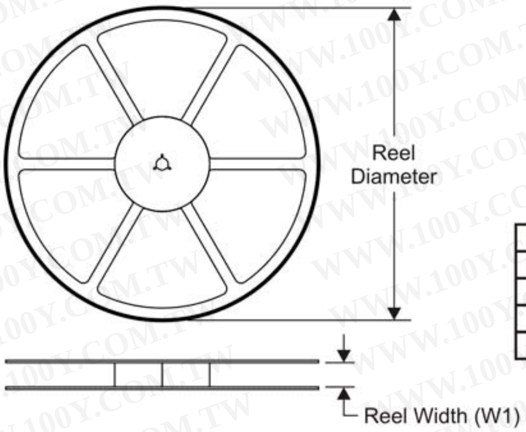
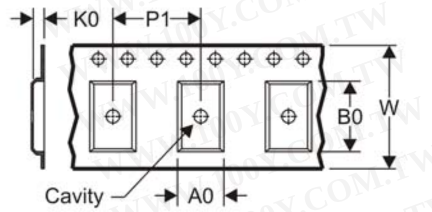
TAPE AND REEL INFORMATION

REEL DIMENSIONS

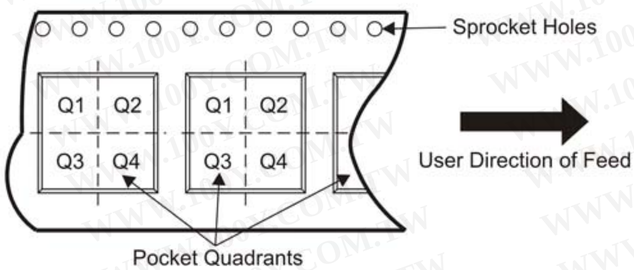


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

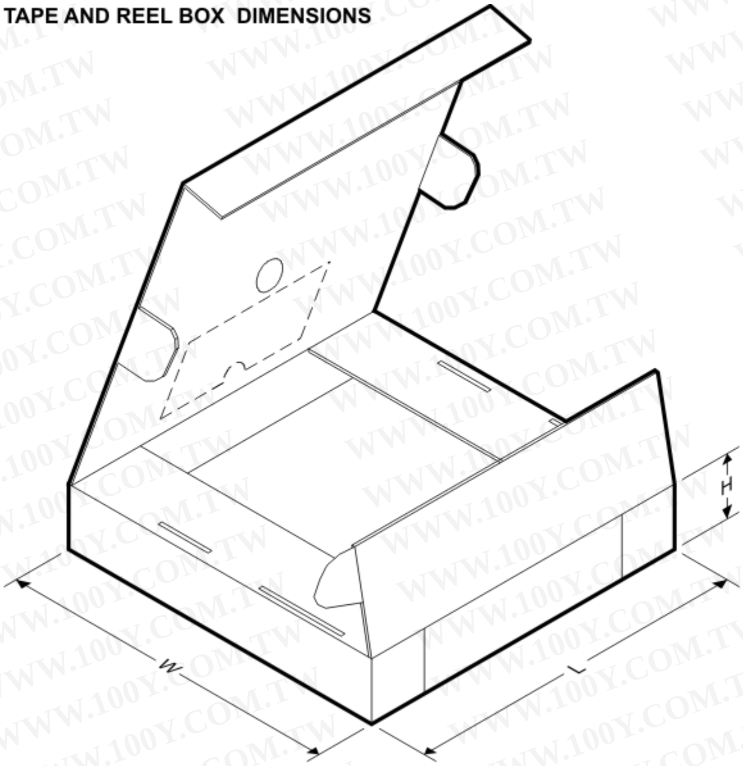
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4281DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4281DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4281DGKR	MSOP	DGK	8	2500	330.0	12.4	5.2	3.3	1.6	8.0	12.0	Q1
THS4281DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

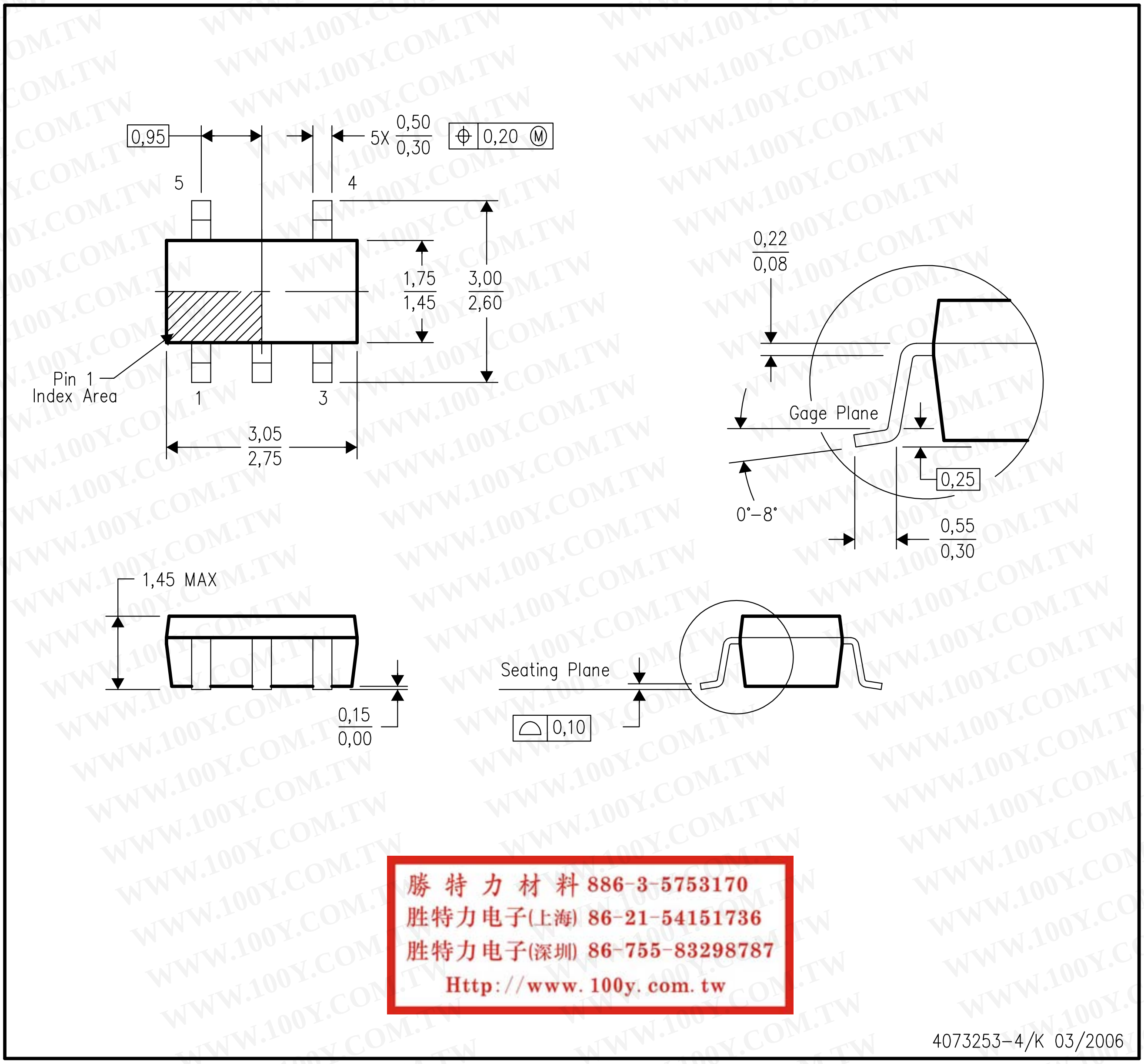
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

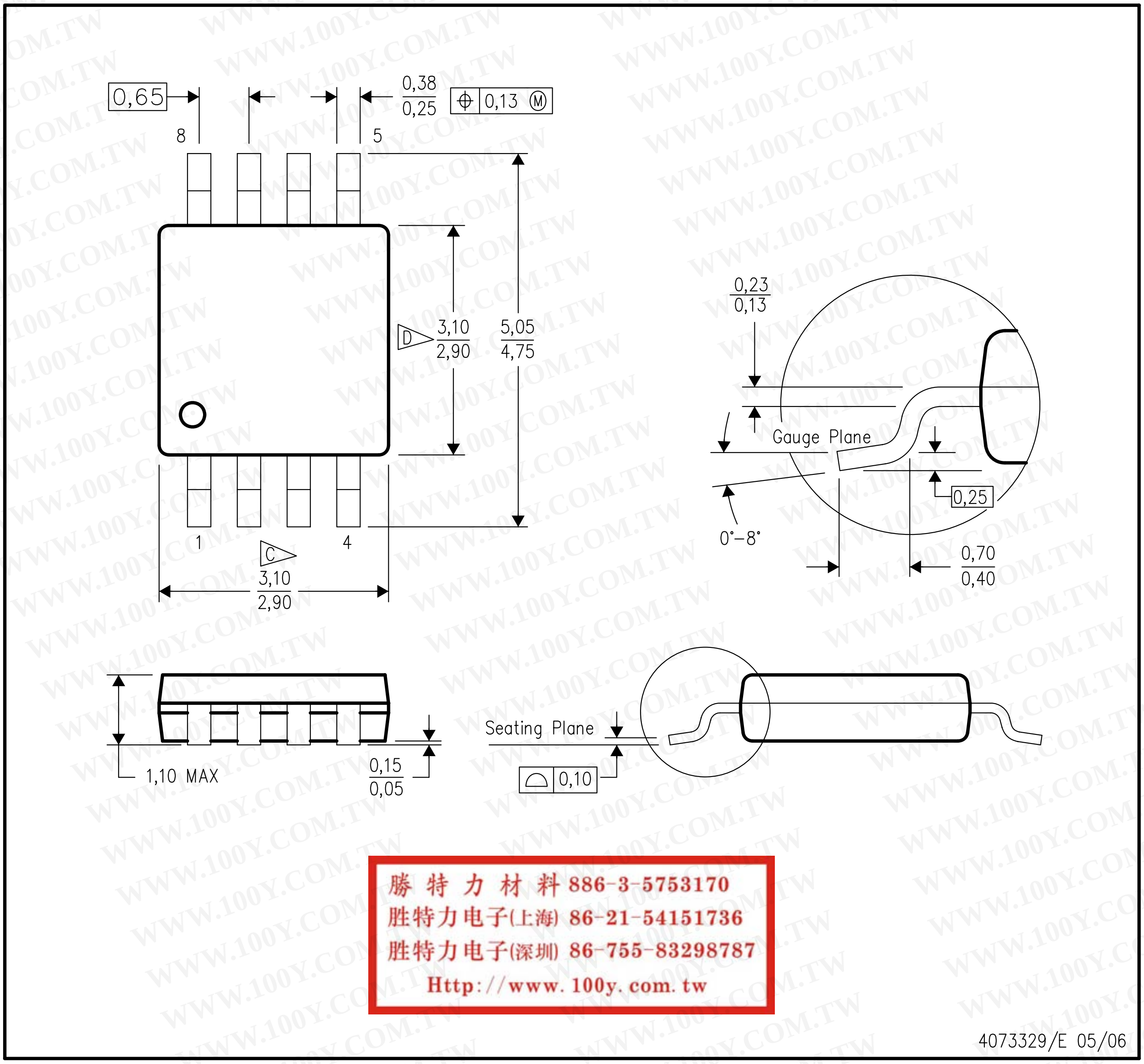
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4281DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
THS4281DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
THS4281DGKR	MSOP	DGK	8	2500	338.1	340.5	21.1
THS4281DR	SOIC	D	8	2500	346.0	346.0	29.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



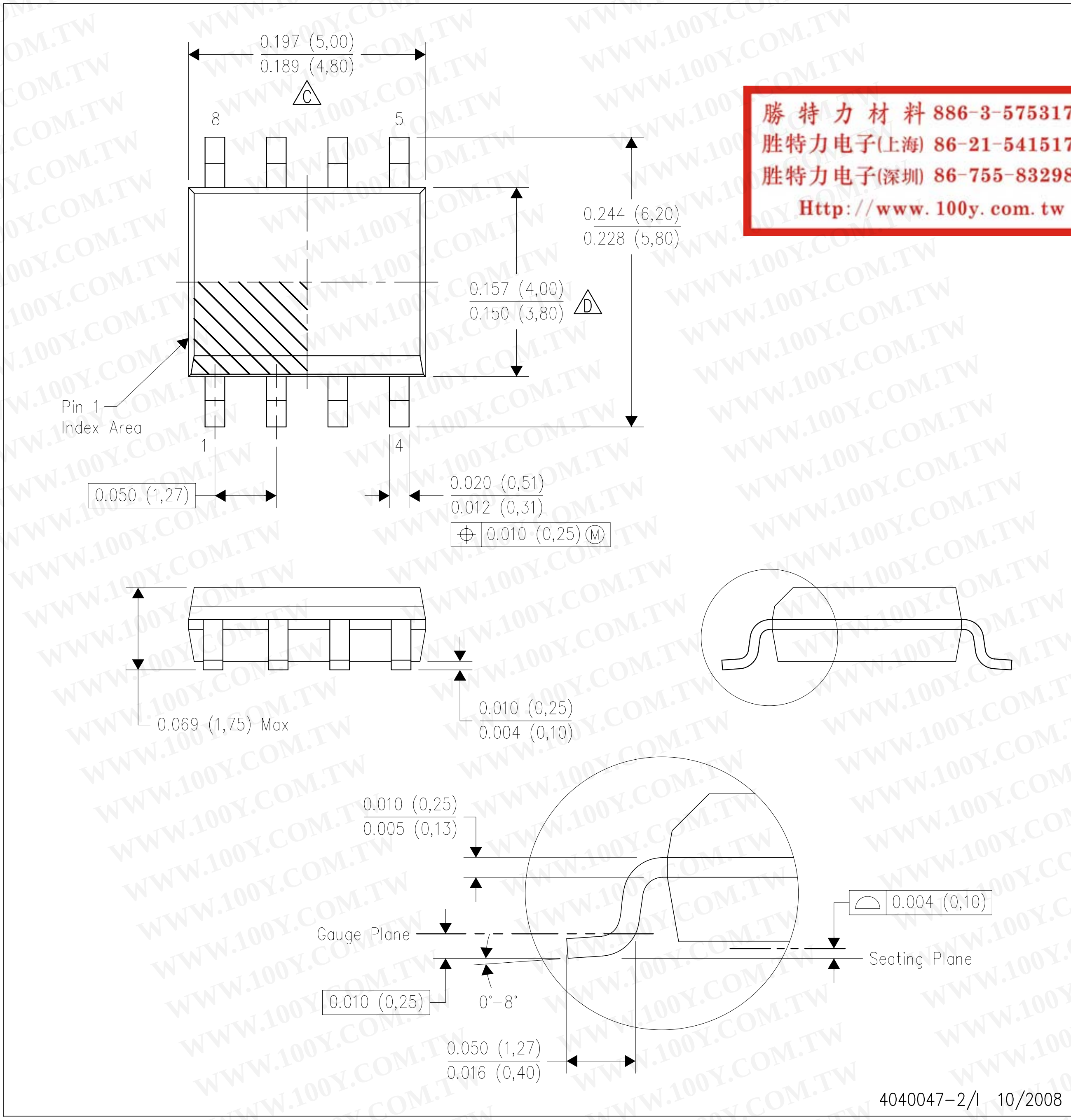
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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