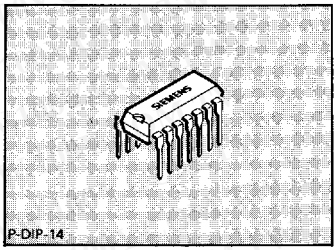
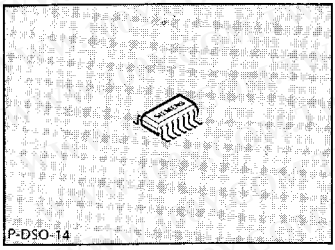
Preliminary Data **Bipolar IC**

Features

- Two window settings
  - direct setting of lower and upper edge voltage (window edges)
  - indirect setting by window center voltage and half window width
- Adjustable hysteresis
- Digital outputs with open collectors for currents up to 50 mA
- Adjustable reference voltage V_{Stab}





Type	Ordering Code	Package
▼ S TCA 965 A	Q67000-A8227	P-DIP-14
▼ S TCA 965 G	Q67000-A2368	P-DSO-14 (SMD)

▼ New type

The window discriminator compares an input voltage to a defined voltage window. The digital outputs show whether the input voltage is below, within or above this window.

The TCA 965 A window discriminator is especially suitable as a tracking or compensating controller with a dead band in control engineering and for the selection of DC voltages within a certain tolerance of the required setpoint value in measurement engineering. When it is used as a Schmitt trigger, switching frequencies up to a typical value of 200 kHz are possible.

Functional Description

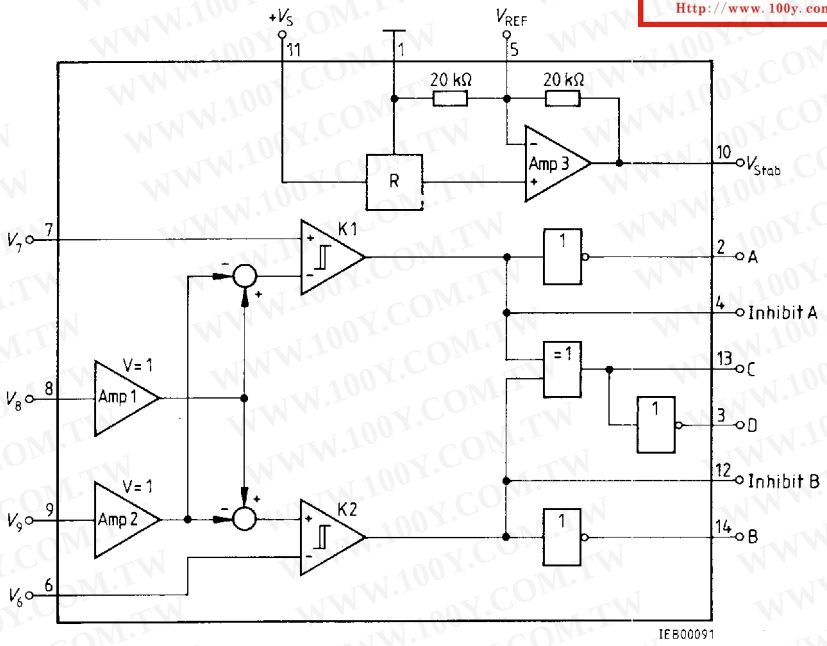
Amplifier Amp 3 increases the voltage of the reference source R to $V_{Stab} = 2 \times V_{REF}$. The amplification factor can be altered by external wiring. With direct setting of the window, the input voltage appears on amplifier Amp 1 (V_8), the upper edge voltage on comparator K2 (V_6) and the lower edge voltage on comparator K1 (V_7).

With indirect setting of the window, the input voltage appears on inputs V_6 and V_7, while the center voltage is connected to amplifier A1 (V_8).

The voltage applied to the input (V_9) of amplifier Amp 2 is subtracted symmetrically from the output voltage of amplifier Amp 1 and added. The comparators switch with hysteresis. The logic gates have open collectors.

If the inhibit input A or B is connected to ground, output A or B will always be high. If output A or B is not to be inhibited, the inhibit inputs can be connected to V_8 or left open-circuit. It is advisable to connect the inhibit inputs to V_8 for an improved signal-to-noise ratio.

Block Diagram

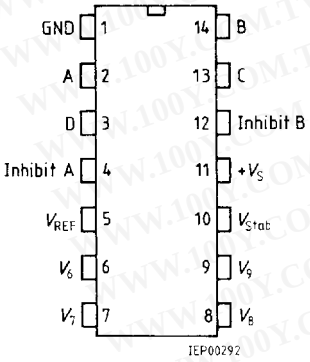


Outputs A, B, C, D are open-collector

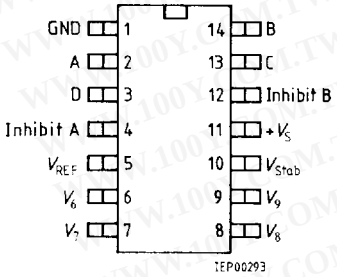
Pin Configuration

(top view)

P-DIP-14



P-DSO-14



Pin Definitions and Functions

Pin	Symbol	Pin Function in direct setting / of window	indirect setting
1	GND	GND	
2	A	Logic output A	
3	D	Logic output D = A ⊕ B EXNOR	
4	Inhibit A	Connected to GND: logic output A = HIGH	
5	V_{REF}	Internal V_{REF} = 3 V	
6	V_6	Upper edge voltage	Input voltage $V_{6/7}$
7	V_7	Lower edge voltage	Input voltage $V_{6/7}$
8	V_8	Input voltage	Center voltage
9	V_9	GND	Half window width
10	V_{Stab}	Internal V_{Stab} = 6 V	
11	$+V_S$	Supply voltage	
12	Inhibit B	Connected to GND: logic output B = HIGH	
13	C	Logic output C = A ⊕ B EXOR	
14	B	Logic output B	

Absolute Maximum Ratings

Maximum ratings for ambient temperature T_A –25 to 85 °C

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Supply voltage (pin 11)	V_S		30	V
Difference in input voltage between pins 6, 7, 8	V_I		15	V
Input voltage (pins 6, 7, 8, 9)	V_I		30	V
Output current (pins 2, 3, 13, 14)	I_Q		50	mA
Output voltage (pins 2, 3, 13, 14) independent of V_S	V_Q		30	V
Voltage on V_{REF} (pin 5)	V_R		8	V
Output current of stabilized voltage (pin 10)	I_{10}		10	mA
Inhibit input voltage (pins 4, 12)	V_{IH}		30	V
Junction temperature	T_J		150	°C
Storage temperature	T_{Stg}	–55	125	°C
Thermal resistance system-air P-DIP-14	$R_{th\ SA}$		80	K/W
P-DSO-14	$R_{th\ SA}$		125	K/W

Operating Range

Supply voltage	V_S	4.5	30	V
Ambient temperature	T_A	–25	85	°C

Electrical Characteristics

$V_S = 10$ V; $T_A = 25$ °C

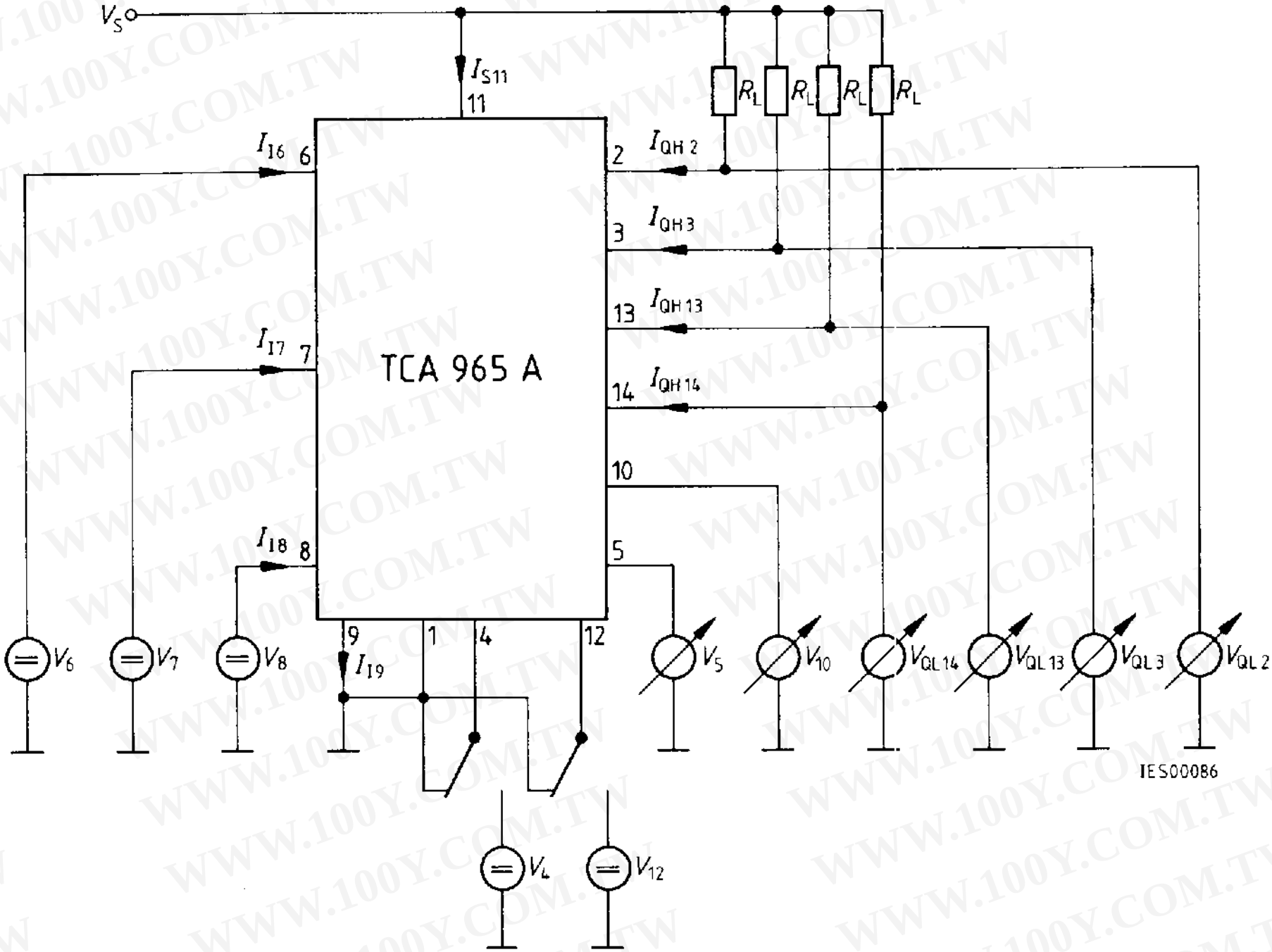
Parameter	Symbol	Limit Values			Unit	Test Conditions	Test Circuit
		min.	typ.	max.			
Current consumption	I_S		5	7	mA	V_2, $V_{13} = V_{QH}$	1
Input current (pins 6, 7, 8)	I_I		20	50	nA		1
Input current, pin 9	$-I_I$		400	3000	nA		1
Input offset voltage in direct setting of window	V_{IO}	−20		20	mV		1
Input offset voltage in indirect setting of window	V_{IO}	−50		50	mV		2
Input-voltage range on pins 6,7,8	V_I	1.5		V_S-1	V	$\Delta V_I < 13$ V	1
Input-voltage range on pin 9	V_I	50		$V_S/2$	mV		2
Differential input voltage	$V_6-(V_8-V_9)$			13	V		
	$(V_8+V_9)-V_7$			13	V		
Reference voltage[1]	V_5	2.8	3	3.2	V	$I_{ref} = 0$	
Stabilized voltage on pin 10[2]	V_{10}	5.5	6	6.5	V	$V_s > 7.9$ V	
TC of reference voltage	αV_5		0.3		mV/K		
Sensitivity of reference voltage to supply-voltage variation	$\Delta V_5/\Delta V_S$		2		mV/V		
Output reverse current	I_{QH}			10	µA		
Output saturation voltage	V_{QL}		100	200	mV	$I_Q = 10$ mA	1
			500	800	mV	$I_Q = 50$ mA	
Hysteresis of window edges	V_U-V_L	18	22	35	mV		
Inhibit threshold	$V_{4,12}$	1		1.8	V		
Inhibit current	$I_{4,12}$		−100		µA		
Switching frequency	f_{dir}	50	80		kHz		1
	f_{ind}	150	200		kHz		2

[1] Range aimed at is 2.85 to 3.15 V

[2] Range aimed at is 5.6 to 6.4 V

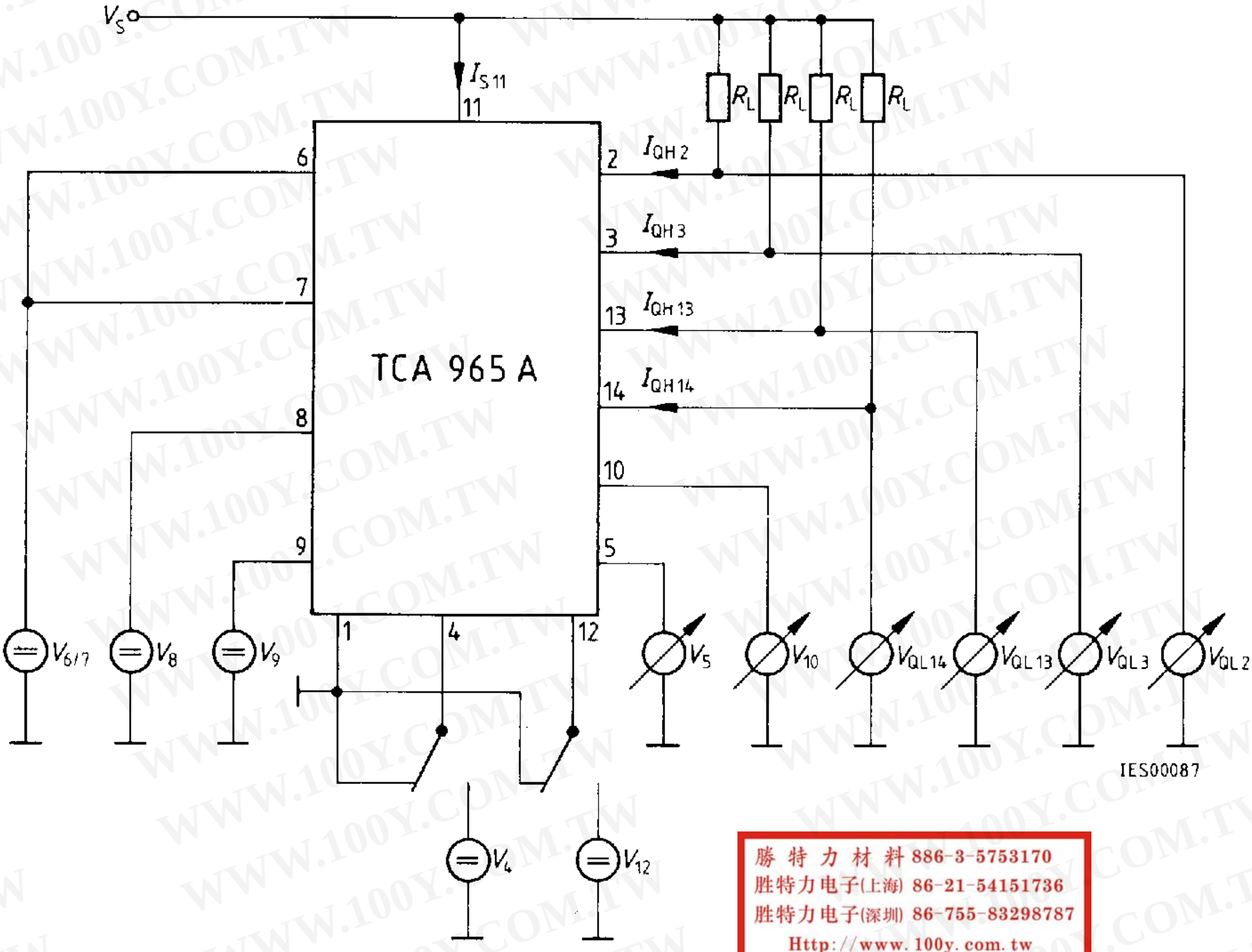
Test Circuit 1

Direct Setting of Window

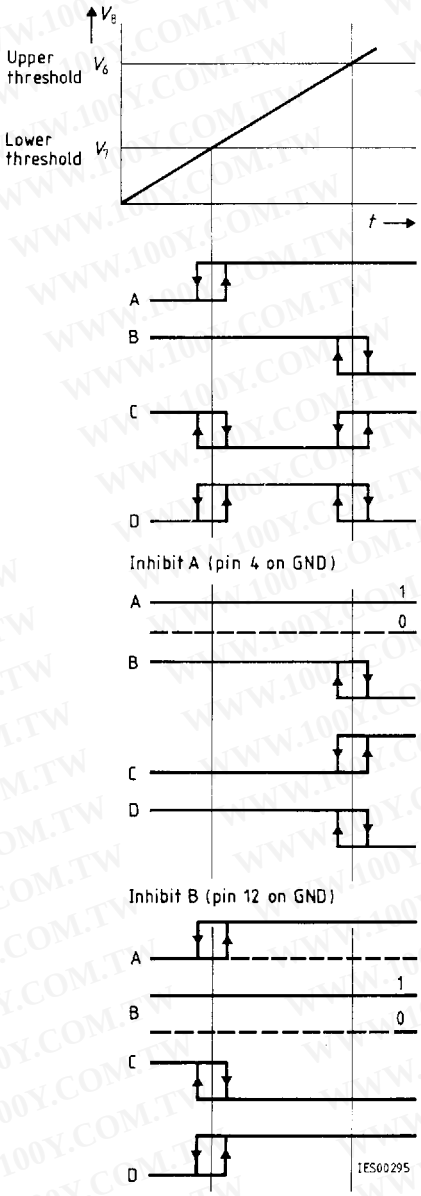


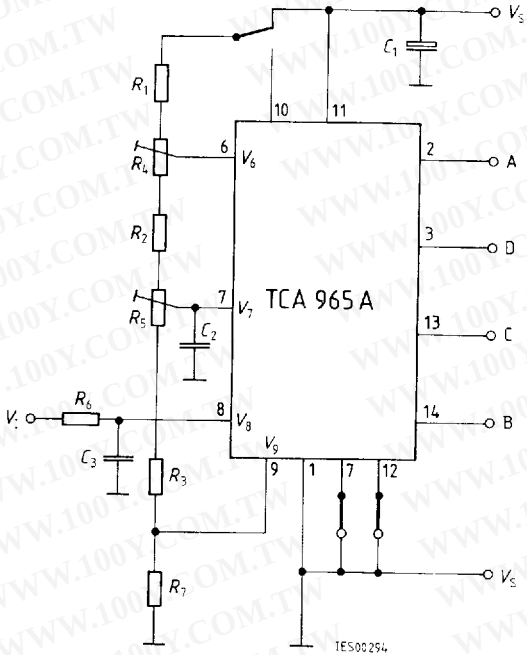
Test Circuit 2

Indirect Setting of Window by Center Voltage and Half Window Width



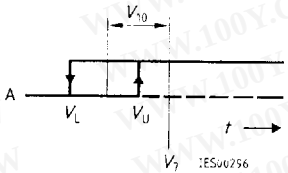
Application Circuit 1: Direct Setting of Window Assignment of Logic Outputs A, B, C, D





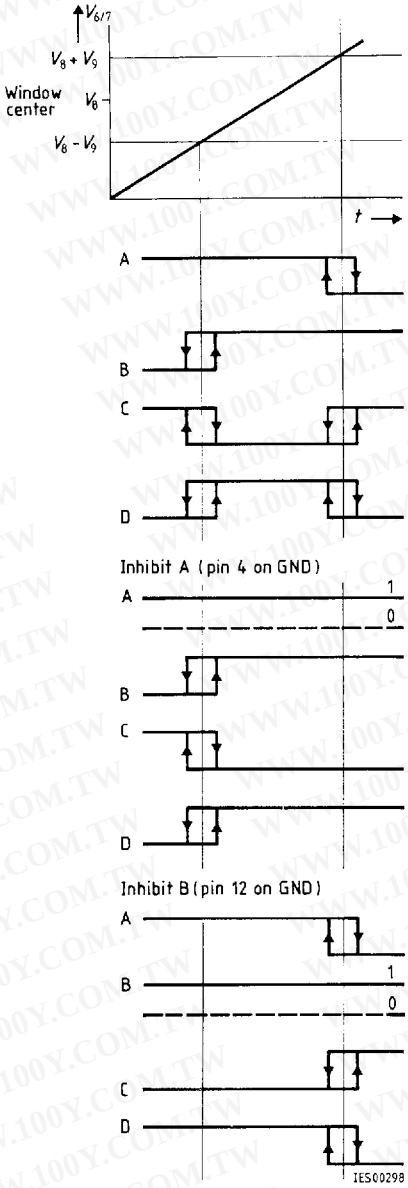
To increase switching frequency, pin 9 is grounded via R_7 (V_S approx. 10 mV) and not directly

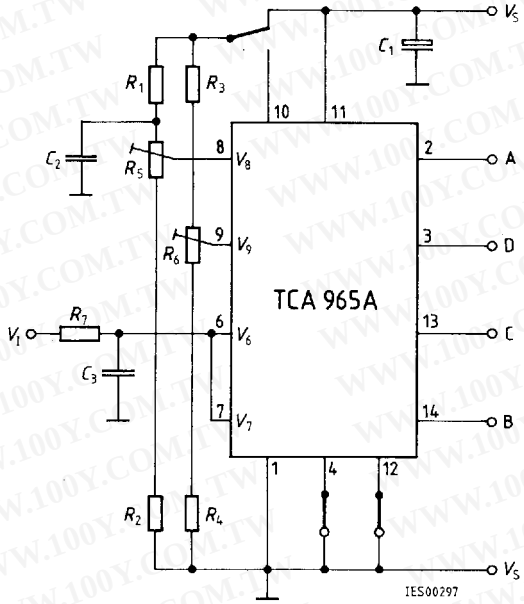
$V_6 - V_9$ = Upper edge voltage
$V_7 + V_9$ = Lower edge voltage
V_8 = Input voltage



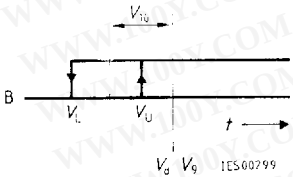
$$V_{10} = \frac{V_L + V_U}{2} - V_7$$

Application Circuit 2: Indirect Setting of Window by Center Voltage and Half-Window Width V
Assignment of Logic Outputs A, B, C, D





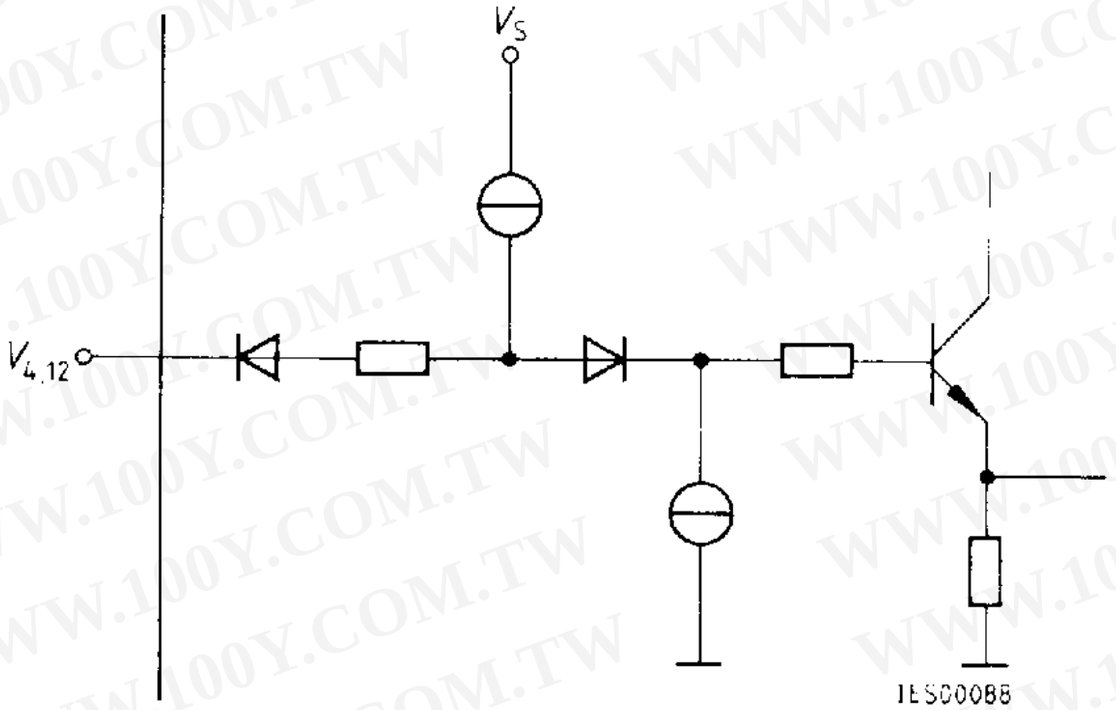
V_6 = V_7 = Input voltage
V_8 = Center voltage
V_9 = Half window width



$$V_{10} = \frac{V_L + V_U}{2} - (V_8 - V_9)$$

Schematic Circuit Diagram

Inhibit-Inputs 4, 12



TCA 965 A

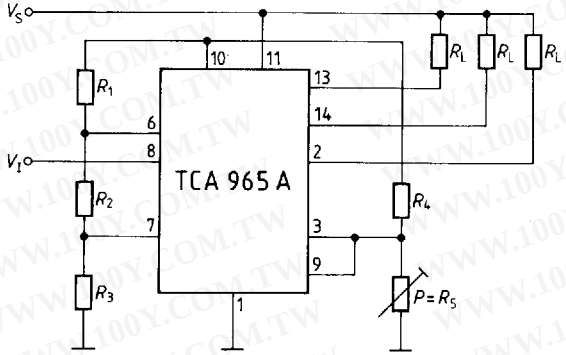
$V_{4,12}$	Output A, B
GND	HIGH
V_S	Normal funct.
Open	Normal funct.

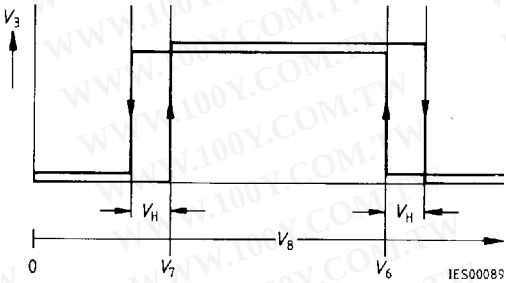
TCA 965 for comparison

$V_{4,12}$	Output A, B
GND	HIGH
V_S	Impermissible
Open	Normal funct.
< 6 V	Low

Application Circuit 3

Symmetrically enlarged edge hysteresis in direct setting of window





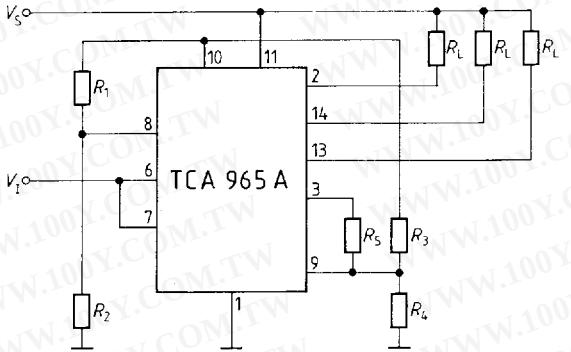
Calculation of hysteresis V_H

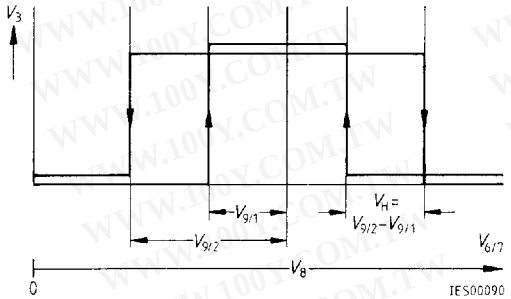
$$V_H = V_{10} \frac{R_5}{R_4 + R_5}$$

$$\frac{V_{10}}{R_4 + R_5} + \frac{V_{10}}{R_1 + R_2 + R_3} \leq 10 \text{ mA}$$

Application Circuit 4

Symmetrically enlarged edge hysteresis in indirect setting of window





Calculation of hysteresis V_H

$$V_H = V_{9/2} - V_{9/1}$$

$$V_{9/1} = V_{10} \frac{R_4 \parallel R_5}{R_3 + R_4 \parallel R_5}$$

$$V_{9/2} = V_{10} \frac{R_4}{R_3 + R_4}$$