National Semiconductor

April 2007

LMH6321
300 mA High Speed Buffer with Adjustable Current Limit

General Description

The LMH6321 is a high speed unity gain buffer that slews at 1800 V/µs and has a small signal bandwidth of 110 MHz while driving a 50Ω load. It can drive ±300 mA continuously and will not oscillate while driving large capacitive loads.

The LMH6321 features an adjustable current limit. The current limit is continuously adjustable from 10 mA to 300 ma with a ±5 mA ±5% accuracy. The current limit is set by adjusting an external reference current with a resistor. The current can be easily and instantly adjusted, as needed by connecting the resistor to a DAC to form the reference current. The sourcing and sinking currents share the same current limit.

The LMH6321 is available in a space saving 8-pin PSOP or a 7-pin TO-263 power package. The PSOP package features an exposed pad on the bottom of the package to increase its heat sinking capability. The LMH6321 can be used within the feedback loop of an operational amplifier to boost the current output or as a stand alone buffer.

Features

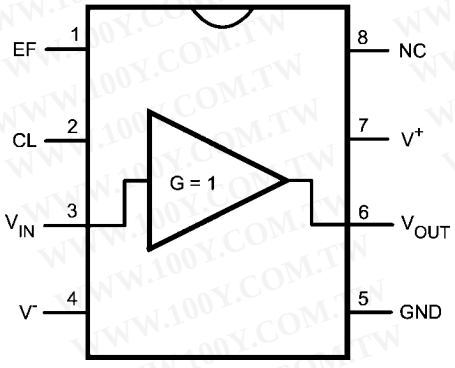
- High slew rate — 1800 V/µs
- Wide bandwidth — 110 MHz
- Continuous output current — ±300 mA
- Output current limit tolerance — ±5 mA ±5%
- Wide supply voltage range — 5V to ±15V
- Wide temperature range — −40°C to +125°C
- Adjustable current limit
- High capacitive load drive
- Thermal shutdown error flag

Applications

- Line driver
- Pin driver
- Sonar driver
- Motor control

Connection Diagrams

8-Pin PSOP



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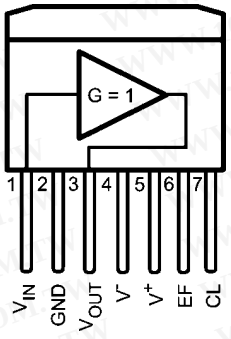
7-Pin TO-263



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Note: V− pin is connected to tab on back of each package

勝 特 力 材 料 886-3-5753170
胜特力电子(上海) 86-21-34970699
胜特力电子(深圳) 86-755-83298787
Http://www.100y.com.tw

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2.5 kV
Machine Model	250V
Supply Voltage	36V (±18V)
Input to Output Voltage (Note 3)	±5V
Input Voltage	$\pm V_{SUPPLY}$
Output Short-Circuit to GND (Note 4)	Continuous
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_{JMAX})	+150°C
Lead Temperature	
(Soldering, 10 seconds)	260°C
Power Dissipation	(Note 8)
C_L Pin to GND Voltage	±1.2V

Operating Ratings

Operating Temperature Range	−40°C to +125°C
Operating Supply Range	5V to ±16V
Thermal Resistance (θ_{JA}),	
PSOP Package (Note 6)	180°C/W
Thermal Resistance (θ_{JC})	
TO-263 Package	4°C/W
Thermal Resistance (θ_{JA})	
TO-263 Package	80°C/W

±15V Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq$ 100 kΩ and R_S = 50Ω, C_L open, unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A_V	Voltage Gain	R_L = 1 kΩ, V_{IN} = ±10V		0.99 **0.98**	0.995		V/V
		R_L = 50Ω, V_{IN} = ±10V		0.86 **0.84**	0.92		V/V
V_{OS}	Input Offset Voltage	R_L = 1 kΩ, R_S = 0V			±4	±35 **±52**	mV
I_B	Input Bias Current	V_{IN} = 0V, R_L = 1 kΩ, R_S = 0V			±2	±15 **±17**	µA
R_{IN}	Input Resistance	R_L = 50Ω			250		kΩ
C_{IN}	Input Capacitance				3.5		pF
R_O	Output Resistance	I_O = ±10 mA			5		Ω
I_S	Power Supply Current	R_L = ∞, V_{IN} = 0			11	14.5 **16.5**	mA
			750 µA into C_L Pin		14.9	18.5 **20.5**	
V_O1	Positive Output Swing	I_O = 300 mA, R_S = 0V, $V_{IN} = \pm V_S$		11.2 **10.8**	11.9		V
	Negative Output Swing	I_O = 300 mA, R_S = 0V, $V_{IN} = \pm V_S$			−11.3	−10.3 **−9.8**	
V_O2	Positive Output Swing	R_L = 1 kΩ, R_S = 0V, $V_{IN} = \pm V_S$		13.1 **12.9**	13.4		V
	Negative Output Swing	R_L = 1 kΩ, R_S = 0V, $V_{IN} = \pm V_S$			−13.4	−12.9 **−12.6**	
V_O3	Positive Output Swing	R_L = 50Ω, R_S = 0V, $V_{IN} = \pm V_S$		11.6 **11.2**	12.2		V
	Negative Output Swing	R_L = 50Ω, R_S = 0V, $V_{IN} = \pm V_S$			−11.9	−10.9 **−10.6**	
V_{EF}	Error Flag Output Voltage	R_L = ∞, V_{IN} = 0, EF pulled up with 5 kΩ to +5V	Normal		5.00		V
			During Thermal Shutdown		0.25		
T_{SH}	Thermal Shutdown Temperature	Measure Quantity is Die (Junction) Temperature			168		°C
		Hysteresis			10		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{SH}	Supply Current at Thermal Shutdown	EF pulled up with 5 kΩ to +5V			3		mA
PSSR	Power Supply Rejection Ratio	R_L = 1 kΩ, V_{IN} = 0V, V_S = ±5V to ±15V	Positive	58 **54**	66		dB
			Negative	58 **54**	64		
SR	Slew Rate	V_{IN} = ±11V, R_L = 1 kΩ			2900		V/µs
		V_{IN} = ±11V, R_L = 50Ω			1800		
BW	−3 dB Bandwidth	V_{IN} = ±20 mV_{PP}, R_L = 50Ω			110		MHz
LSBW	Large Signal Bandwidth	V_{IN} = 2 V_{PP}, R_L = 50Ω			48		MHz
HD2	2nd Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz	R_L = 50Ω		−59		dBc
			R_L = 100Ω		−70		
		V_O = 2 V_{PP}, f = 1 MHz	R_L = 50Ω		−57		
			R_L = 100Ω		−68		
HD3	3rd Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz	R_L = 50Ω		−59		dBc
			R_L = 100Ω		−70		
		V_O = 2 V_{PP}, f = 1 MHz	R_L = 50Ω		−62		
			R_L = 100Ω		−73		
e_n	Input Voltage Noise	f ≥ 10 kHz			2.8		$nV/\sqrt{Hz}$
i_n	Input Current Noise	f ≥ 10 kHz			2.4		$pA/\sqrt{Hz}$
$I_{SC}1$	Output Short Circuit Current Source (Note 7)	V_O = 0V, Program Current into C_L = 25 µA	Sourcing V_{IN} = +3V	4.5 **4.5**	10	15.5 **15.5**	mA
			Sinking V_{IN} = −3V	4.5 **4.5**	10	15.5 **15.5**	
		V_O = 0V Program Current into C_L = 750 µA	Sourcing V_{IN} = +3V	280 **273**	295	308 **325**	mA
			Sinking V_{IN} = −3V	280 **275**	295	310 **325**	
$I_{SC}2$	Output Short Circuit Current Source	R_S = 0V, V_{IN} = +3V (Notes 5, 7)		320 **300**	570	750 **920**	mA
	Output Short Circuit Current Sink	R_S = 0V, V_{IN} = −3V (Notes 5, 7)		300 **305**	515	750 **910**	
V/I Section							
CLV_{OS}	Current Limit Input Offset Voltage	R_L = 1 kΩ, GND = 0V			±0.5	±4.0 **±8.0**	mV
CLI_B	Current Limit Input Bias Current	R_L = 1 kΩ		−0.5 **−0.8**	−0.2		µA
CL CMRR	Current Limit Common Mode Rejection Ratio	R_L = 1 kΩ, GND = −13 to +14V		60 **56**	69		dB

±5V Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$, C_L Open, unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A_V	Voltage Gain	R_L = 1 kΩ, V_{IN} = ±3V		0.99 **0.98**	0.994		V/V
		R_L = 50Ω, V_{IN} = ±3V		0.86 **0.84**	0.92		
V_{OS}	Offset Voltage	R_L = 1 kΩ, R_S = 0V			±2.5	±35 **±50**	mV
I_B	Input Bias Current	V_{IN} = 0V, R_L = 1 kΩ, R_S = 0V			±2	±15 **±17**	µA
R_{IN}	Input Resistance	R_L = 50Ω			250		kΩ
C_{IN}	Input Capacitance				3.5		pF
R_O	Output Resistance	I_{OUT} = ±10 mA			5		Ω
I_S	Power Supply Current	$R_L = \infty$, V_{IN} = 0V			10	13.5 **14.7**	
			750 µA into CL Pin		14	17.5 **19.5**	
V_O1	Positive Output Swing	I_O = 300 mA, R_S = 0V, $V_{IN} = \pm V_S$		1.3 **0.9**	1.9		V
	Negative Output Swing	I_O = 300 mA, R_S = 0V, $V_{IN} = \pm V_S$			−1.3	−0.5 **−0.1**	
V_O2	Positive Output Swing	R_L = 1 kΩ, R_S = 0V, $V_{IN} = \pm V_S$		3.2 **2.9**	3.5		V
	Negative Output Swing	R_L = 1 kΩ, R_S = 0V, $V_{IN} = \pm V_S$			−3.5	−3.1 **−2.9**	V
V_O3	Positive Output Swing	R_L = 50Ω, R_S = 0V, $V_{IN} = \pm V_S$		2.8 **2.5**	3.1		V
	Negative Output Swing	R_L = 50Ω, R_S = 0V, $V_{IN} = \pm V_S$			−3.0	−2.6 **−2.4**	V
PSSR	Power Supply Rejection Ratio	R_L = 1 kΩ, V_{IN} = 0, V_S = ±5V to ±15V	Positive	58 **54**	66		dB
			Negative	58 **54**	64		
$I_{SC}1$	Output Short Circuit Current	V_O = 0V, Program Current into C_L = 25 µA	Sourcing V_{IN} = +3V	4.5 **4.5**	9	14.0 **15.5**	mA
			Sinking V_{IN} = −3V	4.5 **4.5**	9	14.0 **15.5**	
		V_O = 0V, Program Current into C_L = 750 µA	Sourcing V_{IN} = +3V	275 **270**	290	305 **320**	
			Sinking V_{IN} = −3V	275 **270**	290	310 **320**	
$I_{SC}2$	Output Short Circuit Current Source	R_S = 0V, V_{IN} = +3V (Notes 5, 7)		300	470		mA
	Output Short Circuit Current Sink	R_S = 0V, V_{IN} = −3V (Notes 5, 7)		300	400		
SR	Slew Rate	V_{IN} = ±2 V_{PP}, R_L = 1 kΩ			450		V/µs
		V_{IN} = ±2 V_{PP}, R_L = 50Ω			210		
BW	−3 dB Bandwidth	V_{IN} = ±20 mV_{PP}, R_L = 50Ω			90		MHz
LSBW	Large Signal Bandwidth	V_{IN} = 2 V_{PP}, R_L = 50Ω			39		MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SD}	Thermal Shutdown	Temperature		170		°C
		Hysteresis		10		
V/I Section						
CLV_{OS}	Current Limit Input Offset Voltage	R_L = 1 kΩ, GND = 0V		2.7	+5 **±5.0**	mV
CLI_B	Current Limit Input Bias Current	R_L = 1 kΩ, C_L = 0V	−0.5 **−0.6**	−0.2		µA
CL CMRR	Current Limit Common Mode Rejection Ratio	R_L = 1 kΩ, GND = −3V to +4V	60 **56**	65		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Table.

Note 2: Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.

Note 3: If the input-output voltage differential exceeds ±5V, internal clamping diodes will turn on. The current through these diodes should be limited to 5 mA max. Thus for an input voltage of ±15V and the output shorted to ground, a minimum of 2 kΩ should be placed in series with the input.

Note 4: The maximum continuous current must be limited to 300 mA. See the Application section for more details.

Note 5: For the condition where the C_L pin is left open the output current should not be continuous, but instead, should be limited to low duty cycle pulse mode such that the RMS output current is less than or equal to 300 mA.

Note 6: Soldered to PC board with copper foot print equal to DAP size. Natural convection (no air flow). Board material is FR-4.

Note 7: V_{IN} = + or −4V at T_J = −40°C.

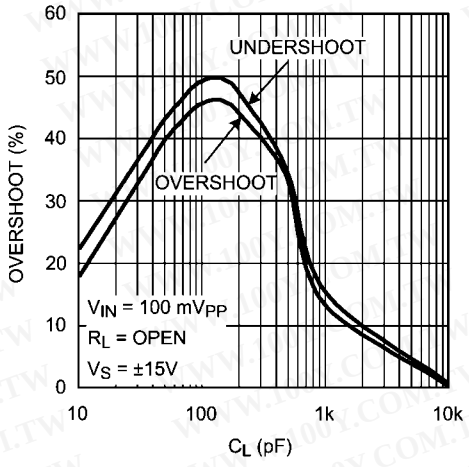
Note 8: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = T_{J(MAX)}-T_A)/\theta_{JA}$. See Thermal Management section of the Application Hints.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin PSOP	LMH6321MR	LMH6321MR	95 Units/Rail	MRA08A
	LMH6321MRX		2.5k Units Tape and Reel	
7-Pin TO-263	LMH6321TS	LMH6321TS	45 Units/Rail	TS7B
	LMH6321TSX		500 Units Tape and Reel	

Typical Performance Characteristics

Overshoot vs. Capacitive Load



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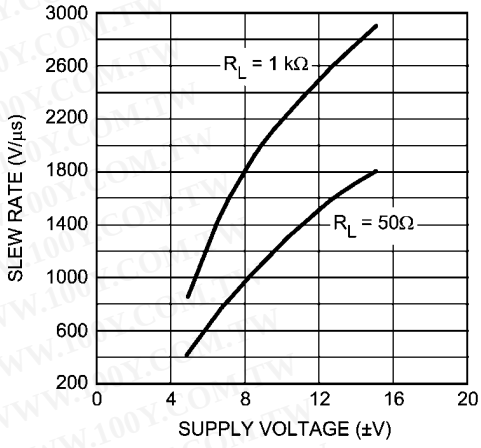
Slew Rate



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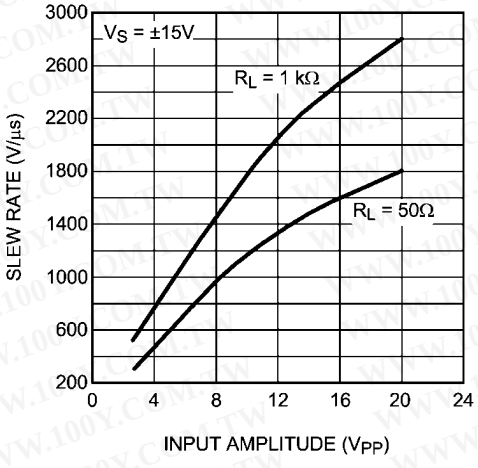
Slew Rate



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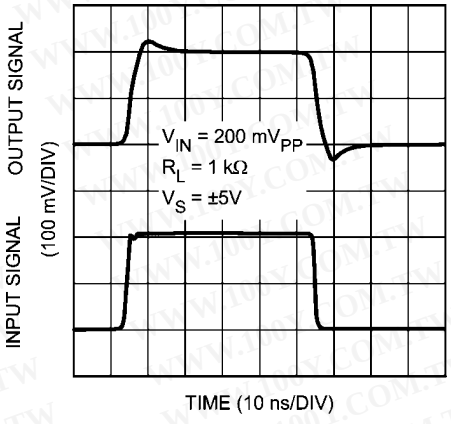
Small Signal Step Response



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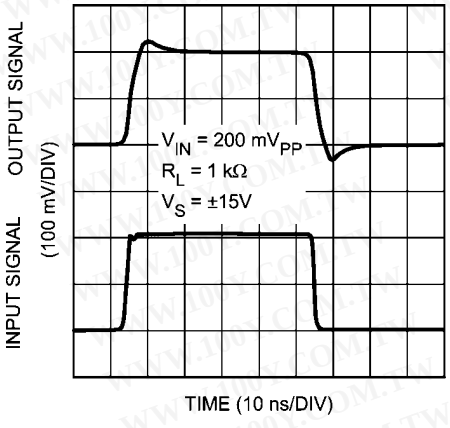
Small Signal Step Response



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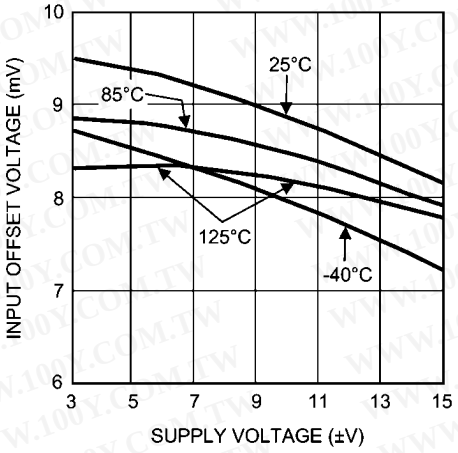
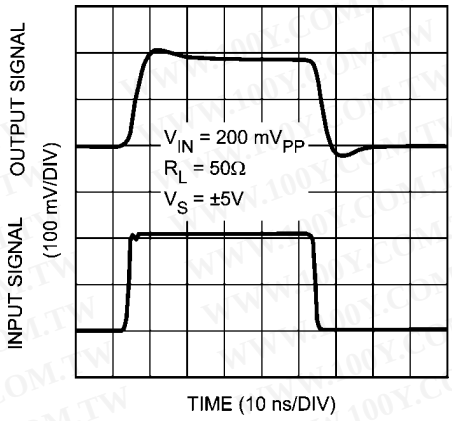
Input Offset Voltage of Amplifier vs. Supply Voltage



20138660

Small Signal Step Response



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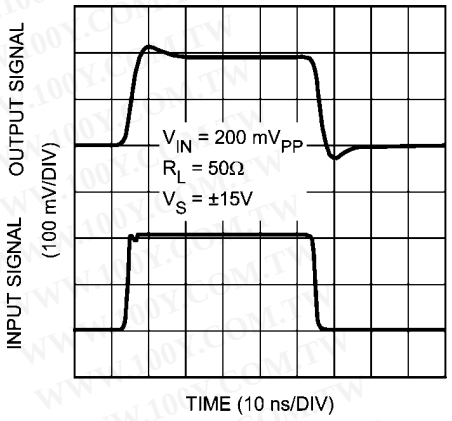
Small Signal Step Response



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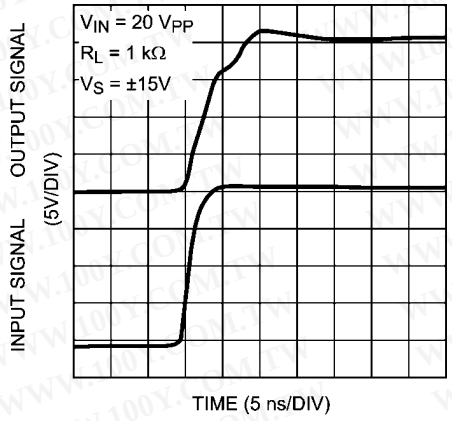
Large Signal Step Response—Leading Edge



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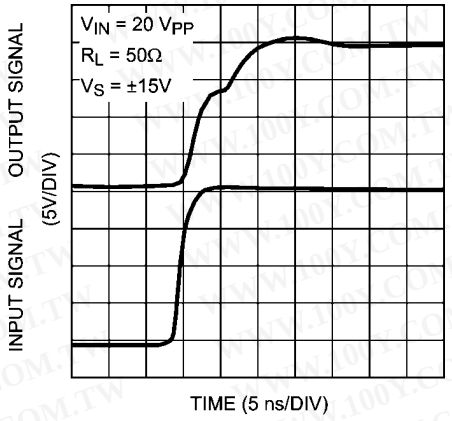
Large Signal Step Response—Leading Edge



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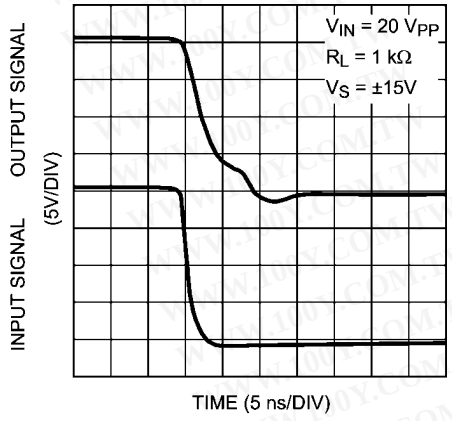
Large Signal Step Response — Trailing Edge



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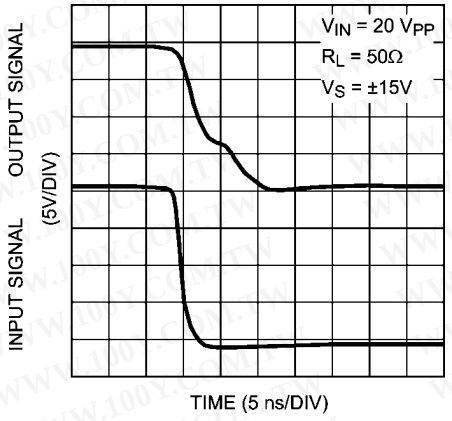
Large Signal Step Response — Trailing Edge



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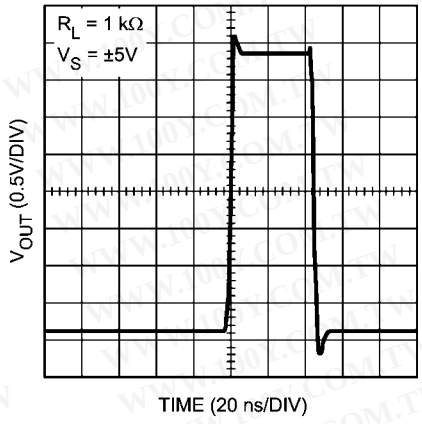
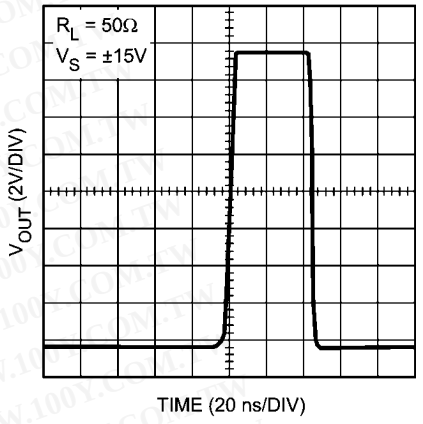
Large Signal Step Response



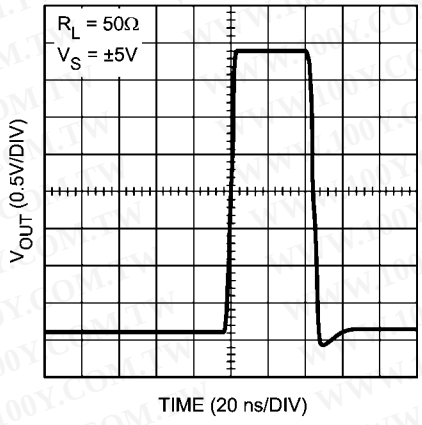
20138648

Large Signal Step Response



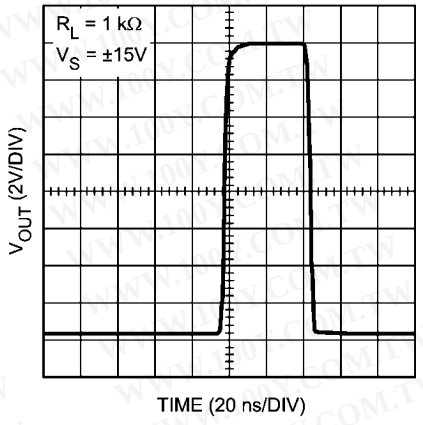
20138647

Large Signal Step Response



20138649

Large Signal Step Response



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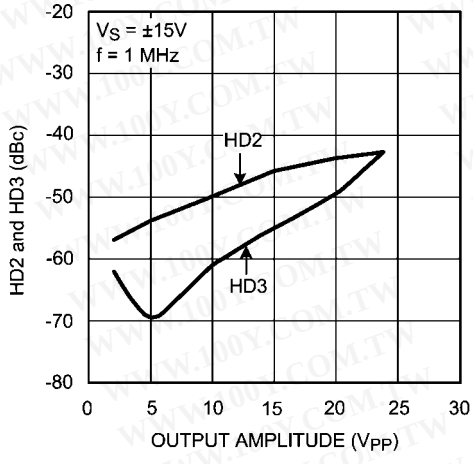
Harmonic Distortion with 50Ω Load



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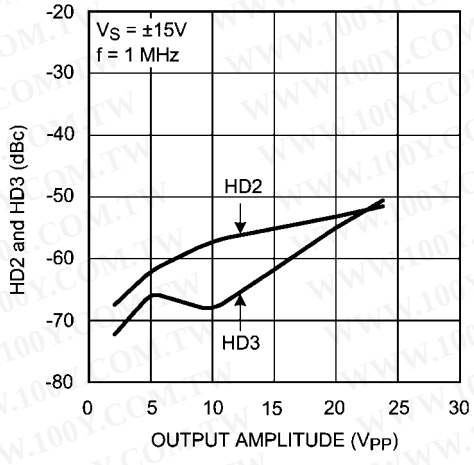
Harmonic Distortion with 100Ω Load



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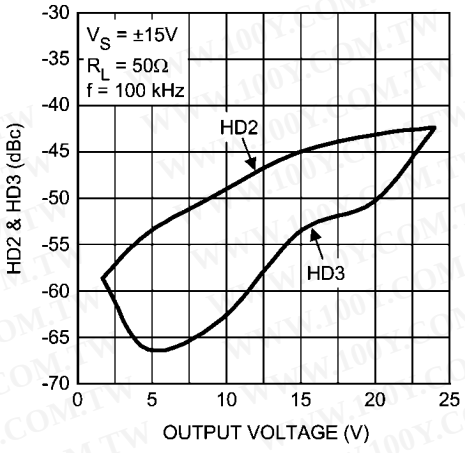
Harmonic Distortion with 50Ω Load



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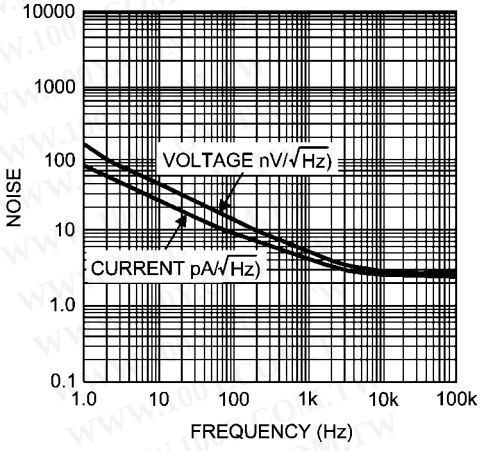
Noise vs. Frequency



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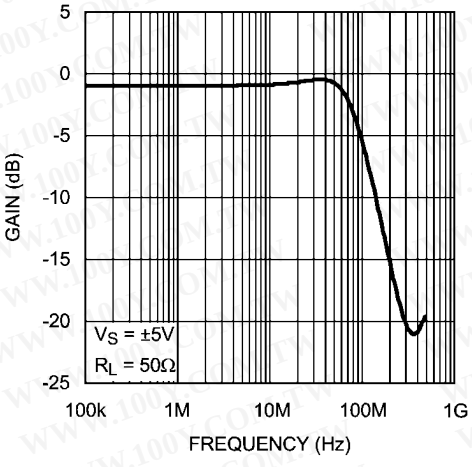
Gain vs. Frequency



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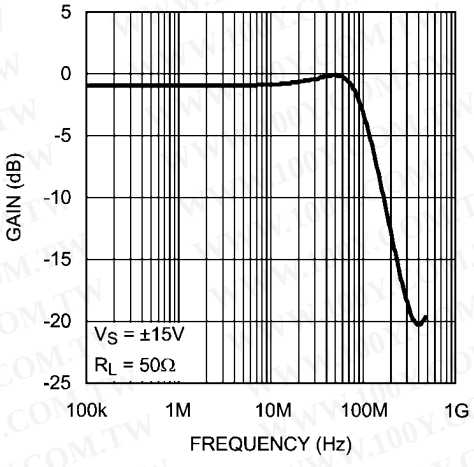
Gain vs. Frequency



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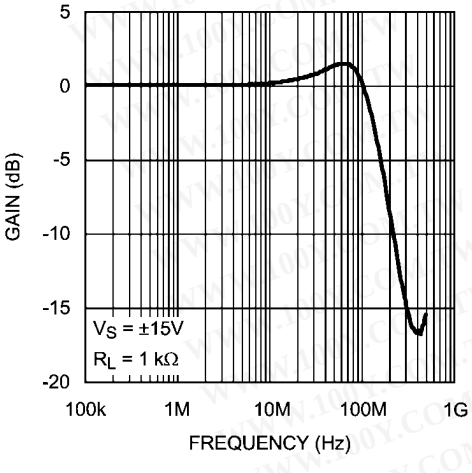
Gain vs. Frequency



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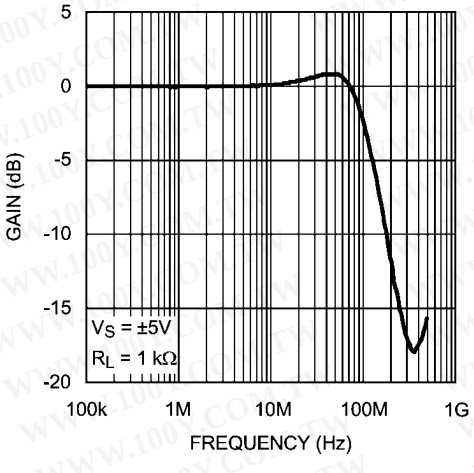
Gain vs. Frequency



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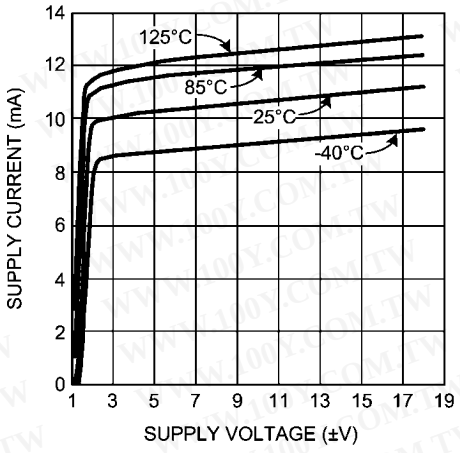
Supply Current vs. Supply Voltage



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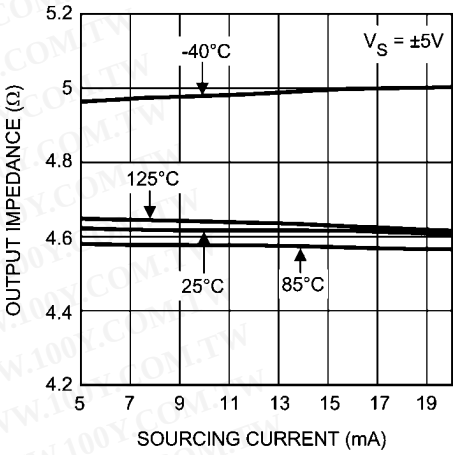
Output Impedance vs. Sourcing Current



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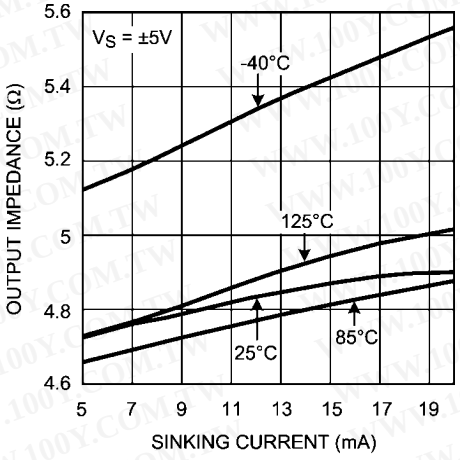
Output Impedance vs. Sinking Current



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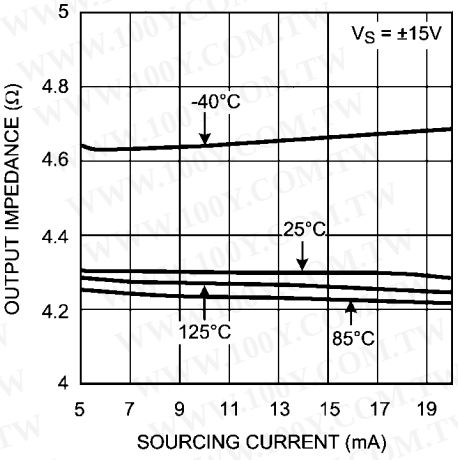
Output Impedance vs. Sourcing Current



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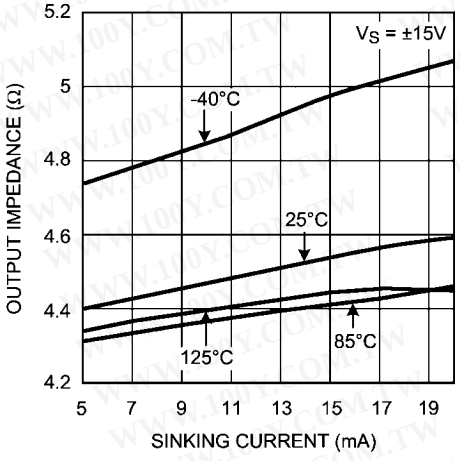
Output Impedance vs. Sinking Current



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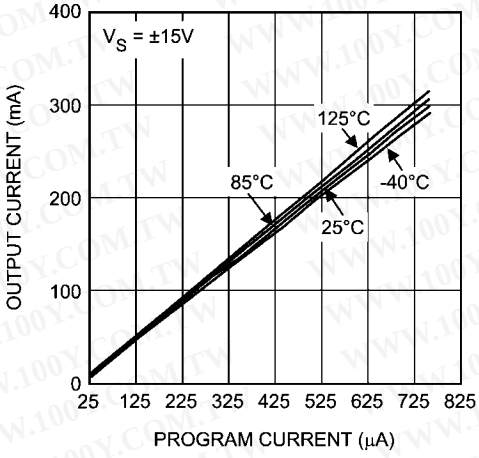
Output Short Circuit Current—Sourcing vs. Program Current



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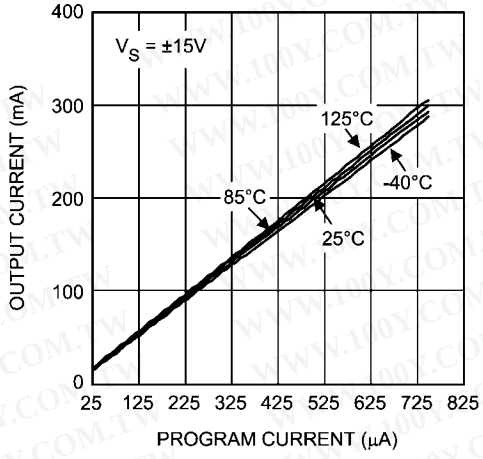
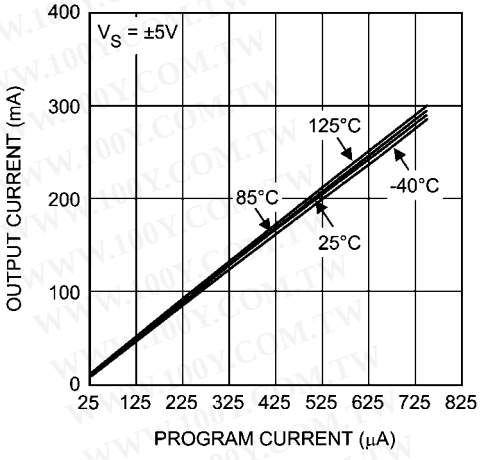
Output Short Circuit Current—Sinking vs. Program Current



20138655

Output Short Circuit Current—Sourcing vs. Program Current



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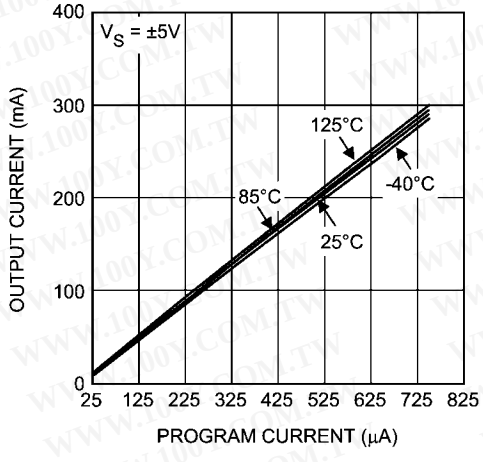
Output Short Circuit Current—Sinking vs. Program Current



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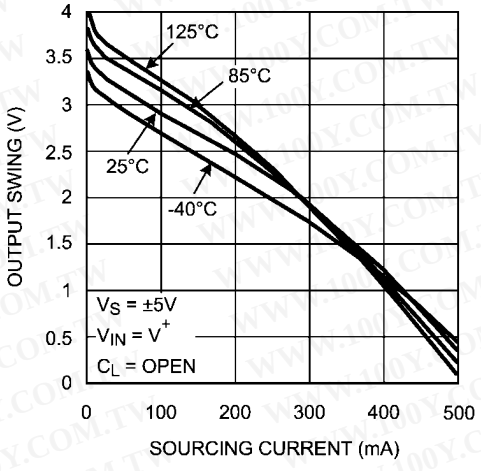
Positive Output Swing vs. Sourcing Current



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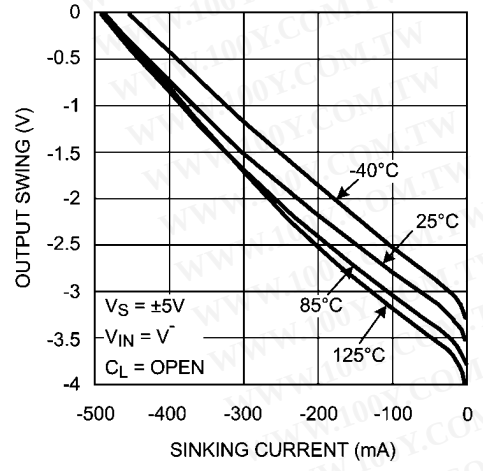
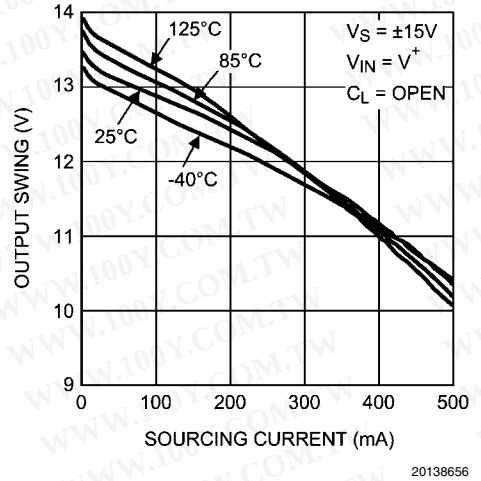
Negative Output Swing vs. Sinking Current



20138624

Positive Output Swing vs. Sourcing Current



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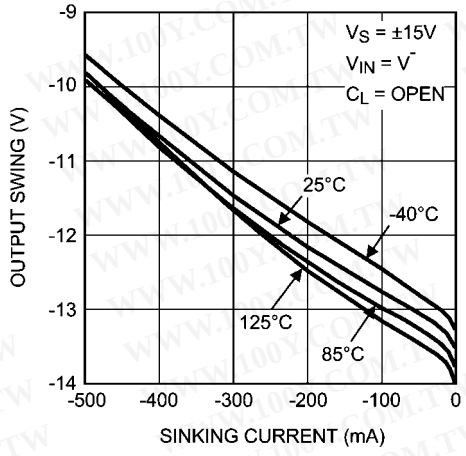
Negative Output Swing vs. Sinking Current



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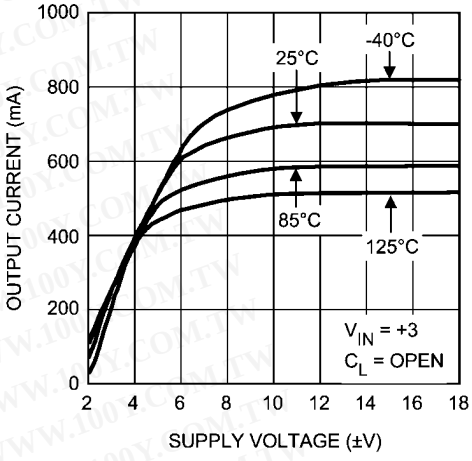
Output Short Circuit Current—Sourcing vs. Supply Voltage



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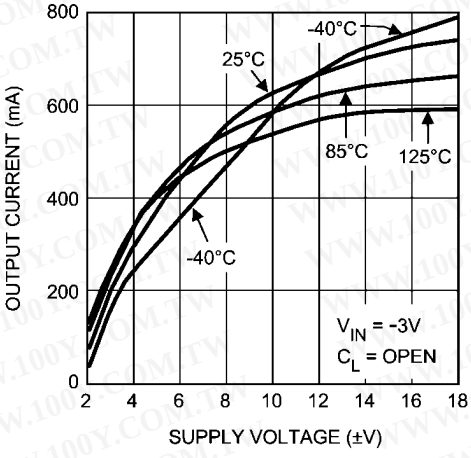
Output Short Circuit Current—Sinking vs. Supply Voltage



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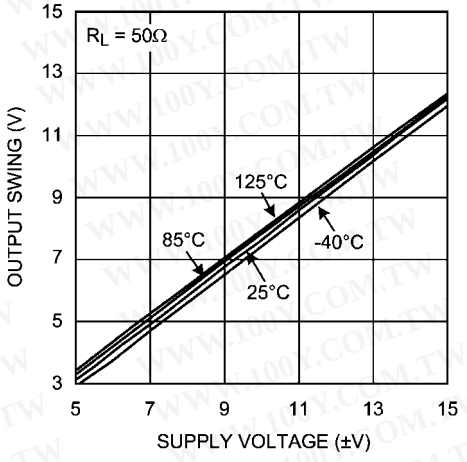
Positive Output Swing vs. Supply Voltage



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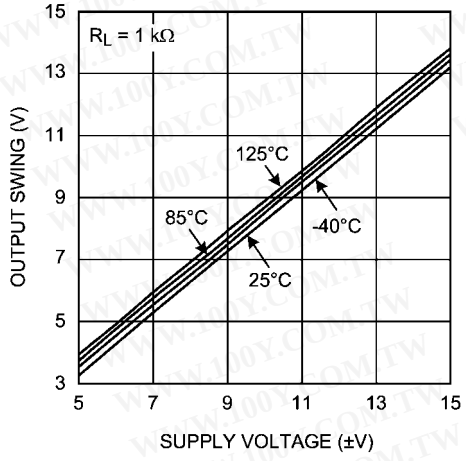
Positive Output Swing vs. Supply Voltage



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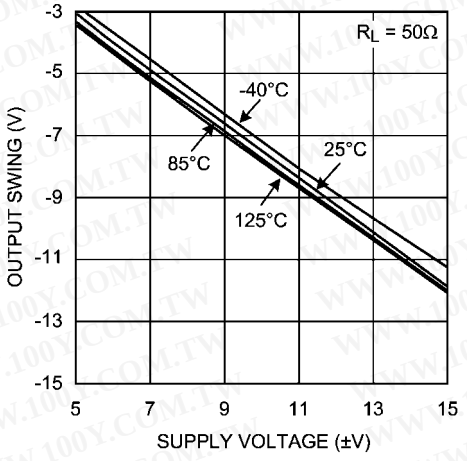
Negative Output Swing vs. Supply Voltage



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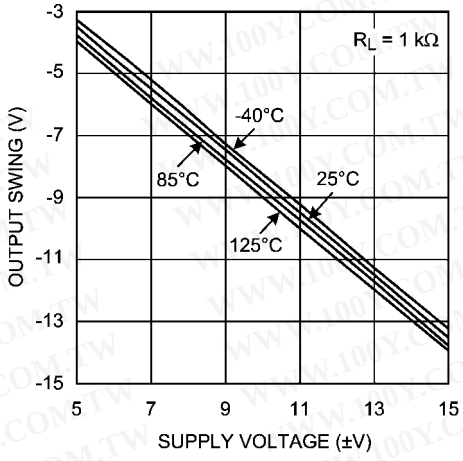
Negative Output Swing vs. Supply Voltage



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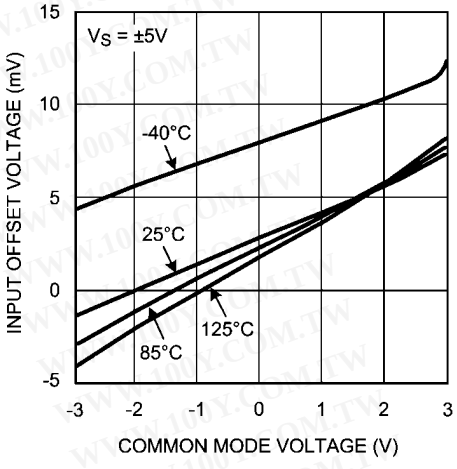
Input Offset Voltage of Amplifier vs. Common Mode Voltage



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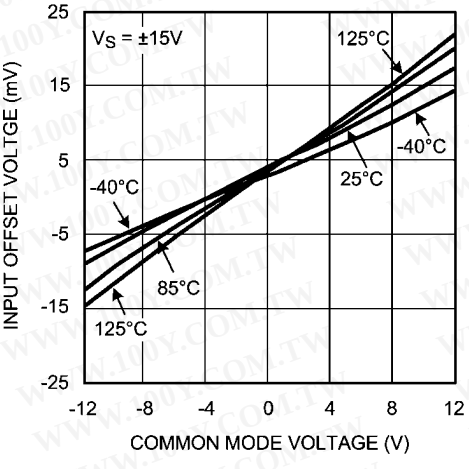
Input Offset Voltage of Amplifier vs. Common Mode Voltage



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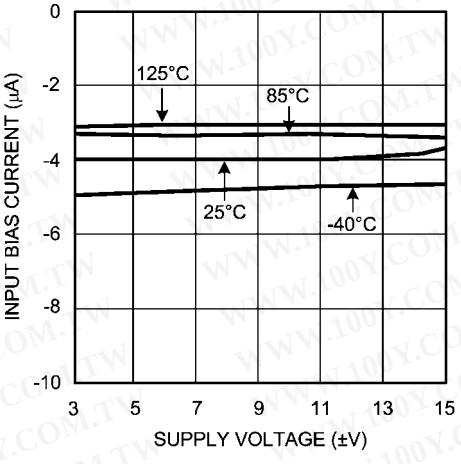
Input Bias Current of Amplifier vs. Supply Voltage



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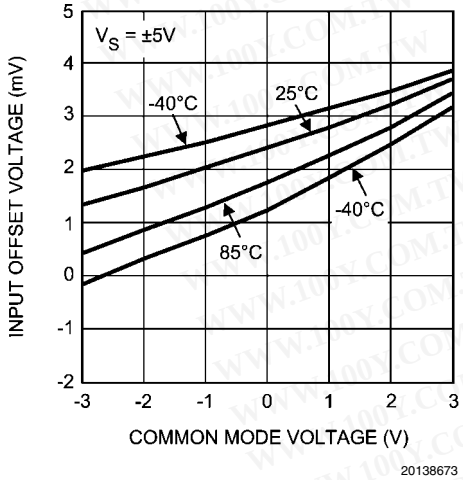
Input Offset Voltage of V/I Section vs. Common Mode Voltage



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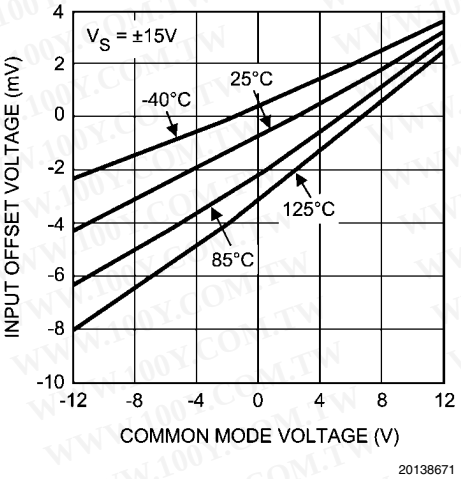
Input Offset Voltage of V/I Section vs. Common Mode Voltage



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Application Hints

BUFFERS

Buffers are often called voltage followers because they have largely unity voltage gain, thus the name has generally come to mean a device that supplies current gain but no voltage gain. Buffers serve in applications requiring isolation of source and load, i.e., high input impedance, low output impedance (high output current drive). In addition, they offer gain flatness and wide bandwidth.

Most operational amplifiers, that meet the other given requirements in a particular application, can be configured as buffers, though they are generally more complex and are, by and large, not optimized for unity gain operation. The commercial buffer is a cost effective substitute for an op amp. Buffers serve several useful functions, either in tandem with op amps or in standalone applications. As mentioned, their primary function is to isolate a high impedance source from a low impedance load, since a high Z source can't supply the needed current to the load. For example, in the case where the signal source to an analog to digital converter is a sensor, it is recommended that the sensor be isolated from the A/D converter. The use of a buffer ensures a low output impedance and delivery of a stable output to the converter. In A/D converter applications buffers need to drive varying and complex reactive loads.

Buffers come in two flavors: Open Loop and Closed Loop. While sacrificing the precision of some DC characteristics, and generally displaying poorer gain linearity, open loop buffers offer lower cost and increased bandwidth, along with less phase shift and propagation delay than do closed loop buffers. The LMH6321 is of the open loop variety.

Figure 1 shows a simplified diagram of the LMH6321 topology, revealing the open loop complementary follower design approach. *Figure 2* shows the LMH6321 in a typical application, in this case, a 50Ω coaxial cable driver.

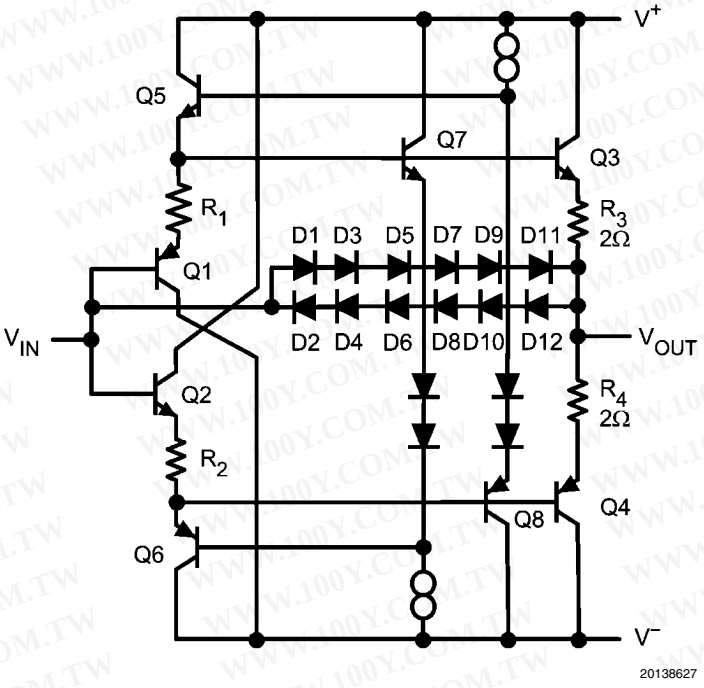


FIGURE 1. Simplified Schematic

SUPPLY BYPASSING

The method of supply bypassing is not critical for frequency stability of the buffer, and, for light loads, capacitor values in the neighborhood of 1 nF to 10 nF are adequate. However, under fast slewing and large loads, large transient currents are demanded of the power supplies, and when combined with any significant wiring inductance, these currents can produce voltage transients. For example, the LMH6321 can slew typically at 1000 V/µs. Therefore, under a 50Ω load condition the load can demand current at a rate, di/dt, of 20 A/µs. This current flowing in an inductance of 50 nH (approximately 1.5" of 22 gage wire) will produce a 1V transient. Thus, it is recommended that solid tantalum capacitors of 5 µF to 10 µF, in parallel with a ceramic 0.1 µF capacitor be added as close as possible to the device supply pins.

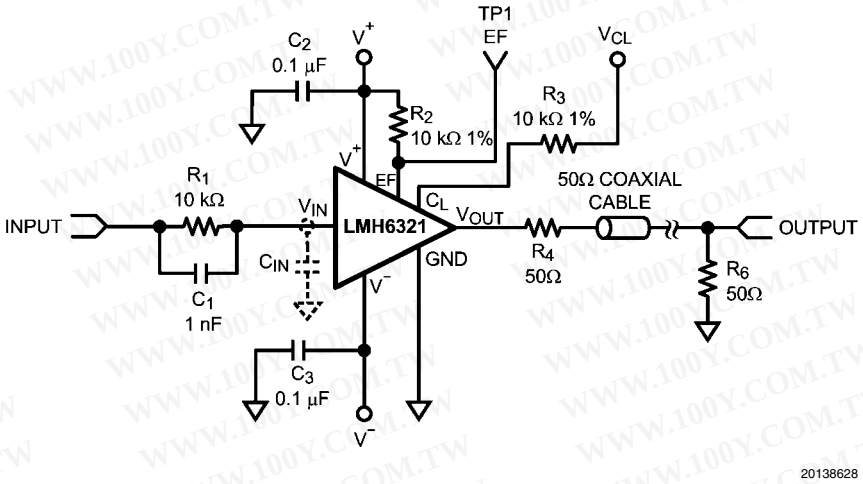


FIGURE 2. 50Ω Coaxial Cable Driver with Dual Supplies

For values of capacitors in the 10 µF to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of their very low ESR (typically less than 10 MΩ) and low ESL.

LOAD IMPEDANCE

The LMH6321 is stable under any capacitive load when driven by a 50Ω source. As shown by the Overshoot vs. Capacitive Load graph in the Typical Performance Characteristics, worst case overshoot is for a purely capacitive load of about 1 nF. Shunting the load capacitance with a resistor will reduce the overshoot.

SOURCE INDUCTANCE

Like any high frequency buffer, the LMH6321 can oscillate with high values of source inductance. The worst case condition occurs with no input resistor, and a purely capacitive load of 50 pF, where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. However, a 100Ω resistor placed in series with the buffer input will ensure stability with a source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

(Refer to the simplified schematic in *Figure 1*).

If the input-to-output differential voltage were allowed to exceed the Absolute Maximum Rating of 5V, an internal diode clamp would turn on and divert the current around the compound emitter followers of Q1/Q3 (D1 – D11 for positive input), or around Q2/Q4 (D2 – D12 for negative inputs). Without this clamp, the input transistors Q1 – Q4 would zener, thereby damaging the buffer.

To limit the current through this clamp, a series resistor should be added to the buffer input (see R_1 in *Figure 2*). Although the allowed current in the clamp can be as high as 5 mA, which would suggest a 2 kΩ resistor from a 15V source, it is recommended that the current be limited to about 1 mA, hence the 10 kΩ shown.

The reason for this larger resistor is explained in the following: One way that the input/output voltage differential can exceed the Abs Max value is under a short circuit condition to ground while driving the input with up to ±15V. However, in the LMH6321 the maximum output current is set by the programmable Current Limit pin (C_L). The value set by this pin is guaranteed to be accurate to 5 mA ±5%. If the input/output differential exceeds 5V while the output is trying to supply the maximum set current to a shorted condition or to a very low resistance load, a portion of that current will flow through the clamp diodes, thus creating an error in the total load current. If the input resistor is too low, the error current can exceed the 5 mA ±5% budget.

BANDWIDTH AND STABILITY

As can be seen in the schematic of *Figure 2*, a small capacitor is inserted in parallel with the series input resistors. The reason for this is to compensate for the natural band-limiting effect of the 1st order filter formed by this resistor and the input capacitance of the buffer. With a typical C_{IN} of 3.5 pF (*Figure 2*), a pole is created at

$$fp2 = 1/(2\pi R_1 C_{IN}) = 4.5 \text{ MHz} \quad (1)$$

This will band-limit the buffer and produce further phase lag. If used in an op amp-loop application with an amplifier that has the same order of magnitude of unity gain crossing as fp2, this additional phase lag will produce oscillation.

The solution is to add a small feed-forward capacitor (phase lead) around the input resistor, as shown in *Figure 2*. The value of this capacitor is not critical but should be such that the time constant formed by it and the input resistor that it is in parallel with (R_{IN}) be at least five times the time constant of $R_{IN}C_{IN}$. Therefore,

$$C_1 = (5R_{IN}/R_1)(C_{IN}) \quad (2)$$

from the Electrical Characteristics, R_{IN} is 250 kΩ.

In the case of the example in *Figure 2*, $R_{IN}C_{IN}$ produces a time-constant of 870 ns, so C_1 should be chosen to be a minimum of 4.4 µs, or 438 pF. The value of C_1 (1000 pF) shown in *Figure 2* gives 10 µs.

OUTPUT CURRENT AND SHORT CIRCUIT PROTECTION

The LMH6321 is designed to deliver a maximum continuous output current of 300 mA. However, the maximum available current, set by internal circuitry, is about 700 mA at room temperature. The output current is programmable up to 300 mA by a single external resistor and voltage source.

The LMH6321 is not designed to safely output 700 mA continuously and should not be used this way. However, the available maximum continuous current will likely be limited by the particular application and by the package type chosen, which together set the thermal conditions for the buffer (see Thermal Management section) and could require less than 300 mA.

The programming of both the sourcing and sinking currents into the load is accomplished with a single resistor. *Figure 3* shows a simplified diagram of the V to I converter and I_{SC} protection circuitry that, together, perform this task.

Referring to *Figure 3*, the two simplified functional blocks, labeled V/I Converter and Short Circuit Protection, comprise the circuitry of the Current Limit Control.

The V/I converter consists of error amplifier A1 driving two PNP transistors in a Darlington configuration. The two input connections to this amplifier are V_{CL} (inverting input) and GND (non-inverting input). If GND is connected to zero volts, then the high open loop gain of A1, as well as the feedback through the Darlington, will force C_L, and thus one end R_{EXT} to be at zero volts also. Therefore, a voltage applied to the other end of R_{EXT} will force a current

$$I_{EXT} = V_{PROG}/R_{EXT} \quad (3)$$

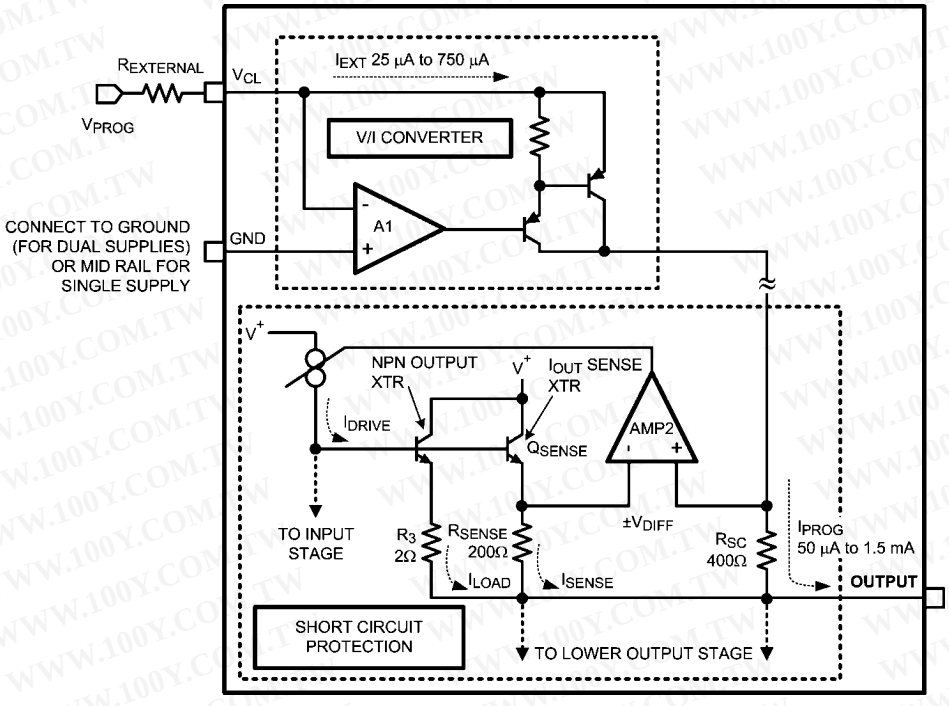
into this pin. Via this pin, I_{OUT} is programmable from 10 mA to 300 mA by setting I_{EXT} from 25 µA to 750 µA by means of a fixed R_{EXT} of 10 kΩ and making V_{CL} variable from 0.25V to 7.5V. Thus, an input voltage V_{CL} is converted to a current I_{EXT}. This current is the output from the V/I converter. It is gained up by a factor of two and sent to the Short Circuit Protection block as I_{PROG}. I_{PROG} sets a voltage drop across R_{SC} which is applied to the non-inverting input of error amp A2. The other input is across R_{SENSE}. The current through R_{SENSE}, and hence the voltage drop across it, is proportional to the load current, via the current sense transistor Q_{SENSE}. The output of A2 controls the drive (I_{DRIVE}) to the base of the NPN output transistor, Q3 which is, proportional to the amount and polarity of the voltage differential (V_{DIFF}) between AMP2 inputs, that is, how much the voltage across R_{SENSE} is greater than or less than the voltage across R_{SC}. This loop gains I_{EXT} up by another 200, thus

$$I_{SC} = 2 \times 200\ (I_{EXT}) = 400\ I_{EXT} \quad (4)$$

Therefore, combining Equations (3) and (4), and solving for R_{EXT} , we get

$$R_{EXT} = 400\ V_{PROG}/I_{SC} \quad (5)$$

If the V_{CL} pin is left open, the output short circuit current will default to about 700 mA. At elevated temperatures this current will decrease.



Only the NPN output I_{SC} protection is shown. Depending on the polarity of V_{DIFF}, AMP2 will turn I_{DRIVE} either on or off.

FIGURE 3. Simplified Diagram of Current Limit Control

THERMAL MANAGEMENT

Heatsinking

For some applications, a heat sink may be required with the LMH6321. This depends on the maximum power dissipation and maximum ambient temperature of the application. To accomplish heat sinking, the tabs on TO-263 and PSOP package may be soldered to the copper plane of a PCB for heatsinking (note that these tabs are electrically connected to the most negative point in the circuit, i. e.,V^-).

Heat escapes from the device in all directions, mainly through the mechanisms of convection to the air above it and conduction to the circuit board below it and then from the board to the air. Natural convection depends on the amount of surface area that is in contact with the air. If a conductive plate serving as a heatsink is thick enough to ensure perfect thermal conduction (heat spreading) into the far recesses of the plate, the temperature rise would be simply inversely proportional to the total exposed area. PCB copper planes are, in that sense, an aid to convection, the difference being that they are not thick enough to ensure perfect conduction. Therefore, eventually we will reach a point of diminishing returns (as seen in *Figure 5*). Very large increases in the copper area will produce smaller and smaller improvement in thermal resistance. This occurs, roughly, for a 1 inch square of 1 oz copper board. Some improvement continues until about 3 square inches, especially for 2 oz boards and better, but beyond that, external heatsinks are required. Ultimately, a reasonable practical value attainable for the junction to ambient thermal resistance is about 30 °C/W under zero air flow.

A copper plane of appropriate size may be placed directly beneath the tab or on the other side of the board. If the conductive plane is placed on the back side of the PCB, it is recommended that thermal vias be used per JEDEC Standard JESD51-5.

Determining Copper Area

One can determine the required copper area by following a few basic guidelines:

1. Determine the value of the circuit's power dissipation, P_D
2. Specify a maximum operating ambient temperature, $T_{A(MAX)}$. Note that when specifying this parameter, it must be kept in mind that, because of internal temperature rise due to power dissipation, the die temperature, T_J, will be higher than T_A by an amount that is dependent on the thermal resistance from junction to ambient, θ_{JA}. Therefore, T_A must be specified such that T_J does not exceed the absolute maximum die temperature of 150° C.
3. Specify a maximum allowable junction temperature, $T_{J(MAX)}$, which is the temperature of the chip at maximum operating current. Although no strict rules exist, typically one should design for a maximum continuous junction temperature of 100°C to 130°C, but no higher than 150° C which is the absolute maximum rating for the part.
4. Calculate the value of junction to ambient thermal resistance, θ_{JA}
5. Choose a copper area that will guarantee the specified $T_{J(MAX)}$ for the calculated θ_{JA}. θ_{JA} as a function of copper area in square inches is shown in *Figure 4*.

The maximum value of thermal resistance, junction to ambient θ_{JA}, is defined as:

$$\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)}) / P_{D(MAX)} \quad (6)$$

where:

$T_{J(MAX)}$ = the maximum recommended junction temperature

$T_{A(MAX)}$ = the maximum ambient temperature in the user's environment

$P_{D(MAX)}$ = the maximum recommended power dissipation

Note: The allowable thermal resistance is determined by the maximum allowable heat rise , $T_{RISE} = T_{J(MAX)} - T_{A(MAX)} = (\theta_{JA})(P_{D(MAX)})$. Thus, if ambient temperature extremes force T_{RISE} to exceed the design maximum, the part must be de-rated by either decreasing P_D to a safe level, reducing θ_{JA}, further, or, if available, using a larger copper area.

Procedure

1. First determine the maximum power dissipated by the buffer, $P_{D(MAX)}$. For the simple case of the buffer driving a resistive load, and assuming equal supplies, $P_{D(MAX)}$ is given by

$$P_{D(MAX)} = I_S (2V^+) + V^{+2}/4R_L \quad (7)$$

   where: I_S = quiescent supply current

2. Determine the maximum allowable die temperature rise,

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)} = P_{D(MAX)}\theta_{JA} \quad (8)$$

3. Using the calculated value of $T_{R(MAX)}$ and $P_{D(MAX)}$ the required value for junction to ambient thermal resistance can be found:

$$\theta_{JA} = T_{R(MAX)}/P_{D(MAX)} \quad (9)$$

4. Finally, using this value for θ_{JA} choose the minimum value of copper area from *Figure 4*.

Example

Assume the following conditions:

$V^+ = V^- = 15V$, $R_L = 50\Omega$, $I_S = 15$ mA $T_{J(MAX)} = 125°C$, $T_{A(MAX)} = 85°C$.

1. From (7)
   $P_{D(MAX)} = I_S (2V^+) + V^{+2}/4R_L = (15\text{ mA})(30V) + 225V^2/200\Omega = 1.58W$
2. From (8)
   $T_{R(MAX)} = 125°C - 85°C = 40°C$
3. From (9)
   $\theta_{JA} = 40°C/1.58W = 25.3°C/W$

Examining the plot of Copper Area vs. θ_{JA}, we see that we cannot attain this low of a thermal resistance for one layer of 1 oz copper. It will be necessary to derate the part by decreasing either the ambient temperature or the power dissipation. Other solutions are to use two layers of 1 oz foil, or use 2 oz copper (see Table 1), or to provide forced air flow. One should allow about an extra 15% heat sinking capability for safety margin.

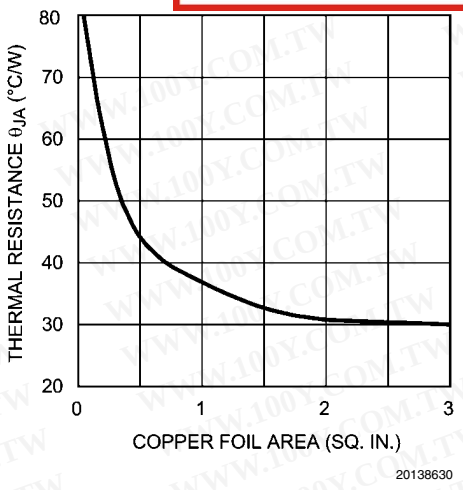


FIGURE 4. Thermal Resistance (typ) for 7-L TO-263 Package Mounted on 1 oz. (0.036 mm) PC Board Foil

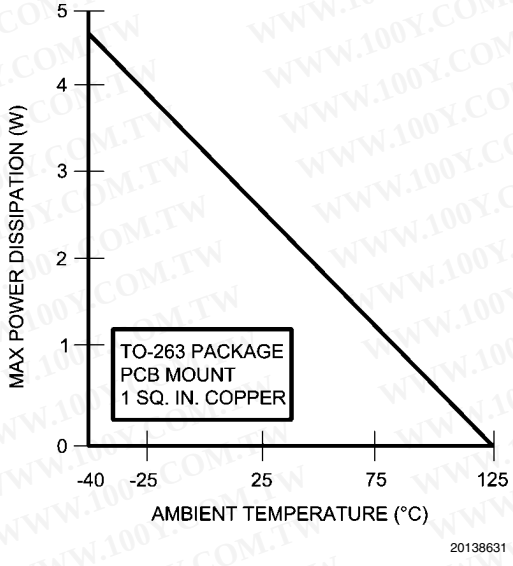


FIGURE 5. Derating Curve for TO-263 package. No Air Flow

TABLE 1. θ_{JA} vs. Copper Area and P_D for TO-263. 1.0 oz cu Board. No Air Flow. Ambient Temperature = 24°C

Copper Area	θJA @ 1.0W (°C/W)	θJA @ 2.0W (°C/W)
1 Layer = 1"x2" cu Bottom	62.4	54.7
2 Layer = 1"x2" cu Top & Bottom	36.4	32.1
2 Layer = 2"x2" cu Top & Bottom	23.5	22.0
2 Layer = 2"x4" cu Top & Bottom	19.8	17.2

As seen in the previous example, buffer dissipation in DC circuit applications is easily computed. However, in AC circuits, signal wave shapes and the nature of the load (reactive, non-reactive) determine dissipation. Peak dissipation can be several times the average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

A selection of thermal data for the PSOP package is shown in Table 2. The table summarized θ_{JA} for both 0.5 watts and 0.75 watts. Note that the thermal resistance, for both the TO-263 and the PSOP package is lower for the higher power dissipation levels. This phenomenon is a result of the principle of Newtons Law of Cooling. Restated in term of heatsink cooling, this principle says that the rate of cooling and hence the thermal conduction, is proportional to the temperature difference between the junction and the outside environment (ambient). This difference increases with increasing power levels, thereby producing higher die temperatures with more rapid cooling.

TABLE 2. θ_{JA} vs. Copper Area and P_D for PSOP. 1.0 oz cu Board. No Airflow. Ambient Temperature = 22°C

Copper Area/Vias	θJA @ 0.5W (°C/W)	θJA @ 0.75W (°C/W)
1 Layer = 0.05 sq. in. (Bottom) + 3 Via Pads	141.4	138.2
1 Layer = 0.1 sq. in. (Bottom) + 3 Via Pads	134.4	131.2
1 Layer = 0.25 sq. in. (Bottom) + 3 Via Pads	115.4	113.9
1 Layer = 0.5 sq. in. (Bottom) + 3 Via Pads	105.4	104.7
1 Layer = 1.0 sq. in. (Bottom) + 3 Via Pads	100.5	100.2
2 Layer = 0.5 sq. in. (Top)/ 0.5 sq. in. (Bottom) + 33 Via Pads	93.7	92.5
2 Layer = 1.0 sq. in. (Top)/ 1.0 sq. in. (Bottom) + 53 Via Pads	82.7	82.2

ERROR FLAG OPERATION

The LMH6321 provides an open collector output at the EF pin that produces a low voltage when the Thermal Shutdown Protection is engaged, due to a fault condition. Under normal operation, the Error Flag pin is pulled up to V+ by an external resistor. When a fault occurs, the EF pin drops to a low voltage and then returns to V+ when the fault disappears. This voltage change can be used as a diagnostic signal to alert a microprocessor of a system fault condition. If the function is not used, the EF pin can be either tied to ground or left open. If this function is used, a 10 kΩ, or larger, pull-up resistor (R_2 in *Figure 2*) is recommended. The larger the resistor the lower the voltage will be at this pin under thermal shutdown. Table 3 shows some typical values of V_{EF} for 10 kΩ and 100 kΩ.

TABLE 3. V_{EF} vs. R_2 *Figure 2*

R_2	@ V+ = 5V	@V+ = 15V
10 kΩ	0.24V	0.55V
100 KΩ	0.036V	0.072V

SINGLE SUPPLY OPERATION

If dual supplies are used, then the GND pin can be connected to a hard ground (0V) (as shown in *Figure 2*). However, if only a single supply is used, this pin must be set to a voltage of one V_{BE} (~0.7V) or greater, or more commonly, mid rail, by a stiff, low impedance source. This precludes applying a resistive voltage divider to the GND pin for this purpose. *Figure 6* shows one way that this can be done.

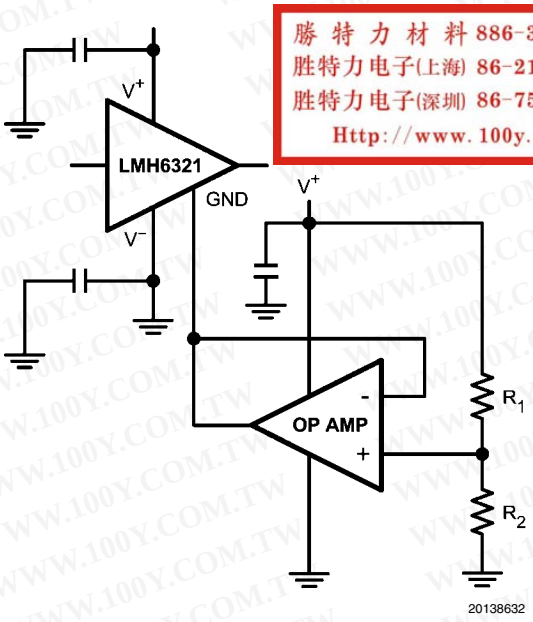


FIGURE 6. Using an Op Amp to Bias the GND Pin to ½ V + for Single Supply Operation

In *Figure 6*, the op amp circuit pre-biases the GND pin of the buffer for single supply operation.

The GND pin can be driven by an op amp configured as a constant voltage source, with the output voltage set by the resistor voltage divider, R_1 and R_2. It is recommended that These resistors be chosen so as to set the GND pin to V+/2, for maximum common mode range.

SLEW RATE

Slew rate is the rate of change of output voltage for large-signal step input changes. For resistive load, slew rate is limited by internal circuit capacitance and operating current (in general, the higher the operating current for a given internal capacitance, the faster is the slew rate). *Figure 7* shows the slew capabilities of the LMH6321 under large signal input conditions, using a resistive load.

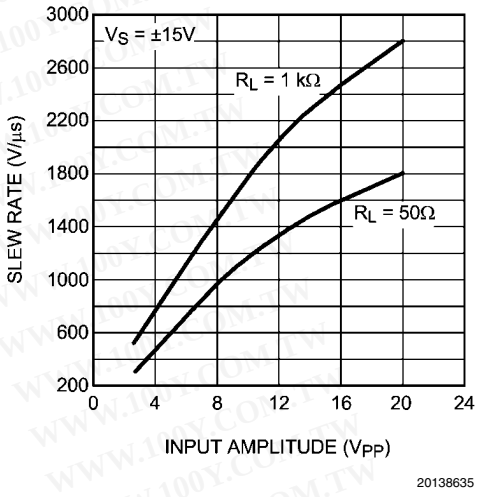


FIGURE 7. Slew Rate vs. Peak-to-Peak Input Voltage

However, when driving capacitive loads, the slew rate may be limited by the available peak output current according to the following expression.

$$dv/dt = I_{PK}/C_L \quad (10)$$

and rapidly changing output voltages will require large output load currents. For example if the part is required to slew at 1000 V/µs with a load capacitance of 1 nF the current demand from the LMH6321 would be 1A. Therefore, fast slew rate is incompatible with large C_L. Also, since C_L is in parallel with the load, the peak current available to the load decreases as C_L increases.

Figure 8 illustrates the effect of the load capacitance on slew rate. Slew rate tests are specified for resistive loads and/or very small capacitive loads, otherwise the slew rate test would be a measure of the available output current. For the highest slew rate, it is obvious that stray load capacitance should be minimized. Peak output current should be kept below 500 mA. This translates to a maximum stray capacitance of 500 pF for a slew rate of 1000 V/µs.

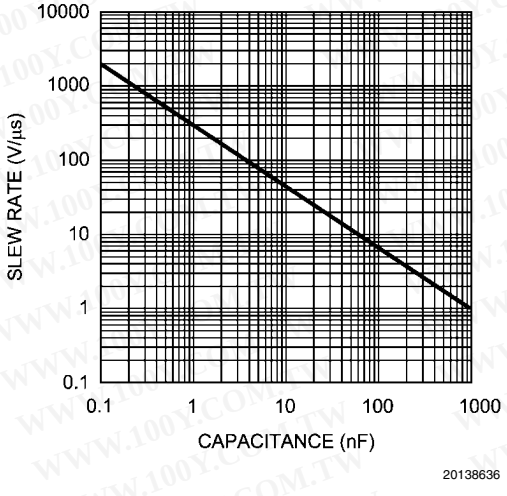
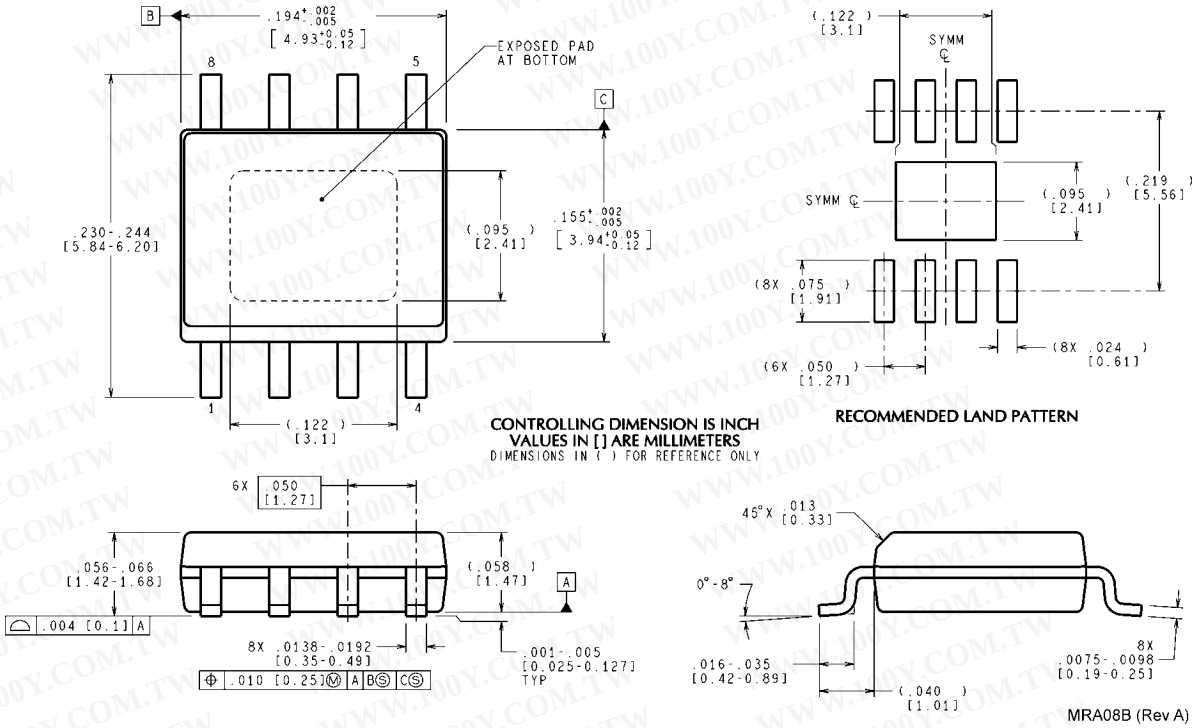
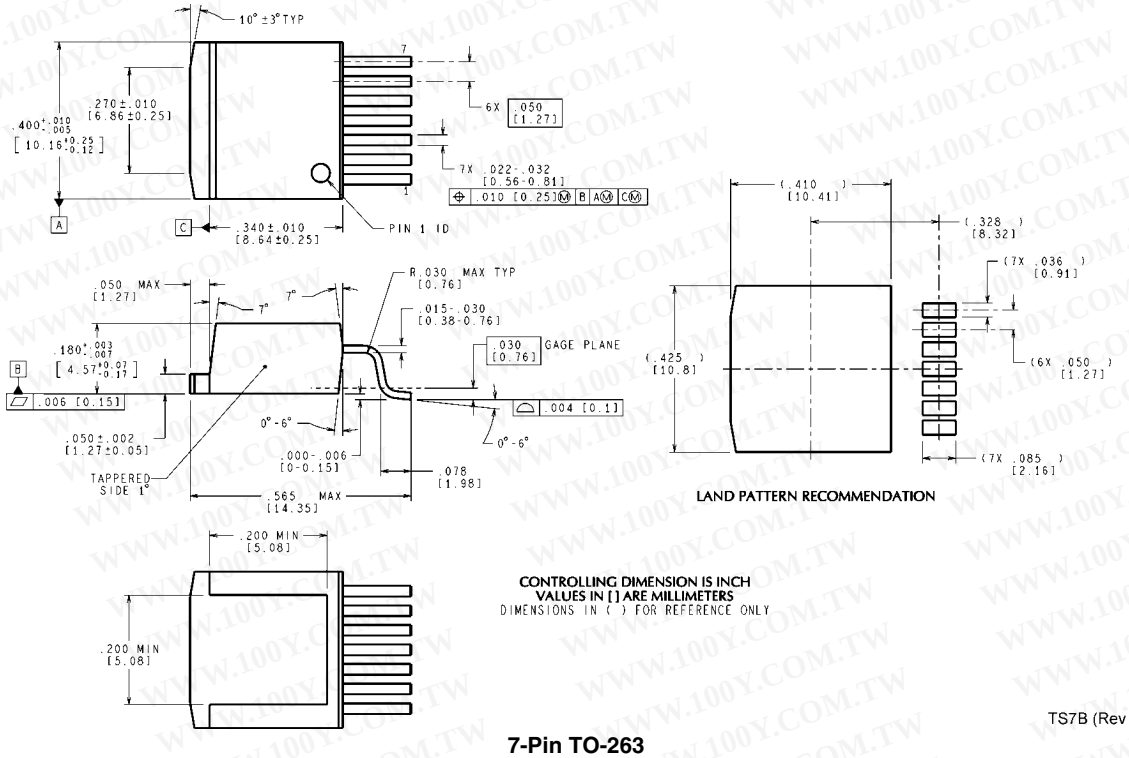


FIGURE 8. Slew Rate vs. Load Capacitance

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin PSOP
NS Package Number MRA08B



7-Pin TO-263
NS Package Number TS7B

Notes

Notes

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