MCP6001/2/4

1 MHz 低功率运算放大器

特征

- 提供 SC-70-5 和 SOT-23-5 封装
- 1 MHz 增益带宽积 （典型值）
- 轨到轨输入 / 输出
- 供电电压：1.8V 至 5.5V
- 供电电流：I_Q = 100 µA （典型值）
- 90° 相位容限 （典型值）
- 温度范围：
  - 工业级：-40°C 至 +85°C
  - 扩展级：-40°C 至 +125°C
- 提供单运放、双运放和四运放封装

应用

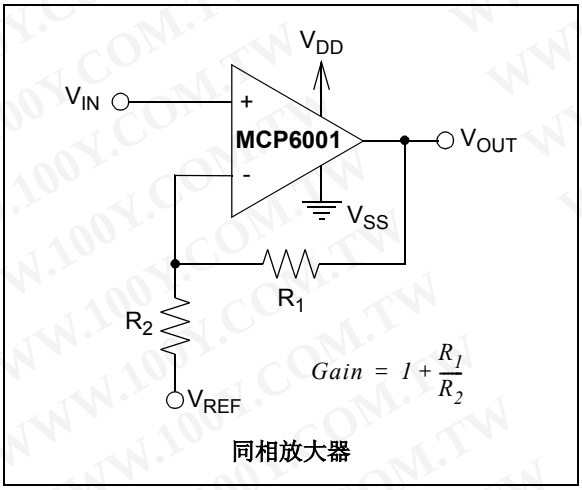
- 汽车
- 便携式设备
- 光电二极管放大器
- 模拟滤波器
- 笔记本电脑和 PDA
- 电池供电系统

工具支持

SPICE 宏模型 （可在 www.microchip.com 网站下载）

FilterLab® 软件 （可在 www.microchip.com 网站下载）

典型应用



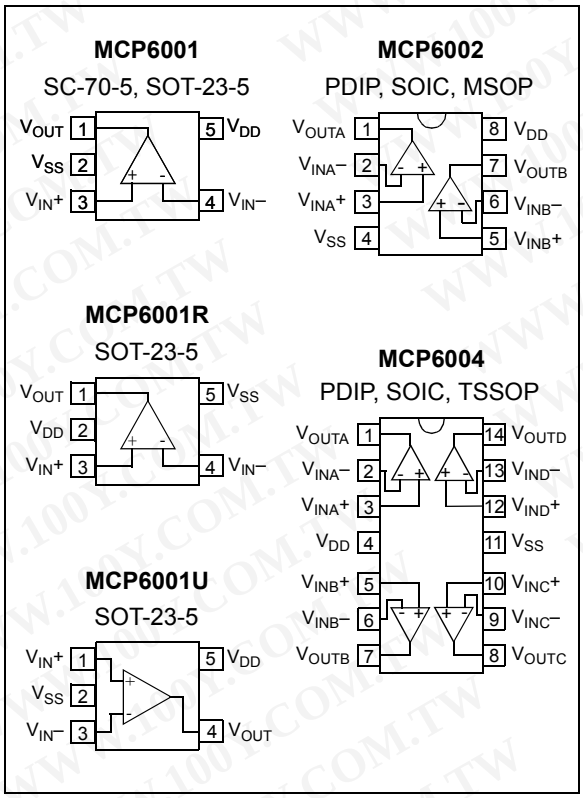
同相放大器

说明

Microchip Technology Inc. 的MCP6001/2/4 系列运算放大器是专门为各种通用应用设计的。这一系列器件具有 1 MHz增益带宽积（Gain Bandwidth Product，GBWP）和 90° 相位容限（典型值）。在 500 pF 的容性负载下，它也同样具有 45° 相位容限 （典型值）。即使单电源供电电压只有 1.8V，这个系列的运算放大器仍可工作，此时静态电流为 100 µA（典型值）。此外，MCP6001/2/4 支持轨到轨输入输出，它的共模输入电压范围为 V_{DD} + 300 mV 到 V_{SS} - 300 mV。这个系列的运算放大器在设计中采用了 Microchip 先进的 CMOS 工艺。

MCP6001/2/4 系列提供了工业级和扩展级的温度范围。电源供电范围为 1.8V 到 5.5V。

封装形式



1.0 电气特性

绝对最大额定值 †

V_{DD} - V_{SS} 7.0V
所有输入输出 .....V_{SS} -0.3V 至 V_{DD} +0.3V
输入电压差分 ..... $|V_{DD} - V_{SS}|$
输出短路电流 ..... 连续
输入引脚电流.....±2 mA
输出引脚和供电引脚电流 .....±30 mA
储存温度..... -65°C 至 +150°C
最大结温 （T_J）.....+150°C
所有引脚 ESD 保护 （HBM；MM）..... ≥ 4 kV; 200V

† 注：如果器件运行条件超过上述各项绝对最大额定值，可能对器件造成永久性损坏。上述参数仅是运行条件的极大值，我们不建议使器件运行在超过或在技术规范以外的条件下。器件长时间工作在绝对最大极限条件下，其稳定性可能受到影响。

DC 特性

电气技术规范：除非另外说明，否则 T_A = +25°C， V_{DD} = +1.8V 至 +5.5V， V_{SS} = GND， V_{CM} = V_{DD}/2， R_L = 10 kΩ 至 V_{DD}/2 且 $V_{OUT} \approx V_{DD}$/2。

参数	符号	最小值	典型值	最大值	单位	条件
输入失调						
输入失调电压	V_{OS}	-4.5	—	+4.5	mV	V_{CM} = V_{SS} **(注 1)**
输入失调温度漂移	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A= -40°C 至 +125°C, V_{CM} = V_{SS}
电源抑制比	PSRR	—	86	—	dB	V_{CM} = V_{SS}
输入偏置电流和阻抗						
输入偏置电流：	I_B	—	±1.0	—	pA	
工业温度范围	I_B	—	19	—	pA	T_A = +85°C
扩展温度范围	I_B	—	1100	—	pA	T_A = +125°C
输入失调电流	I_{OS}	—	±1.0	—	pA	
共模输入阻抗	Z_{CM}	—	10^{13}||6	—	Ω||pF	
差分输入阻抗	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
共模						
共模输入范围	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
共模抑制比	CMRR	60	76	—	dB	V_{CM} = -0.3V至5.3V, V_{DD} = 5V
开环增益						
DC 开环增益 （大信号）	A_{OL}	88	112	—	dB	V_{OUT} = 0.3V 至 V_{DD} - 0.3V, V_{CM} = V_{SS}
输出						
最大输出电压摆幅	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V
输出短路电流	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
电源						
电源电压	V_{DD}	1.8	—	5.5	V	
每个放大器的静态电流	I_Q	50	100	170	µA	I_O = 0, V_{DD} = 5.5V, V_{CM} = 5V

注 1： 日期代码在 2004 年 12 月 （星期代码 49）之前的 MCP6001/2/4 器件测得的最大 / 最小值为 ±7 mV。

AC 特性

电气技术规范：除非另外说明，否则 T_A = +25°C， V_{DD} = +1.8 至 5.5V， V_{SS} = GND， V_{CM} = V_{DD}/2， V_{OUT} ≈ V_{DD}/2， R_L = 10 kΩ 至 V_{DD}/2 且 C_L = 60 pF。

参数	符号	最小值	典型值	最大值	单位	条件
AC 响应						
增益带宽积	GBWP	—	1.0	—	MHz	
相位容限	PM	—	90	—	°	G = +1
转换速率	SR	—	0.6	—	V/µs	
噪声						
输入噪声电压	E_{ni}	—	6.1	—	µVp-p	f = 0.1 Hz 至 10 Hz
输入噪声电压密度	e_{ni}	—	28	—	nV/√Hz	f = 1 kHz
输入噪声电流密度	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

温度特性

电气技术规范：除非另外说明，否则 V_{DD} = +1.8V 至 +5.5V 且 V_{SS} = GND。

参数	符号	最小值	典型值	最大值	单位	条件
温度范围						
工业温度范围	T_A	-40	—	+85	°C	
扩展温度范围	T_A	-40	—	+125	°C	
工作温度范围	T_A	-40	—	+125	°C	**注**
储存温度范围	T_A	-65	—	+150	°C	
封装热阻						
热阻， 5L-SC70	θ_{JA}	—	331	—	°C/Ω	
热阻 , 5L-SOT-23	θ_{JA}	—	256	—	°C/Ω	
热阻 , 8L-PDIP	θ_{JA}	—	85	—	°C/Ω	
热阻 , 8L-SOIC (150 mil)	θ_{JA}	—	163	—	°C/Ω	
热阻 , 8L-MSOP	θ_{JA}	—	206	—	°C/Ω	
热阻 , 14L-PDIP	θ_{JA}	—	70	—	°C/Ω	
热阻 , 14L-SOIC	θ_{JA}	—	120	—	°C/Ω	
热阻 , 14L-TSSOP	θ_{JA}	—	100	—	°C/Ω	

注： 工业级温度的器件可工作在扩展温度范围内，但性能有所下降。在任何情况下，内部结温 （T_J）均不得超过绝对最大参数值 +150°C。

2.0 典型性能曲线

注： 以下图表来自有限样本数的统计结果，仅供参考。所列出的性能特性未经测试，我们不做保证。一些图表中列出的数据可能超出规定的工作范围（如：超出了规定的电源电压范围），因此不在担保范围。

注：除非另外说明，否则 T_A = +25°C， V_{DD} = +1.8V 至 +5.5V， V_{SS} = GND， $V_{CM} = V_{DD}/2$， $V_{OUT} \approx V_{DD}/2$， R_L = 10 kΩ 至 $V_{DD}/2$ 且 C_L = 60 pF。

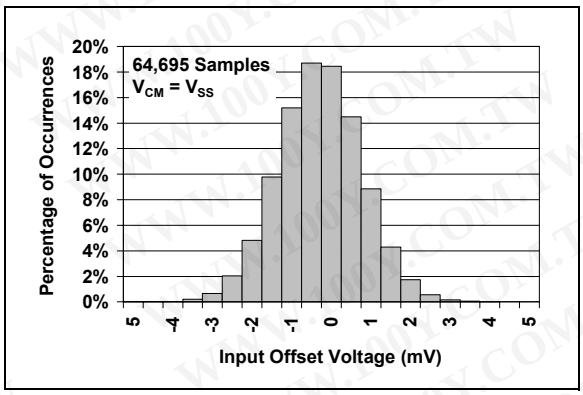


图 2-1： *输入失调电压*

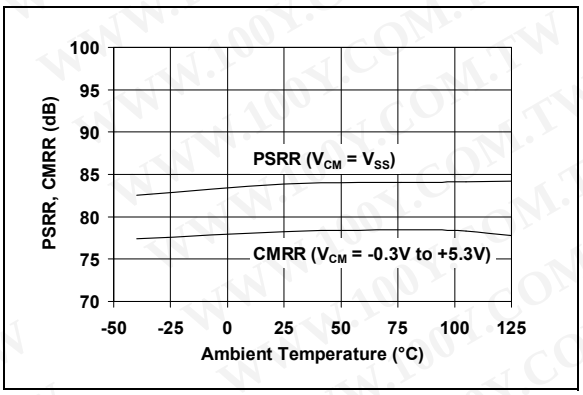


图 2-4： *CMRR, PSRR- 环境温度曲线*

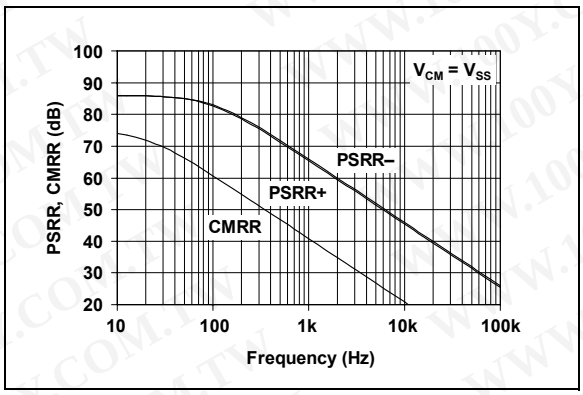


图 2-2： *PSRR,CMRR—频率曲线*

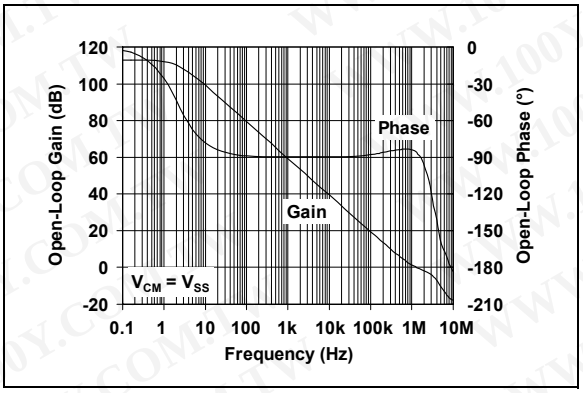


图 2-5： *开环增益，相位—频率曲线*

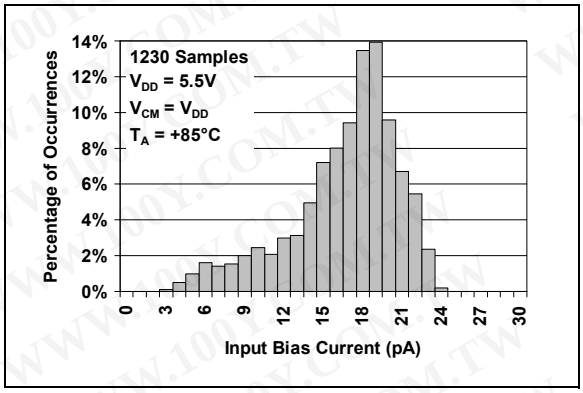


图 2-3： *+85°C 时输入偏置电流*

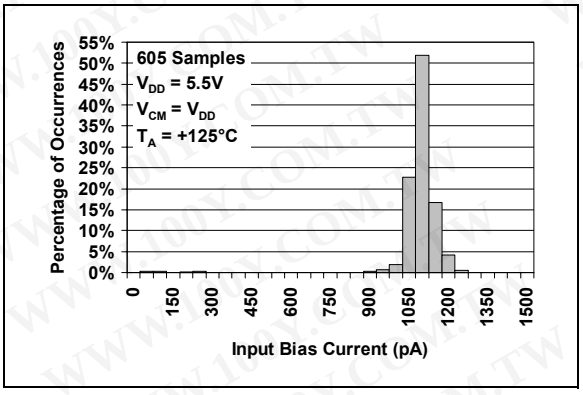


图 2-6： *+125°C 时输入偏置电流*

注：除非另外说明，否则 T_A = +25°C， V_{DD} = +1.8V 至 +5.5V， V_{SS} = GND， $V_{CM} = V_{DD}/2$， $V_{OUT} \approx V_{DD}/2$， R_L = 10 kΩ 至 $V_{DD}/2$ 且 C_L = 60 pF。

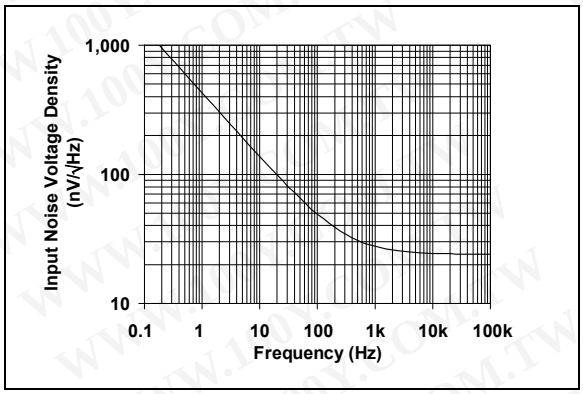


图 2-7： *输入噪声电压密度—频率曲线*

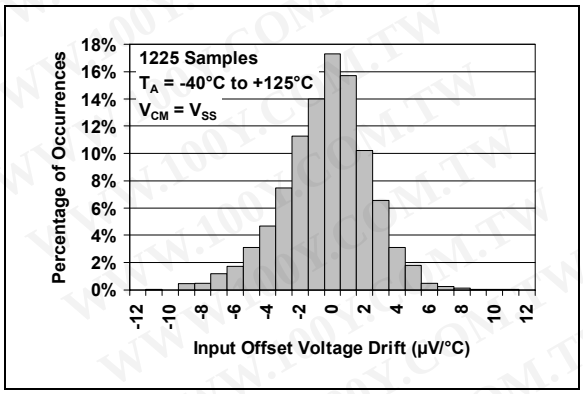


图 2-10： *输入失调电压漂移*

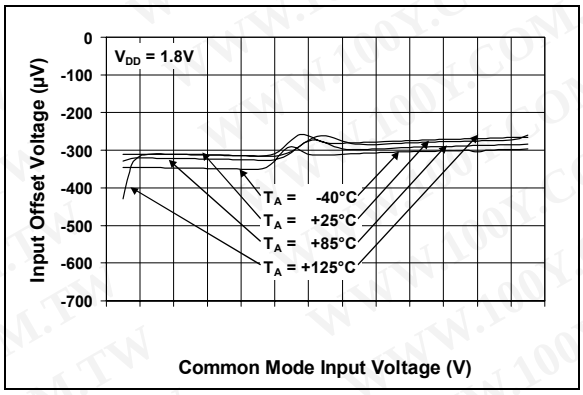


图 2-8： *V_{DD} = 1.8V 时，输入失调电压—共模输入电压曲线*

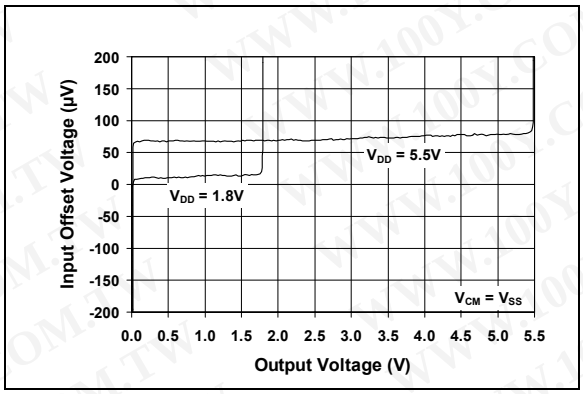


图 2-11： *输入失调电压—输出电压曲线*

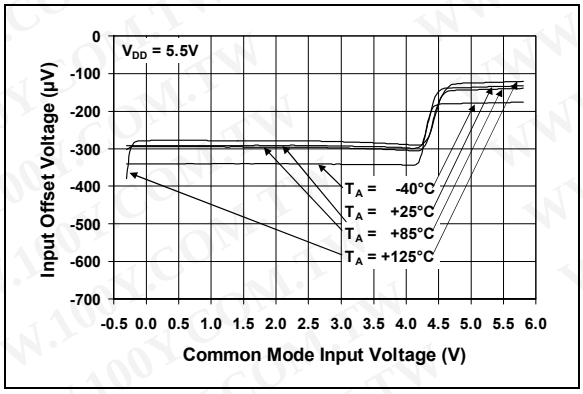


图 2-9： *V_{DD} = 5.5V 时，输入失调电压—共模输入电压曲线*

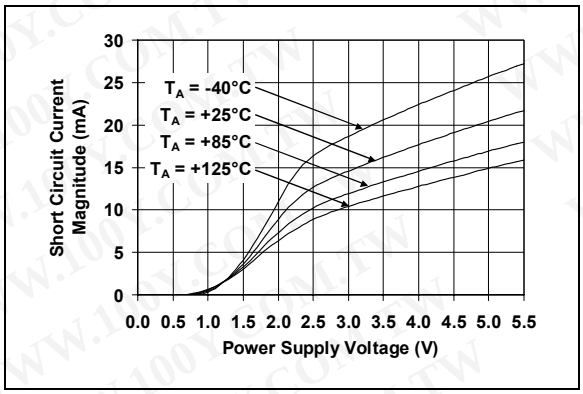


图 2-12： *输出短路电流—电源电压曲线*

注：除非另外说明，否则 T_A = +25°C， V_{DD} = +1.8V 至 +5.5V， V_{SS} = GND， V_{CM} = V_{DD}/2， V_{OUT} ≈ V_{DD}/2， R_L = 10 kΩ 至 V_{DD}/2 且 C_L = 60 pF。

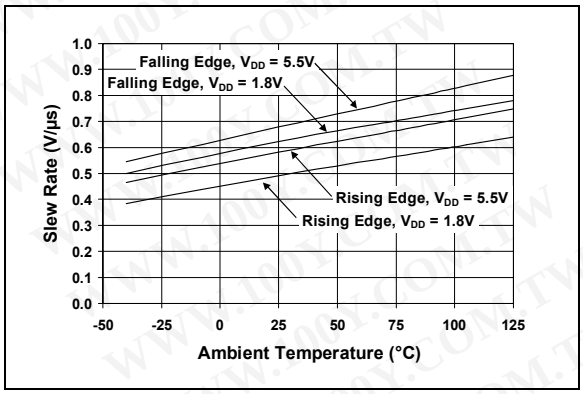


图 2-13： *转换速率—环境温度曲线*

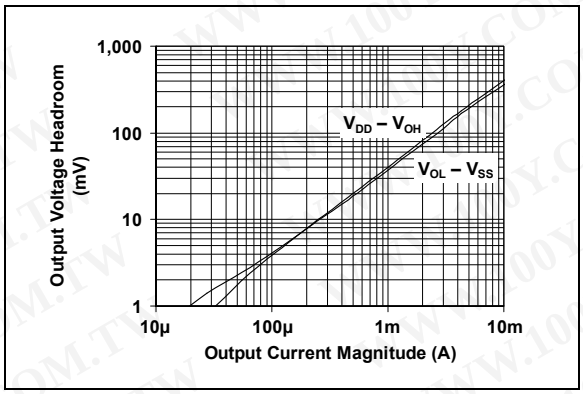


图 2-14： *输出电压裕量—输出电流量级曲线*

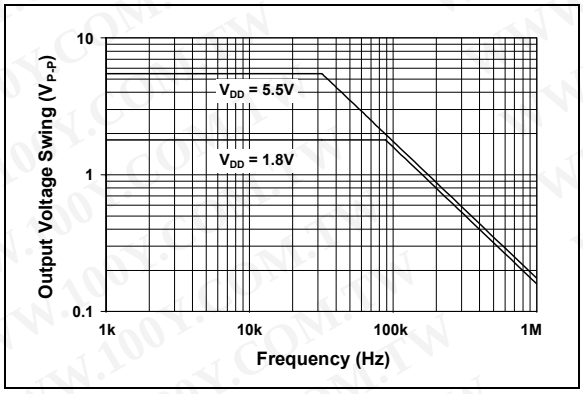


图 2-15： *输出电压摆幅—频率曲线*

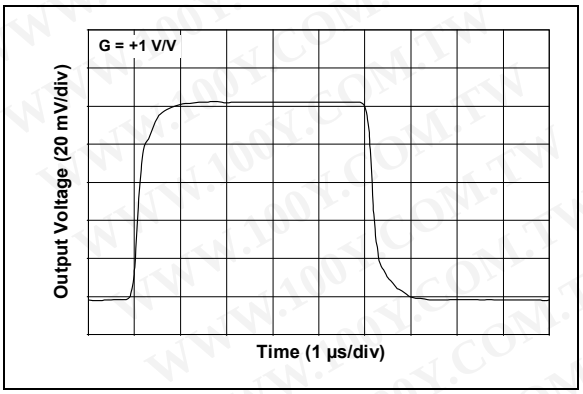


图 2-16： *小信号同相脉冲响应*

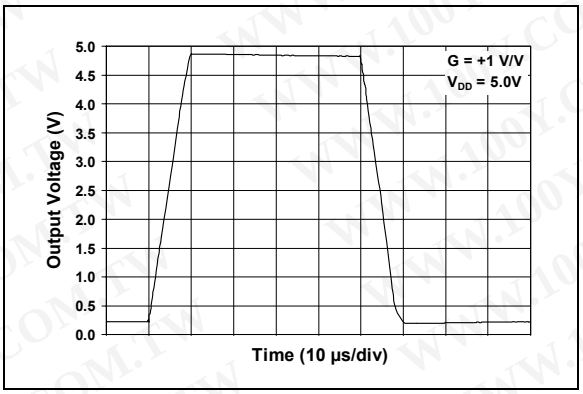


图 2-17： *大信号同相脉冲响应*

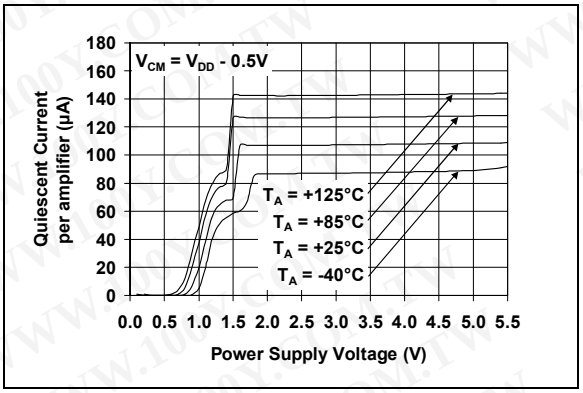


图 2-18： *静态电流—电源电压曲线*

3.0 引脚说明

表 3-1 描述了引脚功能。

表 3-1： 引脚功能表

MCP6001	MCP6001R	MCP6001U	MCP6002	MCP6004	符号	说明
1	1	4	1	1	V_{OUT}, V_{OUTA}	模拟输出 （运放 A）
4	4	3	2	2	$V_{IN}-$, $V_{INA}-$	反相输入 （运放 A）
3	3	1	3	3	$V_{IN}+$, $V_{INA}+$	同相输入 （运放 A）
5	2	5	8	4	V_{DD}	电源正极
—	—	—	5	5	$V_{INB}+$	同相输入 （运放 B）
—	—	—	6	6	$V_{INB}-$	反相输入 （运放 B）
—	—	—	7	7	V_{OUTB}	模拟输出 （运放 B）
—	—	—	—	8	V_{OUTC}	模拟输出 （运放 C）
—	—	—	—	9	$V_{INC}-$	反相输入 （运放 C）
—	—	—	—	10	$V_{INC}+$	同相输入 （运放 C）
2	5	2	4	11	V_{SS}	电源负极
—	—	—	—	12	$V_{IND}+$	同相输入 （运放 D）
—	—	—	—	13	$V_{IND}-$	反相输入 （运放 D）
—	—	—	—	14	V_{OUTD}	模拟输出 （运放 D）

3.1 模拟输出

输出引脚是低阻抗电压源。

3.2 模拟输入

同相和反相输入引脚都是高阻抗CMOS输入，偏置电流较小。

3.3 电源 （V_{SS} 和 V_{DD}）

电源正极（V_{DD}）的电压比电源负极（V_{SS}）高 1.8V 至 5.5V。正常工作时，其它引脚的电压在V_{SS}和V_{DD}之间。

通常，该系列器件都在单 （正极）电源下工作。此时，V_{SS}接地，V_{DD}接电源。V_{DD}需要在靠近其引脚2 mm内的位置连接一个旁路电容 （一般 0.01 µF 至 0.1 µF）。该系列器件可以在靠近V_{DD}引脚100 mm内的位置连接一个大电容（一般 2.2 µF 至 10 µF），并与其它模拟元件共用这个电容。

4.0 应用信息

MCP6001/2/4 系列运放采用 Microchip 公司先进的 CMOS 工艺设计进行生产，专门为低成本、低功耗和各种通用应用设计的。低供电电压、低静态电流和高带宽使 MCP6001/2/4 成为电池供电应用的理想选择。该器件具有高相位容限，这也使得它适用于大容量的容性负载应用中。

4.1 轨到轨输入

MCP6001/2/4 运放设计为当输入引脚电压超过供电电压时，运放会防止相位反转。图 4-1 显示当输入电压超过供电电压时，没有出现任何相位反转。

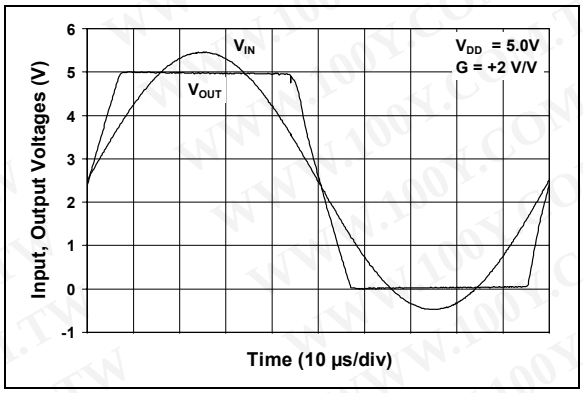


图 4-1： *MCP6001/2/4 显示没有相位反转*

MCP6001/2/4 运放在输入级上采用了二个并联的差分输入级；一个工作在低共模输入电压（V_{CM}），另一个工作在高 V_{CM}。采用这种拓扑，该器件可以在 V_{CM} 为 V_{DD} + 300 mV 和 V_{SS} - 300 mV 的范围内工作。通过测量当 V_{CM} = V_{SS} - 300 mV 和 V_{DD} + 300 mV 时的输入失调电压，来确保该器件正常工作。

超过输入电压范围的输入电压（在 25°C 时 V_{SS} - 0.3V 至 V_{DD} + 0.3V）会引起过量的电流流入或流出输入引脚。超出 ±2 mA 的电流会影响器件的可靠性。超过这个额定值的应用必须外接一个电阻来限制输入电流，如图 4-2 所示。

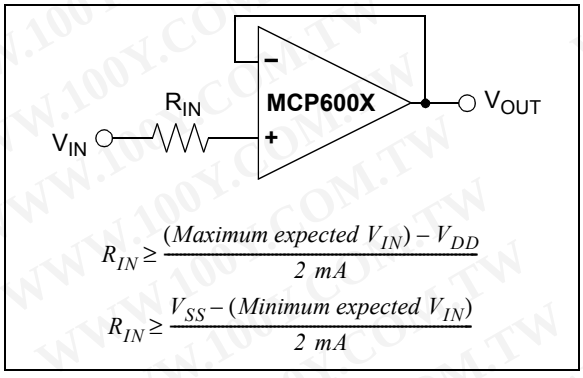


图 4-2： *输入限制电流电阻（R_{IN}）*

4.2 轨到轨输出

当R_L = 10 kΩ连接至V_{DD}/2且V_{DD} = 5.5V时，MCP6001/2/4 运放的输出电压范围是 V_{DD} - 25 mV（最小值）和 V_{SS} + 25 mV（最大值）。请参阅图 2-14，获取更多信息。

4.3 容性负载

对于电压反馈运放来说，驱动大容量容性负载会导致稳定性问题。当容性负载增大时，反馈回路的相位容限会减小，并且闭环带宽也会变窄。这会使得频率响应的增益产生尖峰，并在阶跃响应中产生过冲和振荡。单位增益缓冲器（G = +1）对容性负载最为敏感，但是所有的增益都有同样的表现。

当用这些运放来驱动大容量的容性负载（如，当 G = +1 时，容性负载电容 > 100 pF）时，在输出端串联一个小电阻（图 4-3 中的 R_{ISO}）能使输出负载在高频时呈现阻抗，从而改善反馈回路的相位容限（稳定性）。然而，其带宽一般比没有容性负载的带宽窄。

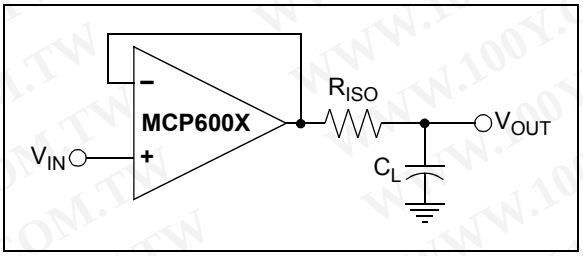


图 4-3： *输出电阻 R_{ISO} 稳定大容量容性负载*

图 4-4 给出了对于不同容性负载和增益， R_{ISO} 的推荐值。 x 轴为归一化容性负载（C_L/G_N），其中 G_N 是电路的噪声增益。对于同相增益， G_N 等于信号增益。而对于反相增益， G_N 为 1+| 信号增益 |（例如：信号增益为 -1 V/V，则 G_N = +2 V/V）。

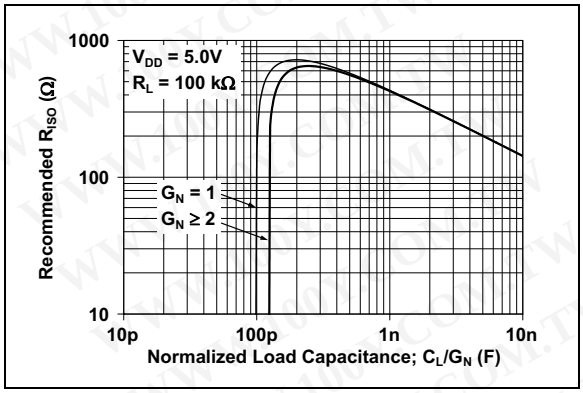


图 4-4： *容性负载的 R_{ISO} 推荐值*

为您的应用选择了 R_{ISO} 后，再次查看产生的频率响应峰值和阶跃响应的过冲。对 R_{ISO} 的值进行适当地修正，直到获得合理的响应。可以利用 MCP6001/2/4 SPICE 宏模型来进行基准评估和模拟。

4.4 电源旁路

在使用这个系列运算放大器时，电源引脚（单电源供电时的 V_{DD}）上应该接一个旁路电容（0.01 µF 至 0.1 µF），连接位置距电源引脚 2 mm 以内，以获得良好的高频性能。该引脚还需要一个大电容（1 µF 或更大），连接位置距电源引脚 100 mm 以内，用以提供大而缓慢的电流。这个大电容可以和其它模拟元件共用。

4.5 PCB 布线漏电流

对那些必须保证较低输入偏置电流的应用来说，必须考虑印刷电路板 （Printed Circuit Board， PCB）的布线漏电流效应。布线漏电流是由于电路板潮湿、积尘或其它污渍而产生的。在湿度很低的条件下，相邻走线之间的典型阻值为 $10^{12}\Omega$。当压差为 5V 时，会产生 5pA 的电流，这一电流远比 MCP6001/2/4 系列在 +25° C 时的偏置电流 （典型值 1 pA）大。

要减小布线漏电流，最简单的方法是在敏感的引脚（或走线）外围设置保护环。保护环的偏置电压与敏感引脚的偏置电压相同。图 4-5 显示了这种布局的示意图。

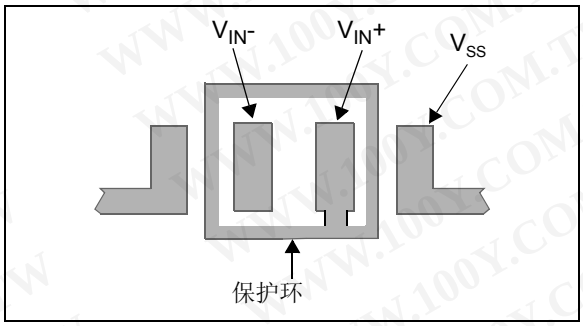


图 4-5： *反相增益时的保护环布局示意图*

1. 同相增益和单位增益缓冲器：
   a. 用一根不和 PCB 布线接触的走线将同相引脚（V_{IN}+）连至输入端。
   b. 将保护环连接到反相输入引脚（V_{IN}–）。这将使保护环偏置为共模输入电压。
2. 对于反相增益和跨阻抗增益放大器（将电流转换为电压的放大器，如光电检测器）：
   a. 将保护环连接到同相输入引脚（V_{IN}+）。这将使保护环偏置为与运放的基准电压（例如 VDD/2 或地）相同的电压。
   b. 用一根不和 PCB 布线接触的走线将反相引脚（V_{IN}–）连至输入端。

4.6 应用电路

4.6.1 单位增益缓冲器

MCP6001/2/4 运放的轨到轨输入输出能力对于单位增益缓冲器的应用来说是非常理想的。该器件的低静态电流和高带宽使它适合作为一个缓冲器配置，应用在一个仪表放大器电路中，如图 4-6 所示。

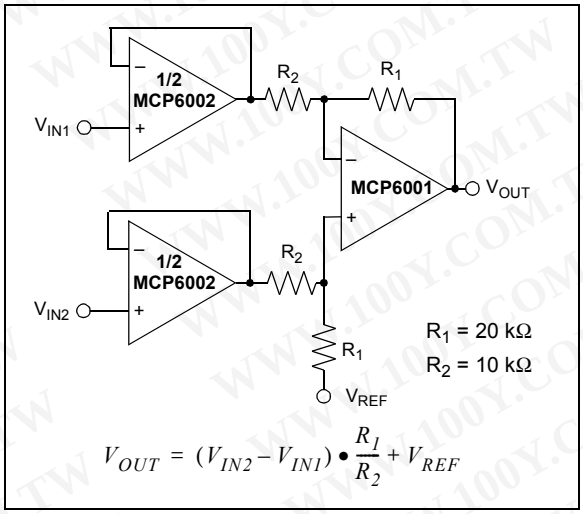


图 4-6： *带有单位增益缓冲器输入的仪表放大器*

4.6.2 有源低通滤波器

MCP6001/2/4 运放的低输入偏置电流使得设计者能用大电阻和小电容来实现有源低通滤波器。然而，随着电阻阻值的增加，由此产生的噪声也会增加。寄生电容和大阻值电阻还会改变频率响应。我们在选择电路元件的时候也需要考虑到这些方面的影响。

通常，运放的带宽大于等于滤波器截止频率的 100 倍时，滤波器的性能会较好。而如果运放的带宽只是滤波器截止频率的10倍，这样的设计对元器件的变化比较敏感。

图 4-7 显示了一个二阶Butterworth滤波器，它的截止频率为 100 kHz，增益为 +1V/V。运放的带宽只是截止频率的 10 倍。各元件值是用 Microchip 的 FilterLab® 软件选定的。

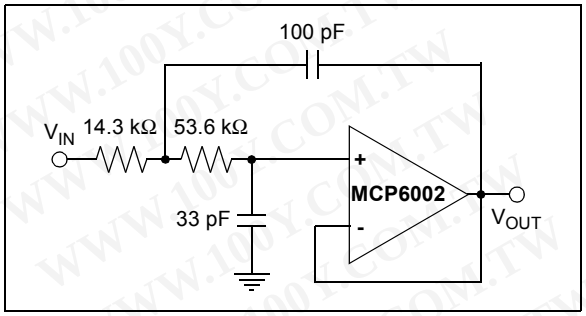


图 4-7： *有源二阶低通滤波器*

4.6.3 峰值检测器

MCP6001/2/4运放具有高输入阻抗、轨到轨输入输出和低偏置输入电流，使得该器件适合应用于峰值检测器。图 4-8显示了一个带有清零和采样开关的峰值检测器电路。峰值检测周期用到了一个时钟 （CLK），如图 4-8 所示。

在 CLK 时钟的上升沿，采样开关闭合开始采样。在定义为 t_{SAMP} 的采样时间里，存储在 C_1 里的峰值电压被采样到 C_2 中。在采样时间结束时（采样信号的下降沿），清零信号变高，清零开关闭合。当清零开关闭合的时候， C_1 在定义为 t_{CLEAR} 的时间内通过 R_1 放电。在清零时间结束时（清零信号的下降沿），运放 A 开始在定义为 t_{DETECT} 的时间内在 C_1 上存储 V_{IN} 的峰值电压。

为了定义 t_{SAMP} 和 t_{CLEAR}，需要决定电容的充放电时间。电容的充电时间受放大器的拉电流限制，而放电时间 （τ）可用 R_1 （$\tau = R_1C_1$）来定义的。 t_{DETECT} 是输入信号通过 C_1 来采样的时间，依赖于输入电压的变化频率。

当输入电压 （V_{IN}）增加时，运放的输出电流限制和存储电容 （C_1 和 C_2）的大小会对转换产生制约。流过电容的电流受制于电容的大小和电压的变化速率。根据这种关系可以决定电压变化速率或转换速率。例如，当运放的短路电流 I_{SC} = 25 mA，负载电容 C_1 = 0.1 µF 时：

公式 4-1：

$$I_{SC} = C_1 \frac{dV_{C1}}{dt}$$

$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$

$$= \frac{25mA}{0.1\mu F}$$

$$\frac{dV_{C1}}{dt} = 250mV/\mu s$$

这个电压变化速率要低于 MCP6001/2/4 的转换速率 0.6 mV/µs。当输入电压摆幅低于 C_1 两端的电压时，D_1 变为反向偏置，使反馈回路变为开路，从而放大器的输出为轨到轨电压。当输入电压增加时，放大器以转换速率得以恢复。基于上面公式中所列出的电压变化速率，放大器需要额外的时间来对 0.1 µF 的电容器充电。选择合适的电容使得电路不受放大器转换速率的限制。因此，电容应该低于 40 µF，而且稳定电阻（R_{ISO}）也需要合理选择。（参见 **4.3 节 “容性负载”**。）

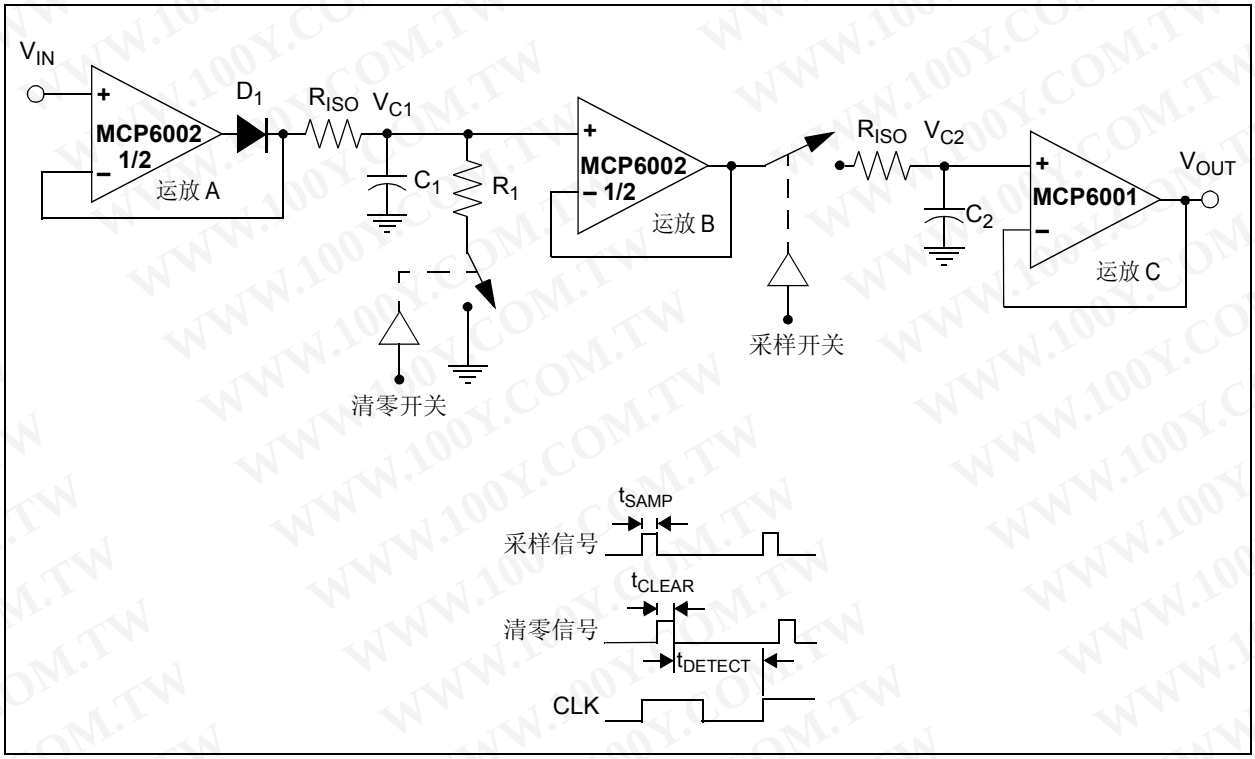


图 4-8： *带有清零和采样 CMOS 模拟开关的峰值检测器*

5.0 设计工具

Microchip 公司提供 MCP6001/2/4 系列运放的基本设计工具。

5.1 SPICE 宏模型

Microchip 公司的网站 www.microchip.com 提供了最新的 MCP6001/2/4 运算放大器的 SPICE 宏模型 。该模型为初始设计工具，在室温条件下和运放运行的线性区内表现最佳。参见模型文件，可以了解更多有关 SPICE 模型的信息。

基准测试是任何设计中极为重要的一个环节，不能用仿真替代。而且，利用此宏模型得到的仿真结果应与数据手册上的技术参数和特性曲线相比较并进行验证。

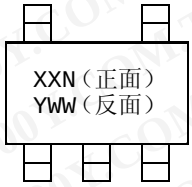
5.2 FilterLab® 软件

Microchip 公司的 FilterLab® 软件是一种创新的工具软件，它大大简化了采用运放的模拟有源滤波器的设计。Microchip 网站 www.microchip.com 上提供了免费的 FilterLab 有源滤波器设计软件，这一软件为您提供完整的滤波器电路原理图，并注明了元件值。该工具软件还可输出 SPICE 格式的滤波器电路，结合宏模型可以仿真实际的滤波器性能。

6.0 封装信息

6.1 封装标识信息

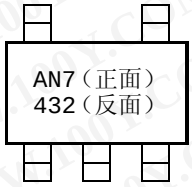
5 引脚 SC-70（**MCP6001**）



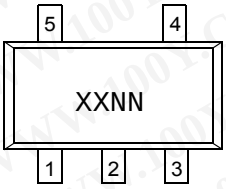
器件	工业级温度编码	扩展级温度编码
MCP6001	ANN	CDN

注： 适用于 5 引脚 SC-70 封装。

示例：（工业级温度）



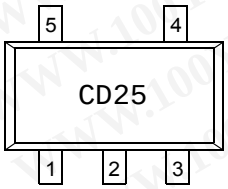
5 引脚 SOT-23（**MCP6001/1R/1U**）



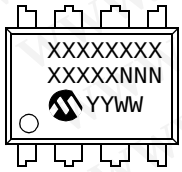
器件	工业级温度编码	扩展级温度编码
MCP6001	AANN	CDNN
MCP6001R	ADNN	CENN
MCP6001U	AFNN	CFNN

注： 适用于5引脚SOT-23封装。

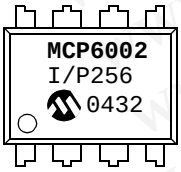
示例：（扩展级温度）



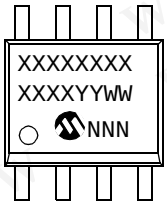
8 引脚 PDIP （300 mil）



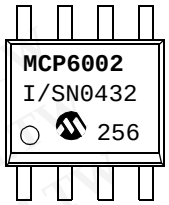
示例：



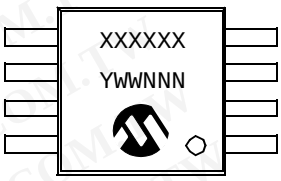
8 引脚 SOIC（150 mil）



示例：



8 引脚 MSOP



示例：

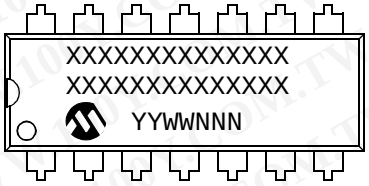
图注：	XX...X	客户信息 *
	YY	年份代码 （日历年的最后两位数字）
	WW	星期代码 （一月一日的星期代码为 “01”）
	NNN	以字母数字排列的追踪代码

注： Microchip 元器件编号若无法在同一行内完整标注，将换行标出，因此会限制客户信息的可用字符数。

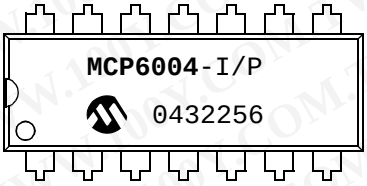
* 标准标识包括 Microchip 器件编号、年份代码、星期代码和追踪代码（工厂编码、掩膜版本和组装编码）。若器件标识超过这些内容，须额外支付一定的费用。请向当地的 Microchip 销售办事处了解确认。

封装标识信息（续）

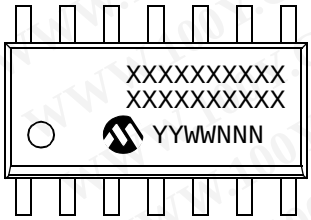
14 引脚 PDIP（300 mil）（**MCP6004**）



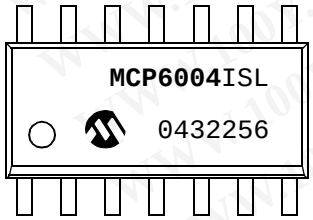
示例：



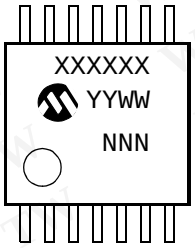
14 引脚 SOIC（150 mil）（**MCP6004**）



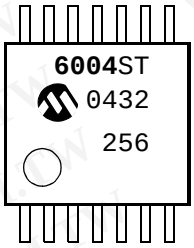
示例：



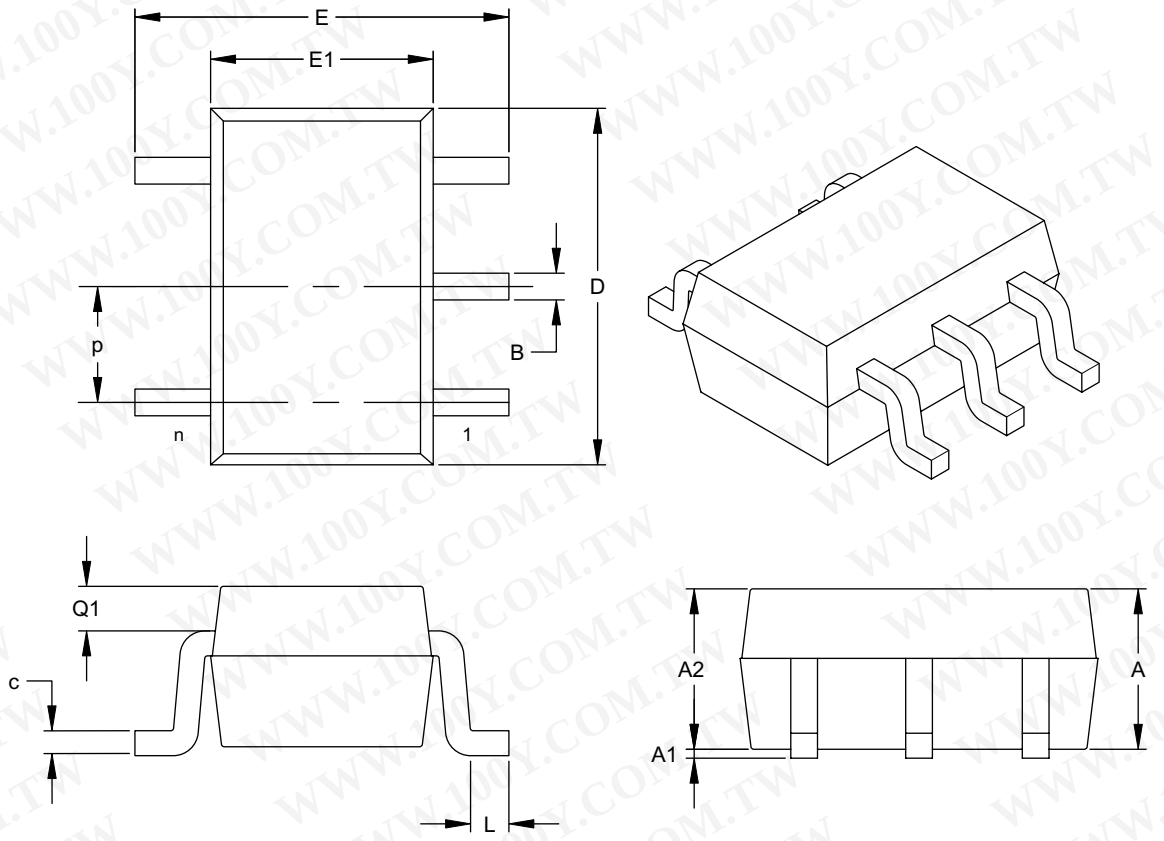
14 引脚 TSSOP（**MCP6004**）



示例：



5 引脚塑料封装 （SC-70）



	单位	英寸			毫米*		
	尺寸范围	最小	正常	最大	最小	正常	最大
引脚数	n		5			5	
引脚间距	p		.026 (BSC)			0.65 (BSC)	
总高度	A	.031		.043	0.80		1.10
塑模封装厚度	A2	.031		.039	0.80		1.00
悬空间隙	A1	.000		.004	0.00		0.10
总宽度	E	.071		.094	1.80		2.40
塑模封装宽度	E1	.045		.053	1.15		1.35
总长度	D	.071		.087	1.80		2.20
底脚长度	L	.004		.012	0.10		0.30
塑模顶部到引脚肩部的高度	Q1	.004		.016	0.10		0.40
引脚厚度	c	.004		.007	0.10		0.18
引脚宽度	B	.006		.012	0.15		0.30

*控制参数

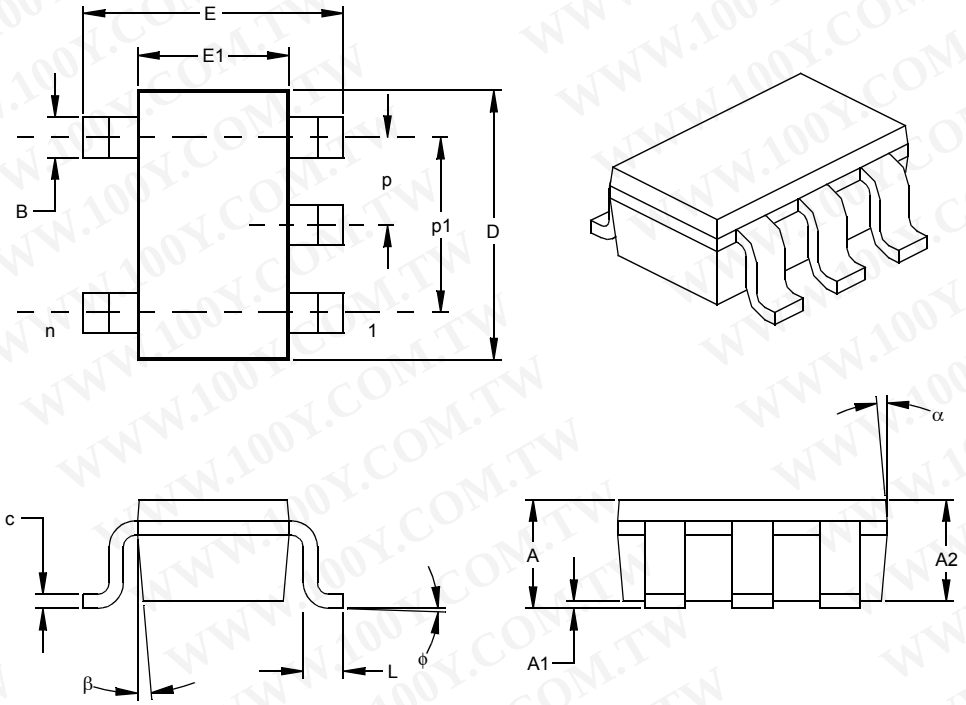
注：

尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.005英寸（0.127毫米）。

JEITA（EIAJ）标准：SC-70

图号 C04-061

5 引脚小型塑料晶体管封装 （OT）（SOT23）

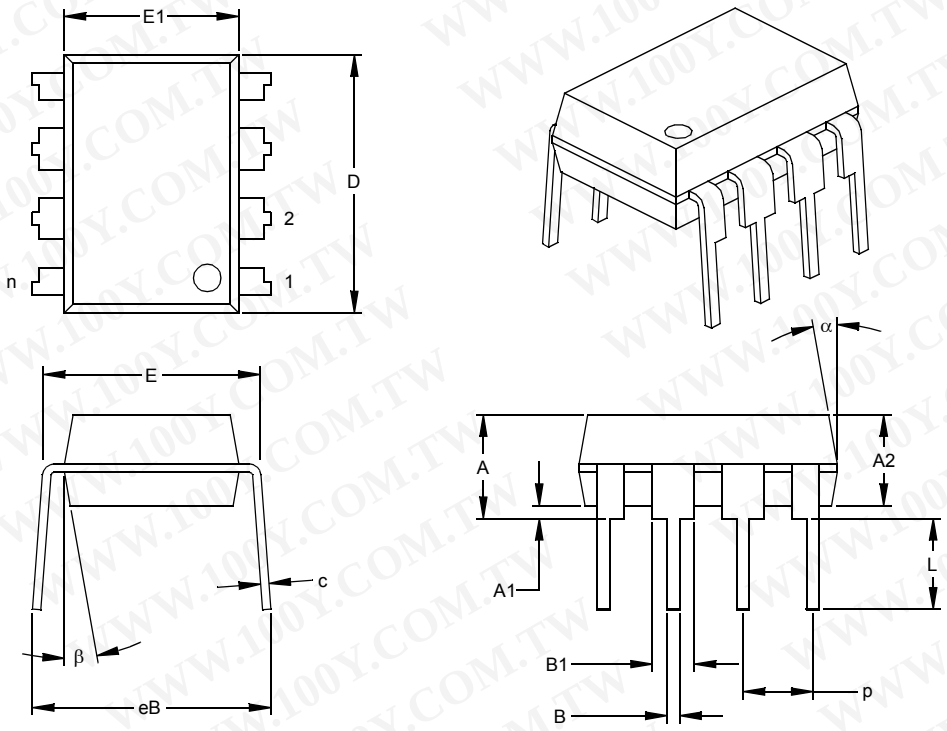


	单位	英寸 *			毫米		
	尺寸范围	最小	正常	最大	最小	正常	最大
引脚数	n		5			5	
引脚间距	p		.038			0.95	
外侧引脚间距（基本）	p1		.075			1.90	
总高度	A	.035	.046	.057	0.90	1.18	1.45
塑模封装厚度	A2	.035	.043	.051	0.90	1.10	1.30
悬空间隙 §	A1	.000	.003	.006	0.00	0.08	0.15
总宽度	E	.102	.110	.118	2.60	2.80	3.00
塑模封装宽度	E1	.059	.064	.069	1.50	1.63	1.75
总长度	D	.110	.116	.122	2.80	2.95	3.10
底脚长度	L	.014	.018	.022	0.35	0.45	0.55
底脚倾斜角	ϕ	0	5	10	0	5	10
引脚厚度	c	.004	.006	.008	0.09	0.15	0.20
引脚宽度	B	.014	.017	.020	0.35	0.43	0.50
塑模顶部锥度	α	0	5	10	0	5	10
塑模底部锥度	β	0	5	10	0	5	10

* 控制参数
§ 重要特性

注：
尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.010 英寸（0.254 毫米）。
等同于 JEDEC 号：MS-178
图号 C04-091

8 引脚塑料双列直插封装 （P） – 300 mil （PDIP）

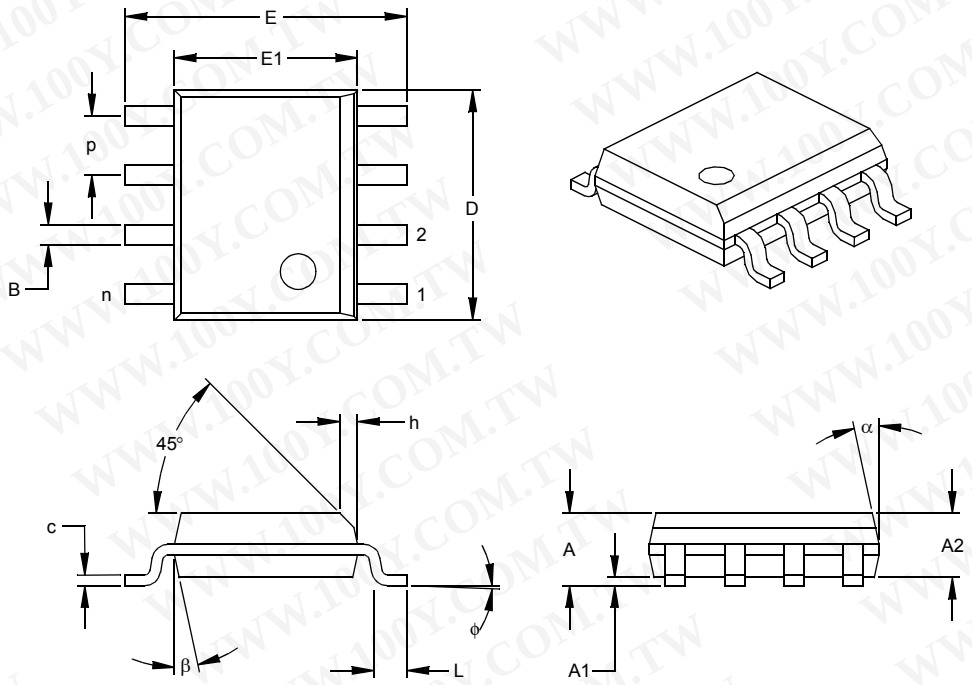


	单位	英寸 *			毫米		
	尺寸范围	最小	正常	最大	最小	正常	最大
引脚数	n		8			8	
引脚间距	p		.100			2.54	
顶端到固定面高度	A	.140	.155	.170	3.56	3.94	4.32
塑模封装厚度	A2	.115	.130	.145	2.92	3.30	3.68
塑模底端到固定面高度	A1	.015			0.38		
肩到肩宽度	E	.300	.313	.325	7.62	7.94	8.26
塑模封装宽度	E1	.240	.250	.260	6.10	6.35	6.60
总长度	D	.360	.373	.385	9.14	9.46	9.78
引脚尖到固定面高度	L	.125	.130	.135	3.18	3.30	3.43
引脚厚度	c	.008	.012	.015	0.20	0.29	0.38
引脚上部宽度	B1	.045	.058	.070	1.14	1.46	1.78
引脚下部宽度	B	.014	.018	.022	0.36	0.46	0.56
总排列距离 §	eB	.310	.370	.430	7.87	9.40	10.92
塑模顶部锥度	α	5	10	15	5	10	15
塑模底部锥度	β	5	10	15	5	10	15

* 控制参数
§ 重要特性

注：
尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.010 英寸（0.254 毫米）。
等同于 JEDEC 号：MS-001
图号 C04-018

8 引脚小型塑料封装 （SN） – 窄条形， 150 mil （SOIC）

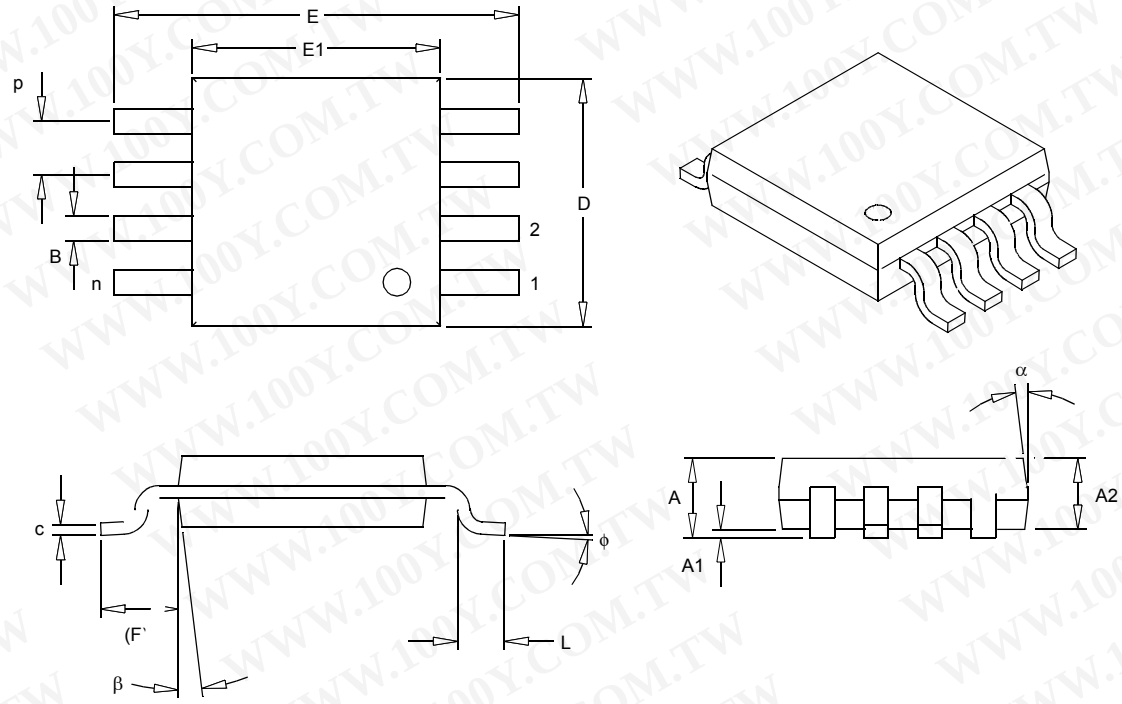


	单位	英寸 *			毫米		
	尺寸范围	最小	正常	最大	最小	正常	最大
引脚数	n		8			8	
引脚间距	p		.050			1.27	
总高度	A	.053	.061	.069	1.35	1.55	1.75
塑模封装厚度	A2	.052	.056	.061	1.32	1.42	1.55
悬空间隙 §	A1	.004	.007	.010	0.10	0.18	0.25
总宽度	E	.228	.237	.244	5.79	6.02	6.20
塑模封装宽度	E1	.146	.154	.157	3.71	3.91	3.99
总长度	D	.189	.193	.197	4.80	4.90	5.00
斜面投影距离	h	.010	.015	.020	0.25	0.38	0.51
底脚长度	L	.019	.025	.030	0.48	0.62	0.76
底脚倾斜角	ϕ	0	4	8	0	4	8
引脚厚度	c	.008	.009	.010	0.20	0.23	0.25
引脚宽度	B	.013	.017	.020	0.33	0.42	0.51
塑模顶部锥度	α	0	12	15	0	12	15
塑模底部锥度	β	0	12	15	0	12	15

* 控制参数
§ 重要特性

注：
尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.010 英寸（0.254 毫米）。
等同于 JEDEC 号：MS-012
图号 C04-057

8 引脚塑料微型封装 （MS）（MSOP）



单位		英寸			毫米 *		
尺寸范围		最小	正常	最大	最小	正常	最大
引脚数	n		8			8	
引脚间距	p		.026 BSC			0.65 BSC	
总高度	A	–	–	.043	–	–	1.10
塑模封装厚度	A2	.030	.033	.037	0.75	0.85	0.95
悬空间隙	A1	.000	–	.006	0.00	–	0.15
总宽度	E		.193 TYP			4.90 BSC	
塑模封装宽度	E1		.118 BSC			3.00 BSC	
总长度	D		.118 BSC			3.00 BSC	
底脚长度	L	.016	.024	.031	0.40	0.60	080
底脚占位（参考）	F		.037 REF			0.95 REF	
底脚倾斜角	φ	0	–	8	0	–	8
引脚厚度	c	.003	.006	.009	0.08	–	0.23
引脚宽度	B	.009	.012	.016	0.22	–	0.40
塑模顶部锥度	α	5	–	15	5	–	15
塑模底部锥度	β	5	–	15	5	–	15

* 控制参数

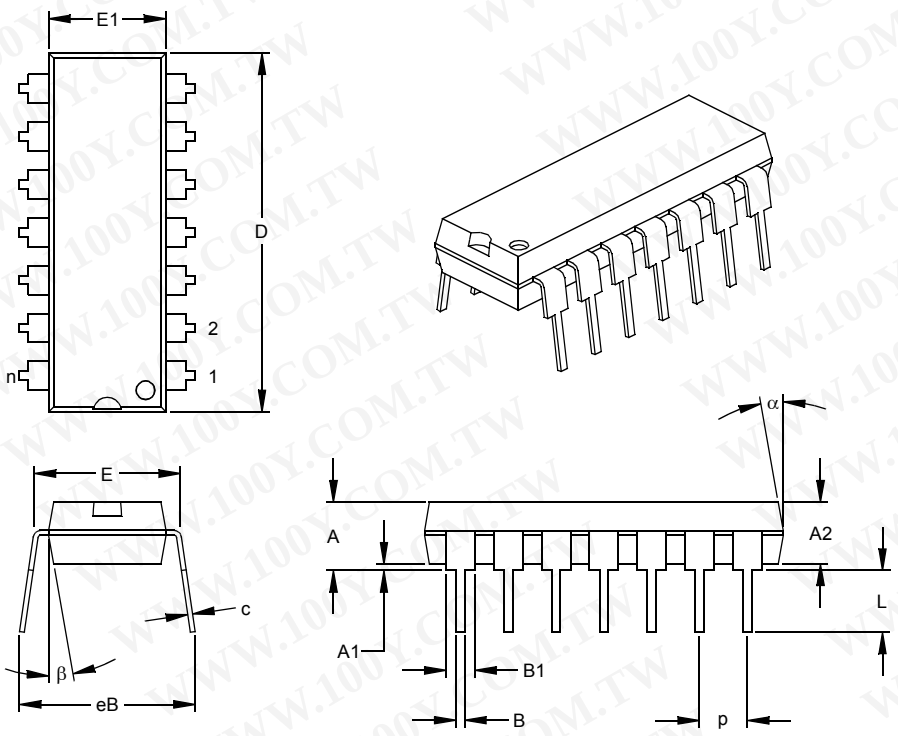
注：

尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.010 英寸（0.254 毫米）。

等同于 JEDEC 号: MO-187

图号 C04-111

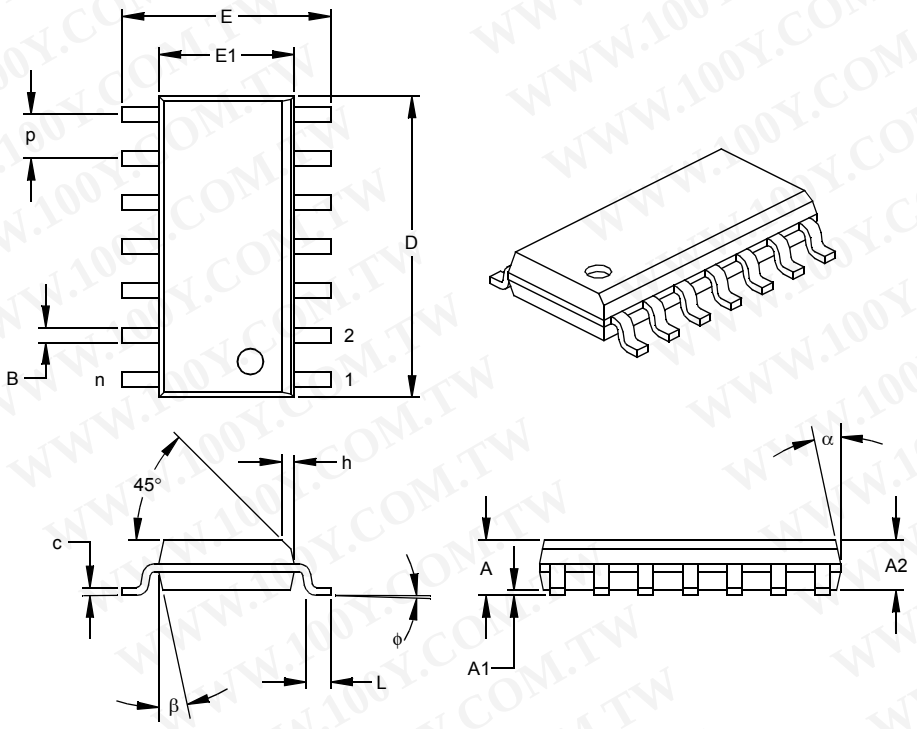
14 引脚塑料双列直插封装 （P） – 300 mil （PDIP）



单位		英寸 *			毫米		
尺寸范围		最小	正常	最大	最小	正常	最大
引脚数	n		14			14	
引脚间距	p		.100			2.54	
顶端到固定面高度	A	.140	.155	.170	3.56	3.94	4.32
塑模封装厚度	A2	.115	.130	.145	2.92	3.30	3.68
塑模底端到固定面高度	A1	.015			0.38		
肩到肩宽度	E	.300	.313	.325	7.62	7.94	8.26
塑模封装宽度	E1	.240	.250	.260	6.10	6.35	6.60
塑模封装长度	D	.740	.750	.760	18.80	19.05	19.30
引脚尖到固定面高度	L	.125	.130	.135	3.18	3.30	3.43
引脚厚度	c	.008	.012	.015	0.20	0.29	0.38
引脚上部宽度	B1	.045	.058	.070	1.14	1.46	1.78
引脚下部宽度	B	.014	.018	.022	0.36	0.46	0.56
总排列距离 §	eB	.310	.370	.430	7.87	9.40	10.92
塑模顶部锥度	α	5	10	15	5	10	15
塑模底部锥度	β	5	10	15	5	10	15

* 控制参数
§ 重要特性
注：
尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.010 英寸（0.254 毫米）。
等同于 JEDEC 号：MS-001
图号 C04-005

14 引脚塑料小型封装 （SL） – 窄条形， 150 mil （SOIC）

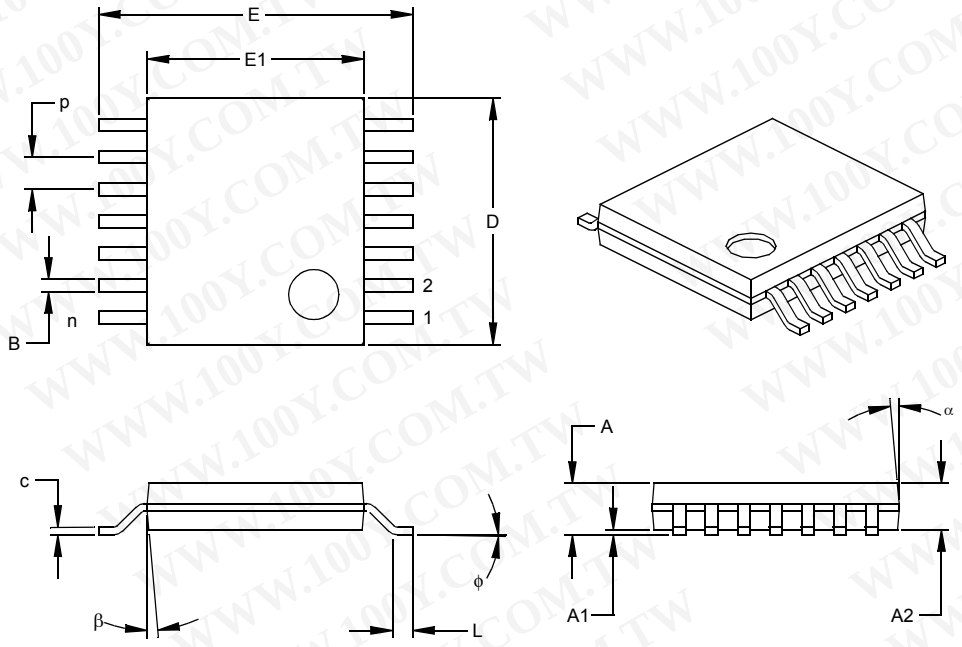


	单位	英寸 *			毫米		
	尺寸范围	最小	正常	最大	最小	正常	最大
引脚数	n		14			14	
引脚间距	p		.050			1.27	
总高度	A	.053	.061	.069	1.35	1.55	1.75
塑模封装厚度	A2	.052	.056	.061	1.32	1.42	1.55
悬空间隙 §	A1	.004	.007	.010	0.10	0.18	0.25
总宽度	E	.228	.236	.244	5.79	5.99	6.20
塑模封装宽度	E1	.150	.154	.157	3.81	3.90	3.99
总长度	D	.337	.342	.347	8.56	8.69	8.81
斜面投影距离	h	.010	.015	.020	0.25	0.38	0.51
底脚长度	L	.016	.033	.050	0.41	0.84	1.27
底脚倾斜角	φ	0	4	8	0	4	8
引脚厚度	c	.008	.009	.010	0.20	0.23	0.25
引脚宽度	B	.014	.017	.020	0.36	0.42	0.51
塑模顶部锥度	α	0	12	15	0	12	15
塑模底部锥度	β	0	12	15	0	12	15

* 控制参数
§ 重要特性

注：
尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.010 英寸（0.254 毫米）。
等同于 JEDEC 号： MS-012
图号 C04-065

14 引脚塑料薄形小型封装 （ST） – 4.4 mm （TSSOP）



	单位	英寸			毫米 *		
	尺寸范围	最小	正常	最大	最小	正常	最大
引脚数	n		14			14	
引脚间距	p		.026			0.65	
总高度	A			.043			1.10
塑模封装厚度	A2	.033	.035	.037	0.85	0.90	0.95
悬空间隙 §	A1	.002	.004	.006	0.05	0.10	0.15
总宽度	E	.246	.251	.256	6.25	6.38	6.50
塑模封装宽度	E1	.169	.173	.177	4.30	4.40	4.50
塑模封装长度	D	.193	.197	.201	4.90	5.00	5.10
底脚长度	L	.020	.024	.028	0.50	0.60	0.70
底脚倾斜角	φ	0	4	8	0	4	8
引脚厚度	c	.004	.006	.008	0.09	0.15	0.20
引脚宽度	B1	.007	.010	.012	0.19	0.25	0.30
塑模顶部锥度	α	0	5	10	0	5	10
塑模底部锥度	β	0	5	10	0	5	10

* 控制参数
§ 重要特性

注：
尺寸 D 和 E1 不包括塑模毛边或突起。每侧的塑模毛边或突起不得超过 0.005 英寸（0.127 毫米）。
等同于 JEDEC 号： MO-153
图号 C04-087

附录 A： 版本历史

版本 A （2002 年 6 月）

此数据手册的第一版。

版本 B （2002 年 10 月）

版本 C （2002 年 12 月）

版本 D （2003 年 5 月）

版本 E （2004 年 12 月）

进行了以下变更：

1. 日期代码在 YYWW = 0449 以后的器件，其 V_{OS} 的技术规范从 ±7.0 mV 改为 ±4.5 mV
2. 修改了 **6.0 节 “封装信息”** 中的封装标识
3. 增加了附录 A：版本历史。

产品标识体系

欲订货，或获取价格、交货等信息，请与我公司生产厂或各销售办事处联系。

器件编号	X	/XX
器件	温度范围	封装

器件：	MCP6001T：	单运放（卷带式包装）（SC-70， SOT-23）
	MCP6001RT：	单运放（卷带式包装）（SOT-23）
	MCP6001UT：	单运放（卷带式包装）（SOT-23）
	MCP6002：	双运放
	MCP6002T：	双运放（卷带式包装）（SOIC， MSOP）
	MCP6004：	四运放
	MCP6004T：	四运放（卷带式包装）（SOIC，MSOP）
温度范围：	I =	表示 -40°C 至 +85°C
	E =	表示 -40°C 至 +125°C
封装：	LT =	表示塑料封装（SC-70），5 引脚（仅限 MCP6001）
	OT =	表示塑料小型晶体管（SOT-23），5 引脚（MCP6001，MCP6001R，MCP6001U）
	MS =	表示塑料 MSOP，8 引脚
	P =	表示塑料 DIP（主体 300 mil），8 引脚，14 引脚
	SN =	表示塑料 SOIC（主体 150 mil），8 引脚
	SL =	表示塑料 SOIC（主体 150 mil），14 引脚
	ST =	表示塑料 TSSOP（主体 4.4mm），14 引脚

示例：

a) MCP6001T-I/LT： 卷带式，工业级温度范围， 5 引脚 SC-70 封装。
b) MCP6001T-I/OT：卷带式，工业级温度范围，5 引脚 SOT-23 封装。
c) MCP6001RT-I/OT： 卷带式，工业级温度范围，5 引脚 SOT-23 封装。
d) MCP6001UT-E/OT： 卷带式，扩展级温度范围， 5 引脚 SOT-23 封装。
e) MCP6001UT-I/OT： 卷带式，工业级温度范围，5 引脚 SOT-23 封装。

a) MCP6002-I/MS： 工业级温度范围， 8 引脚 MSOP 封装。
b) MCP6002-I/P： 工业级温度范围，8 引脚 PDIP 封装。
c) MCP6002-E/P： 扩展级温度范围， 8 引脚 PDIP 封装。
d) MCP6002-I/SN： 工业级温度范围， 8 引脚 SOIC 封装。
e) MCP6002T-I/MS：卷带式，工业级温度范围， 8 引脚 MSOP 封装。
f) MCP6002T-I/SN：卷带式，工业级温度范围， 8 引脚 SOIC 封装。

a) MCP6004-I/P： 工业级温度范围， 14 引脚 PDIP 封装。
b) MCP6004-I/SL： 工业级温度范围， 14 引脚 SOIC 封装。
c) MCP6004-E/SL： 扩展级温度范围，14 引脚 SOIC 封装。
d) MCP6004-I/ST： 工业级温度范围， 14 引脚 TSSOP 封装。
e) MCP6004T-I/SL： 卷带式，工业级温度范围， 14 引脚 SOIC 封装。
f) MCP6004T-I/ST： 卷带式，工业级温度范围， 14 引脚 TSSOP 封装。

MCP6001/1R/1U/2/4

1 MHz, Low-Power Op Amp

Features

- Available in SC-70-5 and SOT-23-5 packages
- Gain Bandwidth Product: 1 MHz (typical)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 6.0V
- Supply Current: I_Q = 100 µA (typical)
- Phase Margin: 90° (typical)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Available in Single, Dual and Quad Packages

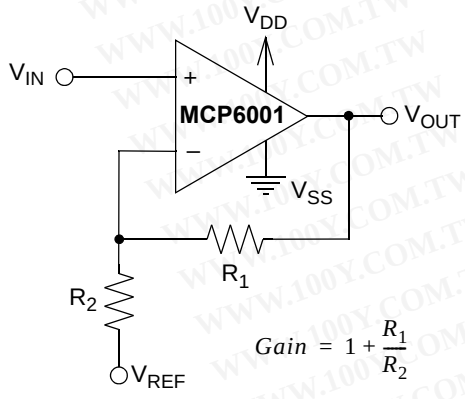
Applications

- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



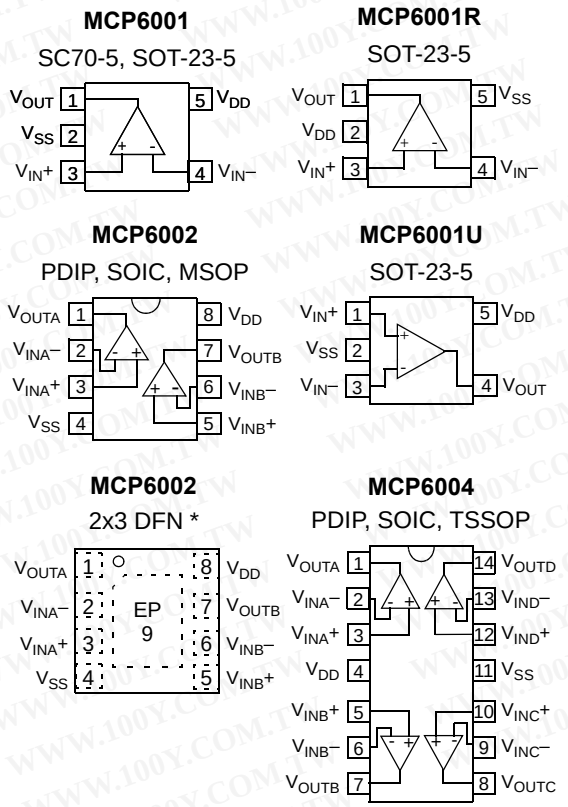
Non-Inverting Amplifier

Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typical). It also maintains 45° phase margin (typical) with a 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100 µA (typical) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 6.0V.

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Analog Input Pins ($V_{IN}+$, $V_{IN}-$).....±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$) †† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....–65°C to +150°C
Maximum Junction Temperature (T_J).....+150°C
ESD Protection On All Pins (HBM; MM) ..... ≥ 4 kV; 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, and $V_{OUT} \approx V_{DD}/2$ (refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV	$V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A= -40°C to +125°C, $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	—	86	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current:	I_B	—	±1.0	—	pA	
Industrial Temperature	I_B	—	19	—	pA	T_A = +85°C
Extended Temperature	I_B	—	1100	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	60	76	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	88	112	—	dB	V_{OUT} = 0.3V to V_{DD} – 0.3V, $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V, 0.5V Input Overdrive
Output Short Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	6.0	V	**Note 2**
Quiescent Current per Amplifier	I_Q	50	100	170	µA	I_O = 0, V_{DD} = 5.5V, V_{CM} = 5V

Note 1: MCP6001/1R/1U/2/4 parts with date codes prior to December 2004 (week code 49) were tested to ±7 mV minimum/maximum limits.

2: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD} = 6.0V. However, the other minimum and maximum specifications are measured at 1.8V and 5.5V.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_L = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to V_L, and C_L = 60 pF (refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1 V/V
Slew Rate	SR	—	0.6	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	6.1	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Industrial Temperature Range	T_A	-40	—	+85	°C	
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC (150 mil)	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-DFN (2x3)	θ_{JA}	—	68	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

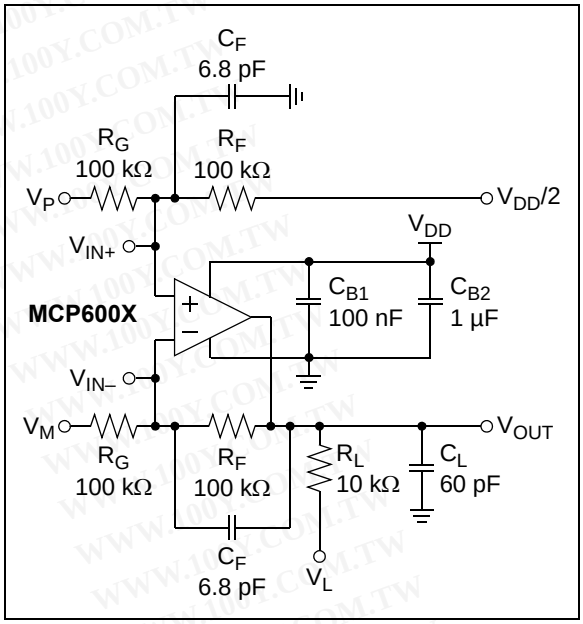


FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L, and C_L = 60 pF.

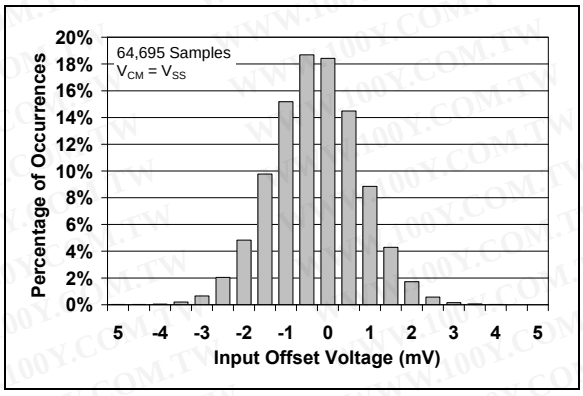


FIGURE 2-1: *Input Offset Voltage.*

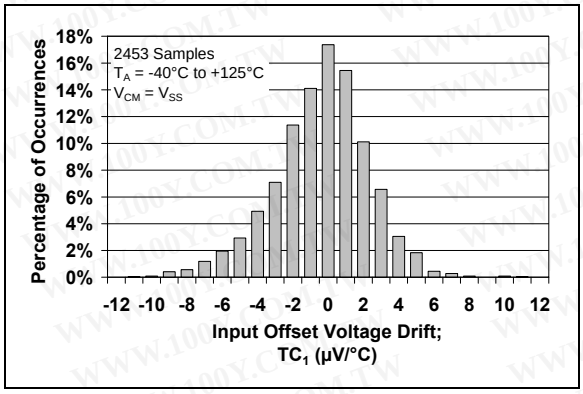


FIGURE 2-2: *Input Offset Voltage Drift.*

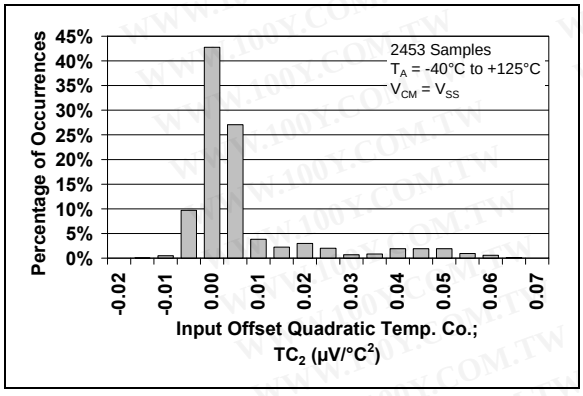


FIGURE 2-3: *Input Offset Quadratic Temp. Co.*

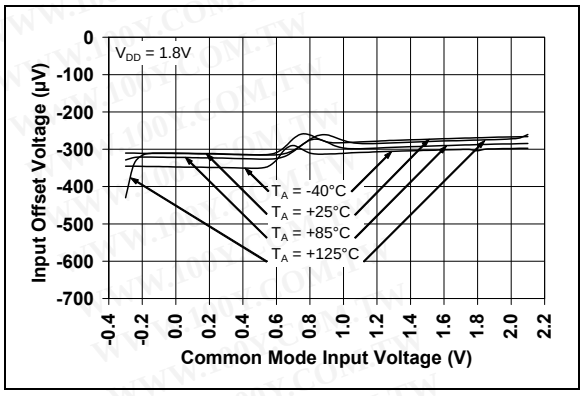


FIGURE 2-4: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 1.8V.*

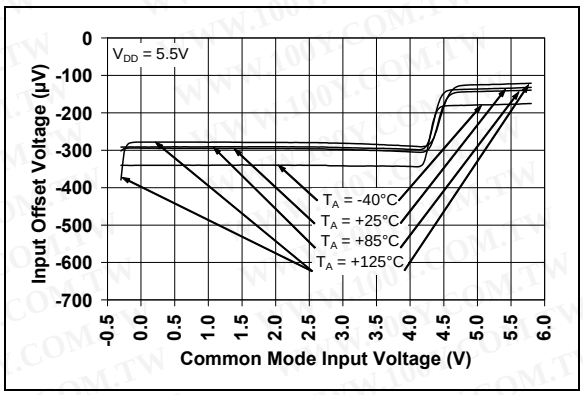


FIGURE 2-5: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

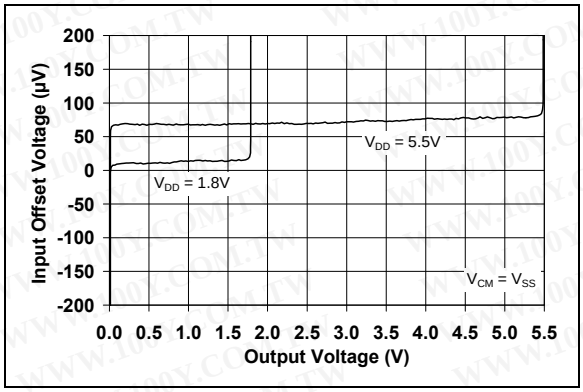


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, and C_L = 60 pF.

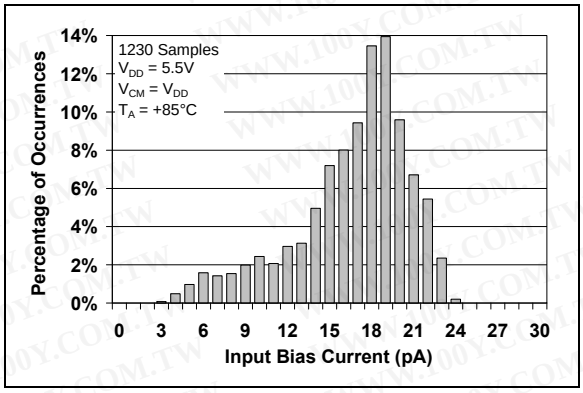


FIGURE 2-7: *Input Bias Current at +85°C.*

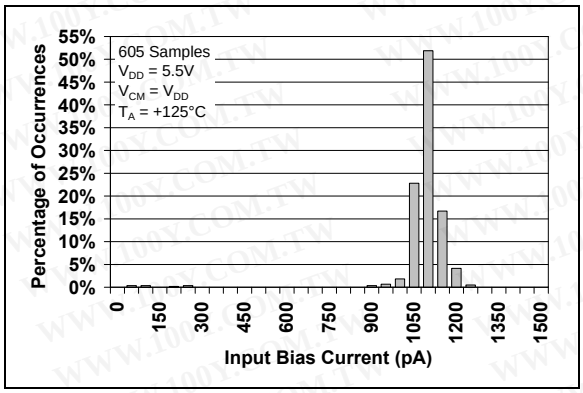


FIGURE 2-8: *Input Bias Current at +125°C.*

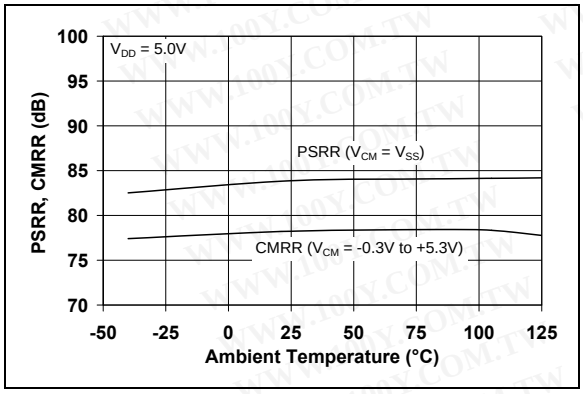


FIGURE 2-9: *CMRR, PSRR vs. Ambient Temperature.*

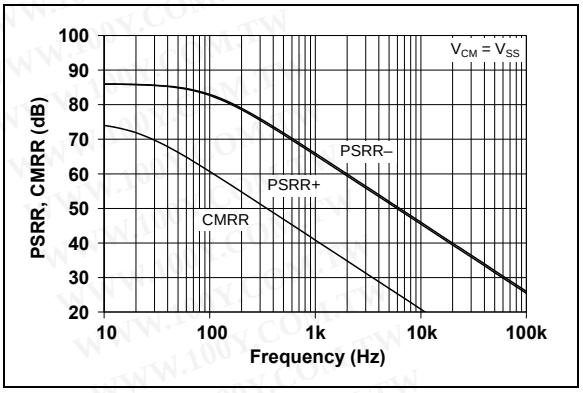


FIGURE 2-10: *PSRR, CMRR vs. Frequency.*

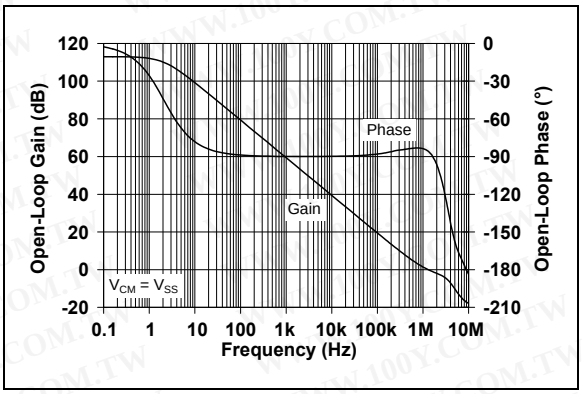


FIGURE 2-11: *Open-Loop Gain, Phase vs. Frequency.*

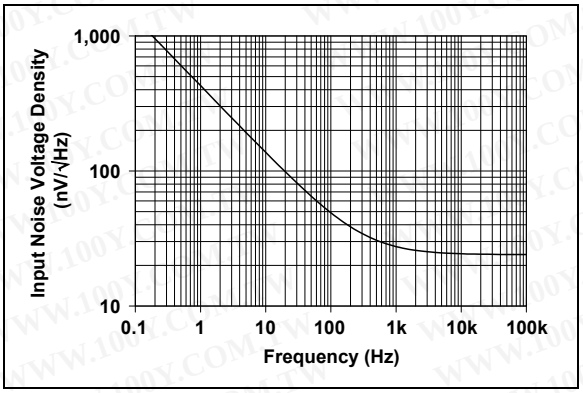


FIGURE 2-12: *Input Noise Voltage Density vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, and C_L = 60 pF.

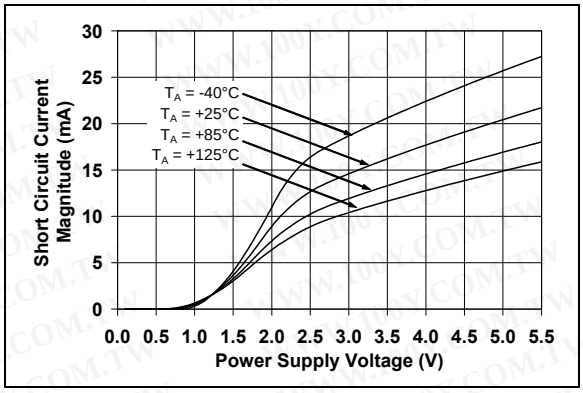


FIGURE 2-13: *Output Short Circuit Current vs. Power Supply Voltage.*

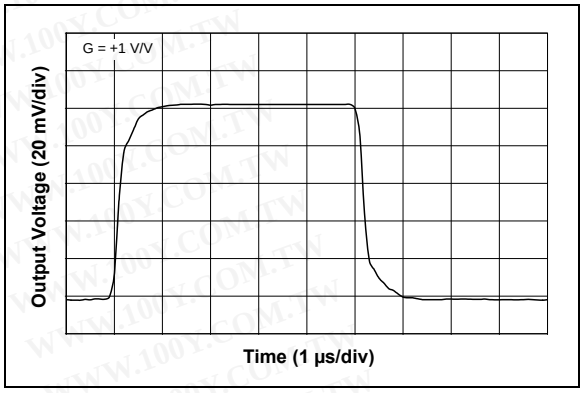


FIGURE 2-16: *Small-Signal, Non-Inverting Pulse Response.*

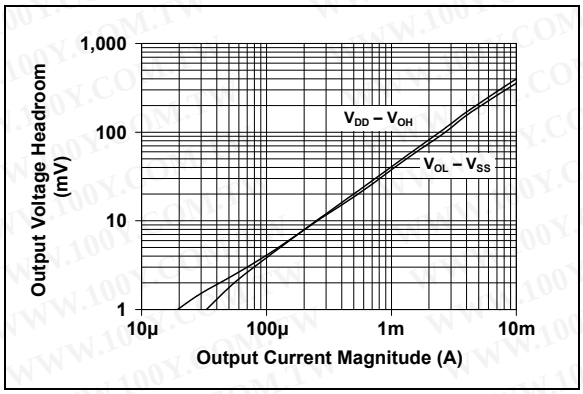


FIGURE 2-14: *Output Voltage Headroom vs. Output Current Magnitude.*

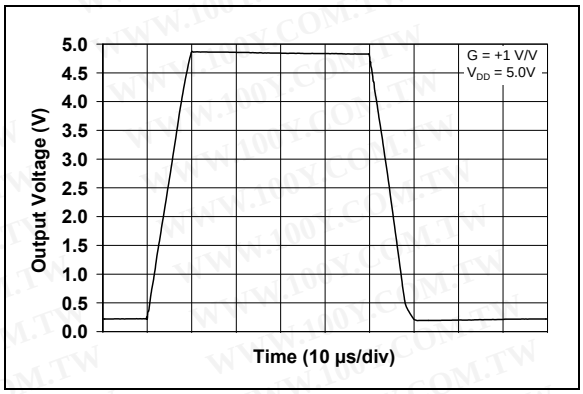


FIGURE 2-17: *Large-Signal, Non-Inverting Pulse Response.*

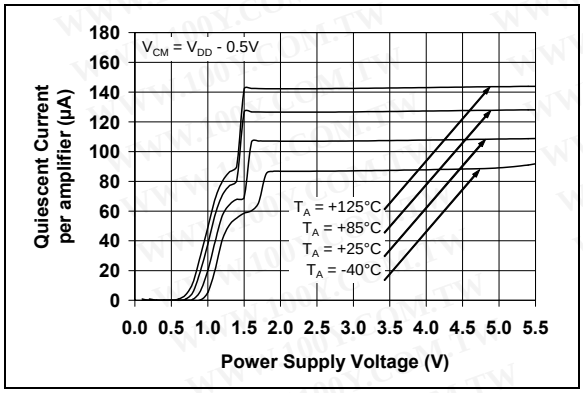


FIGURE 2-15: *Quiescent Current vs. Power Supply Voltage.*

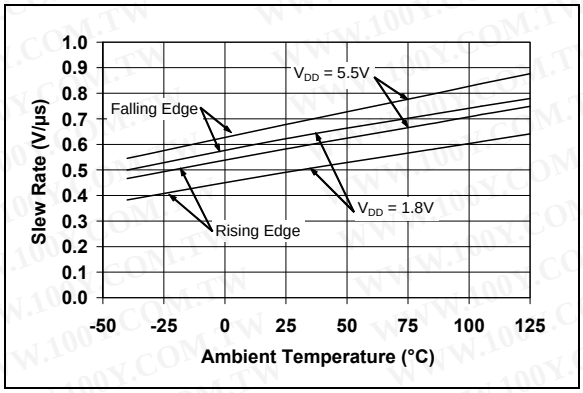


FIGURE 2-18: *Slew Rate vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L, and C_L = 60 pF.

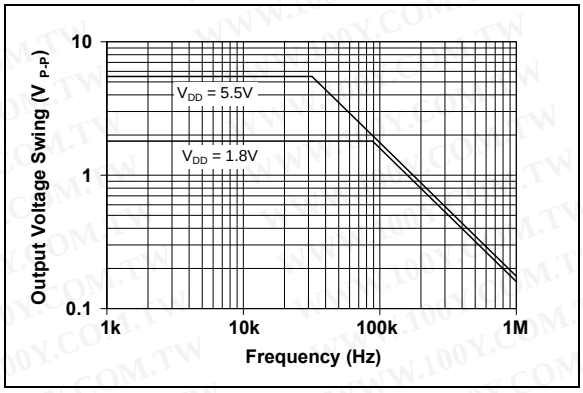


FIGURE 2-19: *Output Voltage Swing vs. Frequency.*

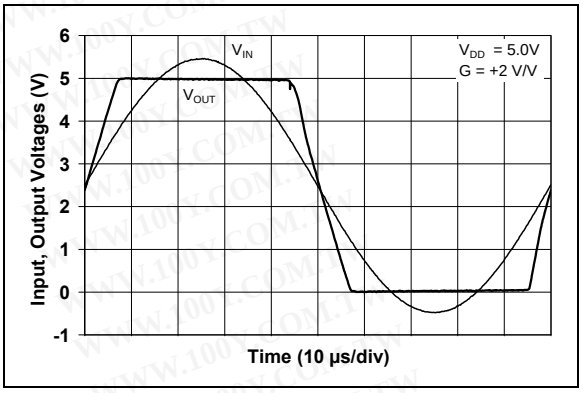


FIGURE 2-21: *The MCP6001/2/4 Show No Phase Reversal.*

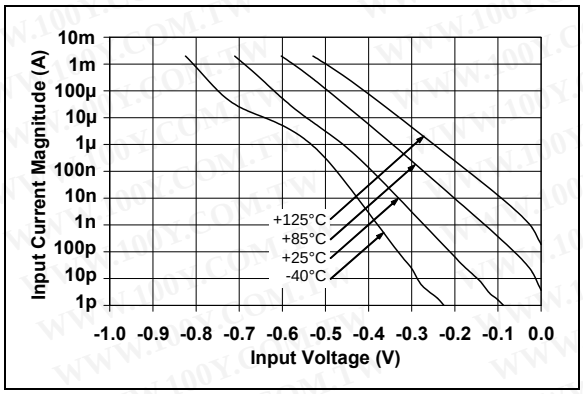


FIGURE 2-20: *Measured Input Current vs. Input Voltage (below V_{SS}).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6001	MCP6001R	MCP6001U	MCP6002		MCP6004	Symbol	Description
SC70-5, SOT-23-5	SOT-23-5	SOT-23-5	MSOP, PDIP, SOIC	DFN 2x3	PDIP, SOIC, TSSOP		
1	1	4	1	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
4	4	3	2	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	1	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
5	2	5	8	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	—	6	6	6	$V_{INB}-$	Inverting Input (op amp B)
—	—	—	7	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
2	5	2	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)
—	—	—	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to VSS.

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 1.8V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V_{SS} pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

4.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. This device has high phase margin, which makes it stable for larger capacitive load applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6001/1R/1U/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-21 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

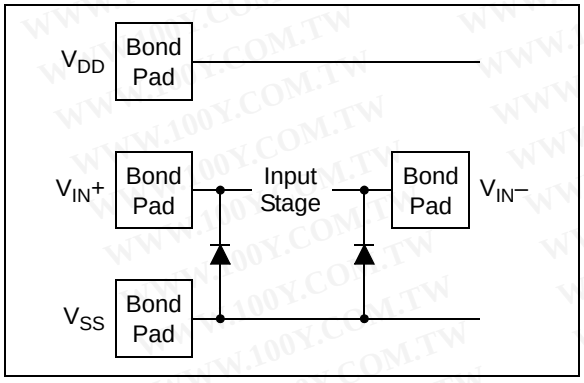


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the V_{IN}+ and V_{IN}– pins (see **Absolute Maximum Ratings †** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}–) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN}+ and V_{IN}–) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

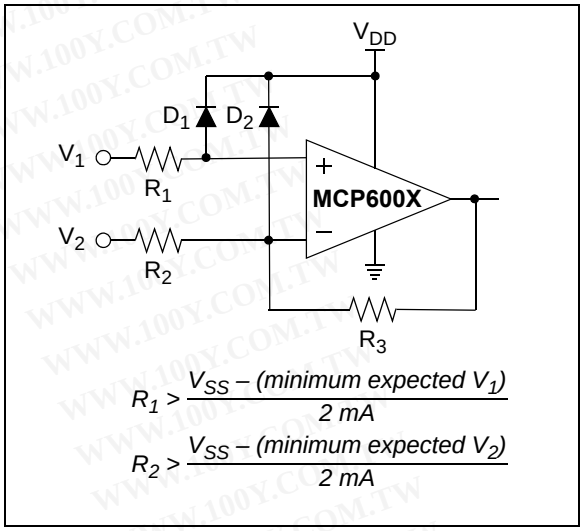


FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, current through the diodes D_1 and D_2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-20. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6001/1R/1U/2/4 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (V_{CM}), while the other operates at high V_{CM}. WIth this topology, the device operates with V_{CM} up to 0.3V above V_{DD} and 0.3V below V_{SS}.

The transition between the two input stages occurs when $V_{CM} = V_{DD} - 1.1V$. For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amps is V_{DD} – 25 mV (minimum) and V_{SS} + 25 mV (maximum) when R_L = 10 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figure 2-14 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

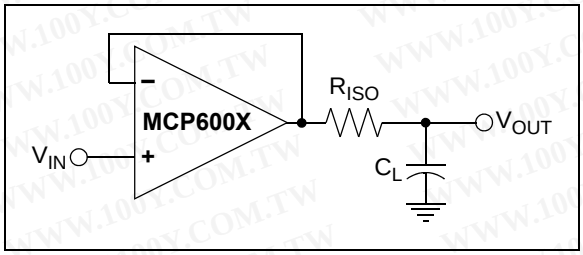


FIGURE 4-3: *Output resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

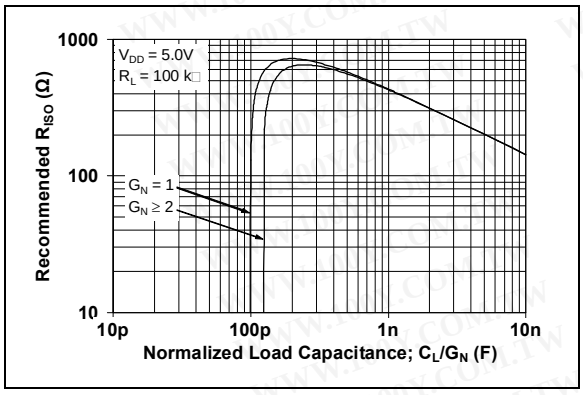


FIGURE 4-4: *Recommended R_{ISO} values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6001/1R/1U/2/4 SPICE macro model are very helpful.

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (MCP6004) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

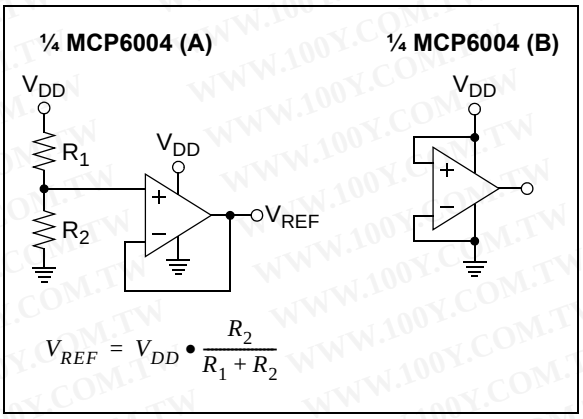


FIGURE 4-5: *Unused Op Amps.*

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6001/1R/1U/2/4 family's bias current at 25°C (typically 1 pA).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

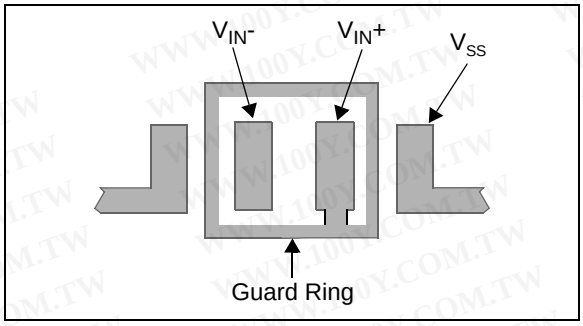


FIGURE 4-6: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 UNITY-GAIN BUFFER

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity-gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 4-7.

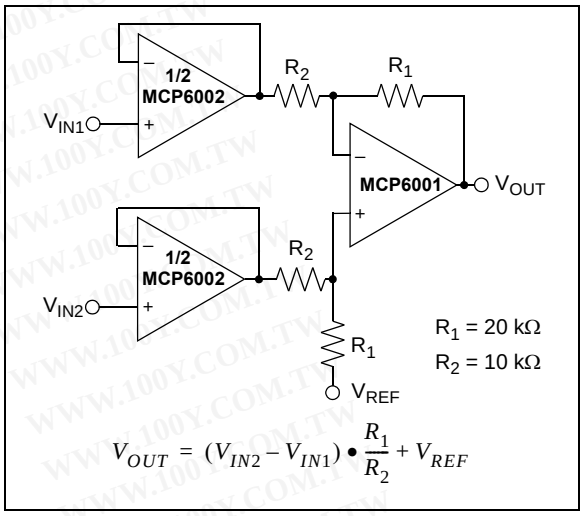


FIGURE 4-7: *Instrumentation Amplifier with Unity-Gain Buffer Inputs.*

4.7.2 ACTIVE LOW-PASS FILTER

The MCP6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100x the filter cutoff frequency (or higher) for good performance. It is possible to have the op amp bandwidth 10X higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 4-8 shows a second-order Butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10x higher than the cutoff frequency. The component values were selected using Microchip's FilterLab® software.

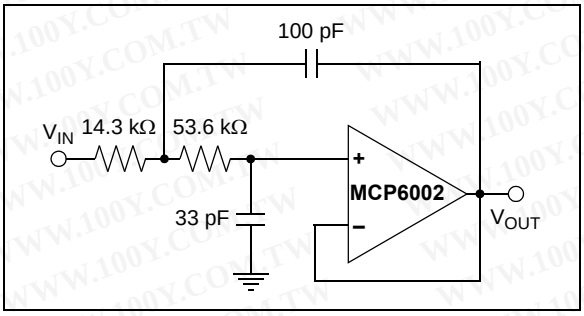


FIGURE 4-8: *Active Second-Order Low-Pass Filter.*

4.7.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applications. Figure 4-9 shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in Figure 4-9.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on C_1 is sampled to C_2 for a sample time defined by t_{SAMP}. At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes, C_1 discharges through R_1 for a time defined by t_{CLEAR}. At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of V_{IN} on C_1 for a time defined by t_{DETECT}.

In order to define t_{SAMP} and t_{CLEAR}, it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time (τ) is defined using R_1 ($\tau = R_1C_1$). t_{DETECT} is the time that the input signal is sampled on C_1 and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both C_1 and C_2), could create slewing limitations as the input voltage (V_{IN}) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with an op amp short circuit current of I_{SC} = 25 mA and a load capacitor of C_1 = 0.1 µF, then:

EQUATION 4-1:

$$I_{SC} = C_1 \frac{dV_{C1}}{dt}$$

$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$

$$= \frac{25mA}{0.1\mu F}$$

$$\frac{dV_{C1}}{dt} = 250mV/\mu s$$

This voltage rate of change is less than the MCP6001/2/4 slew rate of 0.6 V/µs. When the input voltage swings below the voltage across C_1, D_1 becomes reverse-biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1 µF capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than 40 µF and a stabilizing resistor (R_{ISO}) needs to be properly selected. (Refer to **Section 4.3 "Capacitive Loads"**).

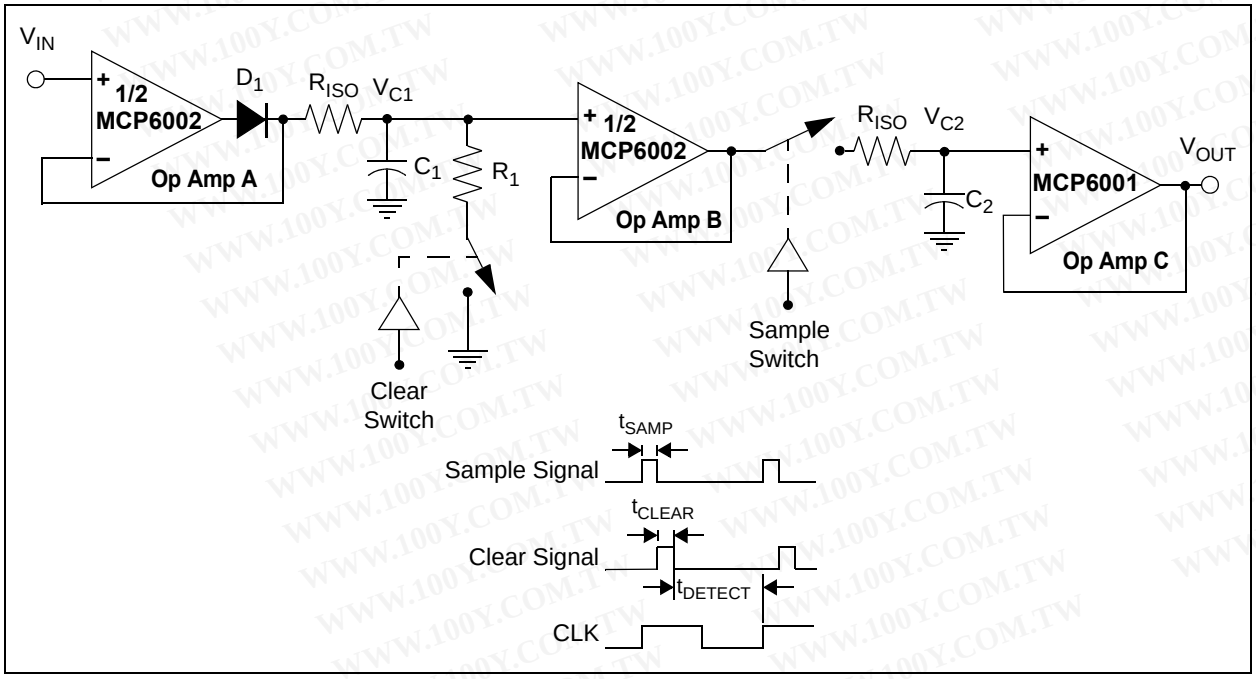


FIGURE 4-9: *Peak Detector with Clear and Sample CMOS Analog Switches.*

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6001/1R/1U/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6001/1R/1U/2/4 op amps is available on the Microchip web site at www.microchip.com. The model was written and tested in official Orcad (Cadence) owned PSPICE. For the other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions can not be guaranteed that it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip web site at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.4 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

5.6 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

- **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177:** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228:** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1297**: *"Microchip 's Op Amp SPICE Macro Models"*

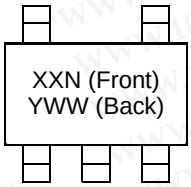
These application notes and others are listed in the design guide:

- *"Signal Chain Design Guide",* DS21825

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

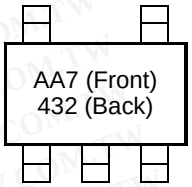
5-Lead SC-70 (**MCP6001**)



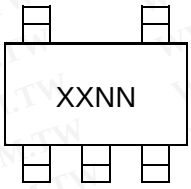
Device	I-Temp Code	E-Temp Code
MCP6001	AAN	CDN

Note: Applies to 5-Lead SC-70.

Example: (I-Temp)



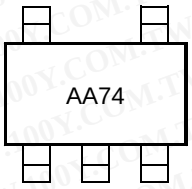
OR



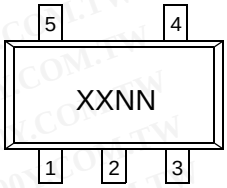
Device	I-Temp Code	E-Temp Code
MCP6001	AANN	CDNN

Note: Applies to 5-Lead SC-70.

OR



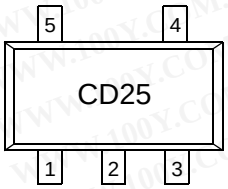
5-Lead SOT-23 (**MCP6001/1R/1U**)



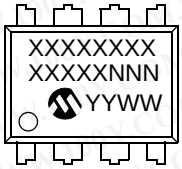
Device	I-Temp Code	E-Temp Code
MCP6001	AANN	CDNN
MCP6001R	ADNN	CENN
MCP6001U	AFNN	CFNN

Note: Applies to 5-Lead SOT-23.

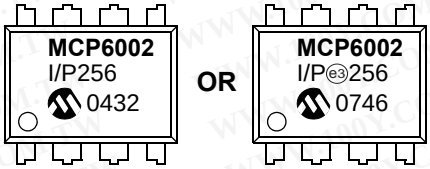
Example: (E-Temp)



8-Lead PDIP (300 mil)

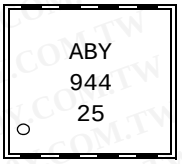


Example:



8-Lead DFN (2 x 3)

Example:

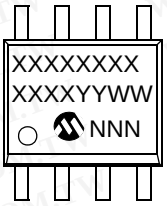


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

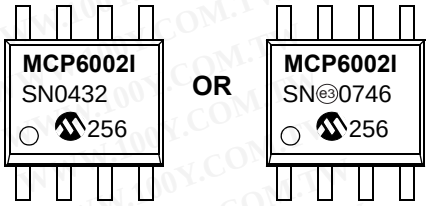
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

8-Lead SOIC (150 mil)



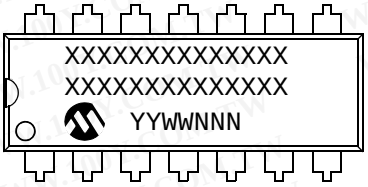
Example:



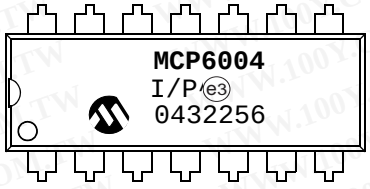
8-Lead MSOP

Example:

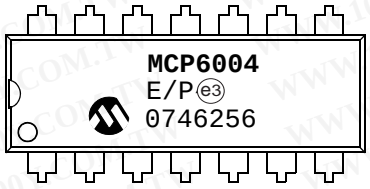
14-Lead PDIP (300 mil) (**MCP6004**)



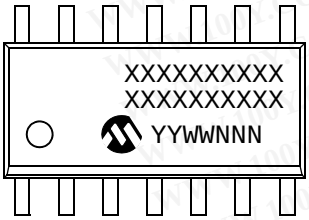
Example:



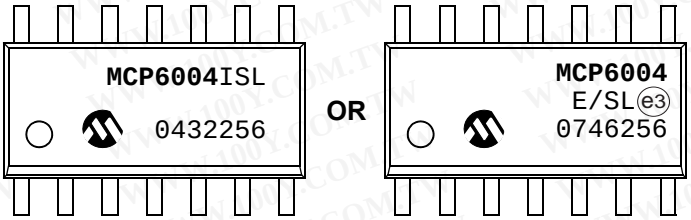
OR



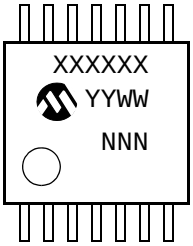
14-Lead SOIC (150 mil) (**MCP6004**)



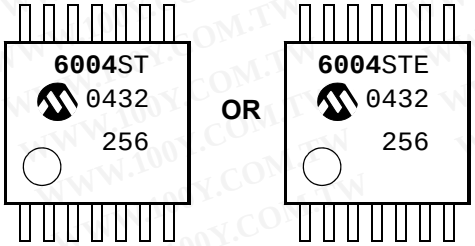
Example:



14-Lead TSSOP (**MCP6004**)

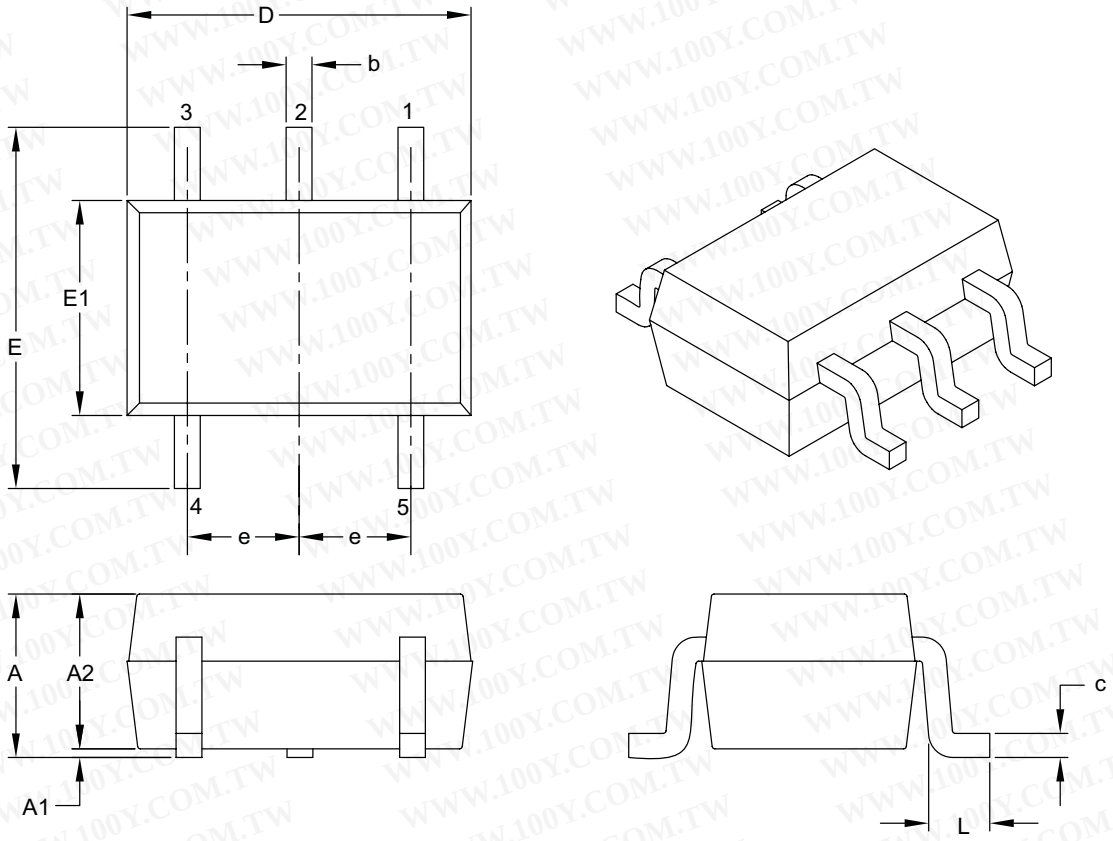


Example:



5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

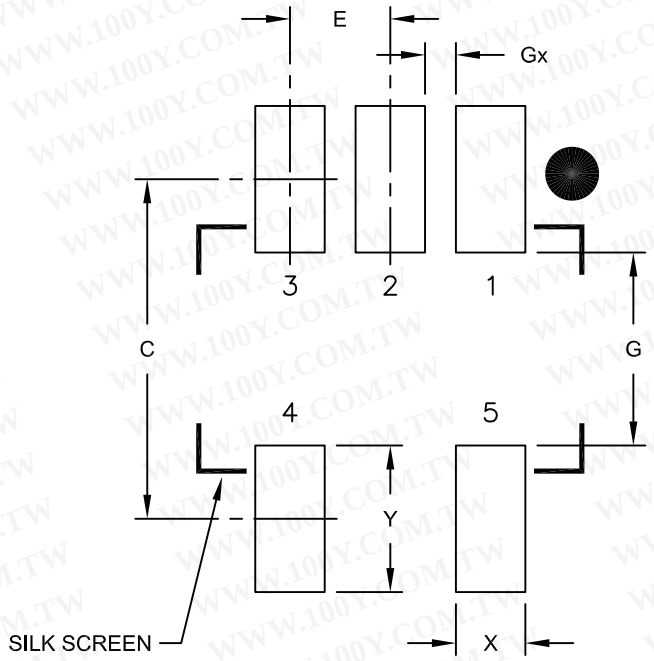
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

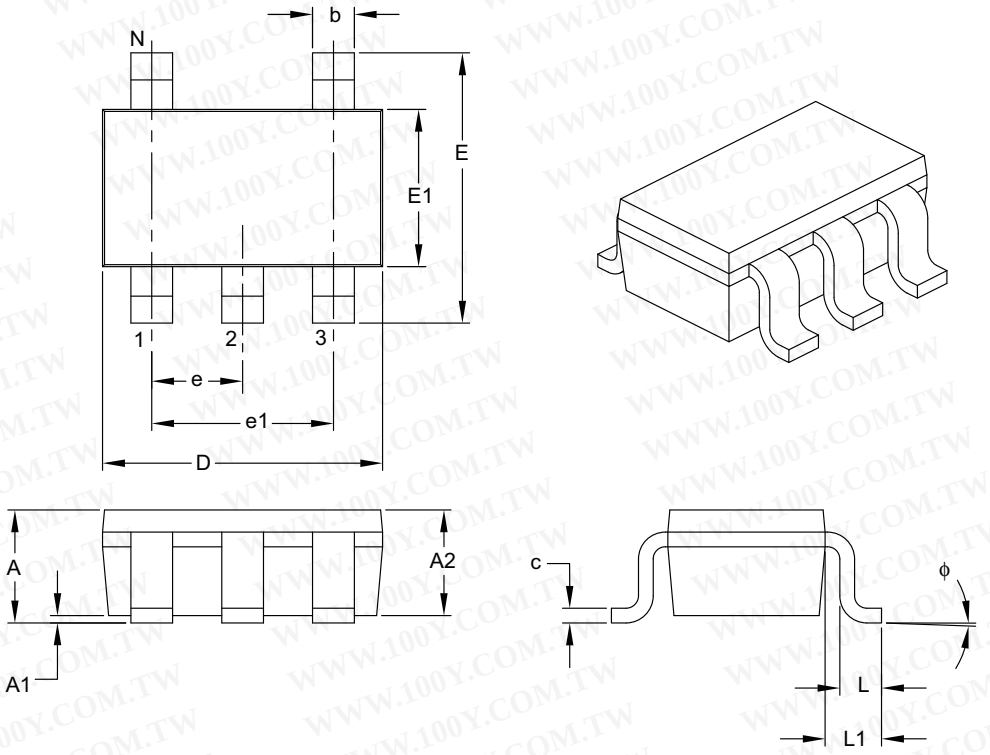
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

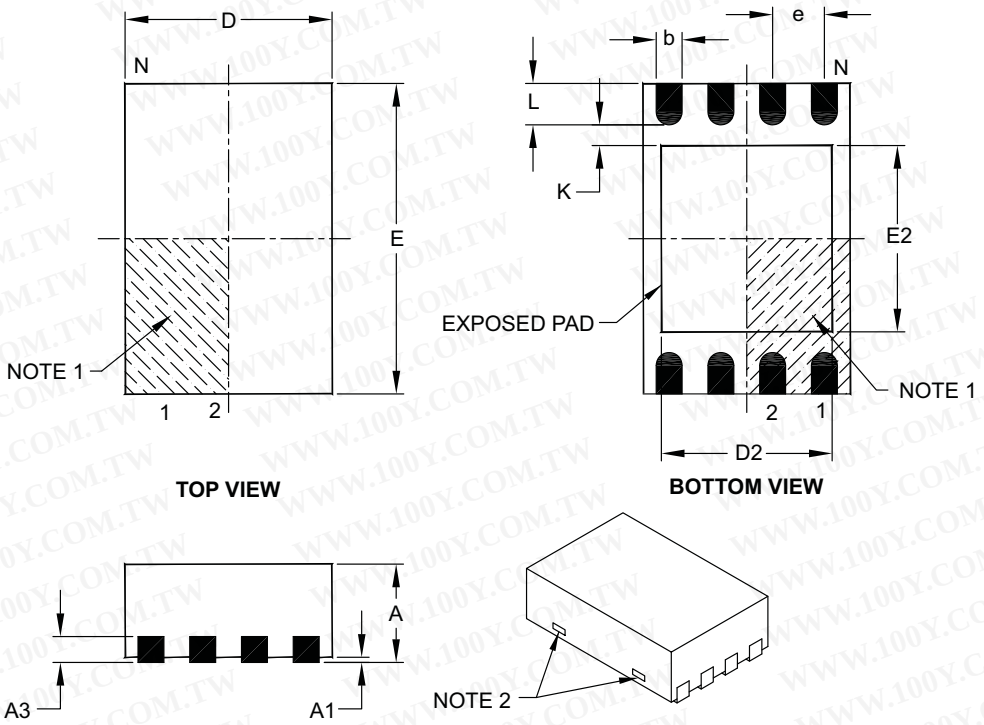
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

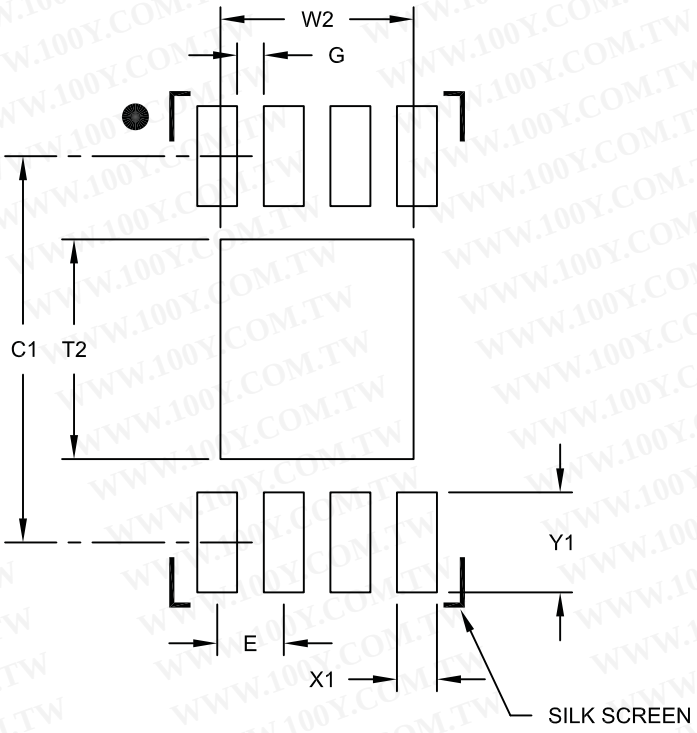
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

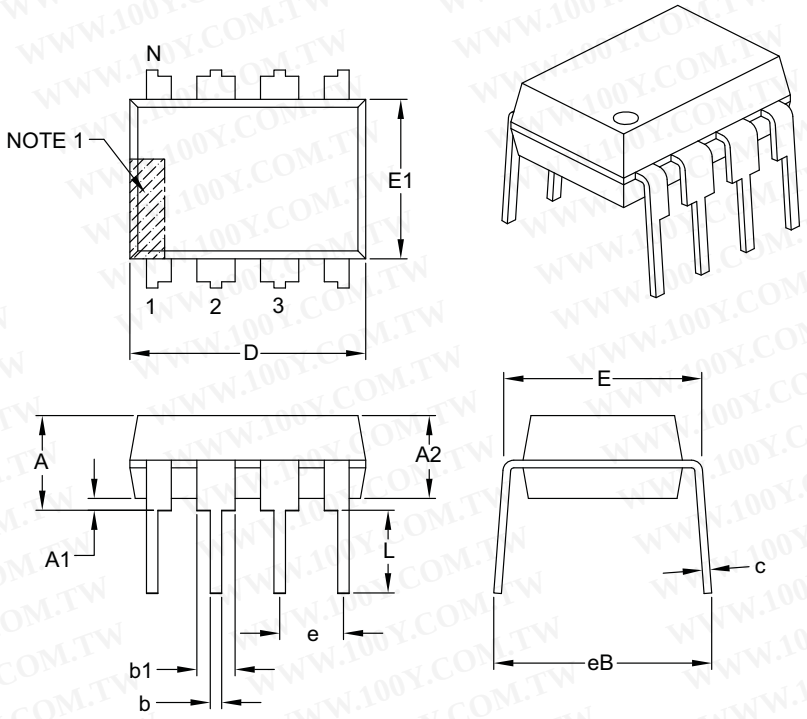
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123A

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

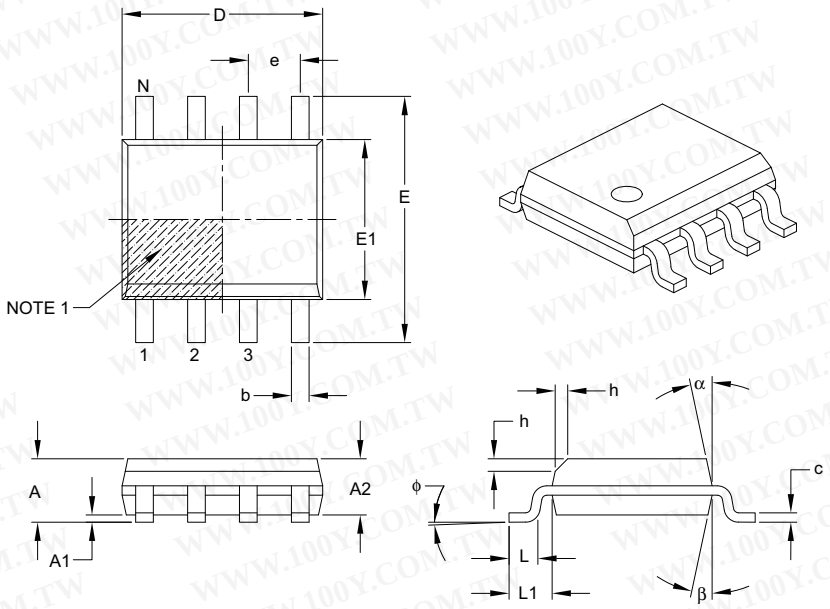
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

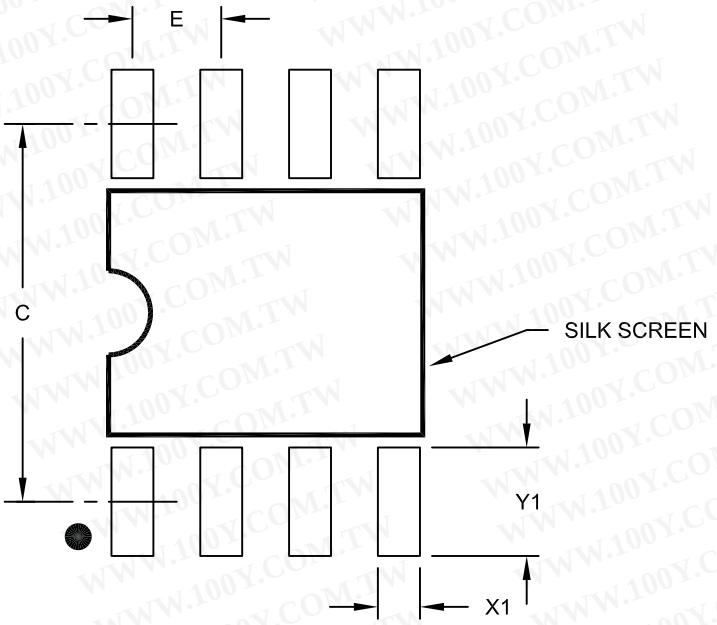
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

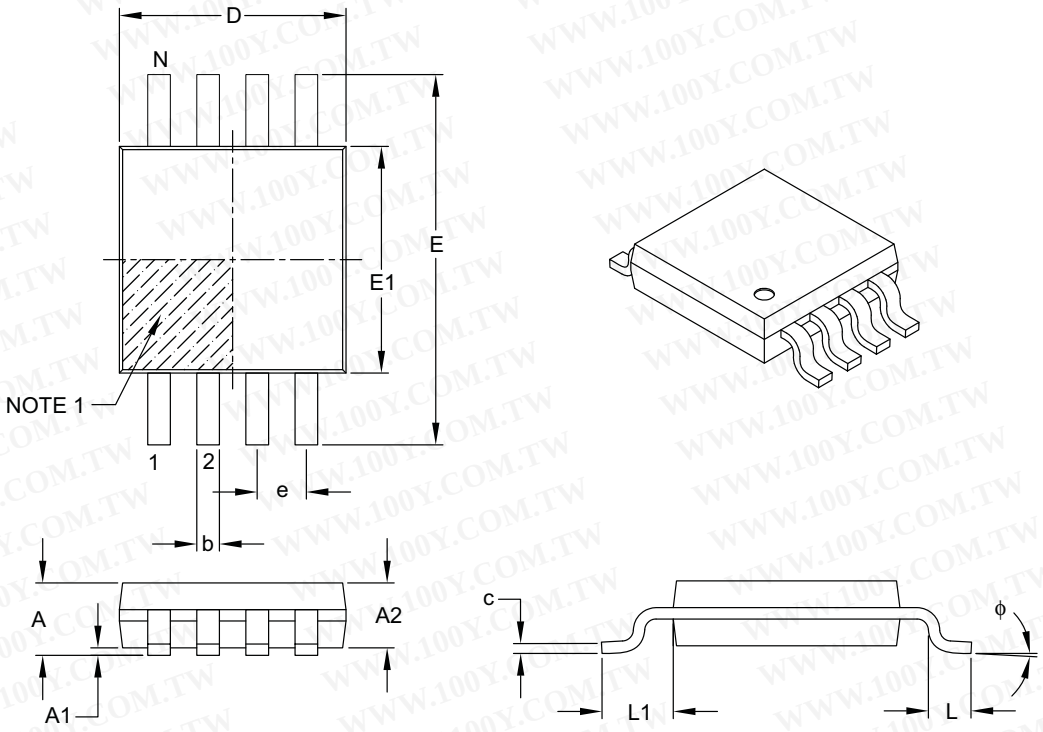
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

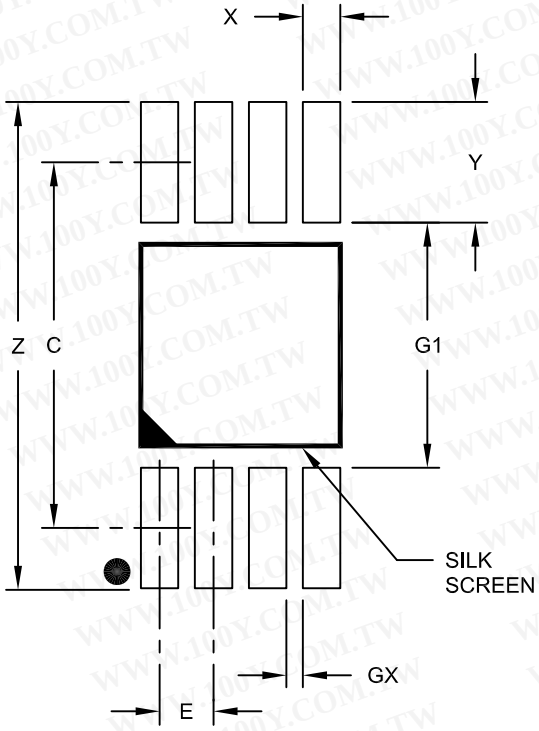
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

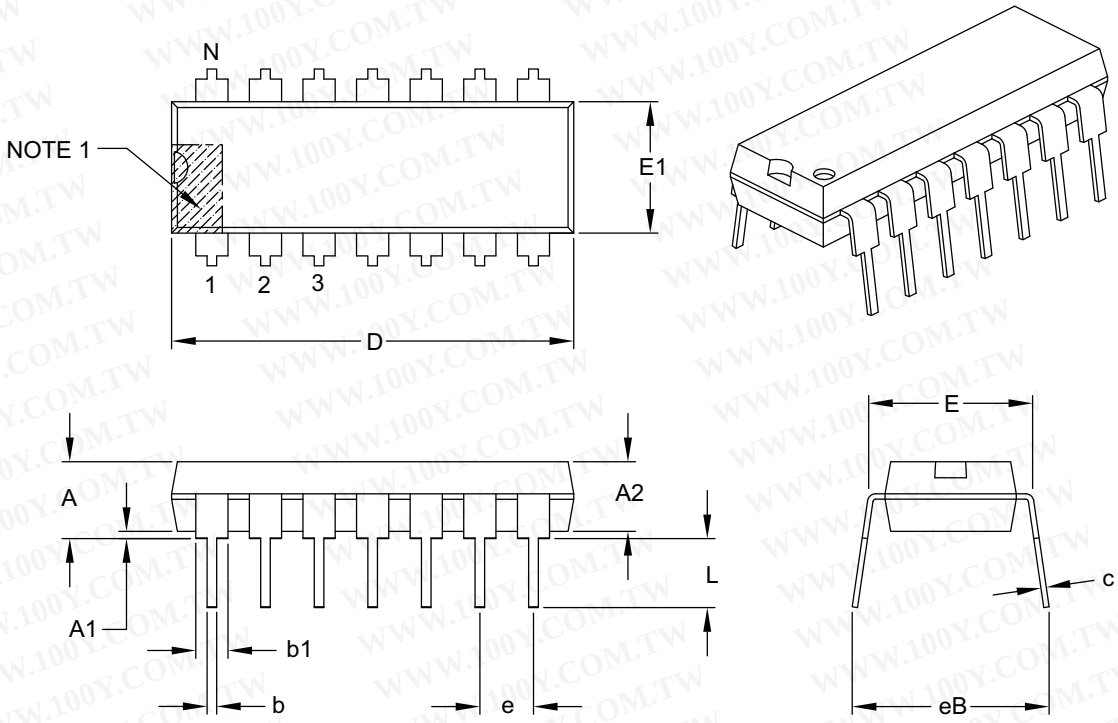
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

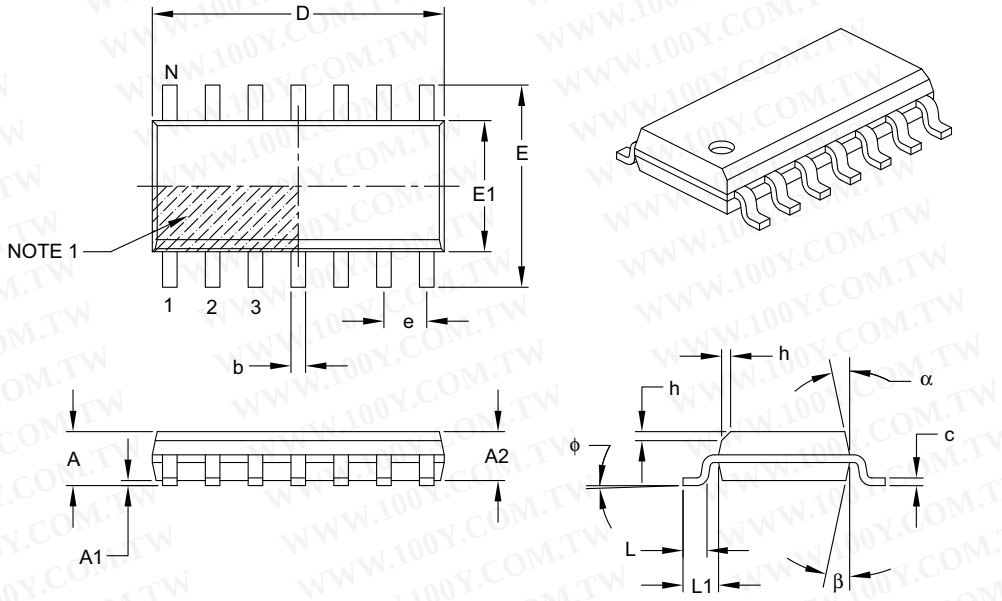
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

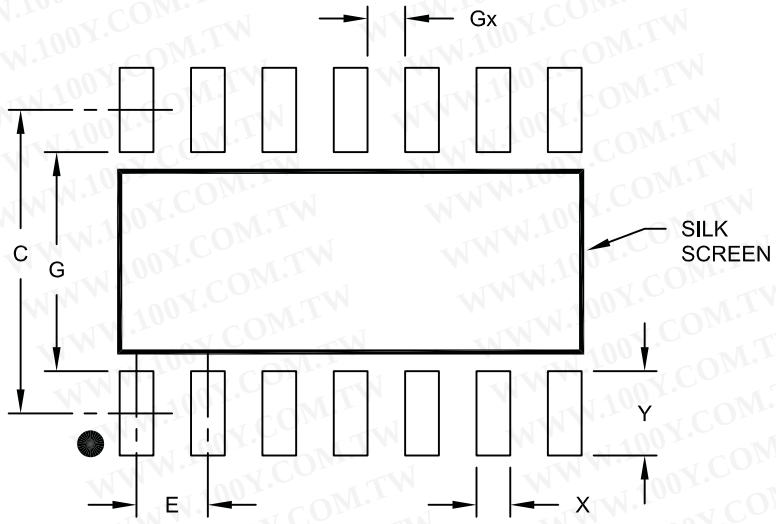
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

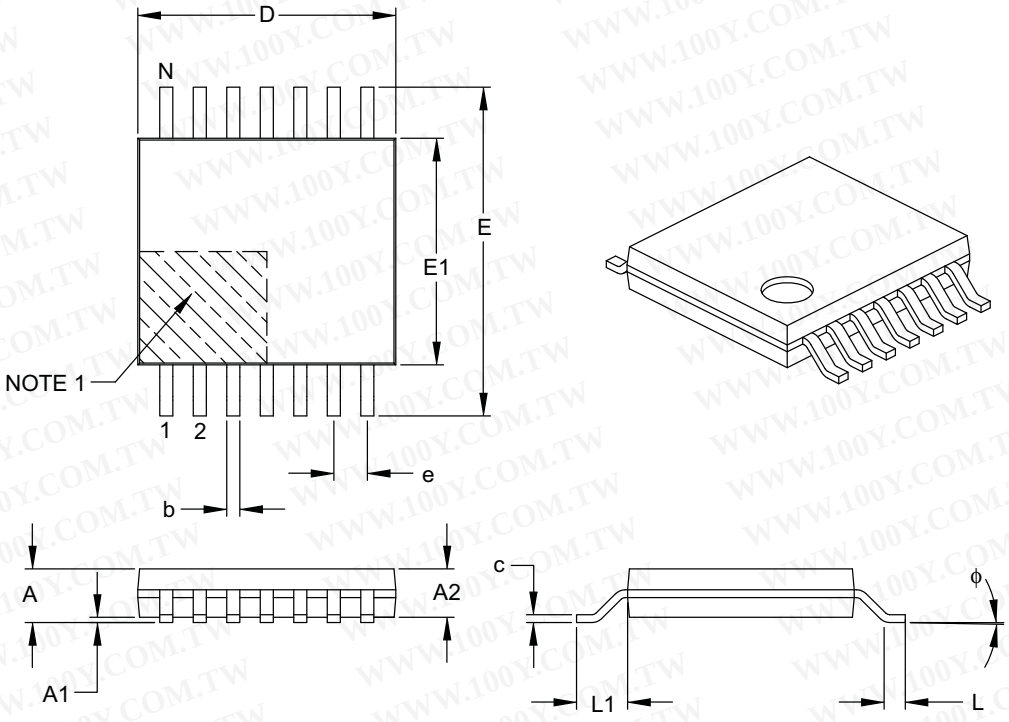
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

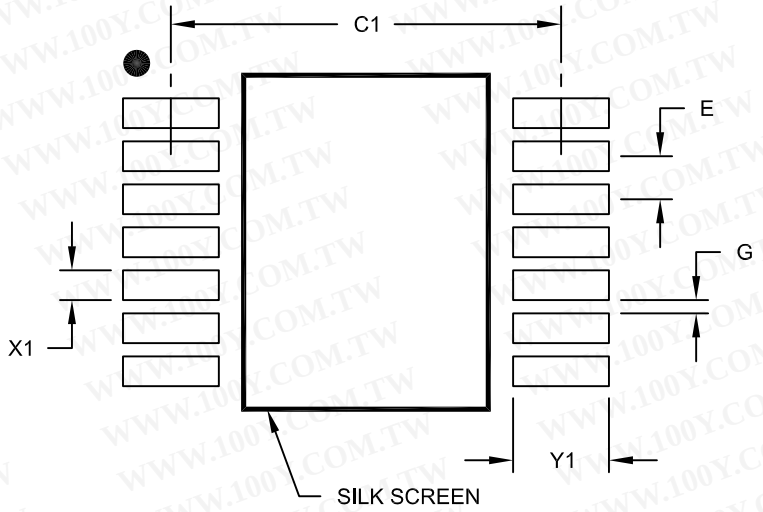
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

APPENDIX A: REVISION HISTORY

Revision J (November 2009)

The following is the list of modifications:

1. Added new 2x3 DFN 8-Lead package on page 1.
2. Updated the Temperature Specifications table with 2x3 DFN thermal resistance information.
3. Updated **Section 1.1 "Test Circuits"**.
4. Updated Figure 2-15.
5. Added the 2x3 DFN column to Table 3-1.
6. Added new **Section 3.4 "Exposed Thermal Pad (EP)"**.
7. Updated **Section 5.1 "SPICE Macro Model"**.
8. Updated **Section 5.5 "Analog Demonstration and Evaluation Boards"**.
9. Updated **Section 5.6 "Application Notes"**.
10. Updated **Section 6.1 "Package Marking Information"** with the new 2x3 DFN package marking information.
11. Updated the package drawings.
12. Updated the Product Identification System section with new 2x3 DFN package information.

Revision H (May 2008)

The following is the list of modifications:

1. **Design Aids:** Name change for Mindi Simulation Tool.
2. **Package Types:** Correct device labeling error.
3. **Section 1.0 "Electrical Characteristics", DC Electrical Specifications:** Changed "Maximum Output Voltage Swing" condition from 0.9V Input Overdrive to 0.5V Input Overdrive.
4. **Section 1.0 "Electrical Characteristics", AC Electrical Specifications:** Changed Phase Margin condition from G = +1 to G= +1 V/V.
5. **Section 5.0 "Design AIDS"**: Name change for Mindi Simulation Tool.

Revision G (November 2007)

The following is the list of modifications:

1. Updated notes to **Section 1.0 "Electrical Characteristics"**.
2. Increased Absolute Maximum Voltage range at input pins.
3. Increased maximum operating supply voltage (V_{DD}).
4. Added test circuits.
5. Added Figure 2-3 and Figure 2-20.
6. Added **Section 4.1.1 "Phase Reversal"**, **Section 4.1.2 "Input Voltage and Current Limits"**, **Section 4.1.3 "Normal Operation"** and **Section 4.5 "Unused Op Amps"**.
7. Updated **Section 5.0 "Design AIDS"**,
8. Updated **Section 6.0 "Packaging Information"**
9. Updated Package Outline Drawings.

Revision F (March 2005)

The following is the list of modifications:

1. Updated **Section 6.0 "Packaging Information"** to include old and new packaging examples.

Revision E (December 2004)

The following is the list of modifications:

1. V_{OS} specification reduced to ±4.5 mV from ±7.0 mV for parts starting with date code YYWW = 0449
2. Corrected package markings in **Section 6.0 "Packaging Information"**.
3. Added Appendix A: Revision History.

Revision D (May 2003)

- Undocumented changes.

Revision C (December 2002)

- Undocumented changes.

Revision B (October 2002)

- Undocumented changes.

Revision A (June 2002)

- Original data sheet release.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6001T:	Single Op Amp (Tape and Reel) (SC-70, SOT-23)
	MCP6001RT:	Single Op Amp (Tape and Reel) (SOT-23)
	MCP6001UT:	Single Op Amp (Tape and Reel) (SOT-23)
	MCP6002:	Dual Op Amp
	MCP6002T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)
	MCP6004:	Quad Op Amp
	MCP6004T:	Quad Op Amp (Tape and Reel) (SOIC, MSOP)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	LT =	Plastic Package (SC-70), 5-lead (MCP6001 only)
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6001, MCP6001R, MCP6001U)
	MS =	Plastic MSOP, 8-lead
	MC =	Plastic DFN, 8-lead
	P =	Plastic DIP (300 mil body), 8-lead, 14-lead
	SN =	Plastic SOIC, (3.99 mm body), 8-lead
	SL =	Plastic SOIC (3.99 body), 14-lead
	ST =	Plastic TSSOP (4.4mm body), 14-lead

Examples:

a)	MCP6001T-I/LT:	Tape and Reel, Industrial Temperature, 5LD SC-70 package
b)	MCP6001T-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
c)	MCP6001RT-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
d)	MCP6001UT-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6002-I/MS:	Industrial Temperature, 8LD MSOP package.
b)	MCP6002-I/P:	Industrial Temperature, 8LD PDIP package.
c)	MCP6002-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6002-E/MC:	Extended Temperature, 8LD DFN package.
e)	MCP6002-I/SN:	Industrial Temperature, 8LD SOIC package.
f)	MCP6002T-I/MS:	Tape and Reel, Industrial Temperature, 8LD MSOP package.
g)	MCP6002T-E/MC:	Tape and Reel, Extended Temperature, 8LD DFN package.
a)	MCP6004-I/P:	Industrial Temperature, 14LD PDIP package.
b)	MCP6004-I/SL:	Industrial Temperature, 14LD SOIC package.
c)	MCP6004-E/SL:	Extended Temperature, 14LD SOIC package.
d)	MCP6004-I/ST:	Industrial Temperature, 14LD TSSOP package.
e)	MCP6004T-I/SL:	Tape and Reel, Industrial Temperature, 14LD SOIC package.
f)	MCP6004T-I/ST:	Tape and Reel, Industrial Temperature, 14LD TSSOP package.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Octopus, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, PIC^{32} logo, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4080

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

03/26/09