

## Window Discriminator

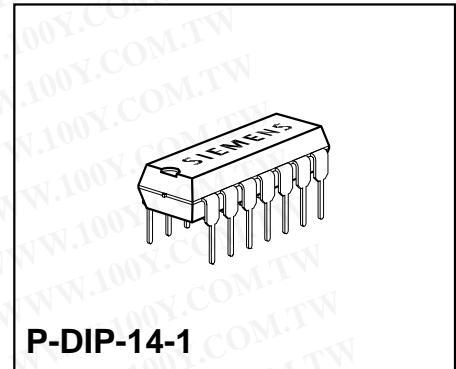
TCA 965 B

### Preliminary

Bipolar IC

### Features

- Two window settings
  - direct setting of lower and upper edge voltage (window edges)
  - indirect setting by window center voltage and half window width
- Adjustable hysteresis
- Digital outputs with open collectors for currents up to 50 mA
- Adjustable reference voltage  $V_{Stab}$



勝特力材料 886-3-5753170  
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[Http://www.100y.com.tw](http://www.100y.com.tw)

Type	Ordering Code	Package
■ TCA 965 B	Q67000-A8338	P-DIP-14-1

■ Not for new design

The window discriminator compares an input voltage to a defined voltage window. The digital outputs show whether the input voltage is below, within or above this window.

The TCA 965 B window discriminator is especially suitable as a tracking or compensating controller with a dead band in control engineering and for the selection of DC voltages within a certain tolerance of the required setpoint value in measurement engineering. When it is used as a Schmitt trigger, switching frequencies up to a typical value of 50 kHz are possible.

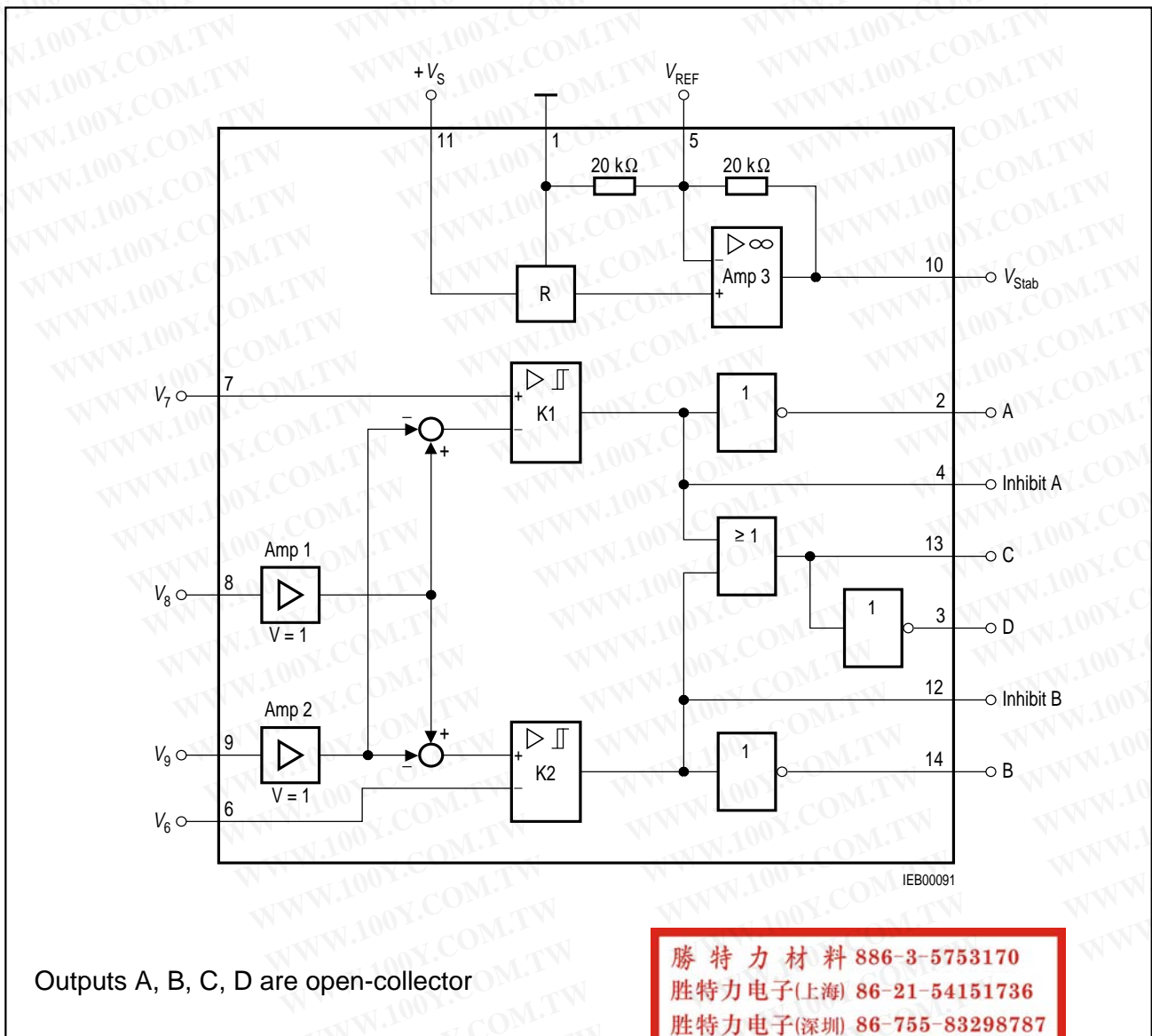
## Functional Description

Amplifier Amp 3 increases the voltage of the reference source  $R$  to  $V_{Stab} = 2 \times V_{REF}$ . The amplification factor can be altered by external wiring. With direct setting of the window, the input voltage appears on amplifier Amp 1 ( $V_8$ ), the upper edge voltage on comparator K2 ( $V_6$ ) and the lower edge voltage on comparator K1 ( $V_7$ ).

With indirect setting of the window, the input voltage appears on inputs  $V_6$  and  $V_7$ , while the center voltage is connected to amplifier A1 ( $V_8$ ).

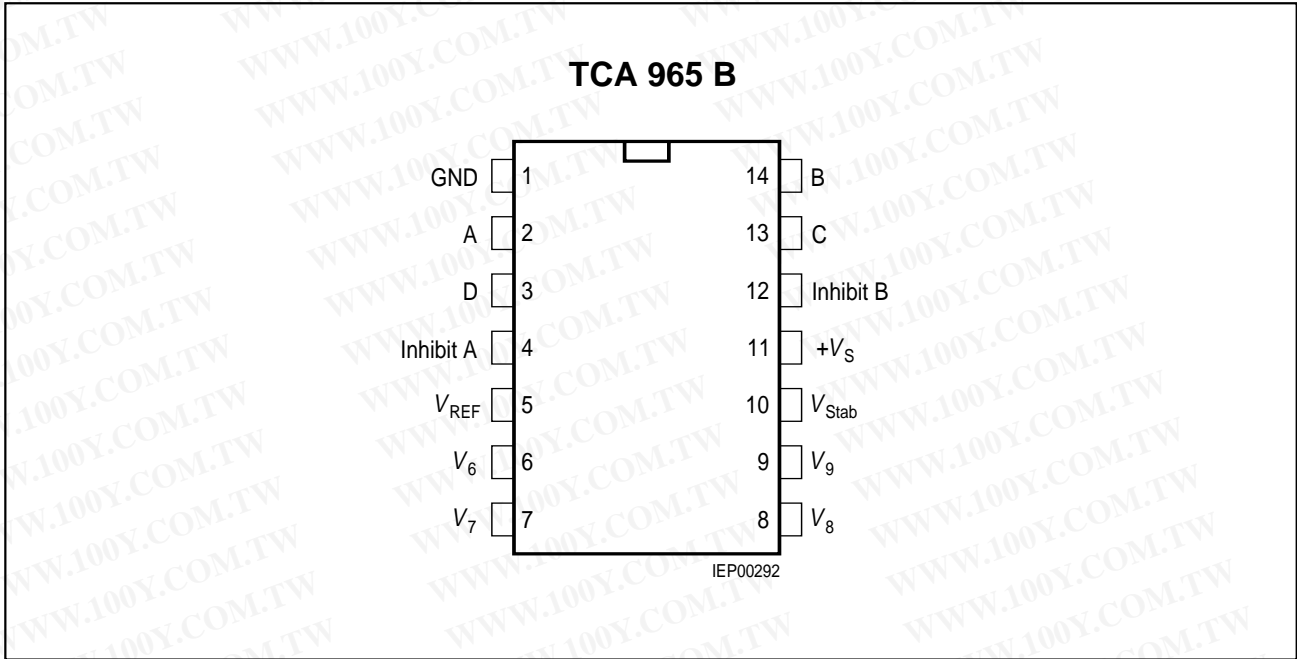
The voltage applied to the input ( $V_9$ ) of amplifier Amp 2 is subtracted symmetrically from the output voltage of amplifier Amp 1 and added. The comparators switch with hysteresis. The logic gates have open-collector outputs.

If the inhibit input A or B is connected to ground, output A or B will always be high.



## Block Diagram

### Pin Configuration (top view)



### Pin Definitions and Functions

Pin	Symbol	Pin Function in	
		Direct Setting	Indirect Setting
1	GND	GND	
2	A	Logic output A	
3	D	Logic output D = A @ B (AND)	
4	Inhibit A	Connected to GND: logic output A = HIGH	
5	$V_{REF}$	Internal $V_{REF} = 3\text{ V}$	
6	$V_6$	Upper edge voltage	Input voltage $V_{6/7}$
7	$V_7$	Lower edge voltage	Input voltage $V_{6/7}$
8	$V_8$	Input voltage	Center voltage
9	$V_9$	GND	Half window width
10	$V_{Stab}$	Internal $V_{Stab} = 6\text{ V}$	
11	$+V_S$	Supply voltage	
12	Inhibit B	Connected to GND: logic output B = HIGH	
13	C	Logic output C = A @ B (NAND)	
14	B	Logic output B	

## Absolute Maximum Ratings

Maximum ratings for ambient temperature  $T_A = -25$  to  $85\text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage (pin 11)	$V_S$	–	30	V
Difference in input voltage between pins 6, 7, 8	$V_I$	–	15	V
Input voltage (pins 6, 7, 8, 9)	$V_I$	–	30	V
Output current (pins 2, 3, 13, 14)	$I_Q$	–	50	mA
Output voltage (pins 2, 3, 13, 14) independent of $V_S$	$V_Q$	–	30	V
Voltage on $V_{REF}$ (pin 5)	$V_R$	–	8	V
Output current of stabilized voltage (pin 10)	$I_{10}$	–	10	mA
Inhibit input voltage (pins 4, 12)	$V_{IH}$	–	7	V
Junction temperature	$T_j$		150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	– 55	125	$^\circ\text{C}$
Thermal resistance system - air P-DIP-14-1	$R_{th SA}$	–	80	K/W

## Operating Range

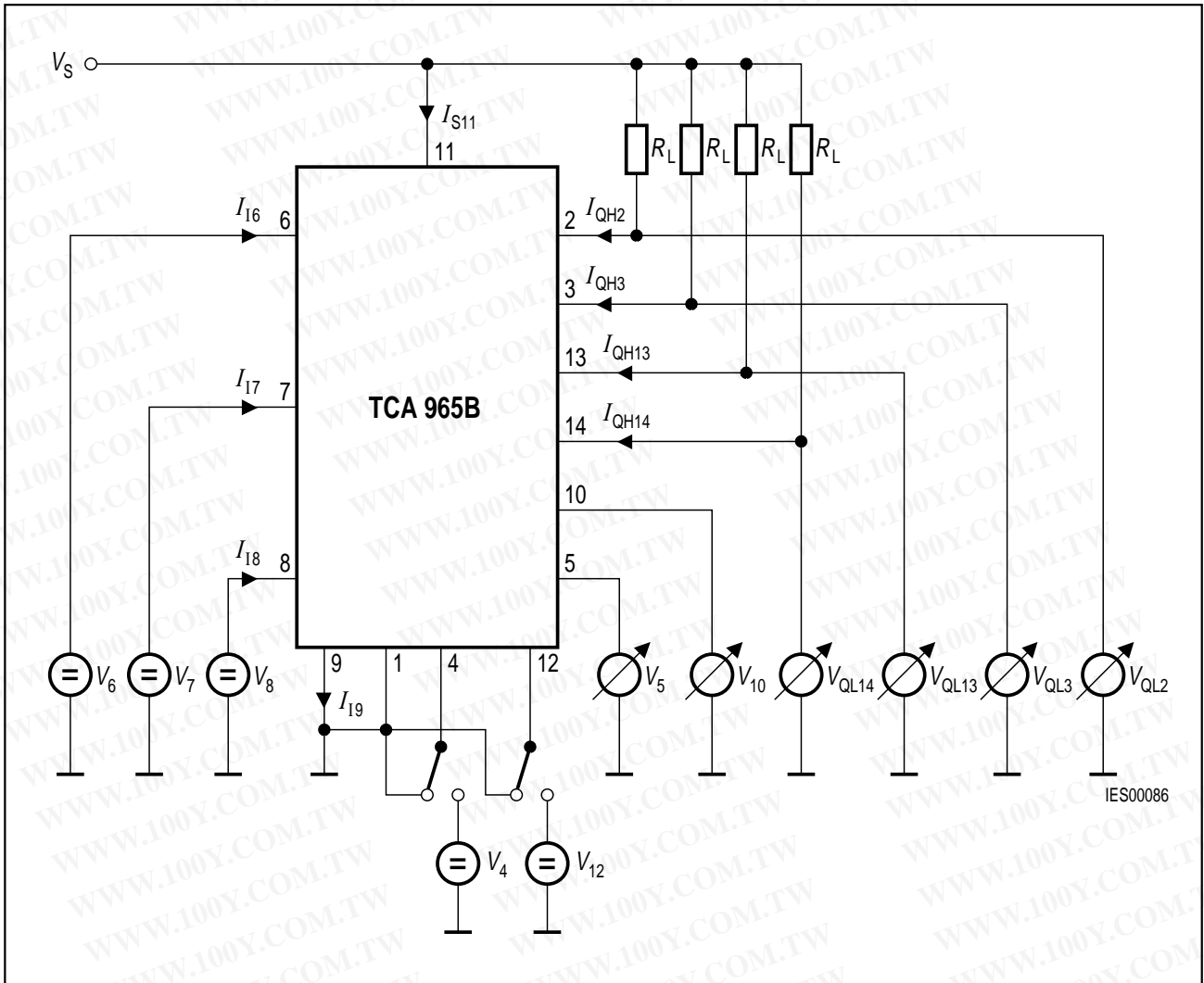
Supply voltage	$V_S$	4.5	30	V
Ambient temperature	$T_A$	– 25	85	$^\circ\text{C}$

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### Characteristics

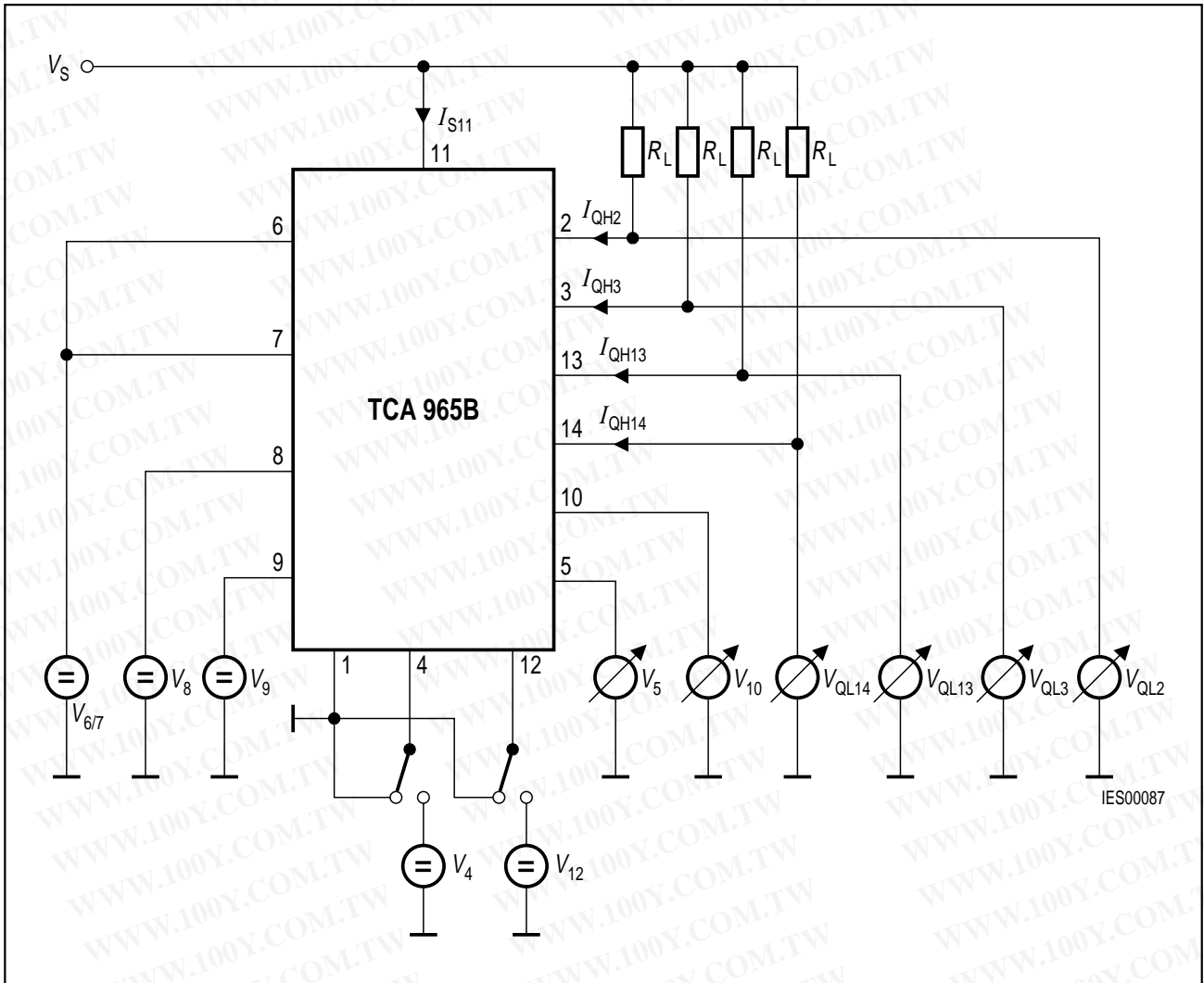
$V_S = 10\text{ V}; T_A = 25\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current consumption	$I_S$	–	5	7	mA	$V_2, V_{13} = V_{QH}$	1
Input current (pins 6, 7, 8)	$I_I$	–	20	50	nA		1
Input current, pin 9	$-I_I$	–	400	3000	nA		1
Input offset voltage in direct setting of window	$V_{IO}$	– 20		20	mV		1
Input offset voltage in indirect setting of window	$V_{IO}$	– 50		50	mV		2
Input-voltage range on pins 6, 7, 8	$V_I$	1.5		$V_S - 1$	V	$\Delta V_I < 13\text{ V}$	1
Input-voltage range on pin 9	$V_I$	50		$V_S/2$	mV		2
Differential input voltage	$V_6 - (V_8 - V_9)$			13	V		
	$(V_8 + V_9) - V_7$			13	V		
Reference voltage	$V_5$	2.8	3	3.2	V	$I_{REF} = 0$	
Stabilized voltage on pin 10	$V_{10}$	5.5	6	6.5	V	$V_S > 7.9\text{ V}$	
TC of reference voltage	$\alpha V_5$		0.4		mV/K		
Sensitivity of reference voltage to supply-voltage variation	$\Delta V_5 / \Delta V_S$		2		mV/V		
Output reverse current	$I_{QH}$	–	–	10	$\mu\text{A}$	–	–
Output saturation voltage	$V_{QL}$		100	200	mV	$I_Q = 10\text{ mA}$	1
			500	800	mV	$I_Q = 50\text{ mA}$	
Hysteresis of window edges	$V_U - V_L$	18	22	35	mV		
Inhibit threshold	$V_{4,12}$	1		1.8	V		
Inhibit current	$I_{4,12}$	–	– 100	–	$\mu\text{A}$	–	–
Switching frequency	$f_{dir}$	–	20	–	kHz	–	1
	$f_{ind}$	–	50	–	kHz	–	2



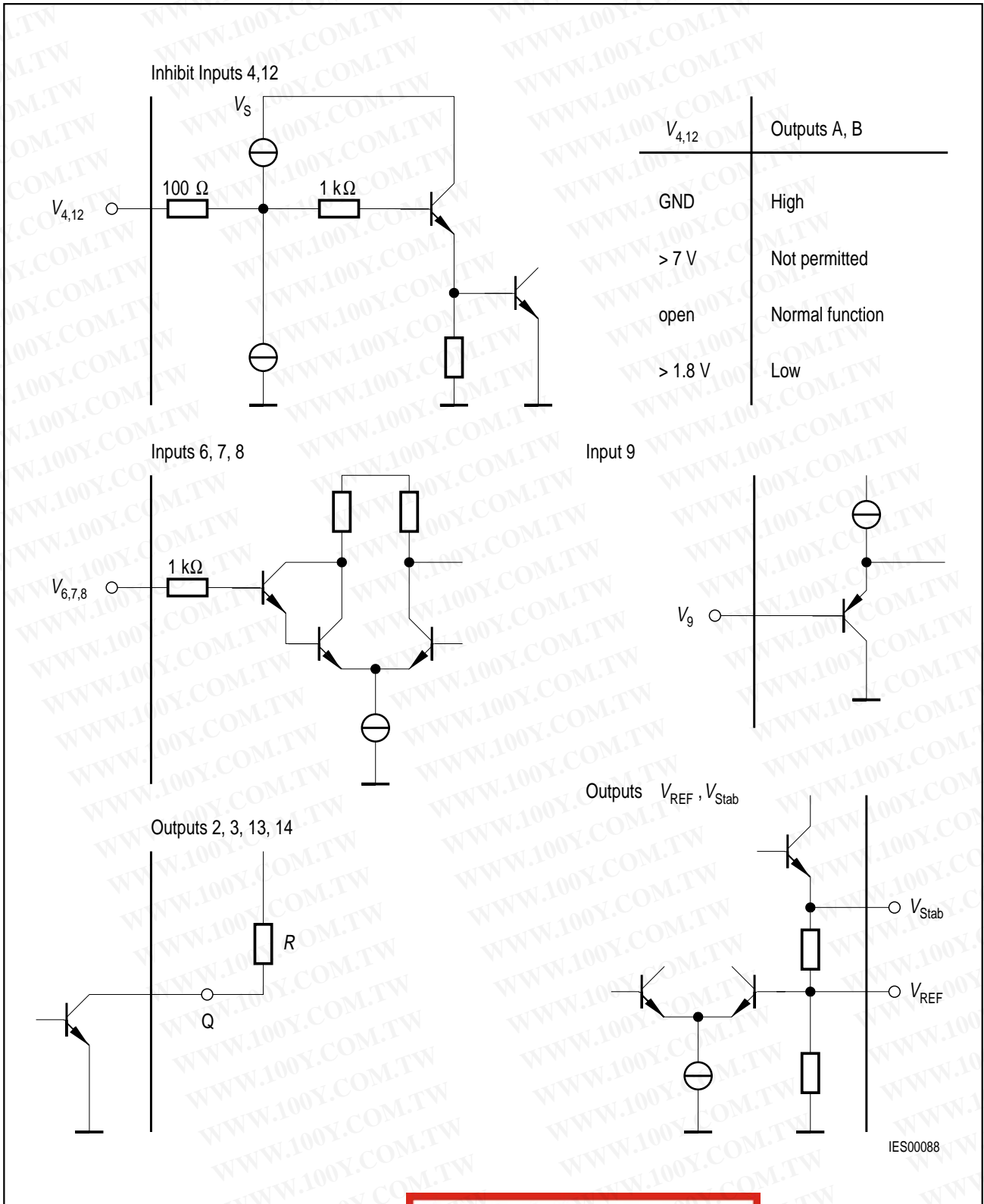
**Test Circuit 1**  
**Direct Setting of Window**

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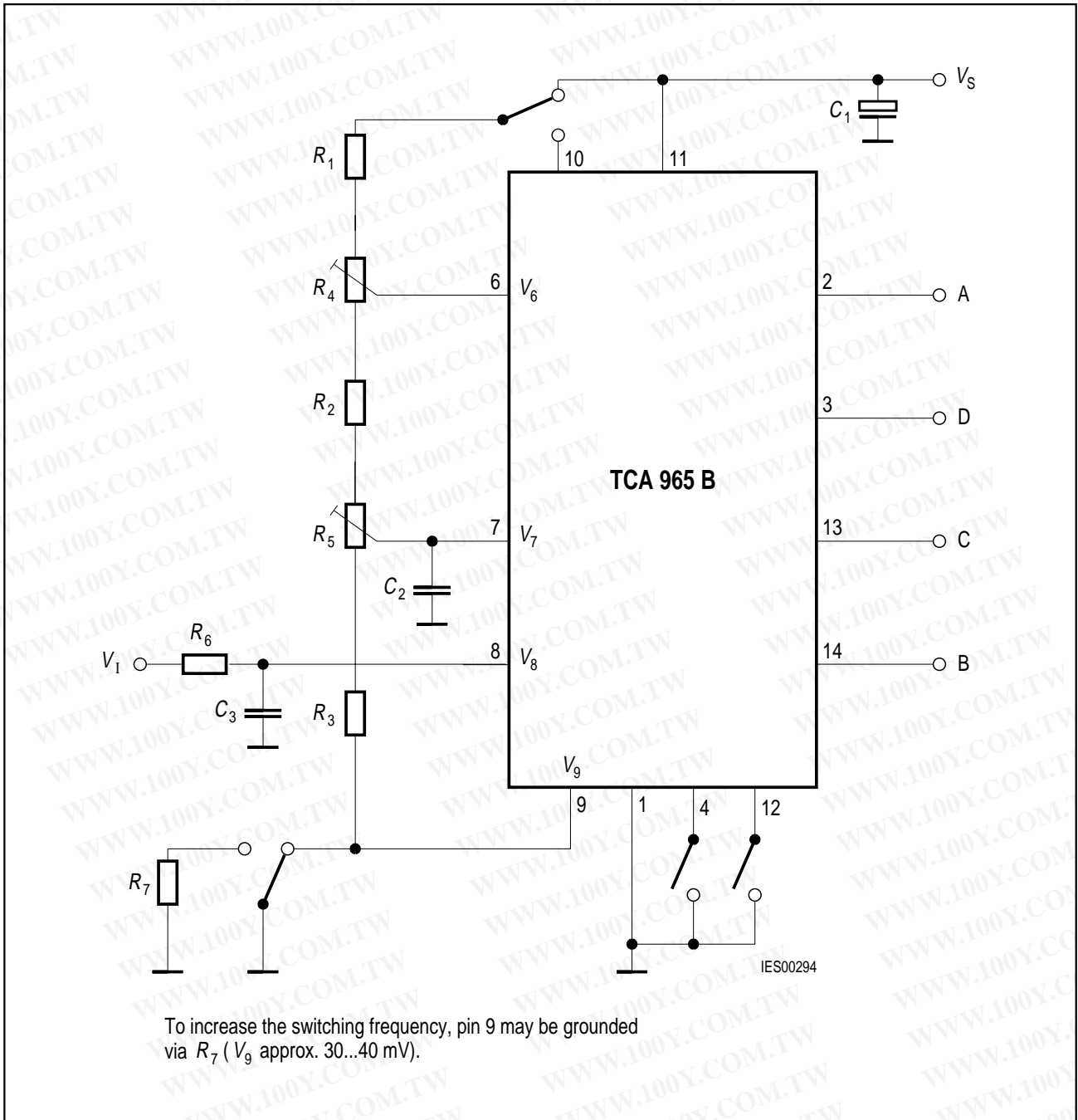
**Test Circuit 2**  
**Indirect Setting of Window by Center Voltage and Half Window Width**

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## Schematic Circuit Diagrams

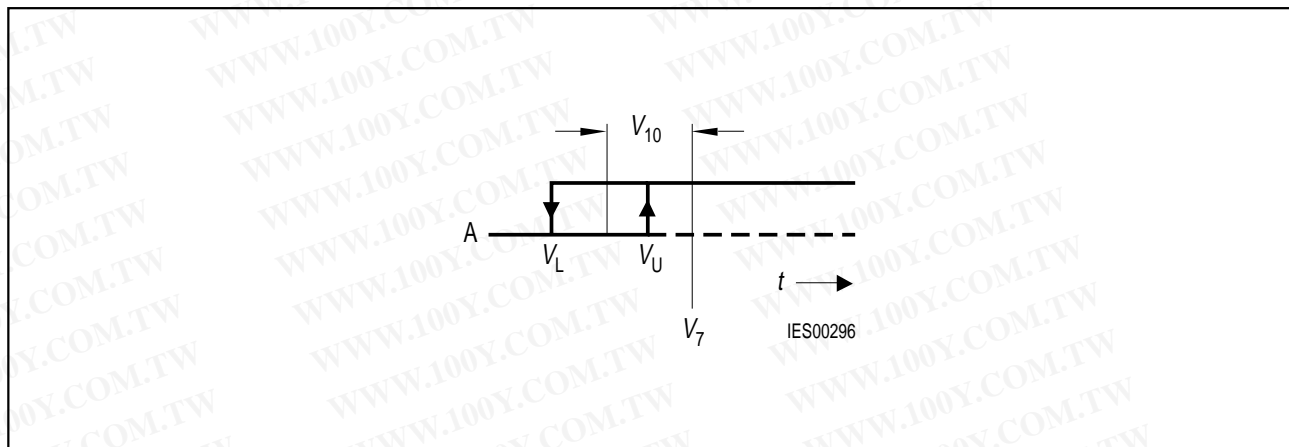
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**Application Circuit 1**  
**Direct Setting of Lower and Upper Edge Voltages**

$V_6 - V_9 =$  Upper edge voltage  
 $V_7 + V_9 =$  Lower edge voltage  
 $V_8 =$  Input voltage

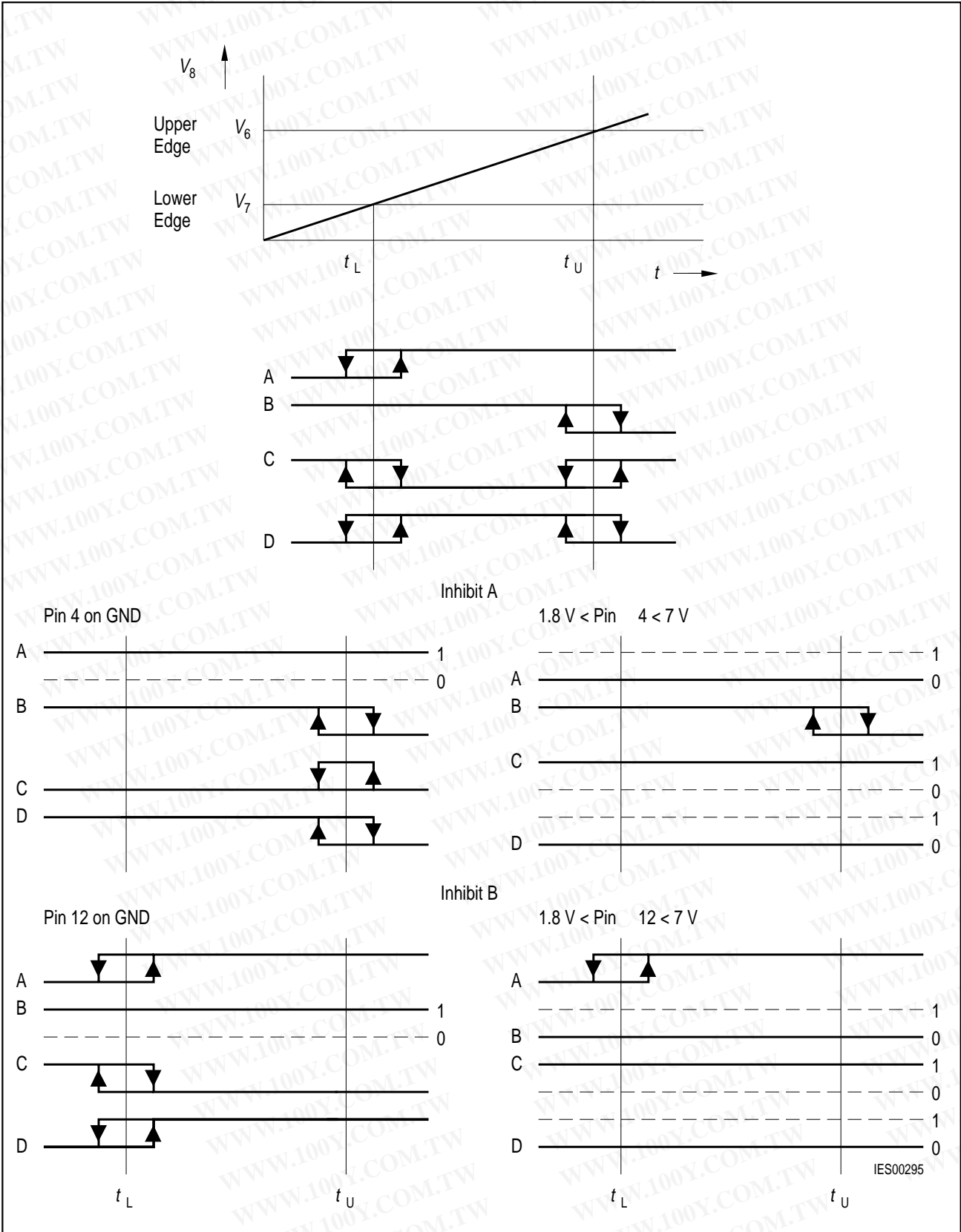
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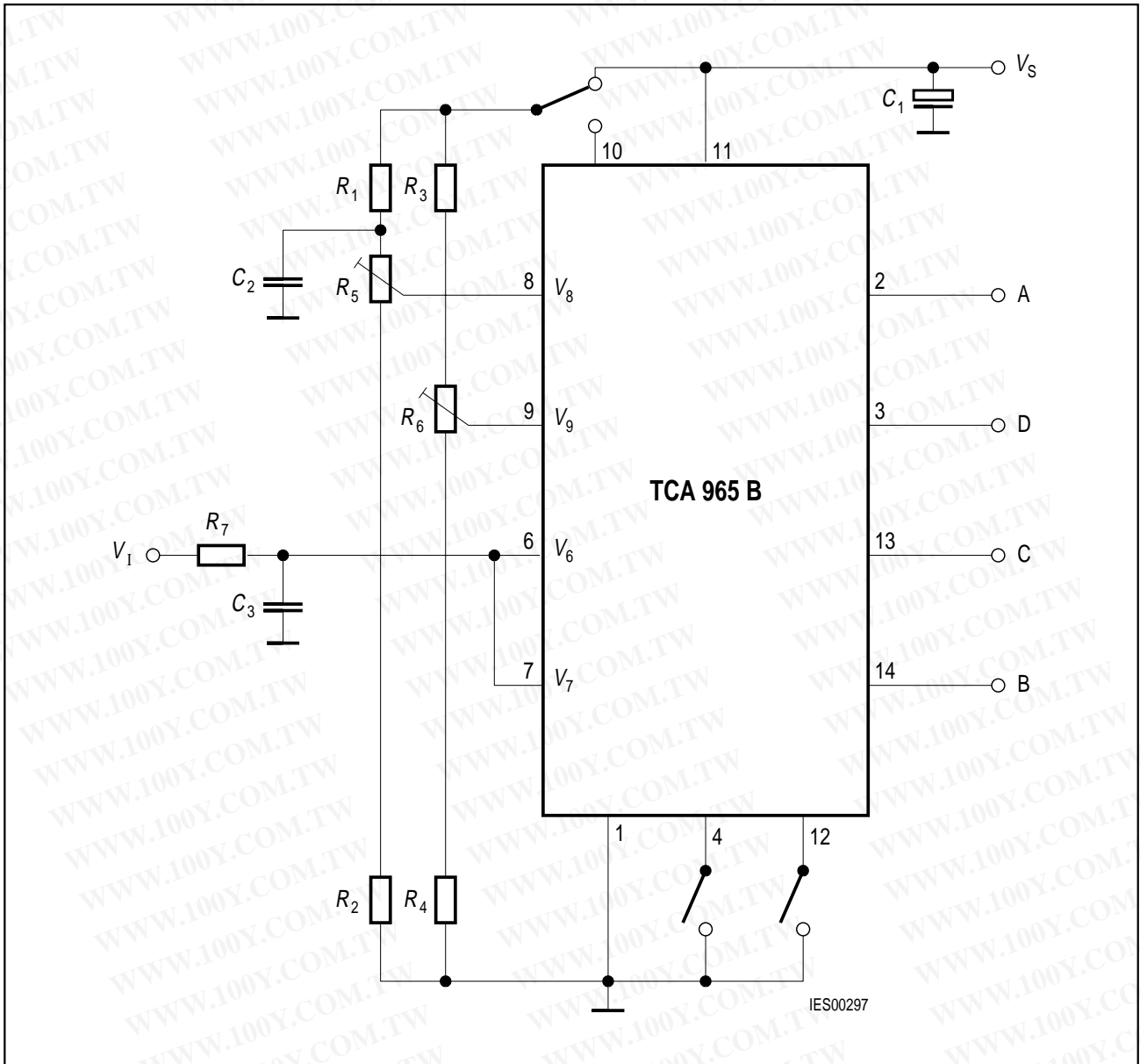
**Definition of the Offset Voltage  $V_{10}$**

$$V_{10} = \frac{V_L + V_U}{2} - V_7$$

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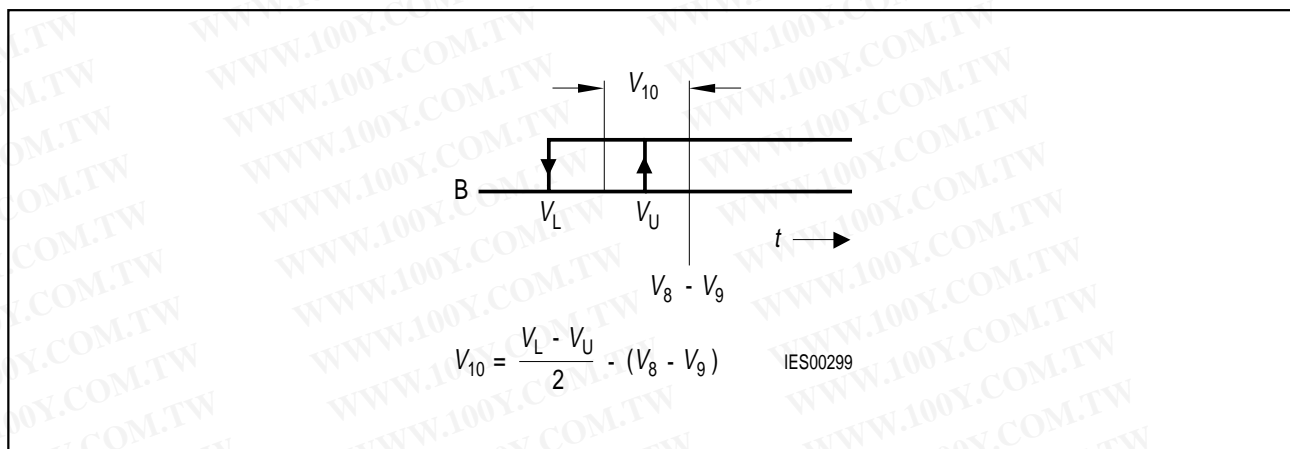


**Application Circuit 1**  
**Direct Setting of Lower and Upper Edge Voltages**



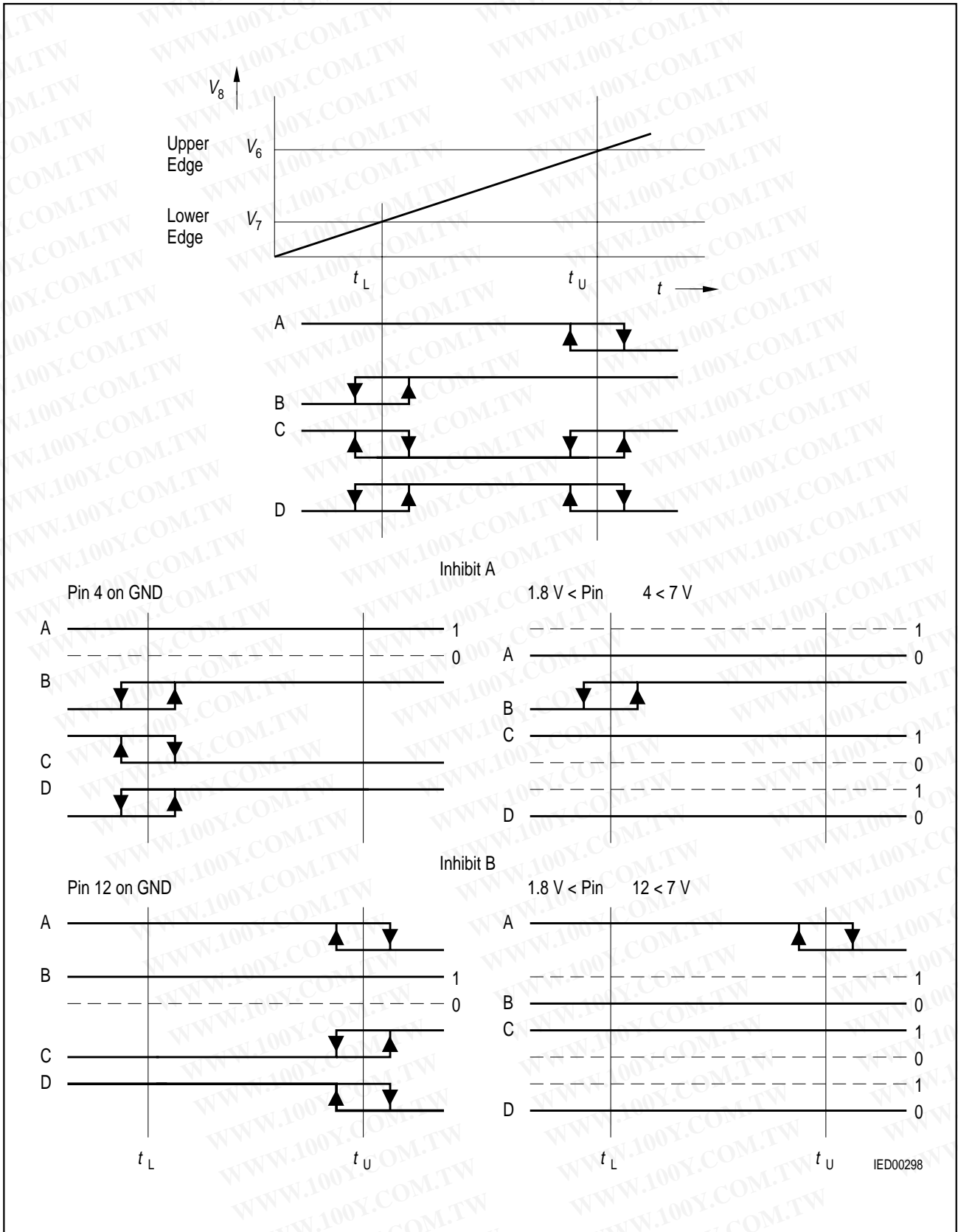
**Application Circuit 2**  
**Indirect Setting of Window by Center Voltage and Half-Window Width V**

- $V_6 = V_7 =$  Input voltage
- $V_8 =$  Center voltage
- $V_9 =$  Half window width

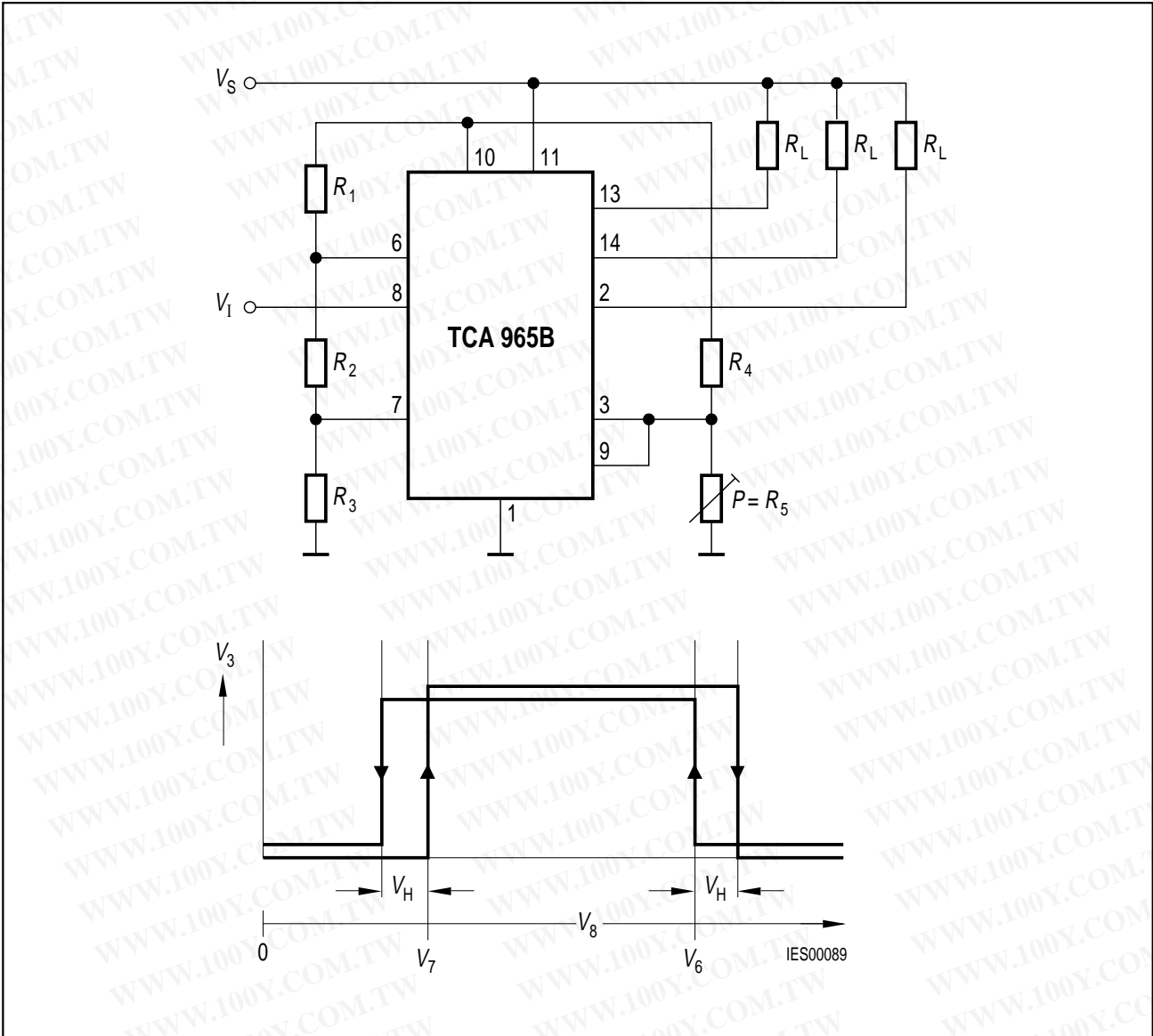


### Definition of the Offset Voltage $V_{10}$

$$V_{10} = \frac{V_L + V_U}{2} - (V_8 - V_9)$$



**Application Circuit 2**  
**Indirect Setting of Window by Center Voltage and Half-Window Width V**

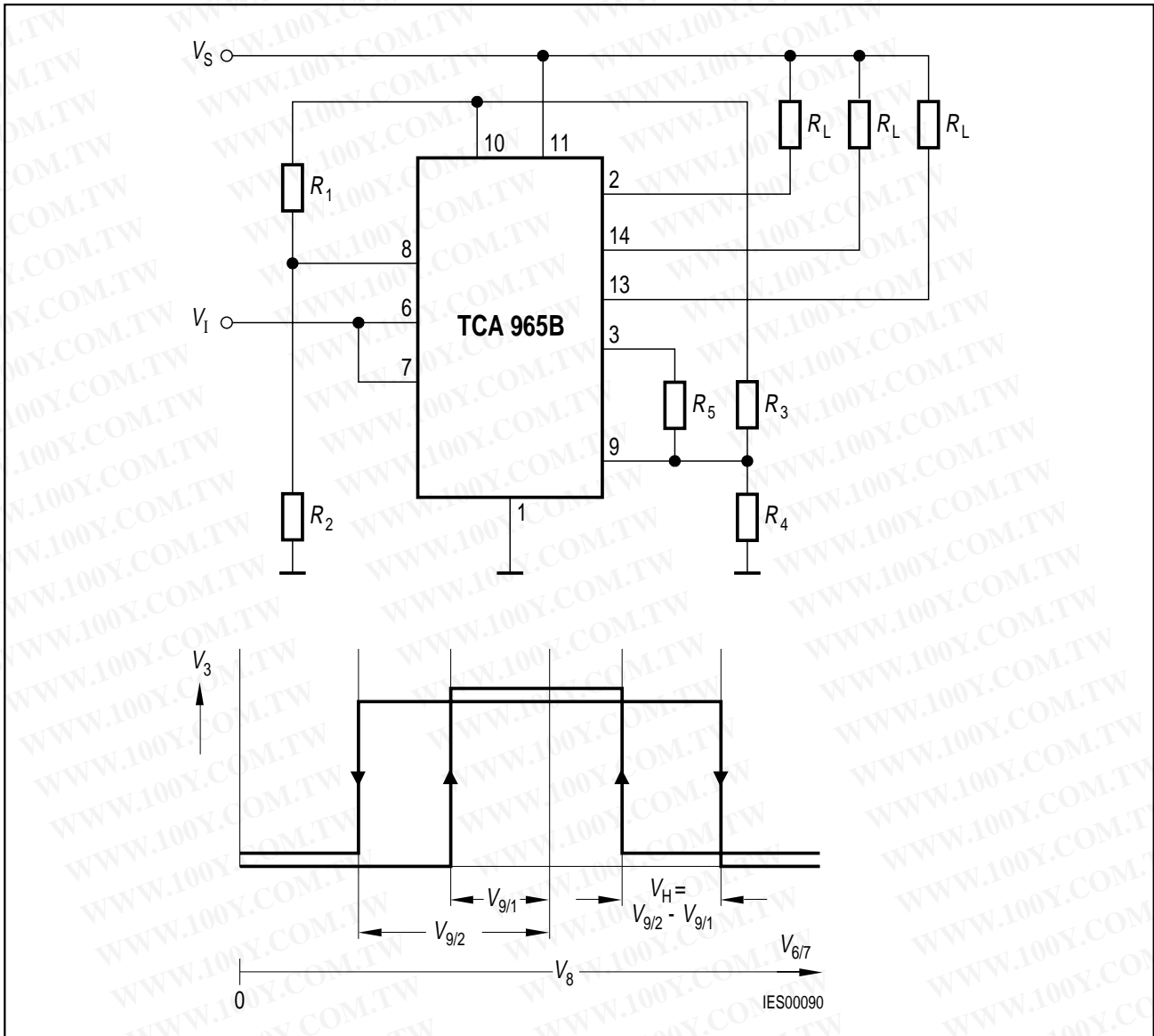


**Application Circuit 3**  
**Symmetrically Enlarged Edge Hysteresis in Direct Setting of Window**

**Calculation of Hysteresis  $V_H$**

$$V_H = V_{10} \frac{R_5}{R_4 + R_5}$$

$$\frac{V_{10}}{R_4 + R_5} + \frac{V_{10}}{R_1 + R_2 + R_3} \leq 10 \text{ mA}$$



**Application Circuit 4**  
**Symmetrically Enlarged Edge Hysteresis in Indirect Setting of Window**

**Calculation of Hysteresis  $V_H$**

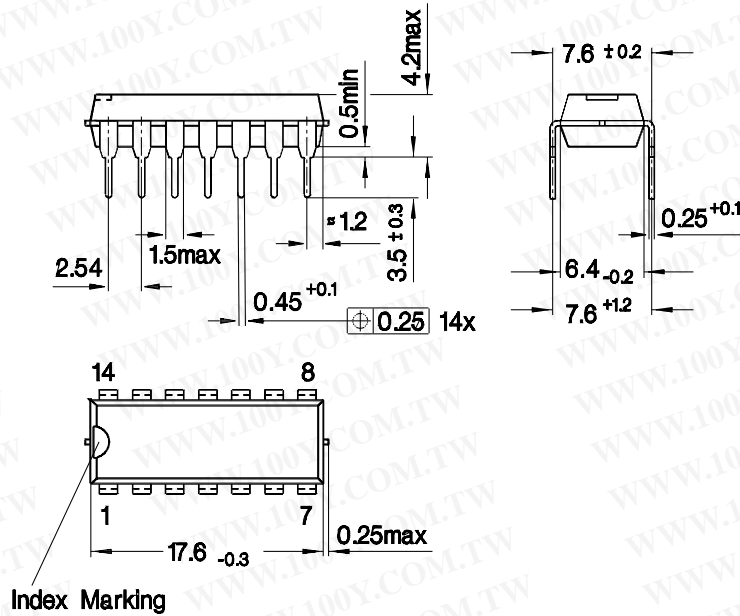
$$V_H = V_{9/2} - V_{9/1}$$

$$V_{9/1} = V_{10} \frac{R_4 \parallel R_5}{R_3 + R_4 \parallel R_5}$$

$$V_{9/2} = V_{10} \frac{R_4}{R_3 + R_4}$$

**P-DIP-14-1**

(Plastic Dual In-line Package)



GPD05005

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm