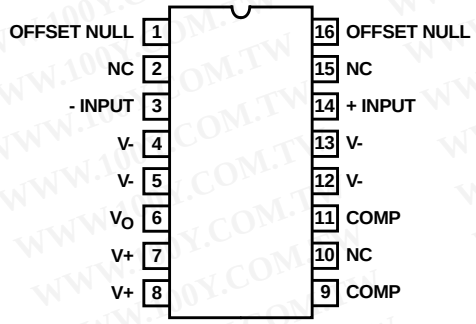
January 1999 File Number 1732.5

220MHz, Video Line Driver, High Speed Operational Amplifier

The CA3450 is a large signal video line driver and high speed operational amplifier capable of driving 50Ω transmission lines and flash A/Ds. The uncompensated unity gain crossing occurs at 230MHz without load. It can operate at dual or single supplies of ±7.25V or 14.5V, respectively. The CA3450 can be compensated with a single capacitor network. It has output drive capability of 75mA SINK or SOURCE. The CA3450 is capable of driving Flash A/Ds in video or high speed instrumentation (accurate) applications with bandwidth up to 10MHz. Offset voltage nulling terminals are also available.

Pinout

CA3450
(PDIP)
TOP VIEW



Features

- High Open Loop Gain at Video Frequencies
  - A_{OL} . . . . . >40dB at f = 5MHz
- Power Bandwidth of 10MHz . . . . . A_{CL} = 5; V_O = ±3.5V
- Slew Rate at Full Load . . . . . 330V/µs ($A_V \geq 10$)
- f_T = 220MHz; C_C = 0pF With a Load of 50Ω ||20pF|| 1MΩ (Scope Input)
- V_{OUT} = ±4.1V Into 75Ω
- Offset Null Terminals

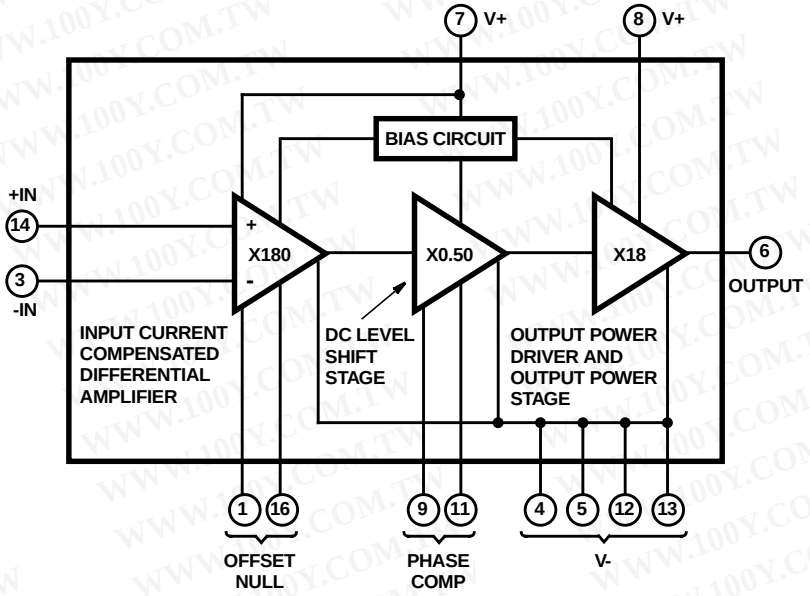
Applications

- Video Line Driver
- High Frequency Unity Gain Buffer
- Pulse Amplifier
- High Speed Comparator
- High Frequency Oscillator and Video Amplifiers
- Driver for A/Ds in Video Applications . . . . . .10MHz BW

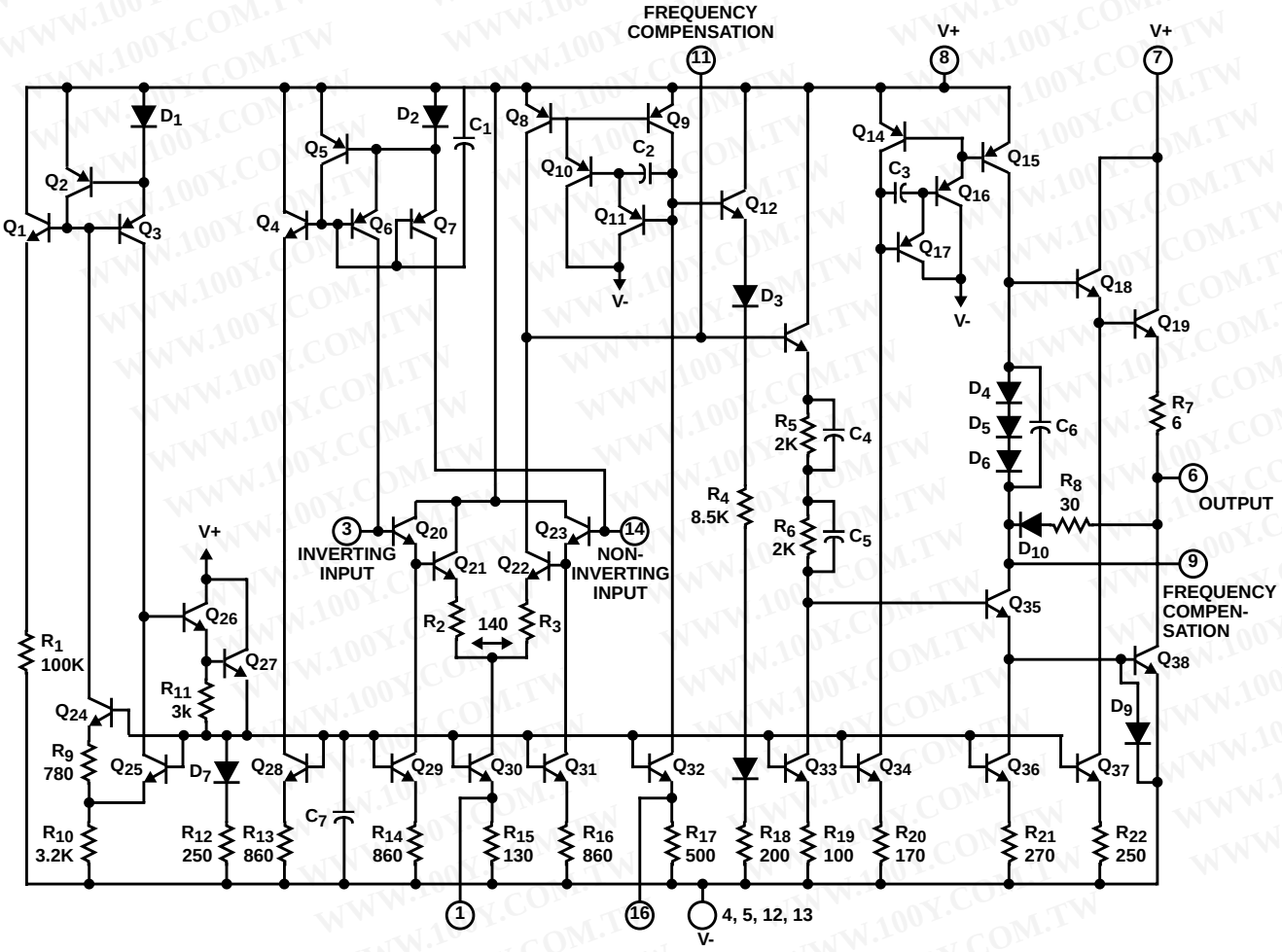
Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3450E	-40 to 85	16 Ld PDIP	E16.3

Block Diagram



Schematic Diagram



Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 14.5V
Differential Input Voltage 5V
Output Current 100mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	60

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

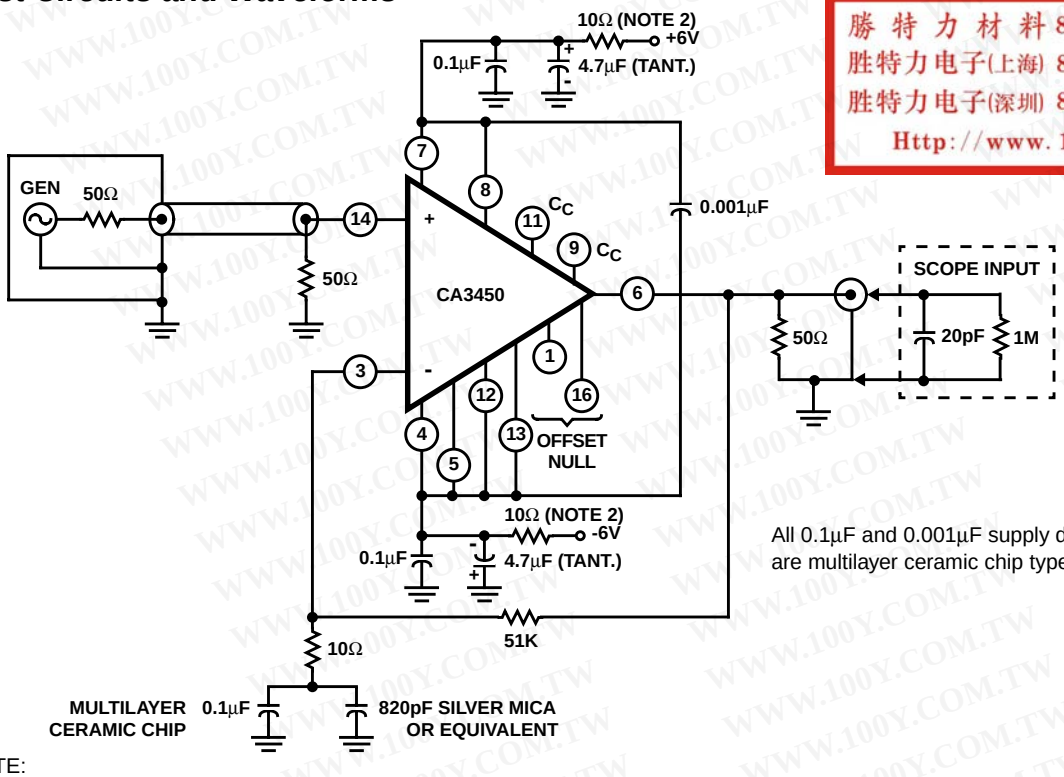
C_C = 5pF, V_{SUPPLY} = ±6V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
DC							
Input Offset Voltage	$\|V_{IO}\|$		25	-	8	20	mV
			Full	-	10	35	mV
Input Bias current	$\|I_{IB}\|$		25	-	100	400	nA
Input Offset Current	$\|I_{IO}\|$		25	-	50	200	nA
Open Loop DC Gain	A_{OL}	V_{OUT} = ±2.5V, R_L = 50Ω	25	60	70	-	dB
			Full	55	-	-	dB
Power Supply Rejection Ratio	PSRR	ΔV = ±1V	25	55	65	-	dB
Common Mode Rejection Ratio	CMRR	V_{ICR} = ±3.5V	25	50	60	-	dB
Common Mode Input Range	V_{ICR}		25	±3.5	±3.7	-	V
			Full	±3.0	-	-	V
Supply Current	I+		25	-	30	40	mA
			Full	-	-	50	mA
DYNAMIC							
-3dB Bandwidth A_V = 1 (See Figure 2) C_C = 5pF		No Load	25	-	200	-	MHz
		R_L = 1MΩ||20pF	25	-	190	-	MHz
		R_L = 50Ω||20pF	25	-	185	-	MHz
Bandwidth (Unity Gain Crossing) A_V = Open Loop C_C = 0 (See Figure 1)		No Load	25	210	230	-	MHz
		R_L = 20pF||1MΩ	25	180	200	-	MHz
		R_L = 50Ω||20pF	25	180	220	-	MHz
Bandwidth (Unity Gain Crossing) A_V = 10, C_C = 0pF $R_{FEEDBACK}$ = 450Ω $R_{PIN\ 3\ -\ G}$ = 50Ω (See Figure 2)		No Load	25	200	210	-	MHz
		50Ω	25	175	190	-	MHz
		1M||20pF	25	180	195	-	MHz
		50Ω||1M||20pF	25	170	188	-	MHz
Transient Response, Overshoot (See Figure 3)	OS	A_V = 1, C_C = 5pF, R_L = 50Ω||20pF	25	-	30	-	%
		A_V = 1, C_C = 5pF, No Load	25	-	20	-	%
		A_V ≥10, C_C = 0pF, R_L = 50Ω||20pF	25	-	10	-	%
Settling Time (See Figure 5) (2V Step, R_L = 50Ω||20pF)	t_S	A_V = -1, C_C = 5pF, 0.1%, 10 Bits	25	-	35	-	ns
		A_V = 1, C_C = 5pF, 0.1%, 10 Bits	25	-	50	-	ns
		A_V = 10, C_C = 0pF, 0.1%, 10 Bits	25	-	35	-	ns
		A_V = 10, C_C = 0pF, 1.0%, 7 Bits	25	-	25	-	ns

Electrical Specifications C_C = 5pF, V_{SUPPLY} = ±6V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP. (^oC)	MIN	TYP	MAX	UNITS
Slew Rate (See Figures 2, 4)	SR	A_V = 1, C_C = 5pF	No Load	25	-	220	-	V/µs
			R_L = 50Ω||20pF	25	-	160	-	V/µs
		A_V ≥10, C_C = 0pF	No Load	25	370	440	-	V/µs
			R_L = 50Ω||20pF	25	300	330	-	V/µs
Full Power Bandwidth (FPBW = SR/π V_{P-P})	FPBW	A_V = 5, C_C = 5pF, V_{OUT} = ±3.5V	No Load	25	-	10	-	MHz
			R_L = 50Ω||20pF	25	-	7.2	-	MHz
		A_V ≥10, C_C = 0pF, V_{OUT} = ±2.0V	No Load	25	29	35	-	MHz
			R_L = 50Ω||20pF	25	24	26	-	MHz
Input Noise Voltage	e_N	f = 1kHz		25	-	12	-	nV/√Hz
Differential Gain	DG	See Figure 8		25	-	0.2	-	%
Differential Phase	DP	See Figure 8		25	-	0.2	-	Degrees
Output Current	I_{OUT}	Into +4V or -4V		25	60	75	-	mA
Output Voltage Swing	V_{OM}^+	R_L = 75Ω		25	3.9	4.1	-	V
	V_{OM}^-			25	-3.9	-4.1	-	V
Input Capacitance	C_I	f = 1MHz		25	-	2.2	-	pF
Input Resistance	R_I			25	-	1	-	MΩ
Output Resistance	R_{OUT}	See Figure 14, A_V = 1, 30MHz		25	-	4	-	Ω

Test Circuits and Waveforms



All 0.1µF and 0.001µF supply decoupling capacitors are multilayer ceramic chip types.

NOTE:

2. A 10Ω, $^1/_4$W supply decoupling resistor is shown in all application circuits of this device. The resistor serves two purposes. First it provides a means of decoupling the IC directly at its terminal without introducing additional supply resonance due to parallel connected capacitors. Second, it also provides protection for the device in event of a sustained short circuit applied directly to the output terminals.

FIGURE 1. OPEN LOOP GAIN vs FREQUENCY TEST CIRCUIT

Test Circuits and Waveforms (Continued)

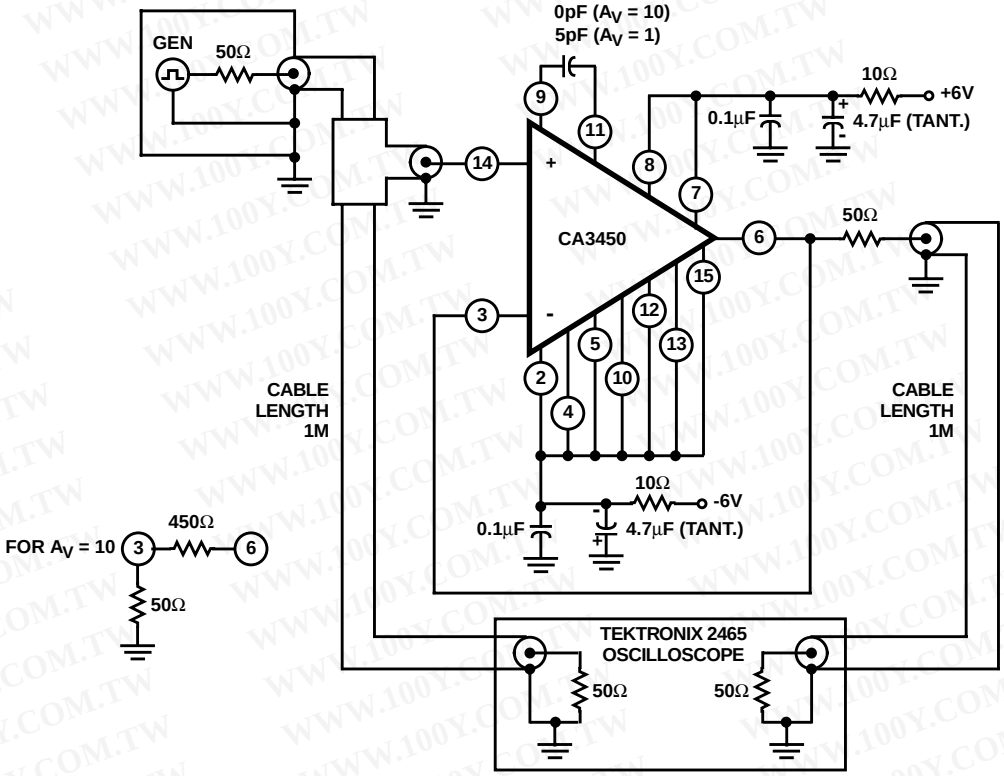


FIGURE 2. UNITY GAIN AND X10 NON-INVERTING AMPLIFIER/AND SLEW RATE TEST CIRCUIT

Transient Response Waveforms

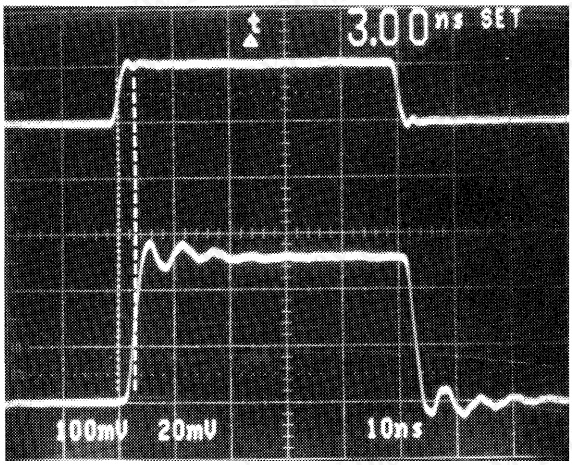


FIGURE 3. TRANSIENT RESPONSE WAVEFORM

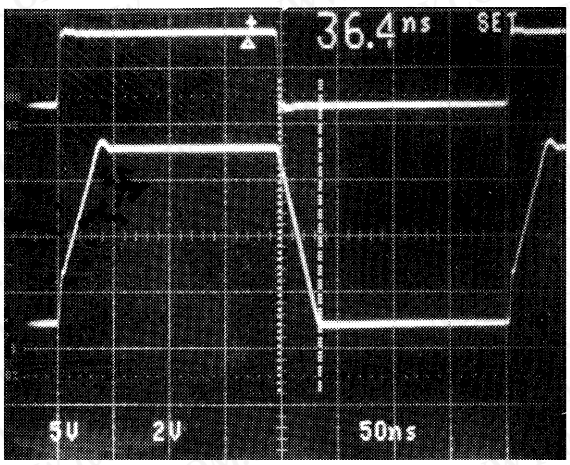


FIGURE 4. SLEW RATE WAVEFORM

Test Circuits and Waveforms (Continued)

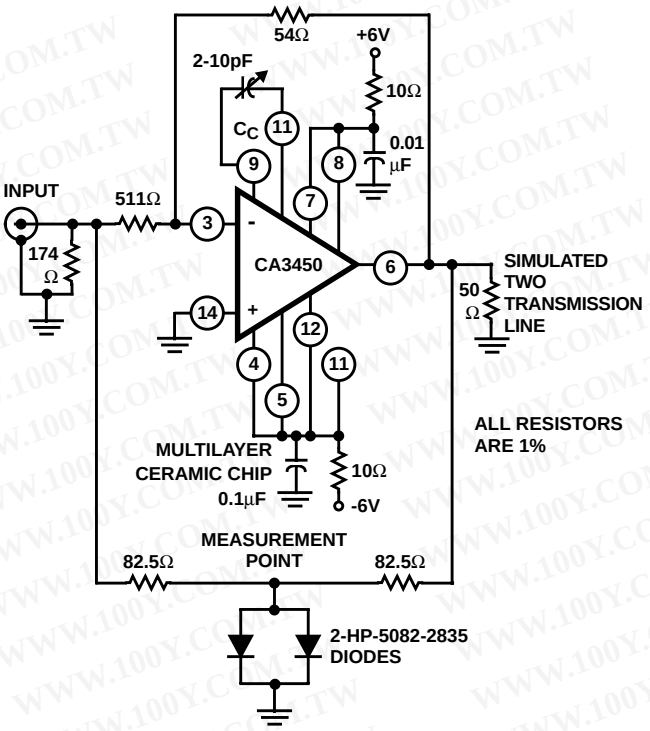


FIGURE 5. CIRCUIT USED TO MEASURE SETTLING TIME

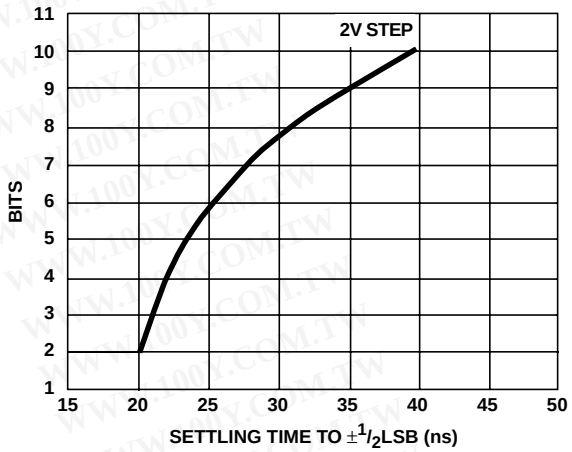


FIGURE 6. ACCURACY IN BITS AS A FUNCTION OF SETTLING TIME

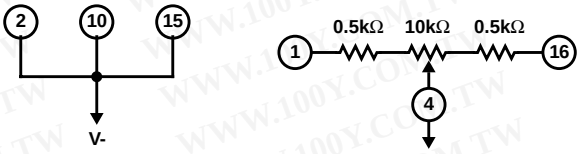


FIGURE 7. NULLING CIRCUIT FOR THE CA3450

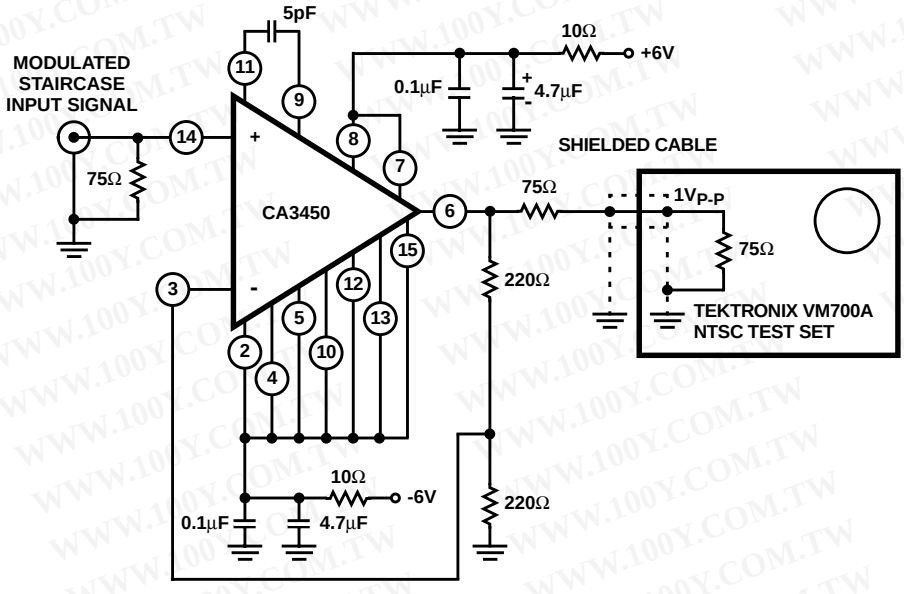


FIGURE 8. CONFIGURATION USED TO MEASURE DIFFERENTIAL GAIN AND PHASE

Test Circuits and Waveforms (Continued)

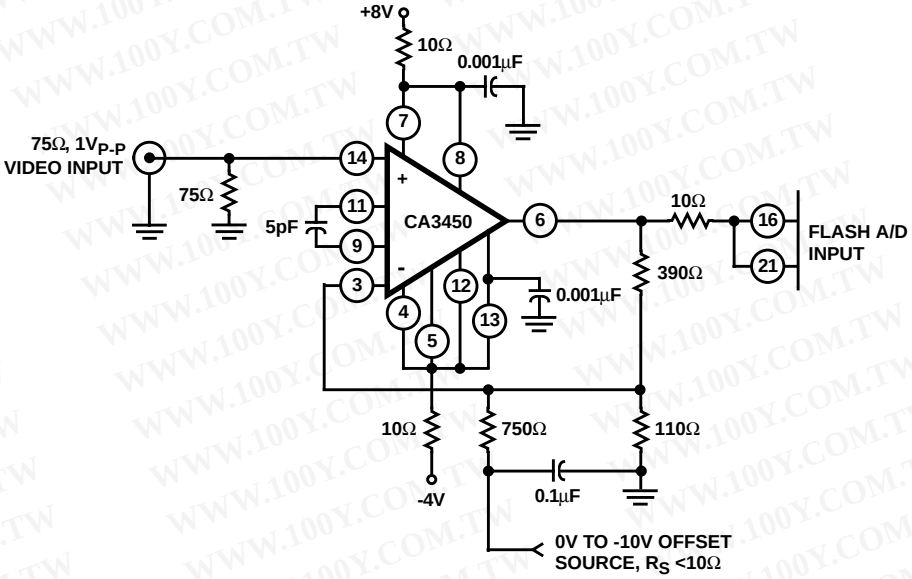


FIGURE 9. TYPICAL HIGH BANDWIDTH X5 AMPLIFIER FOR DRIVING THE CA3318 FLASH A/D

Typical Performance Curves

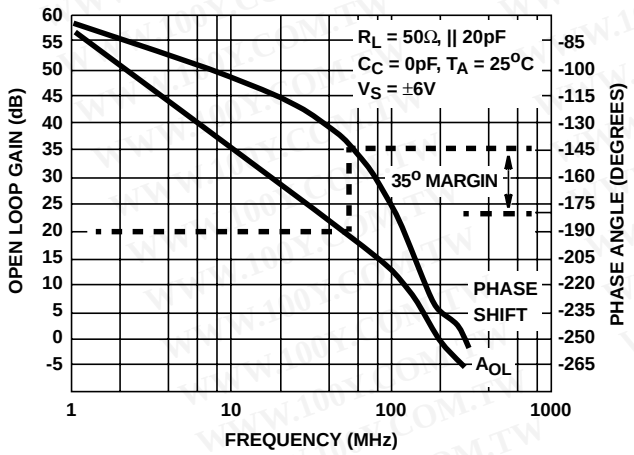


FIGURE 10. BODE PLOT FOR THE CA3450

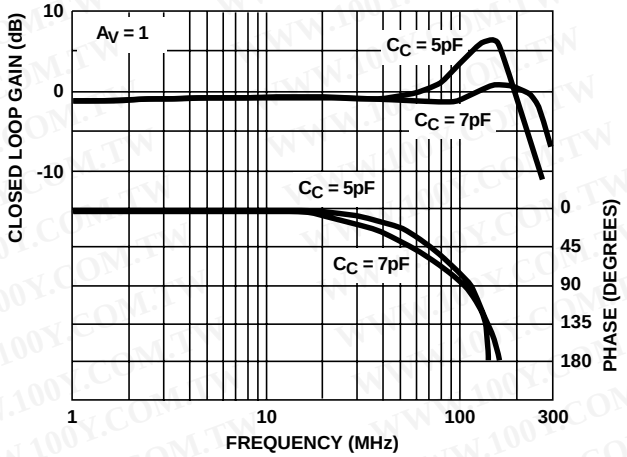


FIGURE 11. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

Typical Performance Curves (Continued)

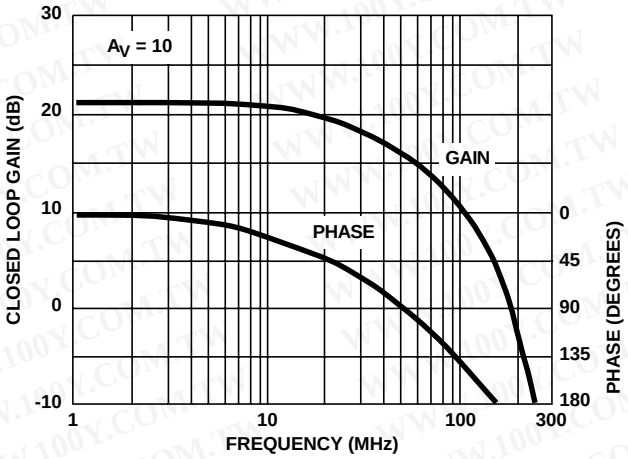


FIGURE 12. CLOSED LOOP GAIN AND PHASE vs FREQUENCY

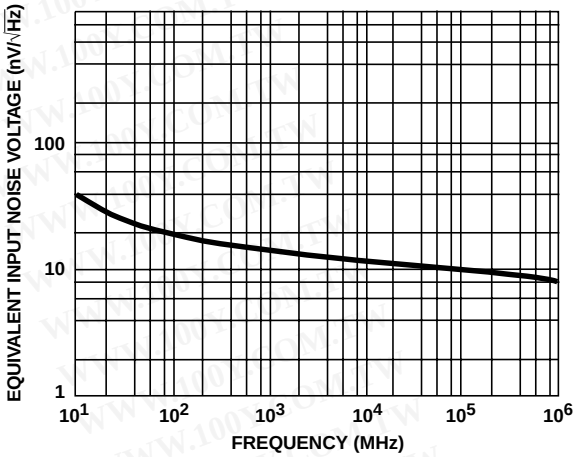


FIGURE 13. EQUIVALENT INPUT NOISE vs FREQUENCY

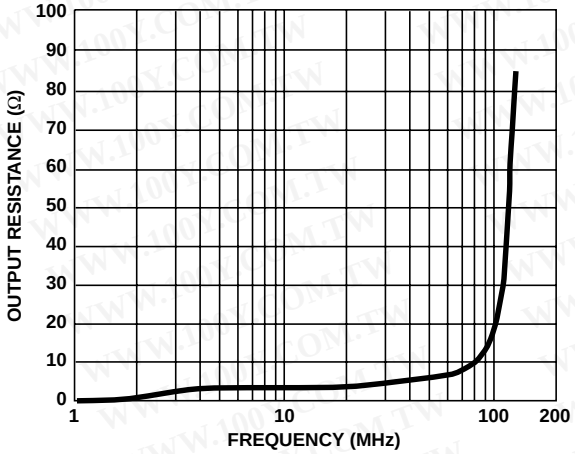


FIGURE 14. OUTPUT RESISTANCE vs FREQUENCY

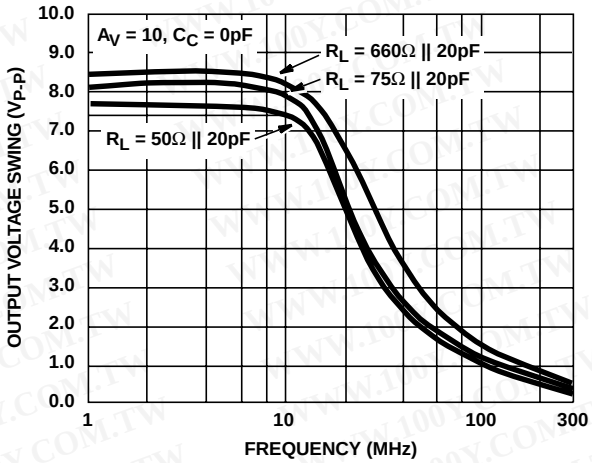
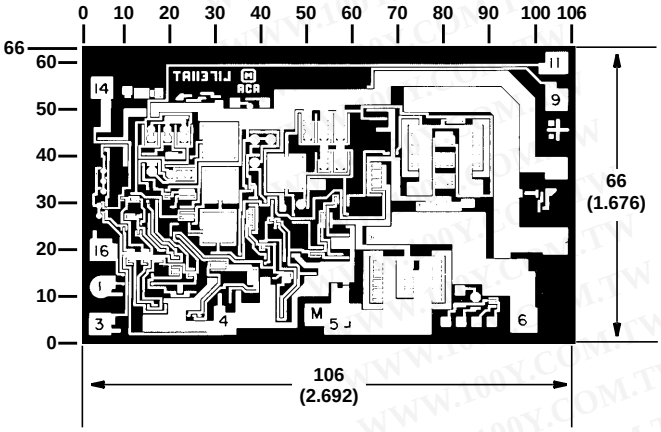


FIGURE 15. OUTPUT VOLTAGE vs FREQUENCY

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3mils to +6mils applicable to the nominal dimensions shown.