



6-Channel, Serial Input Master/Balance Volume Controls

SSM2160

FEATURES

Clickless Digitally Controlled Level Adjustment

SSM2160: 6 Channels

7-Bit Master Control Gives 128 Levels of Attenuation

5-Bit Channel Controls Give 32 Levels of Gain

Master/Channel Step Size Set by External Resistors

100 dB Dynamic Range

Automatic Power-On Mute

Excellent Audio Characteristics:

0.01% THD+N

0.001% IMD (SMPTE)

-90 dBu Noise Floor

-80 dB Channel Separation

90 dB SNR

Single-and Dual-Supply Operation

APPLICATIONS

Home Theater Receivers

Surround Sound Decoders

Circle Surround® and AC-3® Decoders

DSP Soundfield™ Processors

HDTV and Surround TV Audio Systems

Automotive Surround Sound Systems

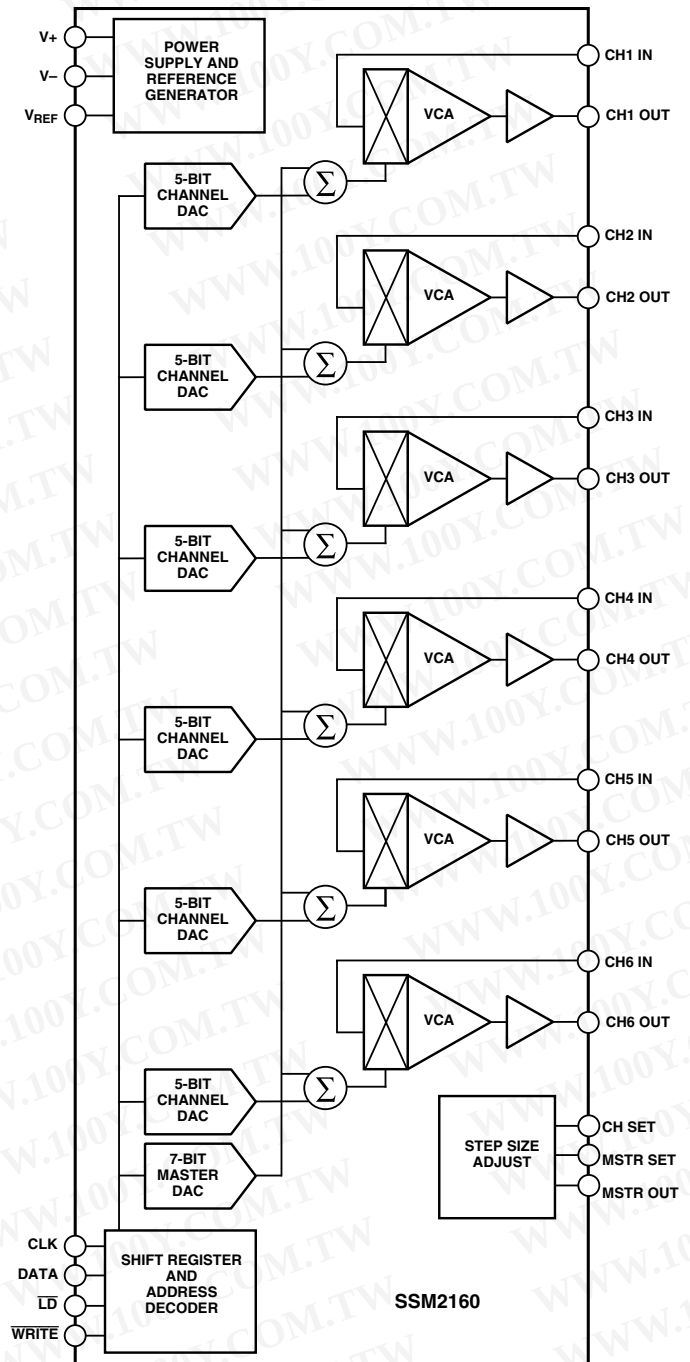
Multiple Input Mixer Consoles and Amplifiers

GENERAL DESCRIPTION

The SSM2160 allows digital control of volume of six audio channels, with a master level control and individual channel controls. Low distortion VCAs (voltage controlled amplifiers) are used in the signal path. By using controlled rate-of-change drive to the VCAs, the "clicking" associated with switched resistive networks is eliminated in the master control. Each channel is controlled by a dedicated 5-bit DAC providing 32 levels of gain. A master 7-bit DAC feeds every control port giving 128 levels of attenuation. Step sizes are nominally 1 dB and can be changed by external resistors. Channel balance is maintained over the entire master control range. Upon power-up, all outputs are automatically muted. A 3-wire or 4-wire serial data bus enables interfacing with most popular microcontrollers. Windows® software and an evaluation board for controlling the SSM2160 are available.

The SSM2160 can be operated from single supplies of +10 V to +20 V or dual supplies from ± 5 V to ± 10 V. An on-chip reference provides the correct analog common voltage for single-supply applications. The SSM2160 comes in a SOIC package; see the Ordering Guide for details.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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SSM2160—SPECIFICATIONS ($V_S = \pm 6\text{ V}$, $T_A = 25^\circ\text{C}$, $A_V = 0\text{ dB}$, $f_{\text{AUDIO}} = 1\text{ kHz}$, $f_{\text{CLOCK}} = 250\text{ kHz}$, $R_L = 10\text{ k}\Omega$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AUDIO PERFORMANCE						
Noise Floor	NFL	$V_{\text{IN}} = \text{GND}$, BW = 20 kHz, $A_V = 0\text{ dB}$ ¹		-90		dBu
Total Harmonic Distortion + Noise	THD+N	Second and Third Harmonics Only, $V_{\text{OUT}} = 0\text{ dBu}$ ² $A_V = 0\text{ dB}$		0.01	0.035	%
Channel Separation		Any Channel to Another		80		dB
Dynamic Range		NFL to Clip Point		100		dB
ANALOG INPUT						
Maximum Level	$V_{\text{IN max}}$	$V_S = \pm 10\text{ V}$			1.8	V rms
Impedance	Z_{IN}	Any Channel		10		k Ω
ANALOG OUTPUT						
Maximum Level ³		$V_S = \pm 10\text{ V}$, All Conditions of Master Attenuation and Channel Gain			1.8	V rms
Impedance	Z_{OUT}			10		Ω
Offset Voltage				20		mV
Minimum Resistive Load	$R_L\text{ min}$		10			k Ω
Maximum Capacitive Load	$C_L\text{ max}$				50	pF
MASTER ATTENUATOR ERROR						
$A_V = 0\text{ dB}$		Measured from Best Fit of All Channels from 0 dB and -127 dB (or Noise Floor)		± 0.5		dB
$A_V = -20\text{ dB}$		Channel Gain = 0 dB		± 1.0		dB
$A_V = -40\text{ dB}$		Channel Gain = 0 dB		± 2.0		dB
$A_V = -60\text{ dB}$		Channel Gain = 0 dB		± 2.5		dB
CHANNEL MATCHING						
					± 1.0	dB
CHANNEL GAIN ERROR						
		Master Attenuation = 0 dB				
$A_V = 0\text{ dB}$				± 0.5		dB
$A_V = 10\text{ dB}$				± 1.0		dB
$A_V = 31\text{ dB}$				± 2.0		dB
MUTE ATTENUATION						
		$V_{\text{IN}} = 0\text{ dBu}$			-95	dB
VOLTAGE REFERENCE						
Accuracy	V_{REF}	Percent of $\frac{(V+) + (V-)}{2}$			± 5	%
Output Impedance					5	Ω
CONTROL LOGIC						
Logic Thresholds						
High (1)		Re: DGND		2.0		V
Low (0)					0.8	V
Input Current					± 1	μA
Clock Frequency				1	1000	kHz
Timing Characteristics		See Timing Diagrams				
POWER SUPPLIES						
Voltage Range						
SSM2160	V_S	Single Supply	10		20	V
SSM2160	$V+, V-$	Dual Supply	± 5		± 10	V
Supply Current		No Load		20	28	mA

NOTES

¹Master = 0 dB; Channel = 0 dB.

²Input level adjusted accordingly. 0 dBu = 0.775 V rms.

³For other than $\pm 10\text{ V}$ supplies, maximum is $V_S/4$.

Specifications subject to change without notice.

TIMING CHARACTERISTICS

Timing Symbol	Description	Min	Typ	Max	Unit
t_{CL}	Input Clock Pulsewidth, Low	200			ns
t_{CH}	Input Clock Pulsewidth, High	200			ns
t_{DS}	Data Setup Time	50			ns
t_{DH}	Data Hold Time	75			ns
t_{CW}	Positive CLK Edge to End of Write	100			ns
t_{WC}	Write to Clock Setup Time	50			ns
t_{LW}	End of Load Pulse to Next Write	50			ns
t_{WL}	End of Write to Start of Load	50			ns
t_L	Load Pulsewidth	250			ns
t_{W3}	Load Pulsewidth (3-Wire Mode)	250			ns

NOTES

1. An idle HI (CLK-HI) or idle LO (CLK-LO) clock may be used. Data is latched on the negative edge.
2. For SPI™ or Microwire™ 3-wire bus operation, tie LD to WRITE and use WRITE pulse to drive both pins. (This generates an automatic internal load signal.)
3. If an idle HI clock is used, t_{CW} and t_{WL} are measured from the final negative transition to the idle state.
4. The first data byte selects an address (MSB HI), and subsequent MSB LO states set gain/attenuation levels. Refer to the Address/Data Decoding Truth Table.
5. Data must be sent MSB first.

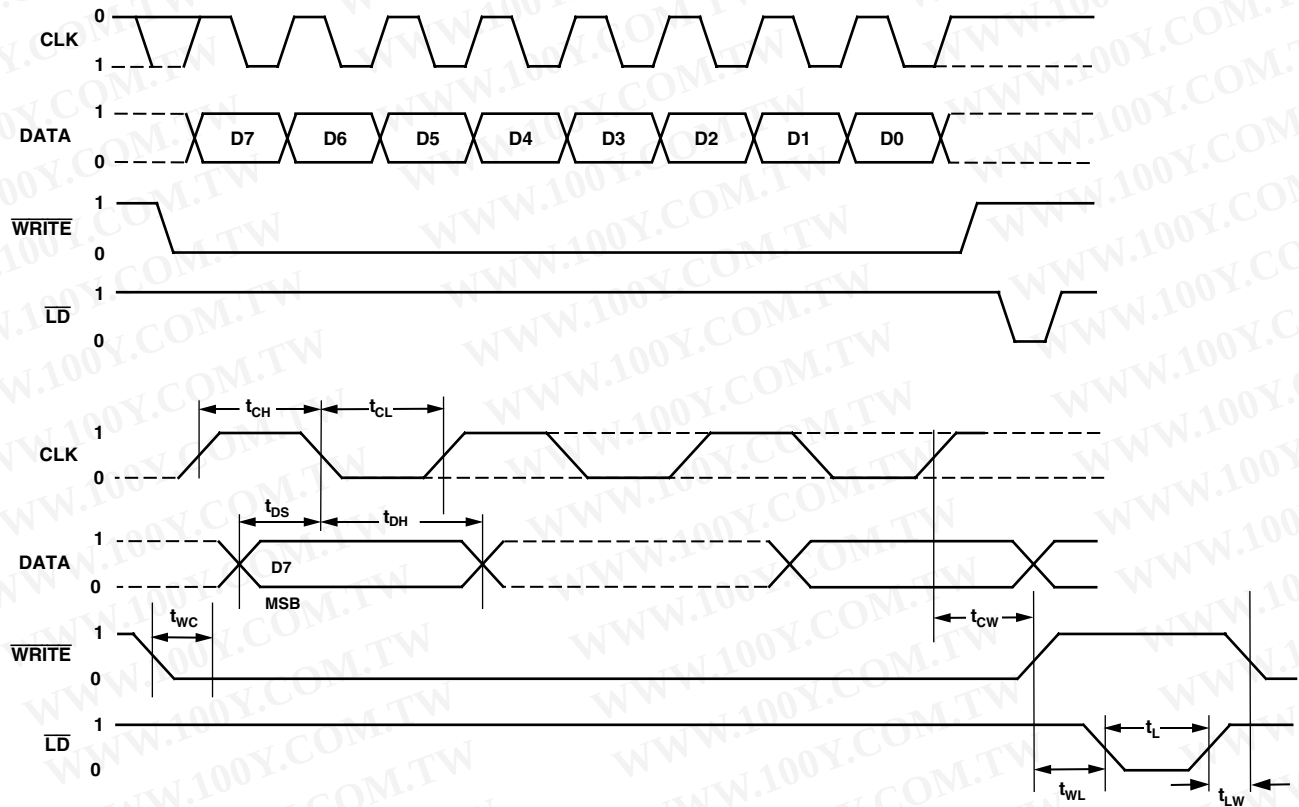


Figure 1. Timing Diagrams

SSM2160

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage

Dual Supply ± 18 V

Single² (V_S) 36 V

Logic Input Voltage -0.3 V to +5 V

Operating Temperature Range 0°C to 70°C

Storage Temperature Range -65°C to +150°C

Junction Temperature Range -65°C to +165°C

Lead Temperature Range (Soldering, 60 sec) 300°C

ESD Ratings

883 (Human Body) Model 2.5 kV

PACKAGE THERMAL INFORMATION

Package Type	θ_{JA} ³	θ_{JC}	Unit
24-Lead SOIC	71	23	°C/W

NOTES

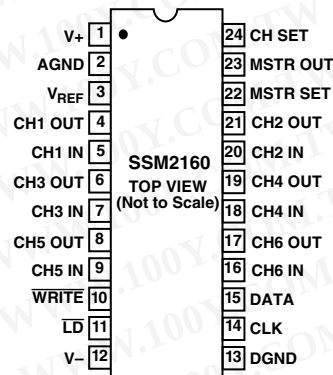
¹ Absolute maximum ratings apply at 25°C, unless otherwise noted.

² V_S is the total supply span from V+ to V-.

³ θ_{JA} is specified for the worst-case conditions for device soldered onto a circuit board for SOIC packages.

PIN CONFIGURATION

24-Lead SOIC



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
SSM2160S	0°C to 70°C	24-Lead SOIC	R-24
SSM2160S-REEL	0°C to 70°C	24-Lead SOIC	R-24
EVAL-SSM2160EB		Evaluation Board	

CAUTION

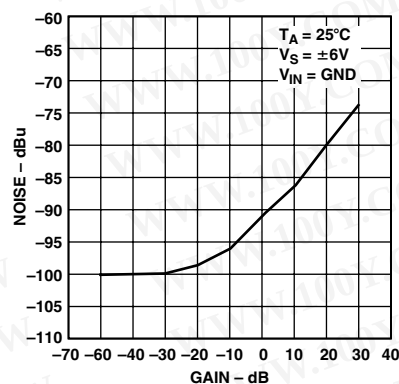
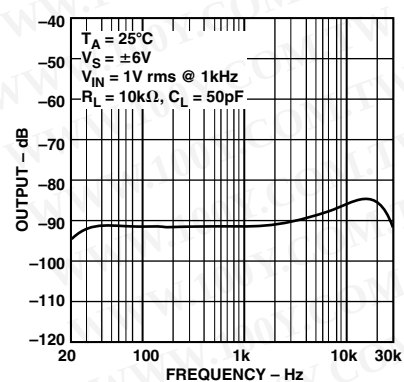
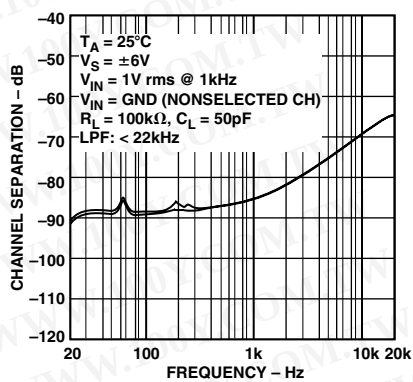
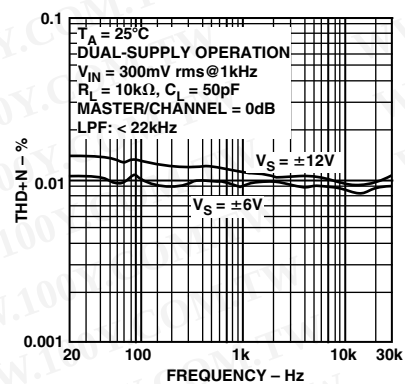
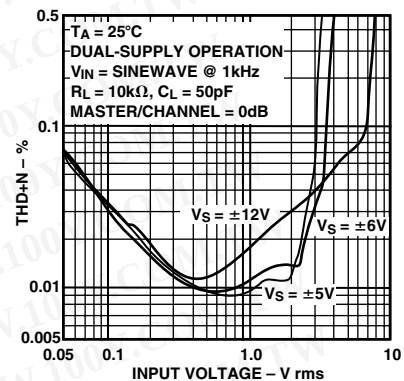
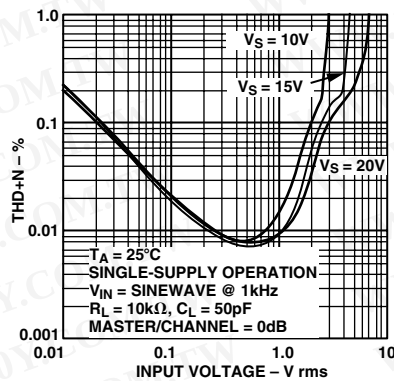
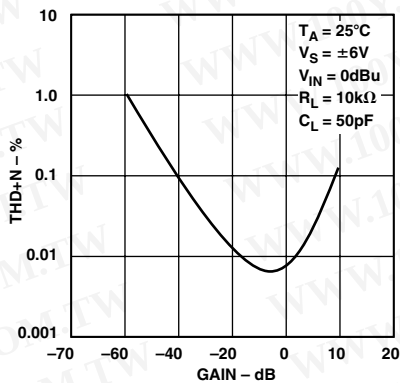
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2160 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



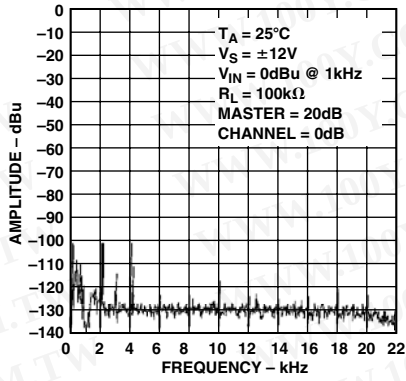
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	V+	Positive Power Supply. Refer to the Application Information section for details on the power supply.
2	AGND	Internal Ground Reference for the Audio Circuitry. When operating the SSM2160 from dual supplies, AGND should be connected to ground. When operating from a single supply, AGND should be connected to V_{REF} , the internally generated voltage reference. AGND may also be connected to an external reference. Refer to the Application Information section for more information on the power supply.
3	V_{REF}	V_{REF} is the internally generated ground reference for the audio circuitry obtained from a buffered divider between V+ and V-. In a dual-supply application with the AGND pin connected to ground, V_{REF} should be left floating. In a single-supply application, V_{REF} should be connected to AGND. Refer to the Application Information section for more information on the power supply.
4	CH1 OUT	Audio Output from Channel 1
5	CH1 IN	Audio Input to Channel 1
6	CH3 OUT	Audio Output from Channel 3
7	CH3 IN	Audio Input to Channel 3
8	CH5 OUT	Audio Output from Channel 5
9	CH5 IN	Audio Input to Channel 5
10	$\overline{WRITE}$	A logic low voltage enables the SSM2160 to receive information at the DATA input (Pin 15). A logic high retains data at their previous settings (Figure 1). Serves as CHIP SELECT.
11	$\overline{LD}$	Loads the Information Retained by $\overline{WRITE}$ into the SSM2160 at logic low (Figure 1).
12	V-	Negative Power Supply. Connect to ground in a single-supply application. Refer to the Application Information section for details on the power supply.
13	DGND	Digital Ground Reference. This pin should always be connected to ground. All digital inputs, including $\overline{WRITE}$, $\overline{LD}$, CLK, and DATA are TTL input compatible; drive currents are returned to DGND.
14	CLK	Clock Input. It is positive edge triggered (Figure 1).
15	DATA	Channel and master control information flows MSB first into the DATA pin. Refer to the Address/Data Decoding Truth Table, Figure 7, for information on how to control the VCAs.
16	CH6 IN	Audio Input to Channel 6
17	CH6 OUT	Audio Output from Channel 6
18	CH4 IN	Audio Input to Channel 4
19	CH4 OUT	Audio Output from Channel 4
20	CH2 IN	Audio Input to Channel 2
21	CH2 OUT	Audio Output from Channel 2
22	MSTR SET	Connected to the inverting input of an I-V converting op amp. It is used to generate a master control voltage from the master control DAC current output. A resistor connected from MSTR OUT to MSTR SET reduces the step size of the master control. See the Master/Channel Step Sizes section for more details. A 10 μ F capacitor should be connected from MSTR OUT to MSTR SET to eliminate the zipper noise in the master control.
23	MSTR OUT	Connected to the output of the I-V converting op amp. See MSTR SET description.
24	CH SET	The step size of the channel control can be increased by connecting a resistor from CH SET to V+. No connection to CH SET is required if the default value of 1 dB per step is desired. Minimum of 10 Ω external resistor. See the Master/Channel Step Sizes section for details.

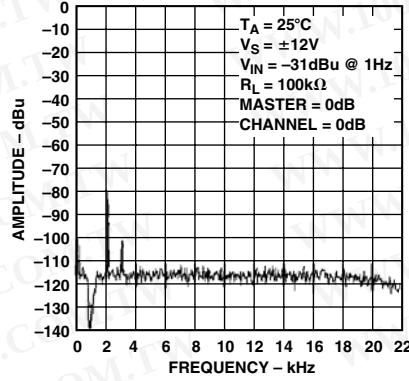
SSM2160—Typical Performance Characteristics



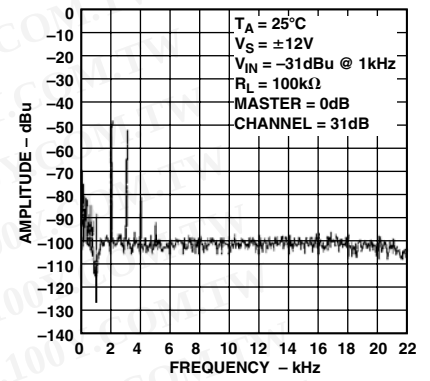
Typical Performance Characteristics—SSM2160



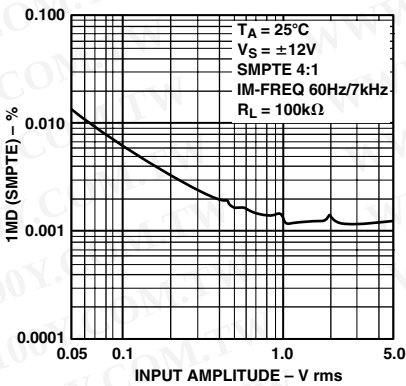
TPC 8. THD vs. Frequency (FFT)



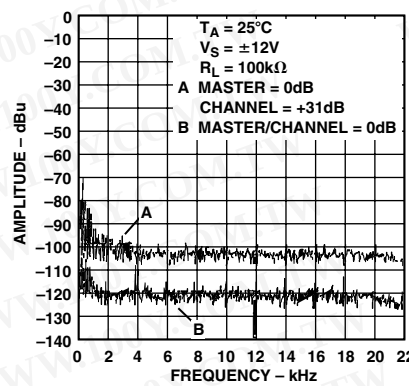
TPC 9. THD vs. Frequency (FFT)



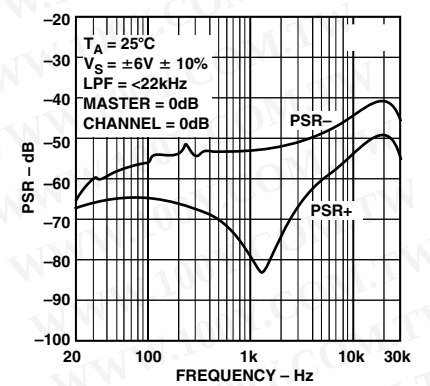
TPC 10. THD vs. Frequency (FFT)



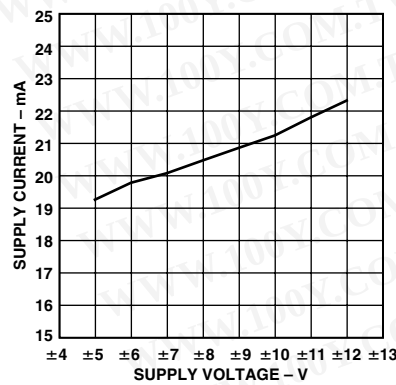
TPC 11. SMPTE IM vs. Amplitude V rms



TPC 12. Noise Floor FFT



TPC 13. PSR vs. Frequency



TPC 14. I_{SV} vs. V_S

SSM2160

APPLICATIONS INFORMATION

General

The SSM2160 is a 6-channel volume control intended for multichannel audio applications. While dual-channel controls sufficed for stereo applications, rapidly emerging home theater surround sound and auto sound venues demand both 4-channel and 6-channel high performance controls. Line level signals are fed to the six high impedance inputs. The system microcontroller sets the gain of the six channels via a 3-wire or 4-wire data bus. In a home theater receiver, the outputs may be fed to the power amplifiers or buffered and connected to pre-out/amp-in ports on the rear panel. Refer to Figure 5 for a typical signal chain using the SSM2160. The master control serves the volume control function, and the channel control serves the balance function. The 6-channel capability allows complete control of the front left, front right, center, rear left, rear right, and sub-bass audio channels.

Power Supplies vs. Signal Levels

The SSM2160 can be operated from dual supplies from ± 5 V to ± 10 V and from single supplies from +10 V to +20 V. To keep power dissipation to a minimum, use the minimum power supply voltages that will support the maximum input and output signal levels. The peak-to-peak output signal level must not exceed 1/4 of the total power supply span, from V+ to V-. This restriction applies for all conditions of input signal levels and gain/attenuation settings. Table I shows supply voltages for several typical output signal levels for the device. An on-chip buffered voltage divider provides the correct analog common voltage for single-supply applications.

Table I. Signal Levels vs. Power Supplies

Max Output, V _{rms} (V p-p)	Max Output (dBu)	Single +V _S (V)	Dual $\pm V_S$ (V)
0.9 (2.5)	+1.3	10	± 5
1.1 (3.0)	+3.0	12	± 6
1.3 (3.7)	+4.5	15	± 7.5
1.8 (5.0)	+7.3	20	± 10

Dual Power Supplies

As shown in Figure 2, the AGND pin should be connected to ground and V_{REF} should be left floating. The digital ground pin, DGND, should always be connected to ground for either single- or dual-supply configurations. Pins 1 and 12 should each have a 10 μ F capacitor connected to ground, with a 0.1 μ F capacitor placed as close as possible to the SSM2160 to help reduce the effects of high frequency power supply noise. When a switching power supply is used, or if the power supply lines are noisy, additional filtering of the power supply lines may be required.

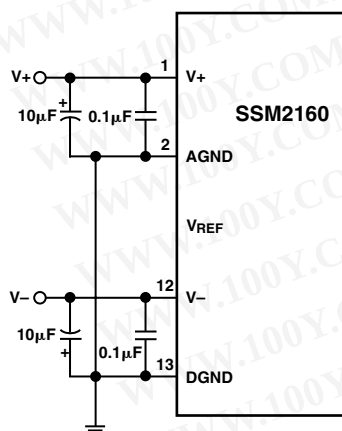


Figure 2. Dual-Supply Configuration

Single Power Supply

When a single supply is used, it is necessary to connect AGND (Pin 2) to V_{REF} (Pin 3), as shown in Figure 3. V_{REF} supplies a voltage midway between the V+ and V- pins from a buffered resistive divider. When supplying this reference to stages ahead of the SSM2160 (to eliminate the need for input dc blocking capacitors, for example), the use of an additional external buffer, as shown in Figure 4, may be necessary to eliminate any noise pickup.

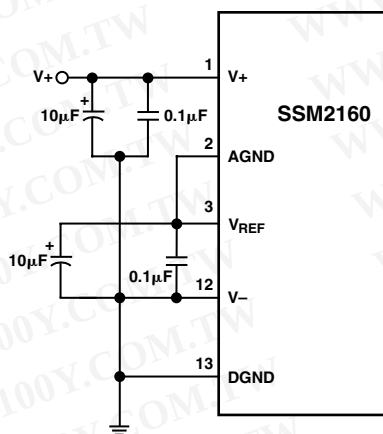


Figure 3. Single-Supply Configuration

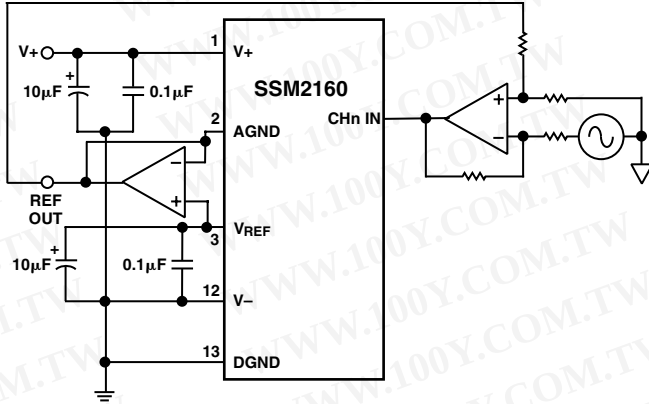


Figure 4. Single-Supply Operation with V_{REF} Buffer

Signal Chain Considerations

The SSM2160 is capable of providing an extremely wide control range, from -127 dB of attenuation (limited only by the noise floor) to $+31$ dB of gain. When configuring the system, the SSM2160 should be in the signal chain where input signals allow the minimum VCA gain to be used, thus ensuring the lowest distortion operation. In consumer products, sources that supply line level signals include FM/AM tuner, phono preamp, cassette deck, CD, laser disk, VCR, LINE, AUX, and microphone preamp. Figure 5 shows a typical application where the SSM2160 has been placed between a surround sound decoder and the power amplification stages. This allows the user to adjust both volume and balance between six speakers through the use of the master and channel controls.

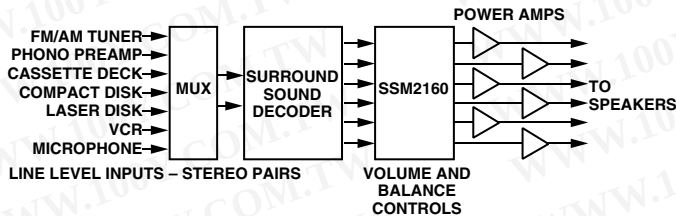


Figure 5. Typical Signal Chain Using the SSM2160

Digital Control Range Plan

The SSM2160 may be modeled as six ganged potentiometers followed by individual programmable gain channel amplifiers, as shown in Figure 6. In actuality, each channel's signal level is set by a VCA that can give gain or attenuation, depending upon the control voltage supplied. The input potentiometers have a maximum gain 0 dB (unity), a minimum gain of -127 dB, and change in 1 dB steps. The channel amplifiers each have minimum gain of 0 dB and a maximum gain of 31 dB and also change in 1 dB steps. The data settings for the attenuation of the master potentiometer and the channel amplifier are shown in Table II.

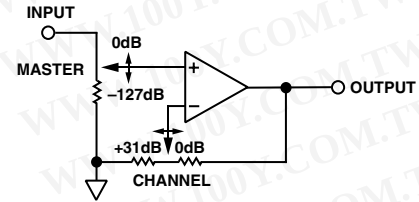


Figure 6. Potentiometer Representation of SSM2160 (One Channel Only)

Table II. Master and Channel Control

		dB	Data Hex	Binary
Master	Min Atten	0	7F	1111111
	Max Atten	-127	00	0000000
Channel	Max Gain	$+31$	00	00000
	Midgain	$+15$	10	10000
	Min Gain	0	1F	11111

When using channel controls as balance controls, the center would be with Channel = $10h$ (or $0Fh$ if desired). Increasing the gain to the maximum would occur at Channel = $00h$. Reducing the gain to minimum would occur at Channel = $1Fh$.

SELECTION	ADDRESS MODE								DATA MODE				
	ADDRESS								DATA				
	MSB	MSB	MSB	MSB	MSB	MSB	MSB	MSB	LSB	LSB	LSB	LSB	LSB
7-BIT MASTER DAC	1	X	X	X	X	0	0	0	0				
5-BIT CHANNEL DAC 1	1	X	X	X	X	0	0	1	0	1	X		
5-BIT CHANNEL DAC 2	1	X	X	X	X	0	1	0	0	1	X		
5-BIT CHANNEL DAC 3	1	X	X	X	X	0	1	1	0	1	X		
5-BIT CHANNEL DAC 4	1	X	X	X	X	1	0	0	0	1	X		
5-BIT CHANNEL DAC 5	1	X	X	X	X	1	0	1	0	1	X		
5-BIT CHANNEL DAC 6	1	X	X	X	X	1	1	0	0	1	X		
NO DAC SELECTED	1	X	X	X	X	1	1	1	0	1	X		
X = DON'T CARE SHADED AREA IS DATA													
0 = MUTE 1 = UNMUTE													

Figure 7. Interface Characteristics, DAC Address/Data Decoding Truth Table

SSM2160

Serial Data Input Format

The standard format for data sent to SSM2160 is an address byte followed by a data byte. This is depicted in the truth table, Figure 7. Two 8-bit bytes are required for each master and each of the six channel updates. The first byte sent contains the address and is identified by the MSB being logic high. The second byte contains the data and is identified by the MSB being logic low. The seven LSBs of the first byte set the attenuation level from 0 dB to -127 dB for the master. The five LSBs of the byte set the channel gain levels from 0 dB to 31 dB.

Serial Data Control Inputs

The SSM2160 provides a simple 3-wire or 4-wire serial interface—see the timing diagram in Figure 1. Data is presented to the DATA pin and the serial clock to the CLK pin. Data may be shifted in at rates up to 1 MHz (typically).

The shift register, CLK, is enabled when the $\overline{\text{WRITE}}$ input is low. The $\overline{\text{WRITE}}$ thus serves as a chip select input; however, the shift register contents are not transferred to the holding register until the rising edge of $\overline{\text{LD}}$. In most cases, $\overline{\text{WRITE}}$ and $\overline{\text{LD}}$ will be tied together, forming a traditional 3-wire serial interface.

To enable a data transfer, the $\overline{\text{WRITE}}$ and $\overline{\text{LD}}$ inputs are driven logic low. The 8-bit serial data, formatted MSB first, is input on the DATA pin and clocked into the shift register on the falling edge of CLK. The data is latched on the rising edge of $\overline{\text{WRITE}}$ and $\overline{\text{LD}}$.

Table III. Input/Output Levels vs. Attenuation/Gain

Input		Gain/Loss			Output	
dBu	mV rms	Master	Channel	Net	dBu	mV rms
0	775	-31	31	0	0	775
-31	22	0	31	31	0	775
-28	31	0	31	31	3	1100

Saturation Prevention

Unlike a passive potentiometer, the SSM2160 can give up to 31 dB of gain, thereby creating a potential for saturating the VCAs, resulting in an undesirable clipping or overload condition. Careful choice of input signal levels and digital gain parameters will eliminate the possibility. A few of the many acceptable gain and attenuation settings that keep the signals within the prescribed limits are shown in Table III. The input and output levels are given in mV rms and dBu (0 dBu = 0.775 V rms).

Line one of the table: the master is not allowed to have less than -31 dB attenuation, and the channel is allowed +31 dB of gain. Since the net gain is zero, there is no possibility of overload with the expected maximum input signal.

Line two of the table shows that input signal limited to -31 dBu will allow +31 dB of channel gain and 0 dB of master attenuation. With an input below -31 dBu, the output will never exceed 0 dBu, so no overloading is possible.

Line three of the table allows an input of -28 dBu, master attenuation of 0 dB, and 31 dB channel gain. The output is a maximum of 3 dBu (1.1 V rms), which is acceptable for power supplies of ± 6 V or more. So long as $V_{p-p} < V_{\text{SUPPLY}}/4$, there will be no overloading (see Table I).

If unity overall gain is required from the SSM2160, there should be *no net gain* between the master (loss) and channel (gain), with both at their lowest attenuation position. Minimum channel gain is recommended for minimum distortion.

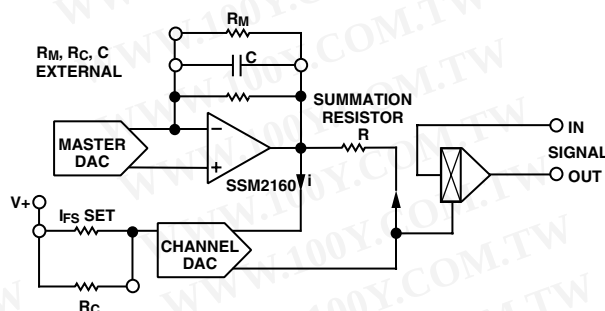


Figure 8. VCA Control Scheme

Control Range and Channel Tracking

Each channel VCA is controlled by its own DAC's output, plus the control signal from the master DAC. This is shown in Figure 8. Channel DACs are configured to *increase* the gain of the VCA in 1 dB steps from 0 dB to 31 dB. Thus, the midpoint (15, or 16 if preferred) should be chosen as the center setting of the electronic balance controls. Since the master DAC feeds all summation nodes, the attenuation of all VCAs simultaneously changes from 0 dB to the noise floor.

Maximum attenuation of all channels occurs when the master is set to -127 dB attenuation, and the channel is set to 0 dB gain.

Minimum attenuation of all channels occurs when the master is set at 0 dB, and the channel is set to 31 dB.

Once the channel-to-channel balance has been set, the master may be changed without changing the balance. This is shown in Figure 9.

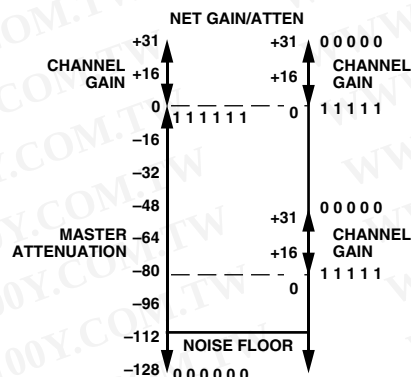


Figure 9. Practical Control Range

Master/Channel Step Sizes

The details of the DAC control of the channel VCAs is depicted in Figure 8. A 7-bit current output DAC and an op amp convert the digitally commanded master control level to an analog voltage. A capacitor across the feedback resistor limits the rate of change at the output to prevent clicking. A 5-bit DAC converts the digitally commanded channel control level to a voltage via a resistor R. These two control signals sum in resistor R and are fed to the channel VCA. Although we present the attenuation and gain as two separate items, in fact, the VCA can be operated smoothly

from a gain condition to an attenuation. The master and channel step sizes default to 1 dB in the absence of external components. The step sizes can be changed by the addition of external resistors if finer resolution is desired.

Control Range vs. Step Size

Before adjusting step sizes from the standard 1 dB, consider the effect on control range. The master control and the channel control provide 1 dB step sizes, which may be modified by the addition of external resistors. As the total number of steps is unchanged, reduction of the step size results in a smaller control range. The range of the control is

$$RANGE = Step\ Size\ (dB) \times (Number\ of\ Levels\ Used)$$

Since the master volume control operates from a 7-bit word, its DAC has 128 levels (including 0). The channel volume control DAC is a 5-bit input, so there are 32 levels for volume control (including 0). As can be seen in Figure 9, the practical control range is set by the noise floor. It can be advantageous to reduce the master step size to give finer steps from zero attenuation down to the noise floor.

Reducing Master Step Size

To reduce the master step size, place resistor R_M between MSTR SET and MSTR OUT. The master step size of the master volume control will then become

$$R_M = \frac{1700 X_M}{1 - X_M}$$

where X_M is the desired master control step size in decibels. See Figure 10 for practical values of R_M . Note that the step size for the master control can only be adjusted to less than 1 dB. No resistor is required for the default value of 1 dB per step. For larger step sizes, use digital control. Noninteger dB step sizes can be obtained by using digital control and a reduced step size.

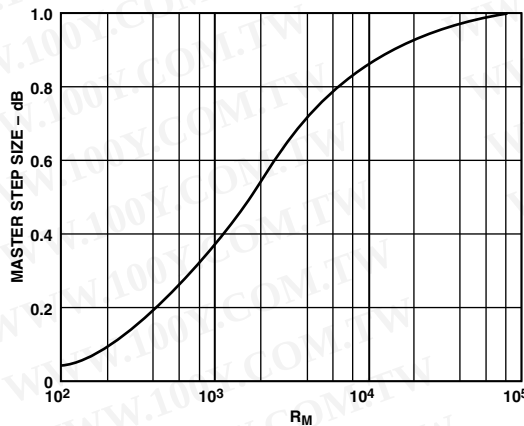


Figure 10. Master Step Size vs. R_M

Example: Modifying Master Step Size to 0.5 dB

A master step size of 0.5 dB is desired for the master control, while a 1 dB step size is adequate for the channel control. Using the preceding equation or Figure 10, R_M is found to be 1700 Ω and is connected between MSTR SET and MSTR OUT. There

could be some variation from lot to lot, so applications requiring precise step size should include a fixed resistor plus a trimmer potentiometer to span the calculated value $\pm 25\%$. In this example, R_C is not needed since the default channel step size is already 1 dB. CH SET is left floating. With this step size, the dynamic range of the master control is

$$DNR = 0.5 \times 127\ dB = 63.5\ dB$$

In this configuration, the maximum master volume is 0 dB, while the minimum volume is -63.5 dB. Since the channel volume can still provide 0 dB to 31 dB of gain, the total system gain can vary between -63.5 dB and $+32$ dB. Note that a 0 dB command setting to the master control always results in unity gain, regardless of the step size.

Channel Step Size

The channel DACs' full-scale current is set by an internal resistor to $V+$. By shunting this resistor, the full-scale current, and therefore the step size, will increase. No provisions are available for reducing the channel step size. To increase the channel step size, place a resistor, R_C , from CH SET to $V+$. Note that a 0 dB setting for a channel will always give unity gain, regardless of how large or small the step size is. This is true for both the master and channel volume controls.

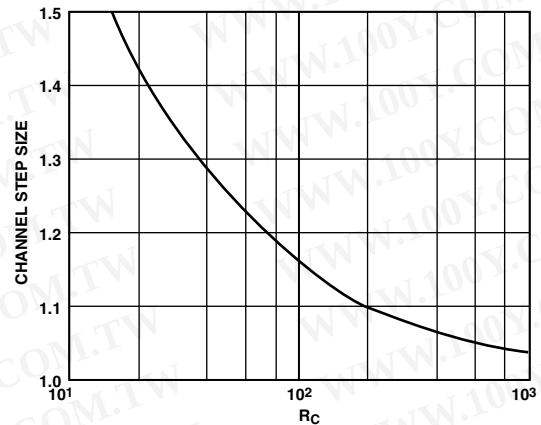


Figure 11. Channel Step Size vs. R_C

Example: Modifying Channel Step Size

A channel step size of 1.3 dB is desired. From Figure 11 we see that a 40 Ω resistor (approximately) connected from CH SET to $V+$ is required. As this varies from lot to lot, the exact value should be determined empirically, or a fixed resistor plus trimmer potentiometer should be used. *Take care not to short Pin 24 to Pin 1 as damage will result.*

Muting

The SSM2160 offers master and channel muting. On power-up, the master mute is activated, thus preventing any transients from entering the signal path and possibly overloading amplifiers down the signal path. Mute is typically better than -95 dB relative to a 0 dBu input. Due to design limitations, the individual channel muting results in increased signal distortion in the unmuted channels. Users should determine if this condition is acceptable in the particular application.

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DC Blocking and Frequency Response

All internal signal handling uses direct coupled circuitry. Although the input and output dc offsets are small, dc blocking is required when the signal ground references are different. This will be the case if the source is from an op amp that uses dual power supplies (i.e., ± 6 V), and the SSM2160 uses a single supply. If the signal source has the capability of operating with an externally supplied signal, connect the V_{REF} (Pin 3) to the source's external ground input either directly or through a buffer as shown in Figure 4.

The same consideration is applied to the load. If the load is returned to AGND, no capacitor is required. When the SSM2160 is operated from a single supply, there will be a dc output level of $+V_s/2$ at the output. This will require dc blocking capacitors if driving a load referred to GND.

When dc blocking capacitors are used at the inputs and outputs, they form a high-pass filter with the input and load resistance, both of which are typically 10 k Ω . To calculate the lower -3 dB frequency of the high-pass filter formed by the coupling capacitor and the input resistance, use either of the following formulas

$$f_c = 1/(2\pi RC)$$

or

$$C = 1/(2\pi R f_c)$$

where

R is the typically 10 k Ω input resistance of the SSM2160 or the load resistance. C is the value of the blocking capacitor when f_c is known.

If a cutoff frequency of 20 Hz were desired, solving for C gives 0.8 μ F for the input or output capacitor. A higher load impedance will allow smaller output capacitors to give the same 20 Hz cutoff. Note that the overall low-pass filter will be the cascade of the two, so the response will be -6 dB at 20 Hz. A practical and economical choice would be 1 μ F/15 V electrolytics.

Signal/Noise Considerations and Channel Center Gain

The SSM2160 should be placed in the signal flow where levels are high enough to result in low distortion and good SNR but not so high to require unusually high power supplies. In a typical application, input and output signal levels will be in the 300 mV $\pm$ 200 mV rms range. This level is typically available from internal and external sources. As previously mentioned, the 31 dB of gain available in the VCA is usually used for balancing the various channels and is usually set to 15 dB or 16 dB in its center position. Due to the nature of VCA performance versus gain, the minimum gain that will allow balancing the channels should be used. If no balance function is required, the channel gain should be set to 0 dB. Use the lowest value of centered gain when less than the full balance range is needed. For example, if only ± 6 dB channel gain variations were needed, the center could be set at 6 dB, giving 6 dB $\pm$ 6 dB, rather than at 15 dB $\pm$ 6 dB. This would result in improved S/N ratio and less distortion.

Digital Interface

Digital logic signals have fast rising and falling edges that can easily be coupled into the signal and ground paths if care is not taken with PC board trace routing, ground management, and

proper bypassing. In addition, limiting the high state logic signal levels to 3.5 V will minimize noise coupling.

Load Considerations

The output of each SSM2160 channel must be loaded with a minimum of 10 k Ω . Connecting a load of less than 10 k Ω will result in increased distortion and may cause excessive internal heating with possible damage to the device. Capacitive loading should be kept to less than 50 pF. Excessive capacitive loading may increase the distortion level and may cause instability in the output amplifiers. If your application requires driving a lower impedance or more capacitive load, use a buffer as shown in Figure 12.

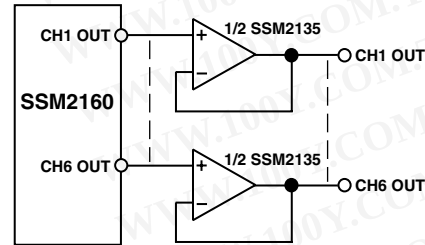


Figure 12. Output Buffers to Drive Capacitive Loads

Windows Software

Windows software is available to customers from Analog Devices to interface the serial port of a PC (running Windows 3.1 or higher) with the SSM2160. Contact your sales representative for details on obtaining the software. For details, see the Evaluation Board section.

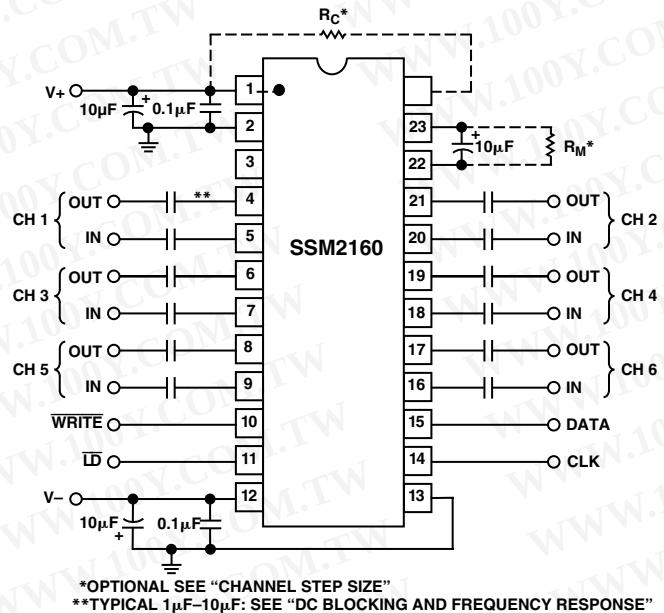


Figure 13. Typical Application Circuit (Dual Supply)

Controlling Stereo Headphones Level and Balance

Figure 14 shows how the SSM2160 can be configured to drive a stereo headphone output amplifier. Note that the minimum load specification precludes driving headphones directly. This example assumes that audio left and right signals are being fed into Channels 1 and 2, respectively. Additional amplifiers could be connected to the outputs to provide additional channels. The master control will set the loudness, and the channel controls will set the balance. The headphone amplifiers may be connected to the same power supplies as the SSM2160. The stereo audio signals are directly coupled to the noninverting input of both op amps. Depending upon the headphones and the signal levels, the optional R1 may be selected to provide additional gain, which is determined by

$$A_V = 1 + \left(\frac{R_2}{R_1} \right)$$

As an example, suppose a high impedance headphone (600 Ω) required a minimum of 25 mW to produce the desired loudness. Further, suppose the system design made available an output level from the SSM2160 of 300 mV. If the output were buffered without gain and applied directly to the headphone, the power would be

$$P = \frac{V^2}{R}$$

$$P = \frac{(0.3)^2}{600} = 0.15 \text{ mW}$$

This is obviously too little power, so we solve the equation for the voltage required to produce the desired power of 25 mW

$$V = \sqrt{PR}$$

$$V = \sqrt{0.025 \times 600} = 3.9 \text{ V}_{rms}$$

The gain of the amplifiers must then be

$$A_V = \frac{3.89}{0.3} = 13$$

$$A_V = 1 + \frac{R_2}{R_1}$$

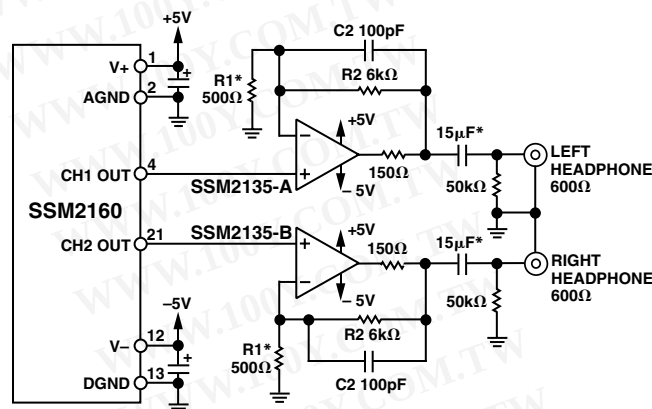
$$\frac{R_2}{R_1} = 12$$

$$R_1 = \frac{R_2}{12} = \frac{6000}{12} = 500 \Omega$$

If lower impedance headphones were used, say 30 Ω , the voltage required would be 0.9 V rms and a gain of 3 would suffice; thus, $R_1 = 2.5 \text{ k}\Omega$ and $R_2 = 5 \text{ k}\Omega$.

The 100 pF capacitor, C2, in parallel with R2, creates a low-pass filter with a cutoff above the audible range, reducing the gain to high frequency noise. A small resistor within the feedback loop protects the output stage in the event of a short circuit at the headphone output but does not measurably reduce the signal swing or loop gain. The dc blocking capacitor at the output establishes a high-pass filter with a -3 dB corner frequency determined by the value of C1 and the headphone impedance. With 600 Ω headphones, an output capacitor of 15 μF sets this corner at 20 Hz. Similarly, a 30 Ω headphone will require 250 μF .

CAUTION: As with all headphone applications, listening to loud sounds can cause permanent hearing loss.



*SEE TEXT FOR ALTERNATE VALUES

Figure 14. Headphone Output Amplifier Configuration

EVALUATION BOARD FOR THE SSM2160

The following information is to be used with the SSM2160 evaluation board, which simplifies connecting the part into existing systems. Audio signals are fed in and out via standard RCA-type audio connectors. A stereo headphone driver socket is provided for the convenience of listening to Channels 1 and 2. Microsoft Windows software is available for controlling the serial data bus of the SSM2160 via the parallel port driver (LPT) of a PC. The software may be downloaded from the Analog Devices website at www.analog.com. The evaluation board comes complete with the necessary parallel port cable and telephone type plug that mates with the evaluation board.

Power Supplies

The evaluation board should be connected to $\pm 6 \text{ V}$ supplies for initial evaluation. If other supply voltages are planned, they can be subsequently changed. The power configuration on the evaluation board is per Figure 2.

Signal Inputs and Outputs

Input load impedances are approximately 10 k Ω , so the load on the sources is relatively light. DC blocking capacitors are provided on the evaluation board. The load impedance connected to the outputs must be no less than 10 k Ω and no more than 50 pF shunt capacitance. This enables driving short lengths of shielded or twisted wire cable. If heavier loads must be driven, use an external buffer as shown in Figure 13. Note that 50 Ω isolation resistors are placed in series with each SSM2160 output and may be jumpered if desired.

Digital Interface

The interconnecting cable provided has a DB25 male connector for the parallel port of the PC and an RJ14 plug that connects to the evaluation board. This cable is all that is required for the computer interface.

Software Installation

If installing the software from a diskette and using Windows 3.1 or later, select the RUN command from the FILE menu of the Program Manager. In the command line, type `a:\setup` and press Enter. If you downloaded the software to your hard disk from the Analog Devices website to, for example, `C:\SSM2160`, on the command line type `C:\SSM2160\SETUP` and press Enter. The software will be automatically installed and a SSM2160 start-up icon will be displayed. Double-click the icon to start the application. Under the menu item Port, select the parallel port

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that is assigned to the connector used on your PC if different from the default LPT1.

Windows Control Panel

The control panel contains all the functions required to control the SSM2160, and each feature is described below. A mouse is needed to operate the various controls. It is possible to overload the VCA by incorrect input levels and master and control settings. If you have not read the sections of the data sheet regarding control planning, do so now. While no damage will occur to the SSM2160, the results will be unpredictable.

Master Volume

The master volume fader controls the 7-bit word that determines the attenuation level. There are 128 levels (2^7) that range from 0 dB attenuation to -127 dB attenuation. To change the level, simply click the up or down arrows or click in the space directly above or below the fader knob, or drag the knob up or down to its desired position. (*Drag* refers to placing the screen cursor arrowhead on the control, pressing and holding the left mouse button while moving the arrow to the desired position.)

Master Mute

Below the master volume fader is the Master Mute button. Click this button to mute all channels. Clicking it again will unmute all channels. The application defaults to Mute when started. Mute reduces outputs to approximately -95 dB below inputs up to 0 dBu.

Channel Volume

Each of the channel fader controls can be set to one of 32 levels of gain, from 0 dB to 31 dB. See the previous section on Master Volume for details.

Channel Mute

Same function as Master Mute but on a channel basis. Due to the design limitations, muting an individual channel results in an increased distortion level of the unmuted channels. Users must determine if this condition is acceptable in their application.

Channel Balance

The channel balance fader adjusts all channels over their range without affecting the master volume setting. Relative channel differences will be maintained until the top or the bottom of the range is reached. The master volume fader does the same function as this fader, which was made available for evaluation convenience.

Master and Channel Fades

Both master and channel fades can be achieved by pressing the MEM 1 button when levels are at a desired starting position and the MEM 2 button at the desired ending position. Fade controls individual channels, and Master Fade controls the master volume. Fade Time sets timing from 0.1 (fastest) to 9.9 (slowest). Press Fade to commence operation. If Fade is pressed again, a fade back to the starting point will occur. The Jump button causes a direct jump to the opposite memory position.

Halt

Halt is a software interrupt in case of a problem or to stop a long fade time.

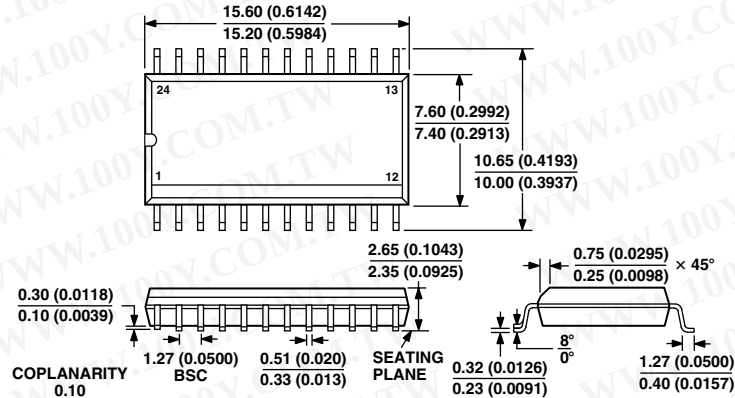
Update

Data currently on display is resent to the SSM2160. This is useful when parts are being substituted in the evaluation board, or when the interface cable is changed.

OUTLINE DIMENSIONS

24-Lead Standard Small Outline Package [SOIC]
(R-24)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AD
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-34970699
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

Revision History

Location	Page
2/03—Data Sheet changed from REV. 0 to REV. A.	
Removed SSM2161 model	Universal
Changes to GENERAL DESCRIPTION	1
Changes to PACKAGE THERMAL INFORMATION	4
Change to ORDERING GUIDE	4
Changes to Power Supplies vs. Signal Levels section	8
Changes to Update section	14
Updated OUTLINE DIMENSIONS	15