Rail-to-Rail, High Output Current Amplifier

AD8397

FEATURES

Dual operational amplifier
Voltage feedback
Wide supply range: from 3 V to 24 V
Rail-to-rail output
- **Output swing to within 0.5 V of supply rails**

High linear output current
- **310 mA peak into 32 Ω on ±12 V supplies while maintaining −80 dBc SFDR**

Low noise
- **4.5 nV/√Hz voltage noise density @ 100 kHz**
- **1.5 pA/√Hz current noise density @ 100 kHz**

High speed
- **69 MHz bandwidth (G = 1, −3 dB)**
- **53 V/µs slew rate (R_{LOAD} = 25 Ω)**

APPLICATIONS

Twisted-pair line drivers
Audio applications
General-purpose high current amplifiers

GENERAL DESCRIPTION

The AD8397 has two voltage feedback operational amplifiers capable of driving heavy loads with excellent linearity. The common-emitter, rail-to-rail output stage surpasses the output voltage capability of typical emitter-follower output stages and can swing to within 0.5 V of either rail while driving a 25 Ω load. The low distortion, high output current, and wide output dynamic range make the AD8397 ideal for applications that require a large signal swing into a heavy load.

Fabricated with ADI's high speed eXtra Fast Complementary Bipolar High Voltage (XFCB-HV) process, the high bandwidth and fast slew rate of the AD8397 keep distortion to a minimum while also dissipating minimum power. The AD8397 is available in a standard 8-lead SOIC package and, for higher power applications, a thermally enhanced 8-lead SOIC EPAD package. Both packages can operate from −40°C to +85°C.

PIN CONFIGURATION

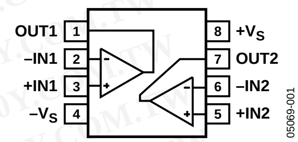

Figure 1. 8-Lead SOIC

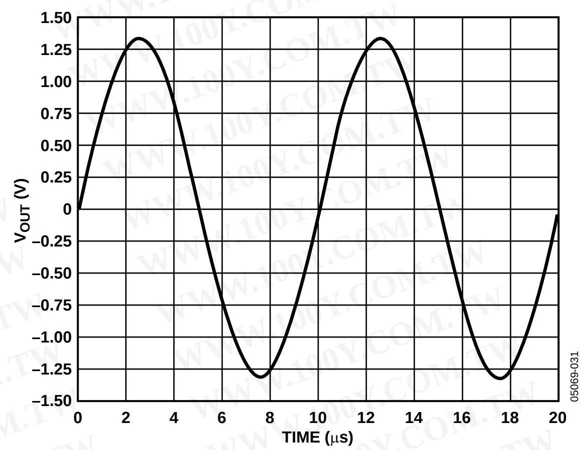

Figure 2. Output Swing, V_S = ±1.5 V, R_L = 25 Ω

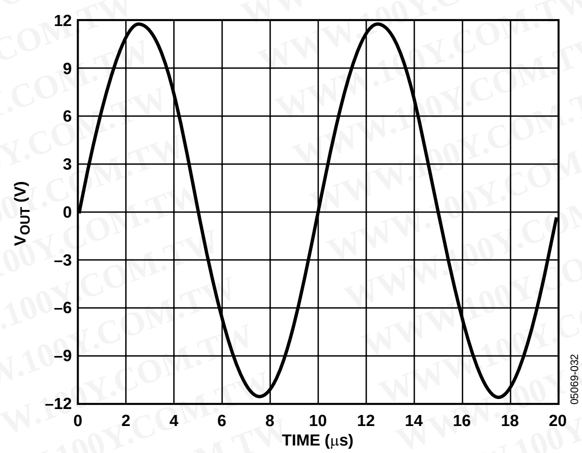

Figure 3. Output Swing, V_S = ±12 V, R_L = 100 Ω

Rev. 0

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REVISION HISTORY

1/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±1.5 V or +3 V (@ T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		50		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		3.6		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		9		MHz
Slew Rate	V_{OUT} = 0.8 V p-p		32		V/μs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 1.4 V p-p, G = +2		−90		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	2.5	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		μA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±0.5 V	81	88		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−71	−80		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 25 Ω	+1.39	+1.43		V_P
−Swing	R_{LOAD} = 25 Ω		−1.4	−1.37	V_P
+Swing	R_{LOAD} = 100 Ω	+1.45	+1.48		V_P
−Swing	R_{LOAD} = 100 Ω		−1.47	−1.44	V_P
Maximum Output Current	SFDR ≤ −70 dBc, f = 100 kHz, V_{OUT} = 0.7 V_P, R_{LOAD} = 4.1 Ω		170		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.0	V
Supply Current		6	7	8.5	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−70	−82		dB

V_S = ±2.5V or +5 V (@ T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted).

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		60		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		4.8		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		14		MHz
Slew Rate	V_{OUT} = 2.0 V p-p		53		V/μs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 2 V p-p, G = +2		−98		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	2.4	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		μA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±1.0 V	85	90		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−76	−80		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 25 Ω	+2.37	+2.42		V_P
−Swing	R_{LOAD} = 25 Ω		−2.37	−2.32	V_P
+Swing	R_{LOAD} = 100 Ω	+2.45	+2.48		V_P
−Swing	R_{LOAD} = 100 Ω		−2.46	−2.42	V_P
Maximum Output Current	SFDR ≤ −70 dBc, f = 100 kHz, V_{OUT} = 1.0 V_P, R_{LOAD} = 4.3 Ω		230		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.6	V
Supply Current		7	9	12	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−75	−85		dB

V_S = ±5 V or +10 V (@ T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted).

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		66		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		6.5		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		14		MHz
Slew Rate	V_{OUT} = 4.0 V p-p		53		V/µs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 6 V p-p, G = +2		−94		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	2.5	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		µA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±2.0 V	85	94		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−84	−94		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 25 Ω	+4.7	+4.82		V_P
−Swing	R_{LOAD} = 25 Ω		−4.74	−4.65	V_P
+Swing	R_{LOAD} = 100 Ω	+4.92	+4.96		V_P
−Swing	R_{LOAD} = 100 Ω		−4.92	−4.88	V_P
Maximum Output Current	SFDR ≤ −80 dBc, f = 100 kHz, V_{OUT} = 3 V_P, R_{LOAD} = 12 Ω		250		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.6	V
Supply Current		7	9	12	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−76	−85		dB

V_S = ±12 V or +24 V (@ T_A = 25°C, G = +1, R_L = 25 Ω, unless otherwise noted).

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.1 V p-p		69		MHz
0.1 dB Flatness	V_{OUT} = 0.1 V p-p		7.6		MHz
Large Signal Bandwidth	V_{OUT} = 2.0 V p-p		14		MHz
Slew Rate	V_{OUT} = 4.0 V p-p		53		V/μs
NOISE/DISTORTION PERFORMANCE					
Distortion (Worst Harmonic)	f_C = 100 kHz, V_{OUT} = 20 V p-p, G = +5		−84		dBc
Input Voltage Noise	f = 100 kHz		4.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1.0	3.0	mV
	T_{MIN} – T_{MAX}		2.5		mV
Input Offset Voltage Match			1.0	2.0	mV
Input Bias Current			200	900	nA
	T_{MIN} – T_{MAX}		1.3		μA
Input Offset Current			50	300	nA
Open-Loop Gain	V_{OUT} = ±3.0 V	90	96		dB
INPUT CHARACTERISTICS					
Input Resistance	f = 100 kHz		87		kΩ
Input Capacitance			1.4		pF
Common-Mode Rejection	ΔV_{CM} = ±1 V	−85	−96		dB
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
+Swing	R_{LOAD} = 100 Ω	+11.82	+11.89		V_P
−Swing	R_{LOAD} = 100 Ω		−11.83	−11.77	V_P
Maximum Output Current	SFDR ≤ −80 dBc, f = 100 kHz, V_{OUT} = 10 V_P, R_{LOAD} = 32 Ω		310		mA
POWER SUPPLY					
Operating Range (Dual Supply)		±1.5		±12.6	V
Supply Current		8.5	11	15	mA/Amp
Power Supply Rejection	ΔV_S = ±0.5 V	−76	−86		dB

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation[1]	See Figure 4
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Thermal resistance for standard JEDEC 4-layer board:
8-lead SOIC: θ_{JA} = 157.6°C/W
8-Lead SOIC EPAD: θ_{JA} = 47.2°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be dissipated safely by the AD8397 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

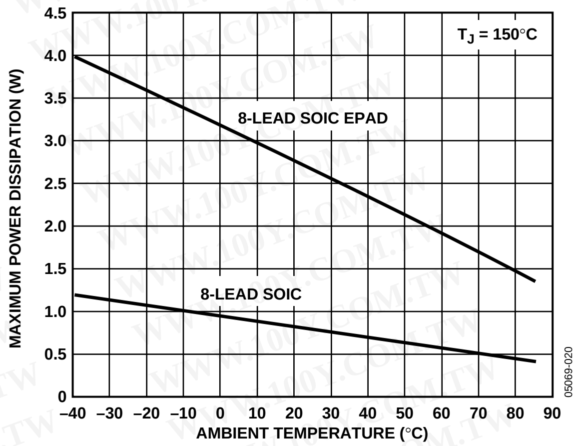

Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

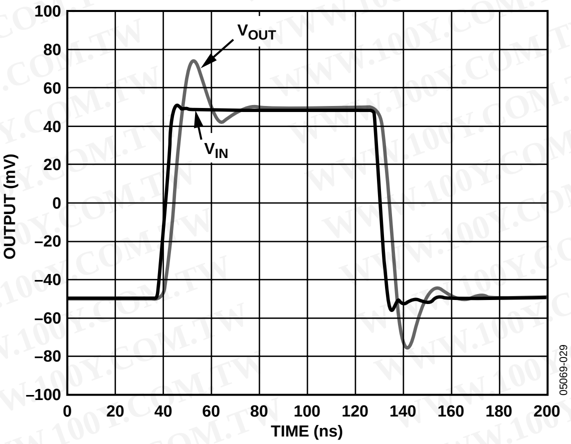

Figure 5. Small Signal Pulse Response (G = +1, V_S = ±5 V, R_L = 25 Ω)

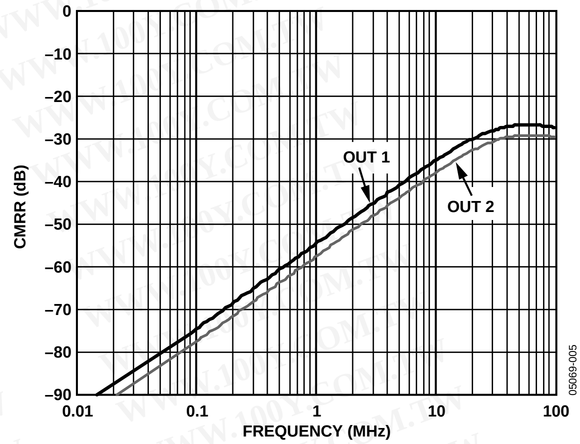

Figure 8. Common-Mode Rejection vs. Frequency (V_S = ±5 V, R_L = 25 Ω)

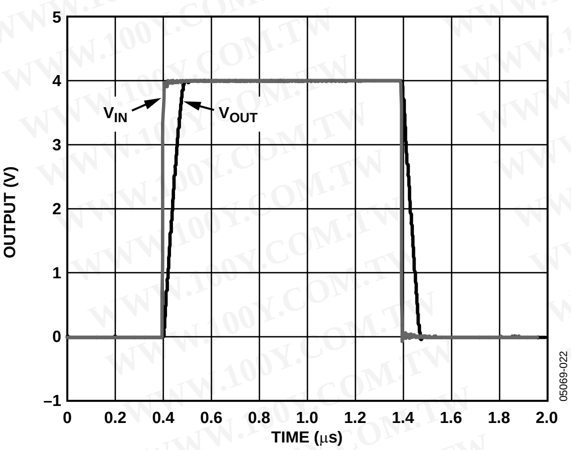

Figure 6. Large Signal Pulse Response (0 V to 4 V, V_S = ±5 V, R_L = 25 Ω)

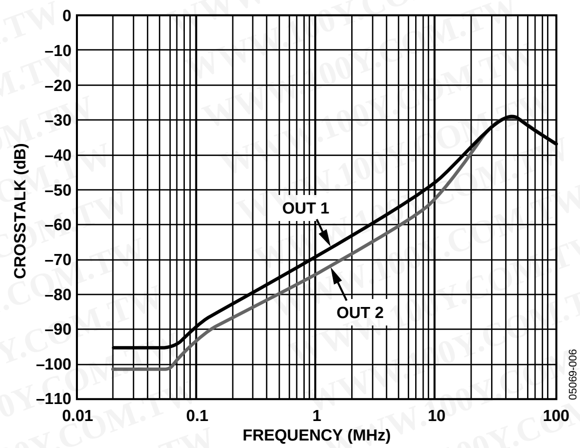

Figure 9. Output-to-Output Crosstalk vs. Frequency (V_S = ±5 V, V_O = 1 V p-p, R_L = 25 Ω)

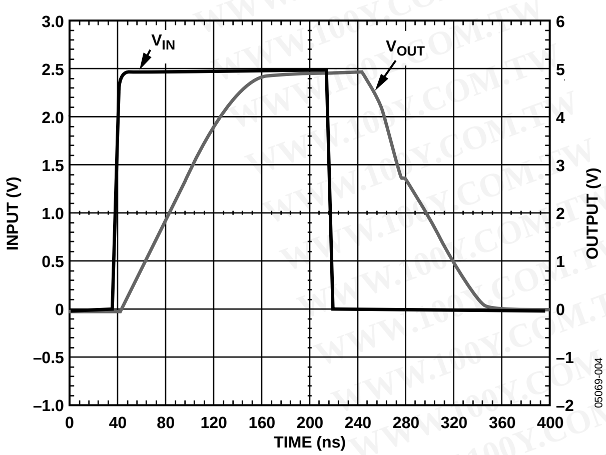

Figure 7. Output Overdrive Recovery (V_S = ±5 V, Gain = +2, R_L = 25 Ω)

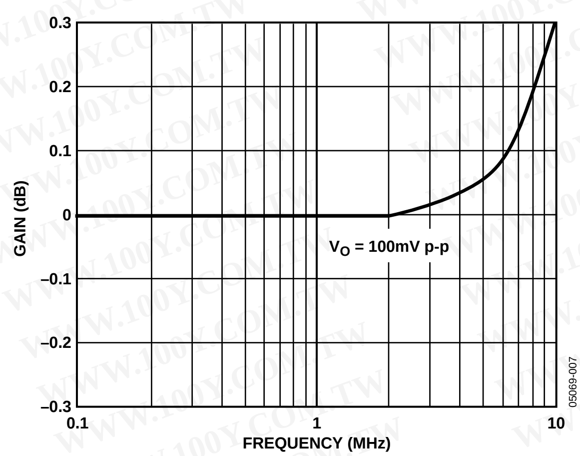

Figure 10. 0.1 dB Flatness (V_S = ±5 V, V_O = 0.1 V p-p, Gain = +1, R_L = 25 Ω)

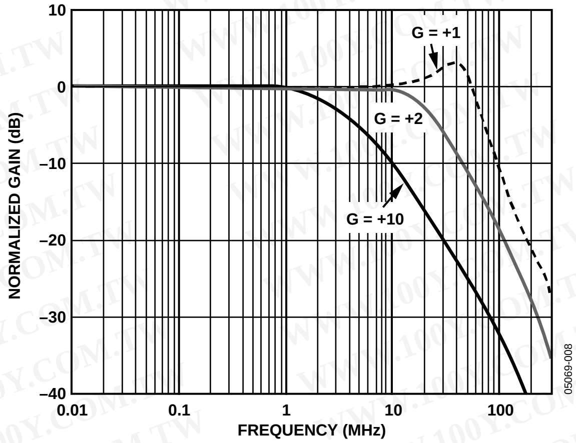

Figure 11. Small Signal Frequency Response for Various Gains (V_S = ±5 V, V_O = 0.1 V p-p, R_L = 25 Ω)

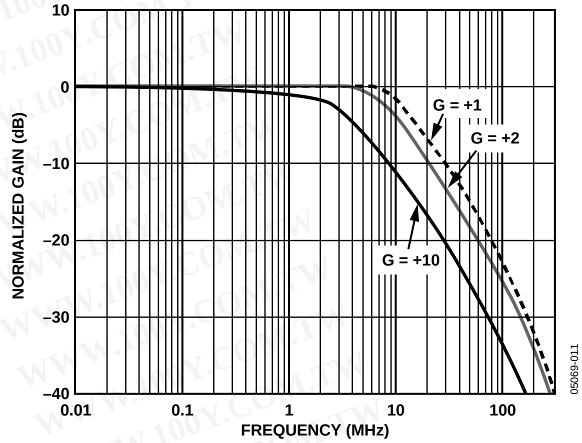

Figure 14. Large Signal Frequency Response for Various Gains (V_S = ±5 V, V_O = 2 V p-p, R_L = 25 Ω)

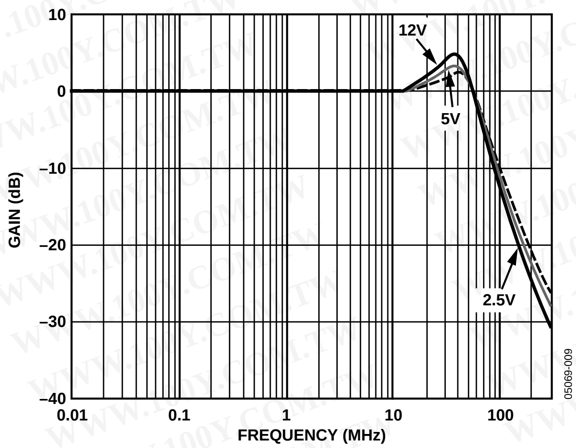

Figure 12. Small Signal Frequency Response for Various Supplies (Gain = +1, V_O = 0.1 V p-p, R_L = 25 Ω)

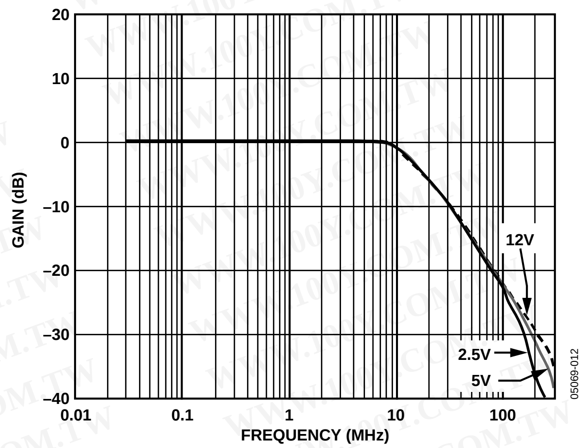

Figure 15. Large Signal Frequency Response for Various Supplies (Gain = +1, V_O = 2 V p-p, R_L = 25 Ω)

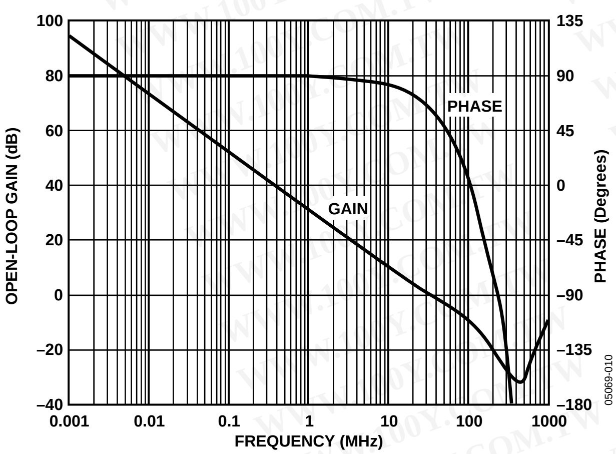

Figure 13. Open Loop Gain and Phase vs. Frequency (V_S = ±5 V, R_L = 25 Ω)

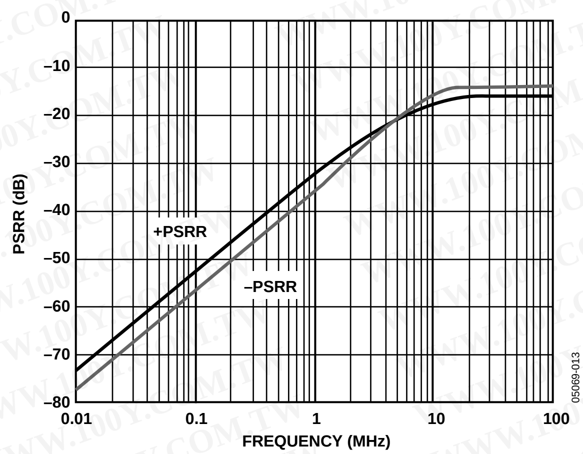

Figure 16. Power Supply Rejection (V_S = ±5 V, R_L = 25 Ω)

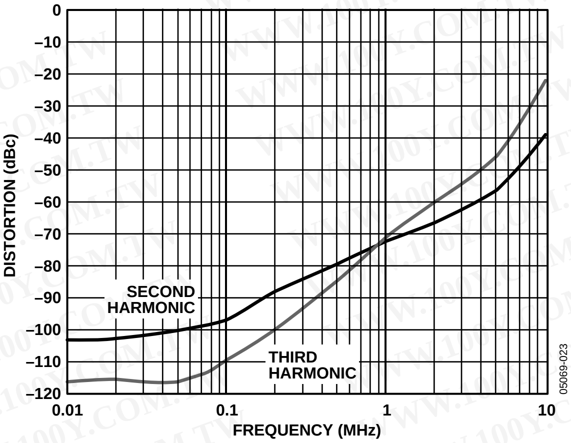

Figure 17. Distortion vs. Frequency
(V_S = ±5 V, V_O = 2 V p-p, G = +2, R_L = 25 Ω)

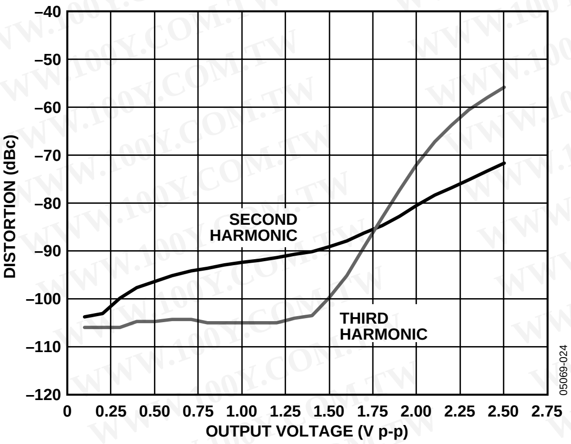

Figure 18. Distortion vs. Output Voltage @ 100 kHz,
(V_S = ±1.5 V, G = +2, R_L = 25 Ω)

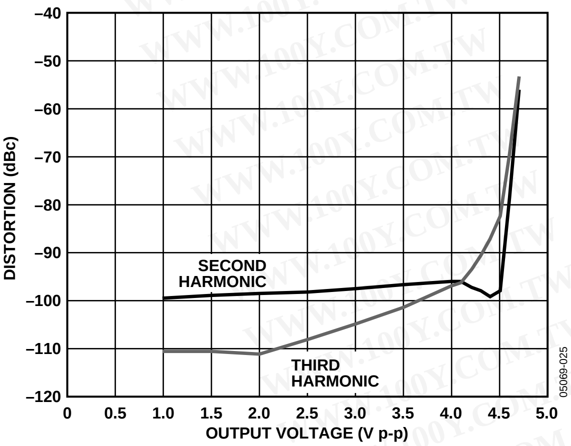

Figure 19. Distortion vs. Output Voltage @ 100 kHz,
(V_S = ±2.5 V, G = +2, R_L = 25 Ω)

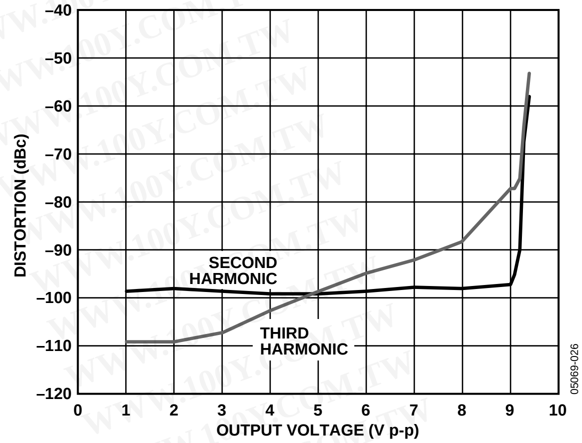

Figure 20. Distortion vs. Output Voltage @ 100 kHz,
(V_S = ±5 V, G = +2, R_L = 25 Ω)

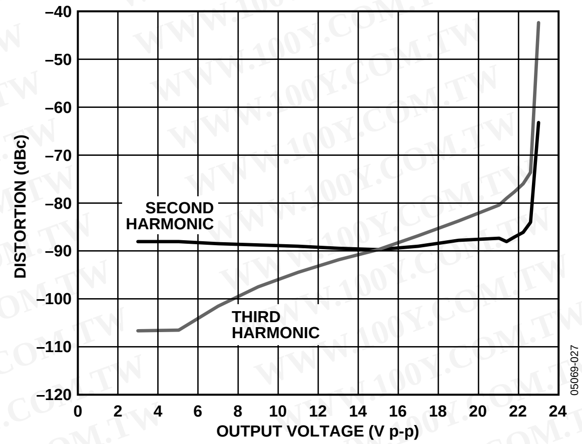

Figure 21. Distortion vs. Output Voltage @ 100 kHz,
(V_S = ±12 V, G = +5, R_L = 50 Ω)

GENERAL DESCRIPTION

The AD8397 is a voltage feedback operational amplifier which features an H-bridge input stage and common-emitter, rail-to-rail output stage. The AD8397 can operate from a wide supply range, ±1.5 V to ±12 V. When driving light loads, the rail-to-rail output is capable of swinging to within 0.2 V of either rail. The output can also deliver high linear output current when driving heavy loads, up to 310 mA into 32 Ω while maintaining −80 dBc SFDR. The AD8397 is fabricated on Analog Devices' proprietary eXtra Fast Complementary Bipolar High Voltage process (XFCB-HV).

POWER SUPPLY AND DECOUPLING

The AD8397 can be powered with a good quality, well-regulated, low noise supply from ±1.5 V to ±12 V. Careful attention should be paid to decoupling the power supply. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize the supply voltage ripple and power dissipation. A 0.1 μF MLCC decoupling capacitor(s) should be located no more than 1/8 inch away from the power supply pin(s). A large tantalum 10 μF to 47 μF capacitor is recommended to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the AD8397 outputs.

LAYOUT CONSIDERATIONS

As with all high speed applications, careful attention should be paid to printed circuit board (PCB) layout in order to prevent associated board parasitics from becoming problematic. The PCB should have a low impedance return path (or ground) to the supply. Removing the ground plane from all layers in the immediate area of the amplifier helps to reduce stray capacitances. The signal routing should be short and direct in order to minimize the parasitic inductance and capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input traces should be kept as far apart as possible from the output traces to minimize coupling (crosstalk) though the board.

When the AD8397 is configured as a differential driver, as in some line driving applications, a symmetrical layout should be provided to the extent possible in order to maximize balanced performance. When running differential signals over a long distance, the traces on the PCB should be close together or any differential wiring should be twisted together to minimize the area of the inductive loop that is formed. This reduces the radiated energy and makes the circuit less susceptible to RF interference. Adherence to stripline design techniques for long signal traces (greater than approximately 1 inch) is recommended.

UNITY-GAIN OUTPUT SWING

When operating the AD8397 in a unity-gain configuration, the output does not swing to the rails and is constrained by the H-bridge input. This can be seen by comparing the output overdrive recovery in Figure 7 and the input overdrive recovery in Figure 22. To avoid overdriving the input and to realize the full swing afforded by the rail-to-rail output stage, the amplifier should be used in a gain of two or greater.

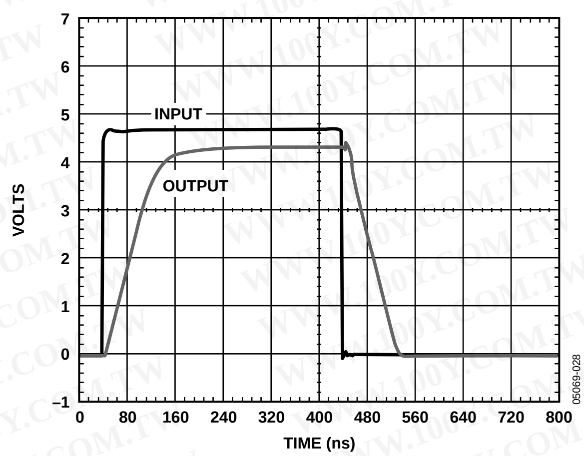

Figure 22. Unity-Gain Input Overdrive Recovery

CAPACITIVE LOAD DRIVE

When driving capacitive loads, many high speed operational amplifiers exhibit peaking in their frequency response. In a gain-of-two circuit, Figure 23 shows that the AD8397 can drive capacitive loads up to 270 pF with only 3 dB of peaking. For amplifiers with more limited capacitive load drive, a small series resistor (R_S) is generally used between the amplifier output and the capacitive load in order to minimize peaking and ensure device stability. Figure 24 shows that the use of a 2.2 Ω series resistor can further extend the capacitive load drive of the AD8397 out to 470 pF, while keeping the frequency response peaking to within 3 dB.

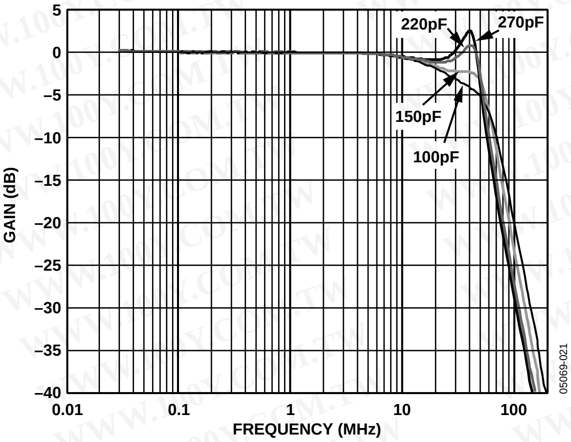

Figure 23. Capacitive Load Peaking Without Series Resistor

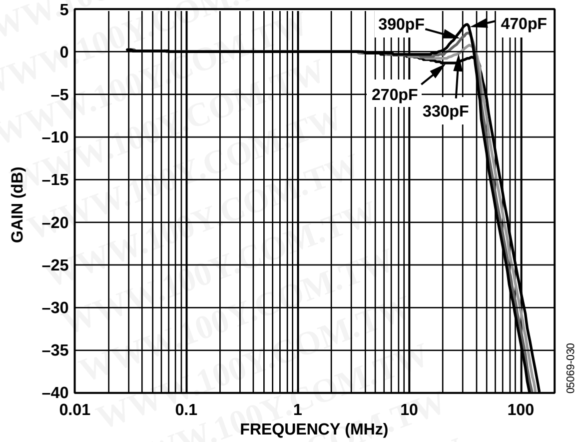

Figure 24. Capacitive Load Peaking with 2.2 Ω Series Resistor

OUTLINE DIMENSIONS

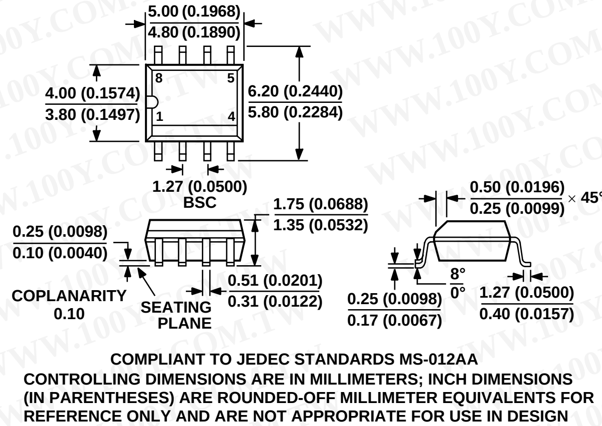

Figure 25. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

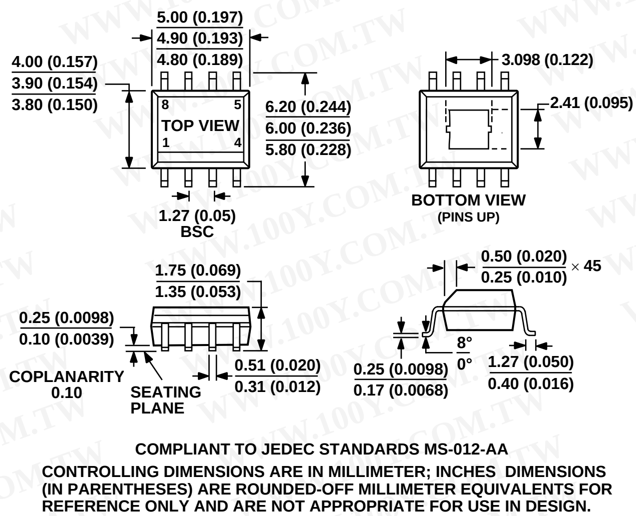

Figure 26. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]
Narrow Body (RD-8-2)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Outline
AD8397ARZ[1]	−40°C to +85°C	8-Lead SOIC	R-8
AD8397ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC	R-8
AD8397ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC	R-8
AD8397ARDZ[1]	−40°C to +85°C	8-Lead SOIC-EPAD	RD-8-2
AD8397ARDZ-REEL[1]	−40°C to +85°C	8-Lead SOIC-EPAD	RD-8-2
AD8397ARDZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC-EPAD	RD-8-2

[1] Z = Pb-free part.

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