800 MHz, Linear-in-dB VGA with AGC Detector

AD8368

FEATURES

Analog variable gain range: −12 dB to +22 dB
Linear-in-dB scaling: 37.5 dB/V
3 dB bandwidth: 800 MHz @ V_{GAIN} = 0.5 V
Integrated rms detector
P1dB: 16 dBm @ 140 MHz
Output IP3: 33 dBm @ 140 MHz
Noise figure at maximum gain: 9.5 dB @ 140 MHz
Input and output impedances: 50 Ω
Single-supply voltage from 4.5 V to 5.5 V
RoHS-compliant, 24-lead LFCSP

APPLICATIONS

Complete IF AGC amplifiers
Gain trimming and leveling
Cellular base stations
Point-to-point radio links
RF instrumentation

FUNCTIONAL BLOCK DIAGRAM

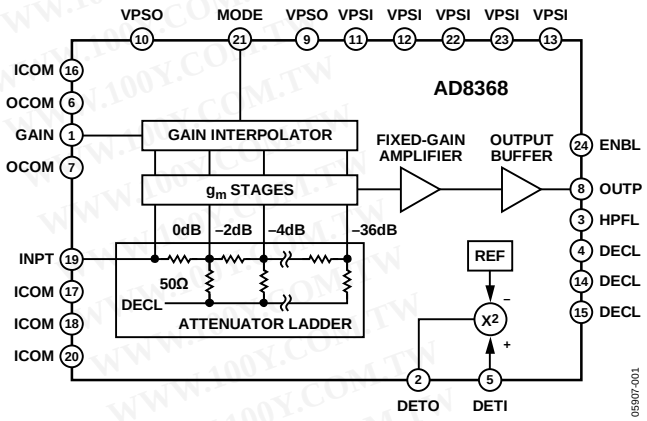

Figure 1.

GENERAL DESCRIPTION

The AD8368 is a variable gain amplifier (VGA) with analog linear-in-dB gain control that can be used from low frequencies to 800 MHz. Its excellent gain range, conformance, and flatness are attributed to the Analog Devices, Inc., X-AMP® architecture, an innovative technique for implementing high performance variable gain control.

The gain range of −12 dB to +22 dB is scaled accurately to 37.5 dB/V with excellent conformance error. The AD8368 has a 3 dB bandwidth of 800 MHz that is nominally independent of gain setting. At 140 MHz, the OIP3 is 33 dBm at maximum gain. The output noise floor is −143 dBm/Hz, which corresponds to a 9.5 dB noise figure at maximum gain. The single-ended input and output impedances are nominally 50 Ω.

The gain of the AD8368 can be configured to be an increasing or decreasing function of the gain control voltage depending on whether the MODE pin is pulled to the positive supply or to ground, respectively. When MODE is pulled high, the AD8368 operates as a typical VGA with increasing gain.

By connecting MODE to ground and using the on-board rms detector, the AD8368 can be configured as a complete automatic gain control (AGC) system with RSSI. The output power is accurately leveled to the internal default setpoint of 63 mV rms (−11 dBm referenced to 50 Ω), independent of the waveform crest factor. Because the uncommitted detector input is available at DETI, the AGC loop can level the signal at the AD8368 output or at any other point in the signal chain over a maximum input power range of 34 dB. Furthermore, the setpoint level can be raised by dividing down the output signal before applying it to the detector.

The AD8368 operates from a supply voltage of 4.5 V to 5.5 V and consumes 60 mA of current. It can be fully powered down to <3 mA by grounding the ENBL pin. The AD8368 is fabricated using the Analog Devices proprietary SiGe SOI complementary bipolar IC process. It is available in a 24-lead LFCSP and operates over the industrial temperature range of −40°C to +85°C. Application boards are available upon request.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

9/08—Rev. A to Rev. B

Added Stability and Layout Considerations Section 16
Changes to Evaluation Board Section, Figure 40, and Table 6 17
Added Figure 41, Figure 42, Figure 43, and Figure 44; Renumbered Sequentially 18
Added Exposed Pad Notation to Outline Dimensions 19

10/07—Rev. 0 to Rev. A

Changes to Table 1 3
Changes to Figure 4 to Figure 6 7
Changes to Figure 16 9
Changes to Figure 31 12
Updated Outline Dimensions 18
Changes to Ordering Guide 18

4/06—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, system impedance Z_0 = 50 Ω, V_{MODE} = 5 V, RF input = 140 MHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
OVERALL FUNCTION					
Frequency Range	LF		800	MHz	3 dB bandwidth
Maximum Input		3		V_P	To avoid input overload
Maximum Output[1]		2		V_P	To avoid clipping
AC Input Impedance		50		Ω	From INPT to ICOM
AC Output Impedance		50		Ω	From OUTP to OCOM
GAIN CONTROL INTERFACE (GAIN)					
Gain Span		34		dB	
Gain Scaling		37.5		dB/V	V_{MODE} = 5 V, 50 mV ≤ V_{GAIN} ≤ 950 mV
		−38		dB/V	V_{MODE} = 0 V, 50 mV ≤ V_{GAIN} ≤ 950 mV
Gain Accuracy		±0.4		dB	100 mV ≤ V_{GAIN} ≤ 900 mV
Maximum Gain		22		dB	V_{GAIN} = 1 V
Minimum Gain		−12		dB	V_{GAIN} = 0 V
V_{GAIN} Range	0		1	V	
Gain Step Response		100		ns	For 6 dB gain step
Gain Input Bias Current			−2	μA	
f = 70 MHz					
Noise Figure		9.5		dB	Maximum gain
Output IP3		34		dBm	f_1 = 70 MHz, f_2 = 71 MHz, V_{GAIN} = 1 V, 0 dBm per output tone
Output P1dB[1]		16		dBm	V_{GAIN} = 0 V, V_{MODE} = 0 V
f = 140 MHz					
Noise Figure		9.5		dB	Maximum gain
Output IP3		33		dBm	f_1 = 140 MHz, f_2 = 141 MHz, V_{GAIN} = 1 V, 0 dBm per output tone
Output P1dB[1]		16		dBm	V_{GAIN} = 0 V, V_{MODE} = 0 V
f = 240 MHz					
Noise Figure		9.7		dB	Maximum gain
Output IP3		33		dBm	f_1 = 240 MHz, f_2 = 241 MHz, V_{GAIN} = 1 V, 0 dBm per output tone
Output P1dB[1]		15		dBm	V_{GAIN} = 0 V, V_{MODE} = 0 V
f = 380 MHz					
Noise Figure		10		dB	Maximum gain
Output IP3		29		dBm	f_1 = 380 MHz, f_2 = 381 MHz, V_{GAIN} = 1 V, 0 dBm per output tone
Output P1dB[1]		13		dBm	V_{GAIN} = 0 V, V_{MODE} = 0 V

[1] Operation at compression is not recommended due to adverse distortion components.

V_S = 5 V, T_A = 25°C, system impedance Z_0 = 50 Ω, V_{MODE} = 5 V, RF input = 140 MHz, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions
SQUARE LAW DETECTOR (DETI, DETO)					
Output Setpoint		−11		dBm	OUTP connected to DETI
DETI DC Bias Level to ICOM		$V_S/2$		V	
DETI Impedance		710		Ω	
		0.6		pF	
DETO Output Range[1]	0.1		$V_S/2$	V	
AGC Step Response		30		µs	For −6 dB input power step (C_{DETO} = 1 nF)
MODE CONTROL INTERFACE (MODE)					
MODE Threshold		3.5		V	
MODE Input Bias Current			50	µA	
POWER INTERFACE (VPSI, VPSO)					
Supply Voltage	4.5	5	5.5	V	
Total Supply Current		60		mA	ENBL high
Disable Current		2		mA	ENBL low
ENABLE INTERFACE (ENBL)					
Enable Threshold		2.5		V	
Enable Response Time		1.5		µs	Time delay following off-to-on transition until output reaches 90% of final value
		3		µs	Time delay following on-to-off transition until supply current is less than 5 mA
ENBL Input Bias Current			150	µA	V_{ENBL} = 5 V

[1] Refer to AGC Operation section.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage (VPSO, VPSI)	5.5 V
ENBL and MODE Select Voltage	5.5 V
RF Input Level	20 dBm
Internal Power Dissipation	440 mW
θ_{JA}	52°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

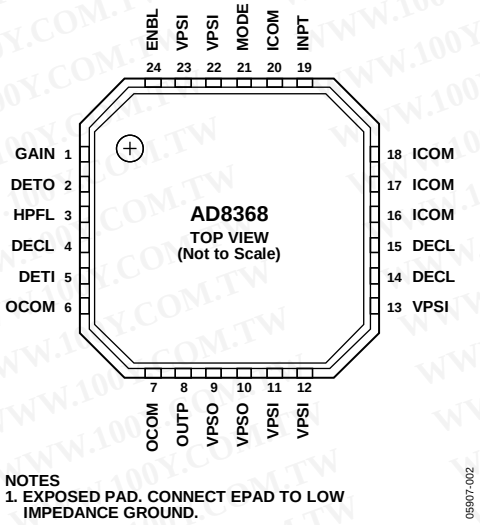

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GAIN	Gain Control.
2	DETO	Detector Output. Provides an output error current for the AGC function.
3	HPFL	High-Pass Filter Connection. A capacitor to ground sets the corner frequency of the internal output offset control loop that controls the minimum usable input frequency.
4, 14, 15	DECL	Decoupling Pin. Nominally ~V_S/2. Decoupling capacitance may need to be adjusted for AGC operation (see the Applications Information section).
5	DETI	Detector Input. DC level referenced to DECL pin.
6, 7	OCOM	Connect OCOM to low impedance ground.
8	OUTP	Signal Output. Must be ac-coupled.
9, 10	VPSO	Positive Supply Voltage, 4.5 V to 5.5 V. VPSO and VPSI must be connected together externally and properly bypassed.
11, 12, 13, 22, 23	VPSI	Positive Supply Voltage, 4.5 V to 5.5 V. VPSO and VPSI must be connected together externally and properly bypassed.
16, 17, 18, 20	ICOM	Connect ICOM to low impedance ground.
19	INPT	Signal Input. Must be ac-coupled.
21	MODE	Gain Direction Control. High for positive slope. Low for negative slope.
24	ENBL	Apply a Positive Voltage (2.5 V ≤ V_{ENBL} ≤ VPSI) to Activate Device.
	EPAD	Exposed Pad. Connect the exposed pad to low impedance ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T = 25°C, system impedance Z_0 = 50 Ω, MODE = 5 V, unless otherwise noted.

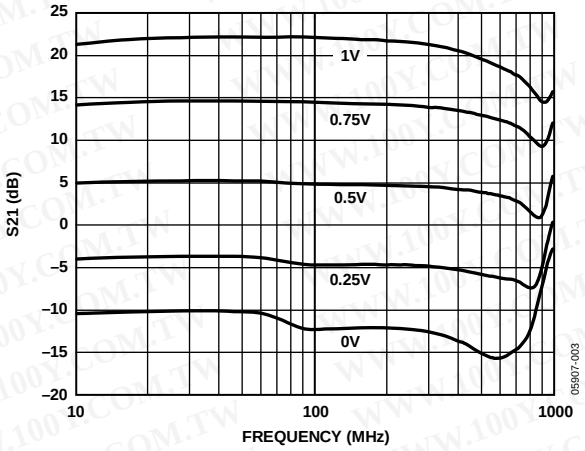

Figure 3. S21 vs. Frequency by V_{GAIN}

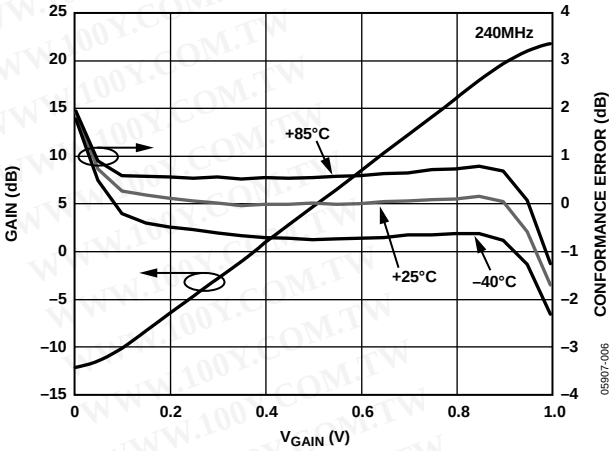

Figure 6. Gain and Conformance Error vs. V_{GAIN} (f = 240 MHz)

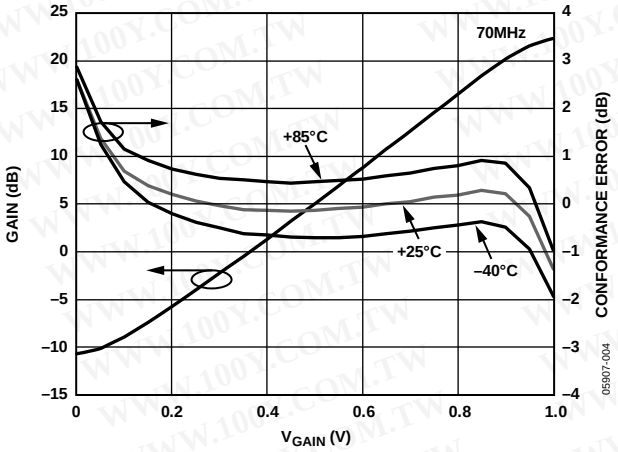

Figure 4. Gain and Conformance Error vs. V_{GAIN} (f = 70 MHz)

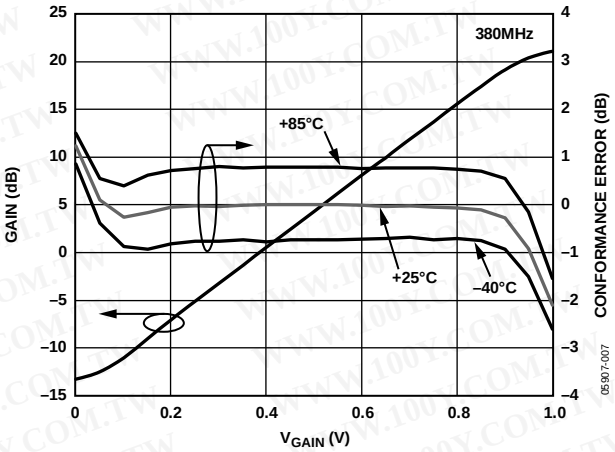

Figure 7. Gain and Conformance Error vs. V_{GAIN} (f = 380 MHz)

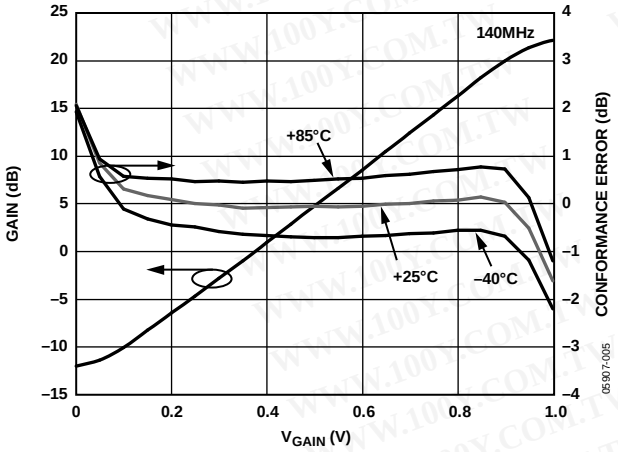

Figure 5. Gain and Conformance Error vs. V_{GAIN} (f = 140 MHz)

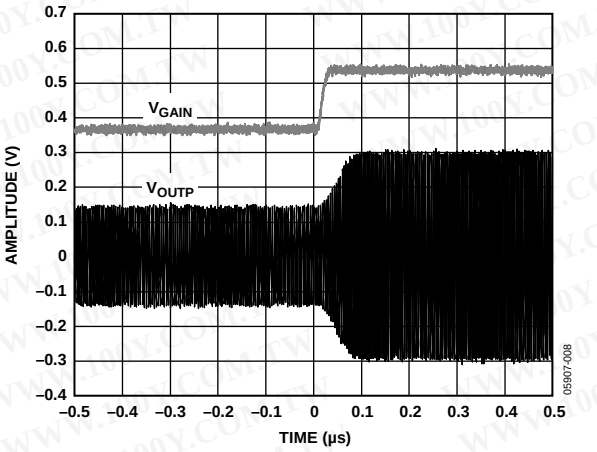

Figure 8. Gain Step Time Domain Response (6 dB Gain Step)

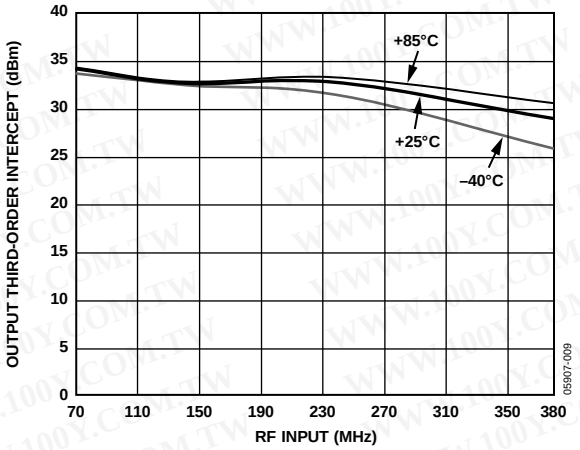

Figure 9. Output Third-Order Intercept vs. RF Input Frequency at Maximum Gain (V_{MODE} = 0 V)

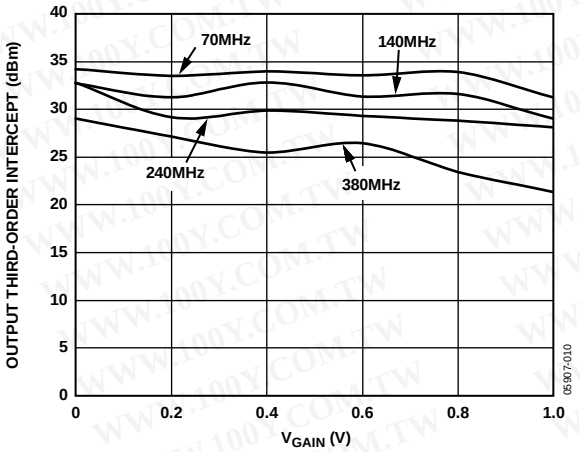

Figure 10. Output Third-Order Intercept vs. V_{GAIN} (V_{MODE} = 0 V)

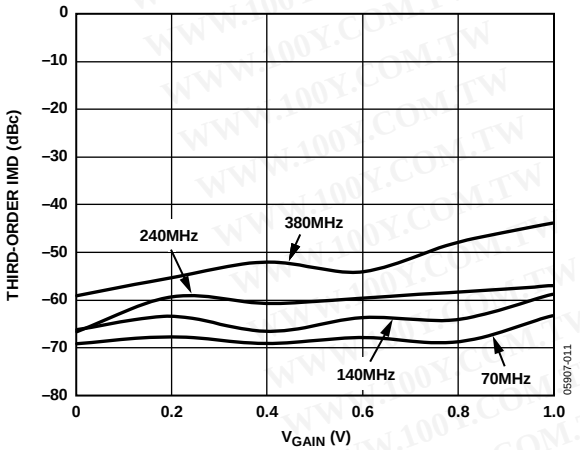

Figure 11. Third-Order IMD vs. V_{GAIN} (Output Power = 0 dBm per Tone, V_{MODE} = 0 V)

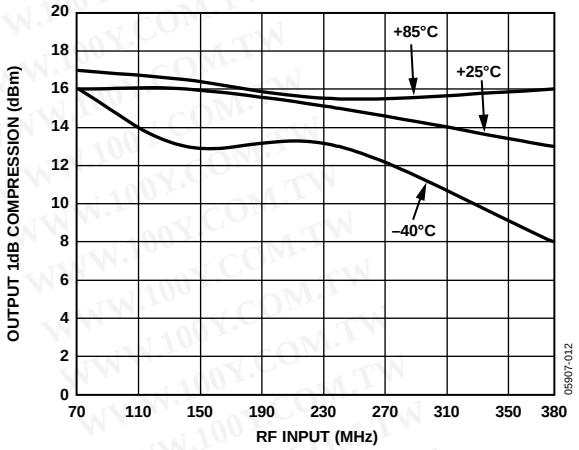

Figure 12. Output 1dB Compression Point vs. RF Input Frequency at Maximum Gain (V_{MODE} = 0 V)

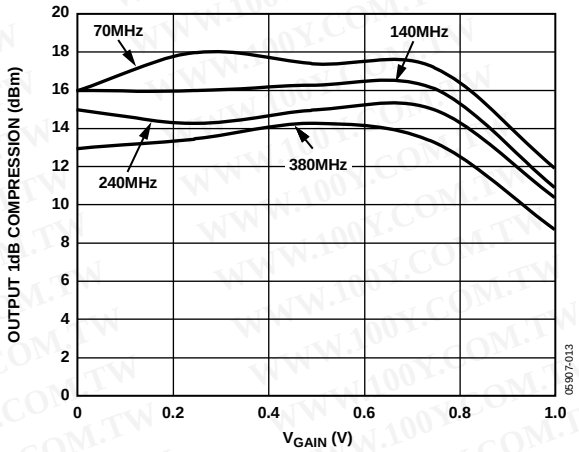

Figure 13. Output 1dB Compression Point vs. V_{GAIN} (V_{MODE} = 0 V)

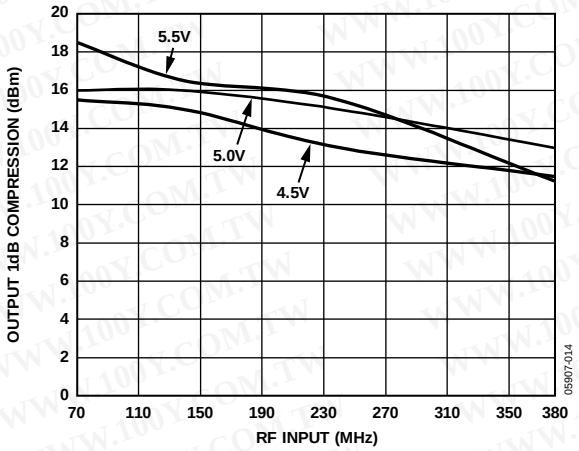

Figure 14. Output 1dB Compression Point vs. RF Input Frequency by Supply Voltage at Maximum Gain (V_{MODE} = 0 V)

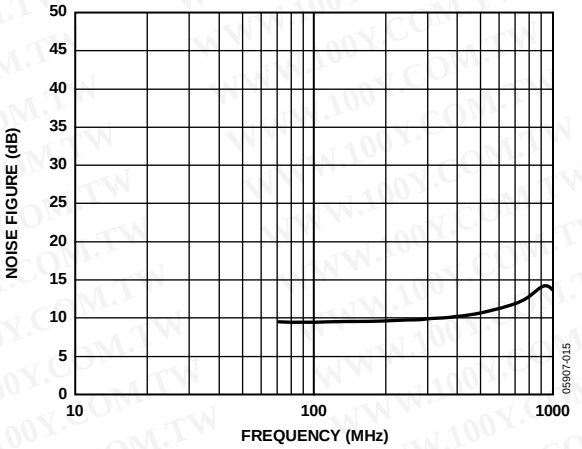

Figure 15. Noise Figure vs. Frequency at Maximum Gain (V_{MODE} = 0 V)

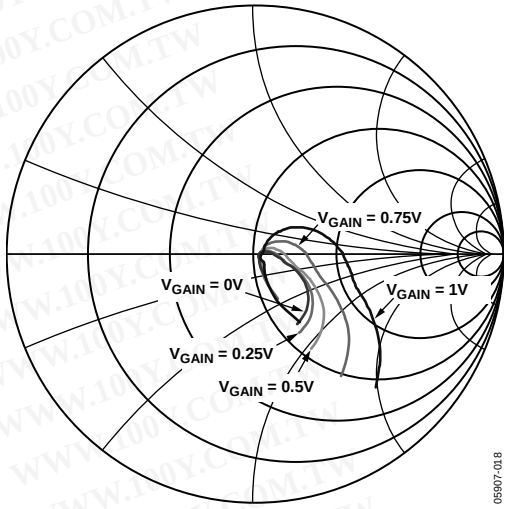

Figure 18. Input Reflection Coefficient vs. Frequency

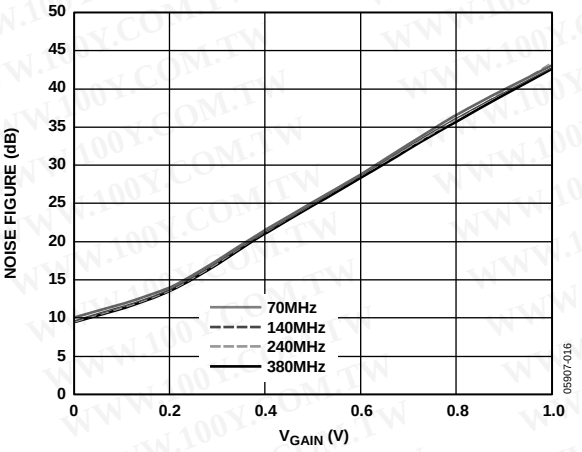

Figure 16. Noise Figure vs. V_{GAIN} (V_{MODE} = 0 V)

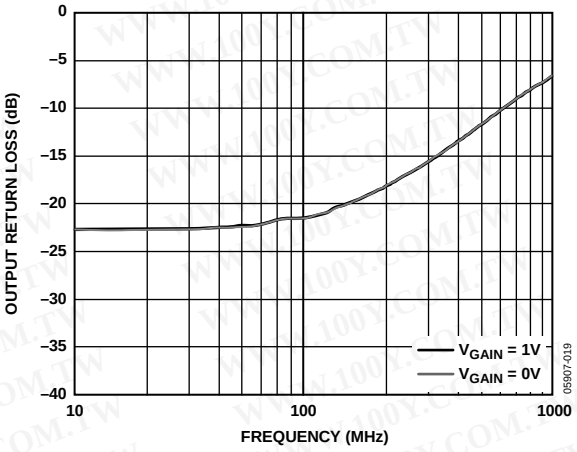

Figure 19. Output Return Loss vs. Frequency

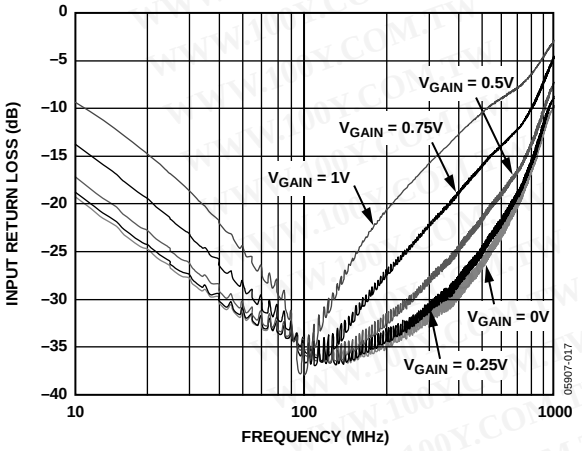

Figure 17. Input Return Loss vs. Frequency

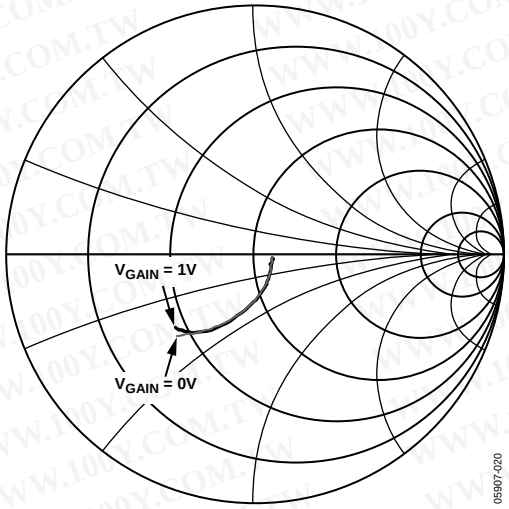

Figure 20. Output Reflection Coefficient vs. Frequency

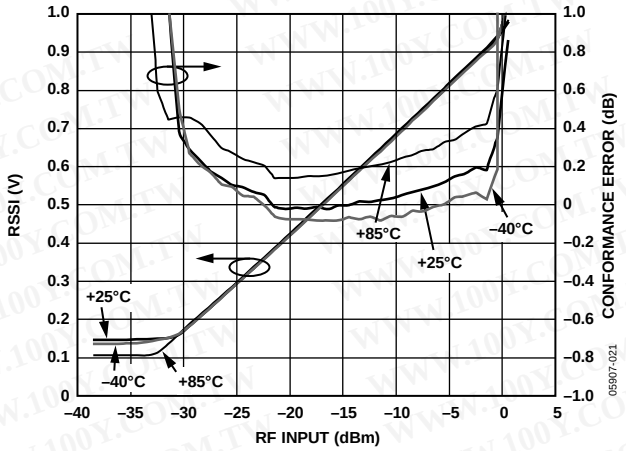

Figure 21. RSSI (V_{DETO}) and Conformance Error vs. Input Power (f = 70 MHz)

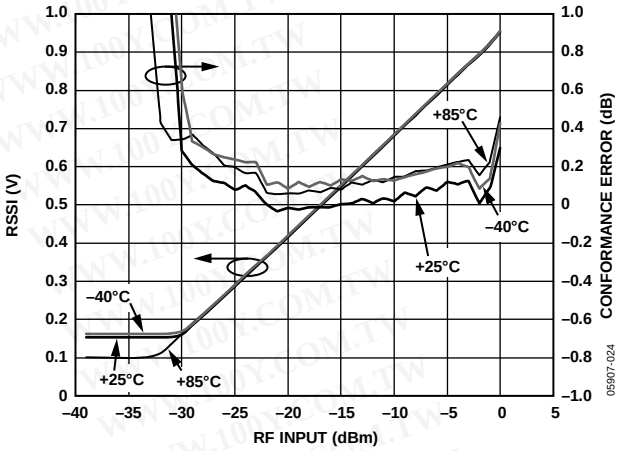

Figure 24. RSSI (V_{DETO}) and Conformance Error vs. Input Power (f = 380 MHz)

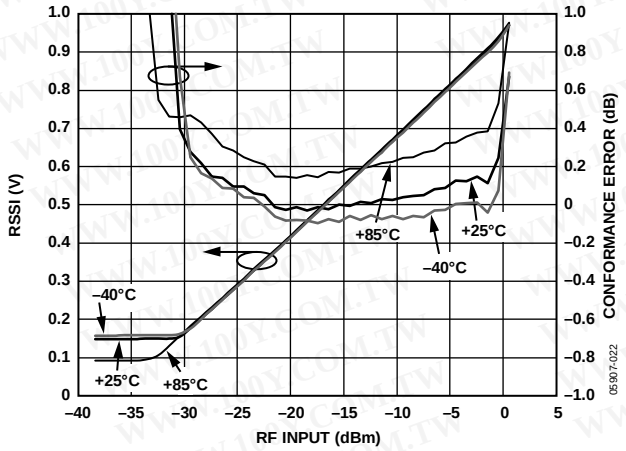

Figure 22. RSSI (V_{DETO}) and Conformance Error vs. Input Power (f = 140 MHz)

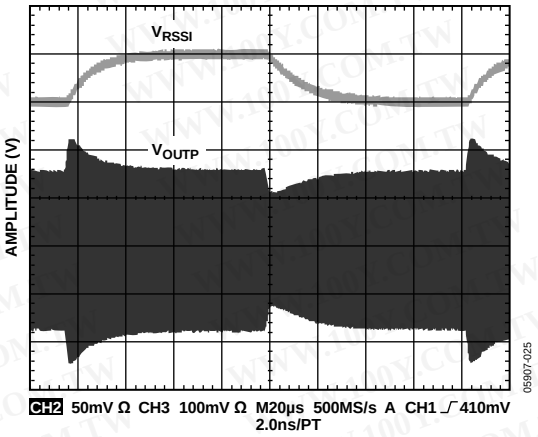

Figure 25. AGC Time Domain Response (3 dB Power Step, C_{DETO} = 1 nF)

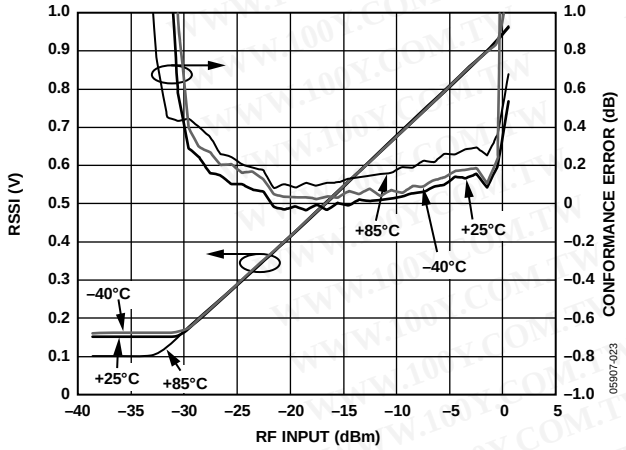

Figure 23. RSSI (V_{DETO}) and Conformance Error vs. Input Power (f = 240 MHz)

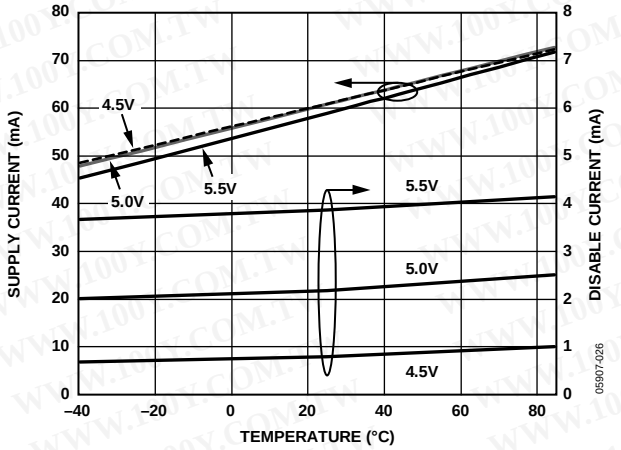

Figure 26. Supply Current and Disable Current vs. Temperature

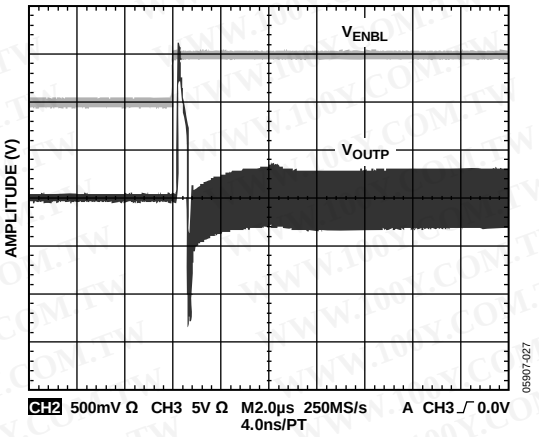

Figure 27. ENBL Response Time

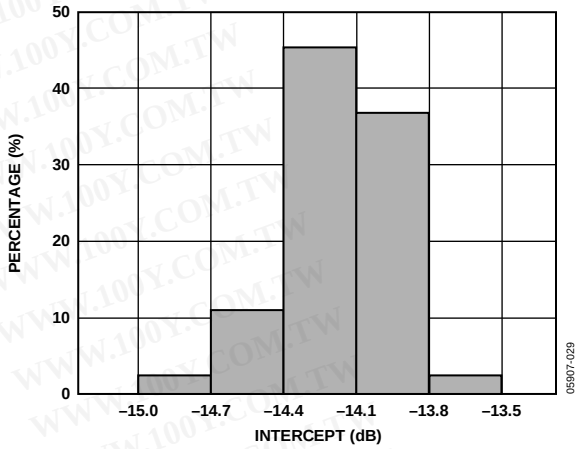

Figure 29. Gain Intercept Distribution (140 MHz)

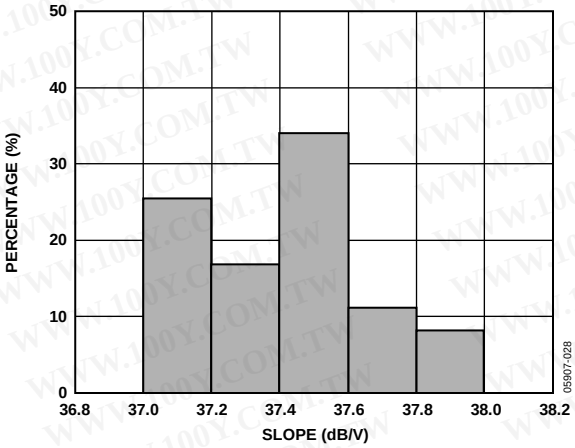

Figure 28. Gain Scaling Distribution (140 MHz)

CIRCUIT DESCRIPTION

The AD8368 is a single-ended VGA with a bandwidth of 800 MHz and a gain control span of 34 dB ranging from −12 dB to +22 dB. It incorporates an uncommitted square law detector that can be used to form a tight AGC loop around the VGA. Using the Analog Devices patented X-AMP architecture, the AD8368 achieves accurate linear-in-dB gain control with excellent linearity (OIP3) and noise figure (NF). The part also features 50 Ω input and output impedances for ease of use.

The main signal path, shown in Figure 30, consists of a variable input attenuator followed by a fixed-gain amplifier and output buffer. This architecture allows for a constant OIP3 and output noise floor as a function of gain setting. As a result, NF and IIP3 increase 1 dB for every 1 dB decrease in gain, resulting in a part with constant dynamic range over gain setting.

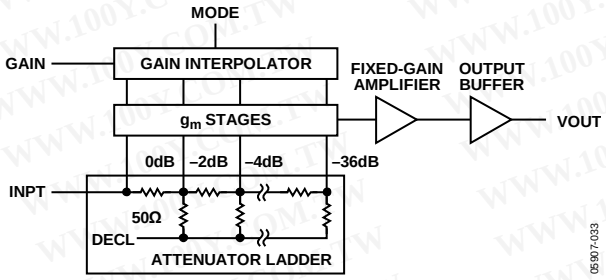

Figure 30. Simplified Block Diagram

INPUT ATTENUATOR AND INTERPOLATOR

The input attenuator is built from an 18-section resistor ladder, providing 2 dB of attenuation at each successive tap point. The resistor ladder acts as a linear input attenuator, in addition to providing an accurate 50 Ω input impedance. The variable transconductance (g_m) stages are used to select the attenuated signal from the appropriate tap point along the ladder and feed this signal to the fixed-gain amplifier. To realize a continuous gain control function from discrete tap points, the gain interpolator creates a weighted sum of signals appearing on adjacent tap points by carefully controlling the variable g_m stages.

FIXED-GAIN STAGE AND OUTPUT BUFFER

The weighted sum of the different tap points is fed into the fixed-gain stage that drives the output buffer. Because the resistive input attenuator is linear and contributes minimal noise as a passive termination, the dynamic range as a function of gain is determined primarily by the noise and the distortion of the fixed-gain amplifier. This architecture explains the constant OIP3 and constant output noise floor with gain setting and the corresponding dB-for-dB increase in IIP3 and NF with decreasing gain. The output buffer has 6 dB of gain and provides a broadband 50 Ω single-ended output impedance.

OUTPUT OFFSET CORRECTION

The dc level at the input, INPT, is driven by an internal reference to $V_S/2$. The reference is made available at the DECL pin for external decoupling with C_{DECL}. The dc level at the output, OUTP, is regulated to the same midsupply reference by an offset correction loop independent of gain setting, temperature, and process. The low-pass response of this loop creates a high-pass corner frequency in the signal path transfer function, which can be set by choosing C_{DECL} and C_{HPFL}.

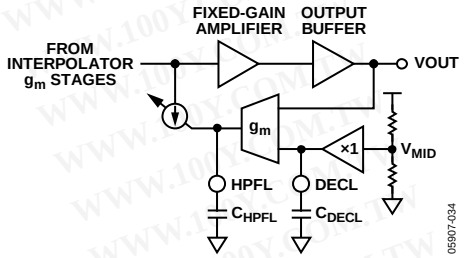

Figure 31. Output Centering Control Loop

The input and output coupling capacitors should be selected to provide low impedances at the frequencies of interest relative to 50 Ω so as not to affect the high-pass corner. In this case, the high-pass corner frequency can be set by either C_{HPFL} or C_{DECL}, which form independent poles in the feedback path of the offset correction loop. The high-pass corner is determined by the highest of these poles, which are given by

$$f_{HP,\,HPFL}(\text{kHz}) = \frac{0.8}{(0.005 + C_{HPFL})}$$

$$f_{HP,\,DECL}(\text{kHz}) = \frac{5700}{(0.005 + C_{DECL})}$$

where C_{HPFL} and C_{DECL} are in nF.

When using this method to set the high-pass frequency, the other capacitor should be sized such that its pole is at least 30× lower in frequency. In addition, note that C_{DECL} represents the total decoupling capacitance at the DECL pins.

INPUT AND OUTPUT IMPEDANCES

The AD8368 offers single-ended broadband 50 Ω input and output impedances. The excellent match to 50 Ω is maintained from part to part, over frequency, and over gain setting. Both the input and output pins must be externally ac-coupled to prevent disruption of the internal dc levels. Sufficiently large coupling capacitors should be used so that their impedance is negligible relative to the 50 Ω presented by the ladder at the input and by the output buffer at the output.

GAIN CONTROL INTERFACE

The AD8368 has a linear-in-dB gain control interface that can be operated in either a gain-up mode or gain-down mode. In the gain-up mode with the MODE pin pulled high, the gain increases with increasing gain voltages. In the gain-down mode, with the MODE pin pulled low, the gain decreases with increasing gain voltages. In both modes of operation, the gain control slope is maintained at +37.5 dB/V or −38 dB/V (depending on mode selection) over temperature, supply, and process as V_{GAIN} varies from 100 mV to 900 mV. To form an AGC loop with the on-board detector around the VGA, the MODE pin has to be pulled low.

The gain functions for MODE pulled high and low are given respectively by

$$Gain_{HIGH}\ (\text{dB}) = 37.5 \times V_{GAIN} - 14$$

$$Gain_{LOW}\ (\text{dB}) = -38 \times V_{GAIN} + 24.8$$

where V_{GAIN} is expressed in volts.

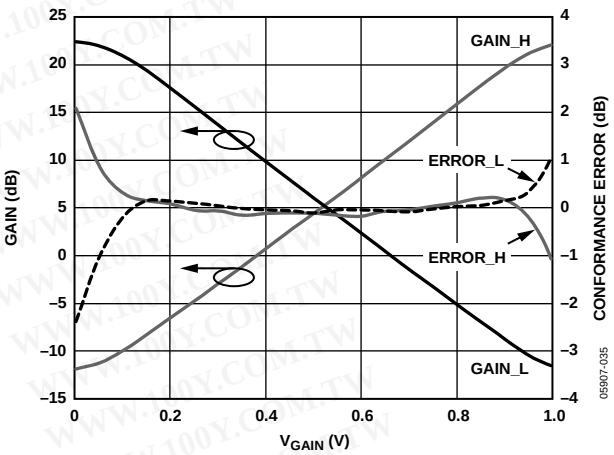

Figure 32. Gain and Conformance Error vs. V_{GAIN}

As shown in Figure 32, the gain function can be either an increasing or decreasing function of V_{GAIN}, depending on the MODE pin.

APPLICATIONS INFORMATION

VGA OPERATION

The AD8368 is a general-purpose VGA suitable for use in a wide variety of applications where accurate, continuous, linear-in-dB gain control over a broad range of frequencies is important. Its stability over temperature and supply in comparison to other variable gain techniques can be traced back to the X-AMP architecture. While having an 800 MHz bandwidth, its low frequency operation can be extended by properly selecting C_{HPFL} and C_{DECL}.

The typical connections for using the AD8368 in VGA mode are illustrated in Figure 33. The input (INPT) and output (OUTP) of the AD8368 should be externally ac-coupled to prevent disrupting the dc levels on the chip. Therefore, a sufficiently large coupling capacitor should be used such that the series impedance of the capacitor is negligible at the frequencies of interest.

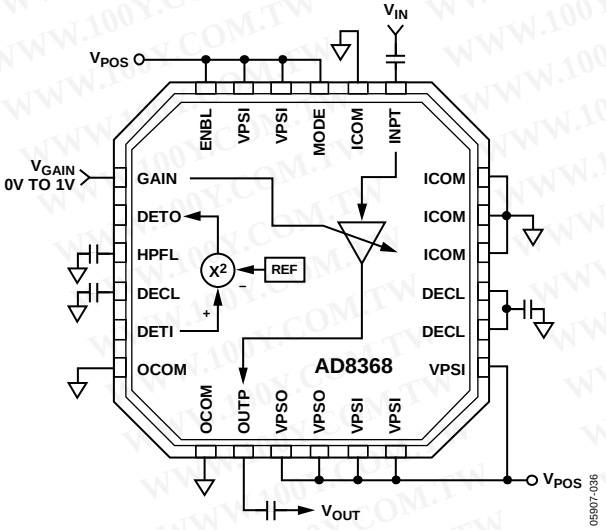

Figure 33. Typical Connections for VGA Mode for Increasing Gain with Increasing V_{GAIN} (MODE High)

The gain control voltage ranging from 0 V to 1 V is applied to the GAIN pin. The MODE pin controls whether the gain of the part is an increasing or decreasing function of the gain voltage. When the MODE pin is pulled high, the gain increases with increasing gain voltages. When the MODE pin is pulled low, the gain decreases with increasing gain voltages. The ENBL pin is used to enable or disable the part. ENBL is active high; when ENBL is pulled low, the part is disabled and draws a fraction of the normal supply current.

The DECL pin provides the internal midsupply dc reference for the AD8368. It should be well decoupled to ground using a large capacitor with low ESR. The capacitors connected to the HPFL pin and DECL pin are used to control the low-pass corner frequency of the output offset correction loop. The resulting high-pass corner frequency is inversely proportional to their values.

AGC OPERATION

The AD8368 can be configured as a standalone AGC amplifier by using the on-board rms detector, as shown in Figure 34. The detector output, DETO, is an error current representing the difference of squares between the root-mean-square (rms) of the sensed signal and an internal reference of 63 mV rms. This error current is integrated on C_{DETO} and connected to the GAIN pin to form the AGC loop.

The 63 mV rms reference corresponds to 178 mV p-p for a sine wave but the detector accuracy is maintained for more complex signals, such as Gaussian noise, complex envelopes, and multi-carrier signals with high peak-to-average ratios.

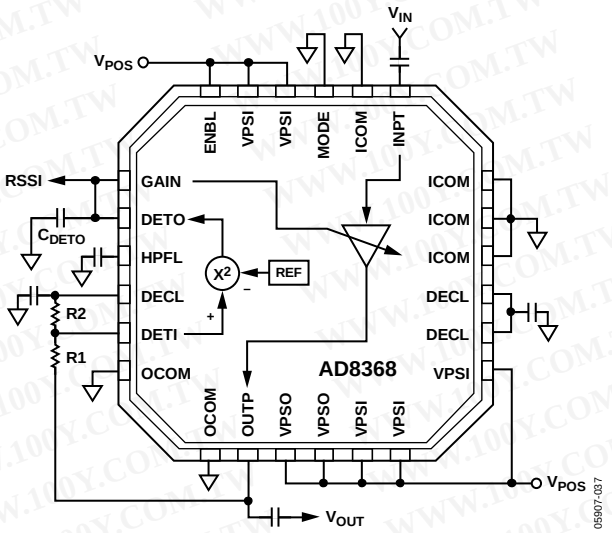

Figure 34. AGC Mode of Operation

The AGC mode of operation requires a specific gain direction. The gain must fall as V_{DETO} increases to restore the needed balance against the setpoint. Therefore, the MODE pin must be pulled low. By connecting the signal at OUTP directly to the detector input (DETI), the output level is driven to the 63 mV rms reference setpoint.

The output setpoint can be increased using an external resistive divider network between OUTP and DETI, referenced to DECL as depicted in Figure 34. In this configuration, the rms output voltage is forced to (1 + R1/R2) 63 mV rms by the AGC loop. For a 0 dBm (224 mV rms referenced to 50 Ω) output setpoint, this ratio is 3.5. After correcting for the input impedance of DETI, the choice of R1 = 226 Ω and R2 = 100 Ω yields a setpoint of roughly 0 dBm. This very accurate leveling function is shown in Figure 35, where the rms output is held to within 0.2 dB of the 0 dBm setpoint for >30 dB range of input levels.

Figure 35. Output Power vs. Input Power in AGC Mode at 140 MHz

Note that to achieve the accurate level of AGC output power, the DECL capacitor must be adjusted for the corresponding RF frequency. The DECL capacitor value varies depending on board parasitics. Table 5 shows the DECL capacitor value based on the evaluation board parasitics.

Table 5. DECL Capacitor Value

IF Frequency (MHz)	C4 (pF)	C20 (pF)
70	1000	2200
140	270	560
240	68	150
380	33	68
480	15	39

A valuable feature of using a square law detector in AGC mode is that the RSSI voltage is a true reflection of signal power and can be converted to an absolute power measurement for any given source impedance. The RSSI in units of dBm referenced to 50 Ω and based on the voltage available on the DETO pin is given by

$$RSSI = -11 + 20\log_{10}(1 + R1/R2) + 38 \times V_{DETO} - 24.8$$

Figure 36 shows a plot of the RSSI voltage at DETO as input power is swept.

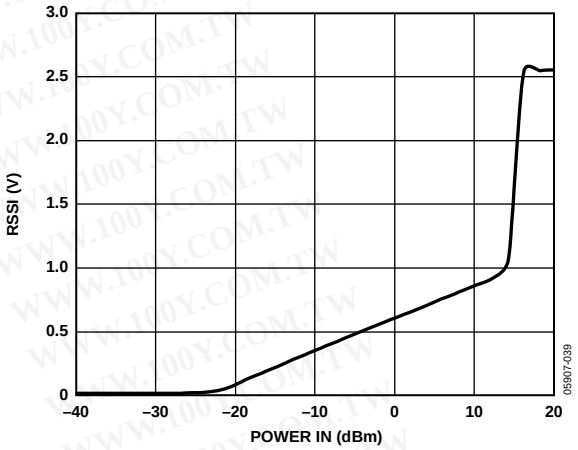

Figure 36. Monitoring the GAIN/DETO RSSI Voltage vs. Input Power

In some cases, it can be found that, if driven into AGC overload, the AD8368 requires unusually long times to recover; that is, the voltage at DETO remains at an abnormally high value, and the gain is at its lowest value. To avoid this situation, it is recommended that a clamp be placed on the DETO pin, as shown in Figure 37.

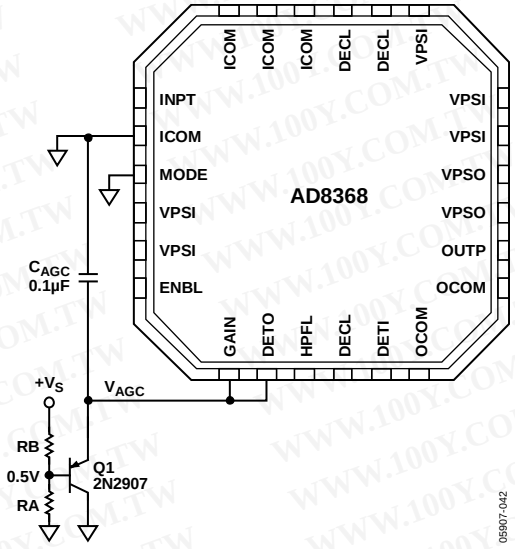

Figure 37. External Clamp to Prevent AGC Overload

The resistive divider network, RA and RB, should be designed such that the base of Q1 is driven to 0.5 V.

The choice of C_{DETO} is a compromise of averaging time constant, response time, and carrier leakage. If C_{DETO} is selected to be too small to speed up the response time, the AGC loop could start tracking and leveling any amplitude envelope and corrupt the constellation. Figure 38 illustrates a 16 QAM, 100 ksymbols per second constellation with a degraded error vector magnitude (EVM) of 5%. By increasing C_{DETO} to 0.01 µF, the EVM is improved to 1.1%.

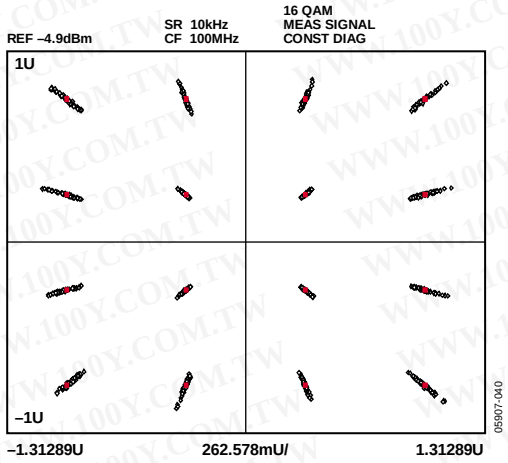

Figure 38. Degraded Error Vector Magnitude Performance for 16 QAM at 100 ksymbols per second (C_{DETO} Too Small)

Figure 39 illustrates the measured EVM performance for a 16 QAM modulation at 10 Msymbols per second using C_{DETO} = 1 nF.

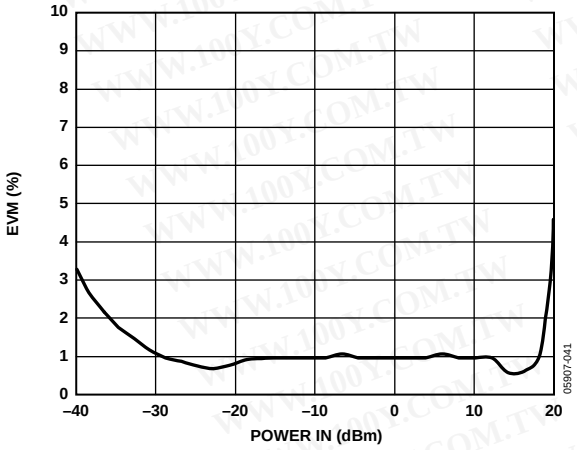

Figure 39. Error Vector Magnitude Performance for 16 QAM 10 Msymbols per second

STABILITY AND LAYOUT CONSIDERATIONS

In some applications, the printed circuit board (PCB) parasitic, in combination with the source impedance presented by the driving stage, can present some troublesome impedance at high frequency and can potentially unstablize the amplifier under certain extreme conditions, such as high gain and high temperature. To avoid such scenarios, it is recommended to include a simple parallel RL snubbing network directly at the input terminal of the AD8368. Figure 40 depicts an example of this network. The RL network formed by R3 and L1 is used to minimize the negative impact due to reflective source conditions at high RF frequencies and ensures the amplifier operates unconditionally stable and maintains the typical device performance.

On the underside of the chip scale package, there is an exposed compressed paddle. This paddle is internally connected to the ground of the chip. Solder the paddle to the low impedance ground plane on the PCB to ensure specified electrical performance and to provide thermal relief. It is also recommended that the ground planes on all layers under the paddle be stitched together with vias to reduce thermal impedance.

EVALUATION BOARD

The standard evaluation board schematic and layout artwork is presented in Figure 41 through Figure 44. The evaluation board is fabricated on a multilayer FR-4 board, with 50 Ω-controlled impedance transmission lines for the RF input and output traces. The board is powered by a single supply in the 4.5 V to 5.5 V range. The power supply is decoupled by 0.1 µF and 1 nF capacitors at each power supply pin. Additional decoupling, in the form of a series resistor or inductor at the supply pins, can also be added. Table 6 details the various configuration options of the evaluation board.

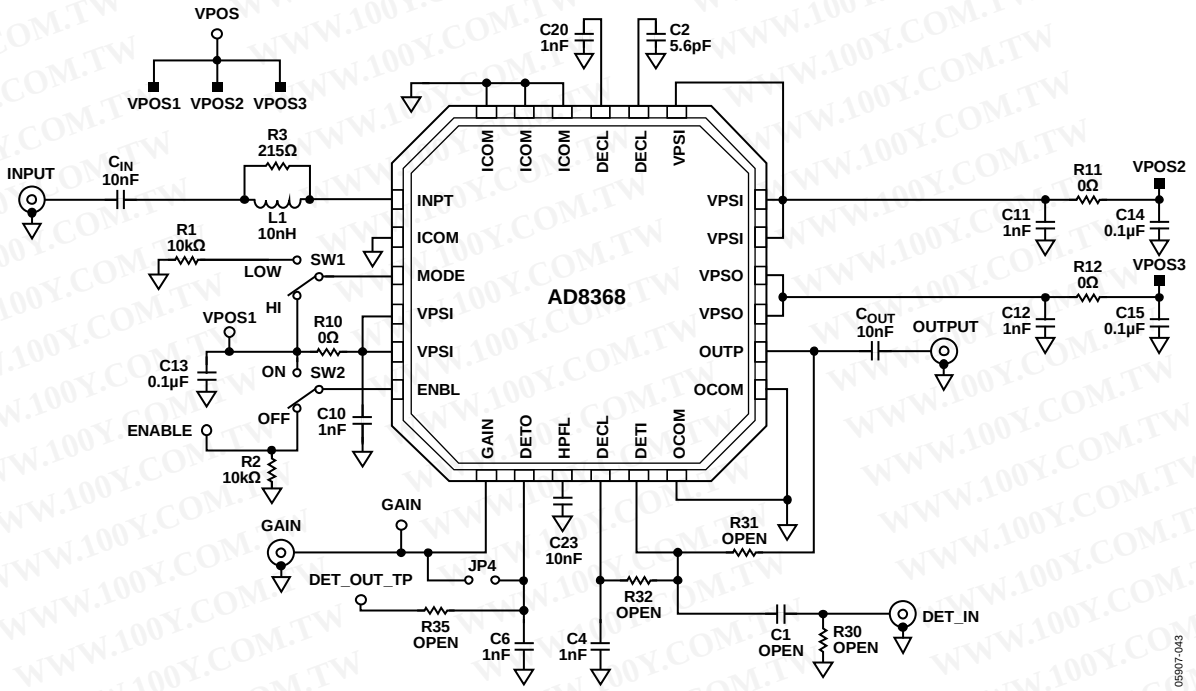

Figure 40. Evaluation Board

Table 6. Evaluation Board Configuration Options

Component	Function	Default Conditions
R1, R2, R3, L1	Pull-Down Resistors for MODE and ENBL. RL network. Prevent potential instability impact due to PCB parasitics and/or certain extreme conditions (see the Stability and Layout Considerations section).	R1 = R2 = 10 kΩ R3 = 215 Ω L1 = 10 nH
R10, R11, R12, C10, C11, C12, C13, C14, C15	Supply Decoupling. Jumpers, power supply decoupling resistors, and filter capacitors.	R10 = R11 = R12 = 0 Ω C10 = C11 = C12 = 1 nF C13 = C14 = C15 = 0.1 µF
C_{IN}	RF Input. C_{IN} provides dc block for RF input.	C_{IN} = 10 nF
C_{OUT}	RF Output. C_{OUT} provides dc block for RF output.	C_{OUT} = 10 nF
R31, R32	Feedback Path for AGC Operation. For a default setpoint of 63 mV rms, set R31 = 0 Ω and remove R32. For other AGC setpoints, rms voltage = (1 + n) × 63 mV rms, where n = R31/R32.	R31 = R32 = Open (VGA mode)
R35	Populate with 0 Ω to feed detector output RSSI voltage to DET_OUT_TP.	R35 = Open
C23	Sets the corner frequency of the output offset control loop high-pass filter.	C23 = 10 nF
C1, R30	Used for driving the detector externally. Set R30 to 50 Ω for matching. Set C1 to be a large ac coupling capacitor.	C1 = Open R30 = Open
C6	DETO Capacitor. Needs to be made larger for lower data rates (see the AGC Operation section).	C6 = 1 nF
C20, C2, C4	DECL Capacitor. Needs to be adjusted based on RF frequency in AGC operation (see the AGC Operation section).	C20 = C4 = 1 nF C2 = 5.6 pF

Component	Function	Default Conditions
JP4	Jumper for AGC Mode of Operation. Provides feedback from the detector output to the gain pin.	JP4 = not populated (VGA mode)
SW1	Mode Switch. Low mode puts the part in gain-down mode. High mode puts the part in gain-up mode. AGC operation requires gain-down mode.	SW1 = JP2
SW2	Power-Down. The part is disabled when the enable pin is tied to ground.	SW2 = JP3

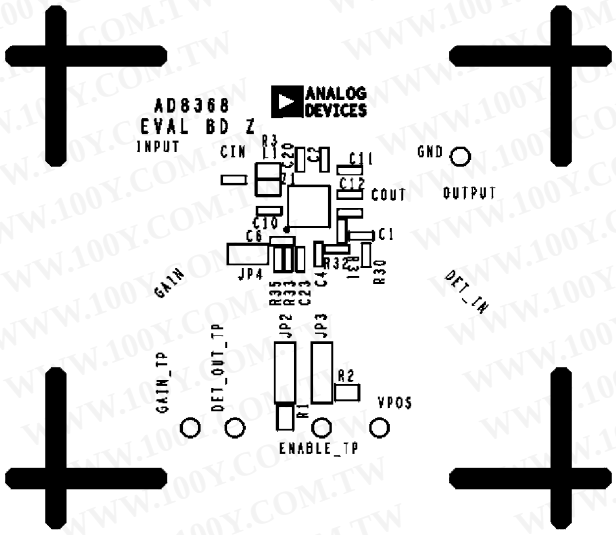

Figure 41. Component Side Silkscreen

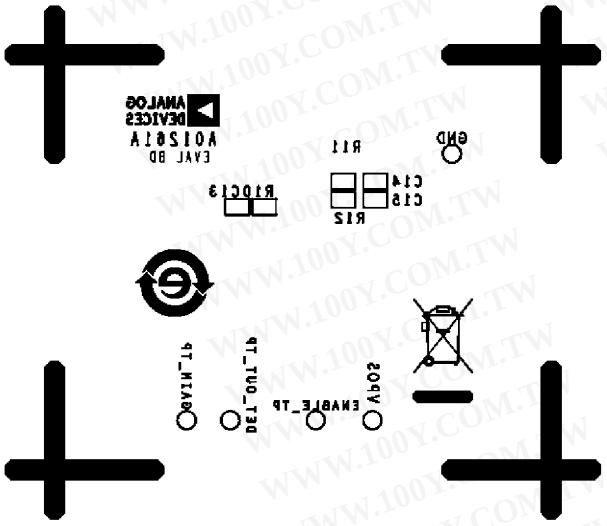

Figure 42. Circuit Side Silkscreen

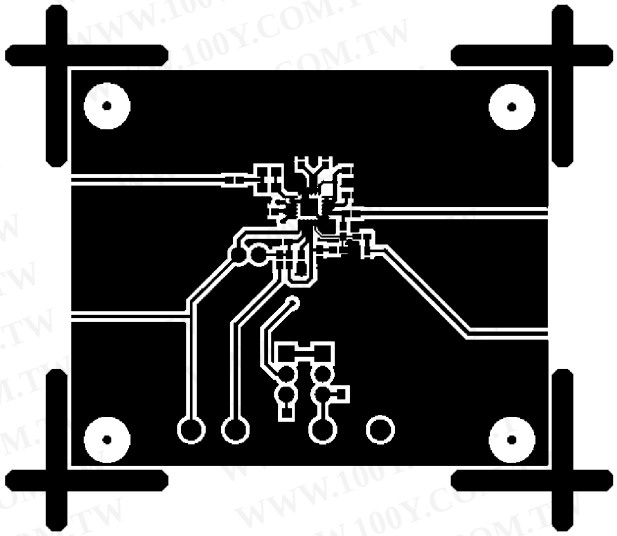

Figure 43. Component Side Layout

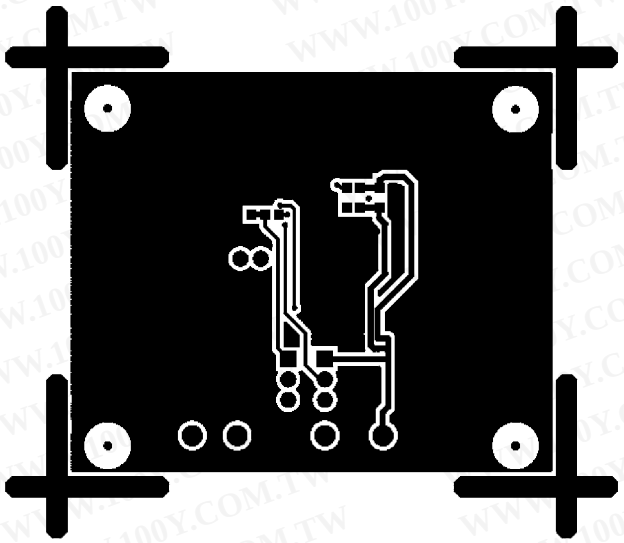

Figure 44. Circuit Side Layout

OUTLINE DIMENSIONS

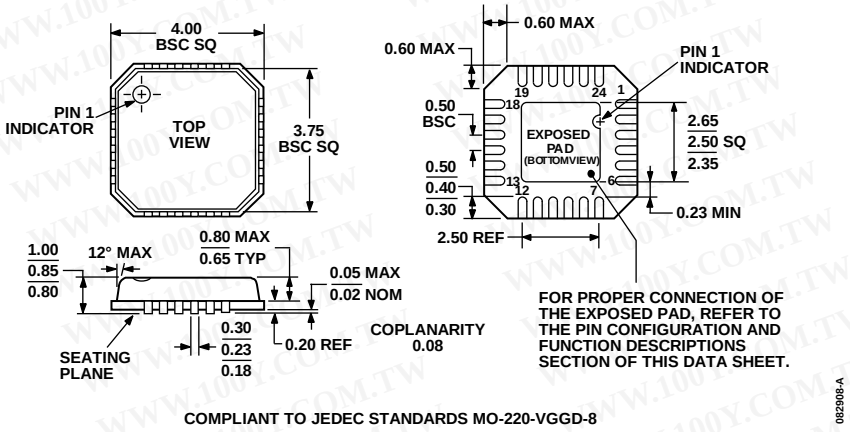

Figure 45. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8368ACPZ-REEL7[1]	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-24-3	1,500
AD8368ACPZ-WP[1, 2]	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-24-3	64
AD8368-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] WP = waffle pack.

NOTES

D05907-0-9/08(B)