General-Purpose, Low Cost, DC-Coupled VGA

AD8337

FEATURES

- Low noise
  - Voltage noise = 2.2 nV/√Hz
  - Current noise = 4.8 pA/√Hz (positive input)
- Wide bandwidth (−3 dB) = 280 MHz
- Nominal gain range: 0 dB to 24 dB (preamp gain = 6 dB)
- Gain scaling: 19.7 dB/V
- DC-coupled
- Single-ended input and output
- High speed uncommitted op amp input
- Supplies: +5 V, ±2.5 V, or ±5 V
- Low power: 78 mW with ±2.5 V supplies

APPLICATIONS

- Gain trim
- PET scanners
- High performance AGC systems
- I/Q signal processing
- Video
- Industrial and medical ultrasound
- Radar receivers

GENERAL DESCRIPTION

The AD8337 is a low noise, single-ended, linear-in-dB, general-purpose variable gain amplifier (VGA) usable at frequencies from dc to 100 MHz; the −3 dB bandwidth is 280 MHz. Excellent bandwidth uniformity across the entire gain range and low output-referred noise makes the AD8337 ideal for gain trim applications and for driving high speed analog-to-digital converters (ADCs).

Excellent dc characteristics combined with high speed make the AD8337 particularly suited for industrial ultrasound, PET scanners, and video applications. Dual-supply operation enables gain control of negative-going pulses, such as those generated by photodiodes or photomultiplier tubes.

The AD8337 uses the popular and versatile X-AMP® architecture, exclusively from Analog Devices, Inc., with a gain range of 24 dB. The gain control interface provides precise linear-in-dB scaling of 19.7 dB/V, referenced to VCOM.

FUNCTIONAL BLOCK DIAGRAM

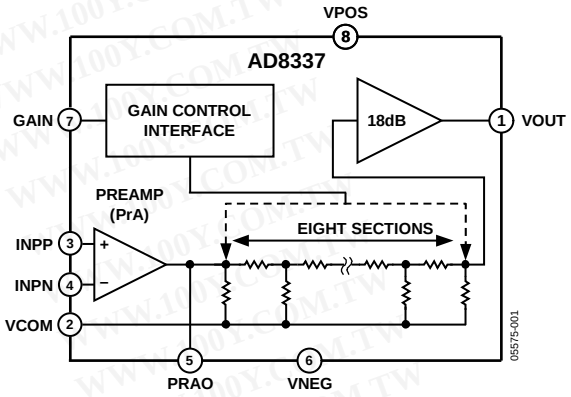


Figure 1.

The AD8337 includes an uncommitted operational current-feedback preamplifier (PrA) that operates in inverting or noninverting configurations. Using external resistors, the device can be configured for gains of 6 dB or greater. The AD8337 is characterized by a noninverting PrA gain of 2× using two external 100 Ω resistors. The attenuator has a range of 24 dB, and the output amplifier has a fixed gain of 8× (18.06 dB). The lowest nominal gain range is 0 dB to 24 dB and can be shifted up or down by adjusting the preamp gain. Multiple AD8337 devices can be connected in series for larger gain ranges, interstage filtering to suppress noise and distortion, and nulling offset voltages.

The operating temperature range of the AD8337 is −40°C to +85°C, and is available in an 8-lead, 3 mm × 3 mm LFCSP.

Rev. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

9/08—Rev. B to Rev. C

Changes to Table 1 ... 3
Added Exposed Pad Note to Figure 2 and Table 3 ... 6
Changes to Figure 49 ... 14
Changes to Evaluation Boards Section ... 23
Changes to Circuit Options Section ... 24
Changes to Output Protection Section ... 24
Changes to Measurement Setup Section ... 25
Changes to Board Layout Considerations Section ... 25
Changes to Bill of Materials Section ... 27
Updated Outline Dimensions, Changes to Ordering Guide ... 29

2/07—Rev. A to Rev. B

Changes to Figure 30, Figure 31, and Figure 32 ... 11
Changes to Single-Supply Operation and AC Coupling Section ... 19
Moved Noise Section to Page ... 19
Changes to Ordering Guide ... 24

6/06—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Table 3 ... 6
Changes to Figure 22, Figure 25, and Figure 26 ... 10
Changes to Figure 39 and Figure 40 ... 13
Changes to Figure 74 and Figure 75 ... 23
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25

9/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±2.5 V, T_A = 25°C, PrA gain = +2, V_{COM} = GND, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω, including a 20 Ω snubbing resistor, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
GENERAL PARAMETERS					
−3 dB Small Signal Bandwidth	V_{OUT} = 10 mV p-p		280		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p		100		MHz
Slew Rate	V_{OUT} = 2 V p-p		625		V/µs
	V_{OUT} = 1 V p-p		490		V/µs
Input Voltage Noise	f = 10 MHz		2.15		nV/√Hz
Input Current Noise	f = 10 MHz		4.8		pA/√Hz
Noise Figure	V_{GAIN} = 0.7 V, R_S = 50 Ω, unterminated		8.5		dB
	V_{GAIN} = 0.7 V, R_S = 50 Ω, shunt terminated with 50 Ω		14		dB
Output-Referred Noise	V_{GAIN} = 0.7 V (gain = 24 dB)		34		nV/√Hz
	V_{GAIN} = −0.7 V (gain = 0 dB)		21		nV/√Hz
Output Impedance	DC to 10 MHz		1		Ω
Output Signal Range	R_L ≥ 500 Ω, V_S = ±2.5 V, +5 V		V_{COM} ± 1.3		V
	R_L ≥ 500 Ω, V_S = ±5 V		V_{COM} ± 2.4		V
Output Offset Voltage	V_{GAIN} = 0.7 V (gain = 24 dB)	−25	±5	+25	mV
DYNAMIC PERFORMANCE					
Harmonic Distortion	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		−72		dBc
HD3			−66		dBc
HD2	f = 10 MHz		−62		dBc
HD3			−63		dBc
HD2	f = 45 MHz		−58		dBc
HD3			−56		dBc
Input 1 dB Compression Point	V_{GAIN} = −0.7 V, f = 10 MHz (preamp limited)		8.2		dBm
	V_{GAIN} = +0.7 V, f = 10 MHz (VGA limited)		−9.4		dBm
Two-Tone Intermodulation Distortion (IMD3)	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−71		dBc
	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−57		dBc
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−58		dBc
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−45		dBc
Output Third-Order Intercept	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f = 10 MHz		34		dBm
	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f = 45 MHz		28		dBm
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f = 10 MHz		35		dBm
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f = 45 MHz		26		dBm
Overload Recovery	V_{GAIN} = 0.75 V, V_{IN} = 50 mV p-p to 500 mV p-p		50		ns
Group Delay Variation	1 MHz < f < 100 MHz, full gain range		±1		ns

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	V_S = ±5 V				
Harmonic Distortion	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		−85		dBc
HD3			−75		dBc
HD2	f = 10 MHz		−90		dBc
HD3			−80		dBc
HD2	f = 35 MHz		−75		dBc
HD3			−76		dBc
Input 1 dB Compression Point	V_{GAIN} = −0.7 V, f = 10 MHz		14.5		dBm
	V_{GAIN} = +0.7 V, f = 10 MHz		−1.7		dBm
Two-Tone Intermodulation Distortion (IMD3)	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−74		dBc
	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−60		dBc
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−64		dBc
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−49		dBc
Output Third-Order Intercept	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f = 10 MHz		35		dBm
	V_{GAIN} = 0 V, V_{OUT} = 1 V p-p, f = 45 MHz		28		dBm
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f = 10 MHz		36		dBm
	V_{GAIN} = 0 V, V_{OUT} = 2 V p-p, f = 45 MHz		28		dBm
Overload Recovery	V_{GAIN} = 0.7 V, V_{IN} = 0.1 V p-p to 1 V p-p		50		ns
ACCURACY					
Absolute Gain Error	−0.7 V < V_{GAIN} < −0.6 V		0.7 to 3.5		dB
	−0.6 V < V_{GAIN} < −0.5 V	−1.25	±0.35	+1.25	dB
	−0.5 V < V_{GAIN} < +0.5 V	−1.0	±0.25	+1.0	dB
	0.5 V < V_{GAIN} < 0.6 V	−1.25	±0.35	+1.25	dB
	0.6 V < V_{GAIN} < 0.7 V		−0.7 to −3.5		dB
GAIN CONTROL INTERFACE					
Gain Scaling Factor	−0.6 V < V_{GAIN} < +0.6 V		19.7		dB/V
Gain Range			24		dB
Intercept	V_{GAIN} = 0 V		12.65		dB
Input Voltage (V_{GAIN}) Range	No foldover	$-V_S$		$+V_S$	V
Input Impedance			70		MΩ
Bias Current	−0.7 V < V_{GAIN} < +0.7 V		0.3		µA
Response Time	24 dB gain change		200		ns
POWER SUPPLY					
Supply Voltage	V_{POS} to V_{NEG} (dual- or single-supply operation)	4.5	5	10	V
V_S = ±2.5 V					
Quiescent Current	Each supply (VPOS and VNEG)	10.5	15.5	23.5	mA
Power Dissipation	No signal, VPOS to VNEG = 5 V		78		mW
PSRR	V_{GAIN} = 0.7 V, f = 1 MHz		−40		dB
V_S = ±5 V					
Quiescent Current	Each supply (VPOS and VNEG)	13.5	18.5	25.5	mA
Power Dissipation	No signal, VPOS to VNEG = 10 V		185		mW
PSRR	V_{GAIN} = 0.7 V, f = 1 MHz		−40		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

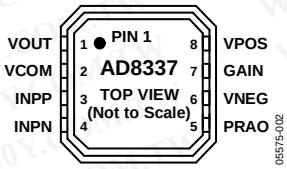
Parameter	Rating
Voltage	
Supply Voltage (VPOS, VNEG)	±6 V
Input Voltage (INPx)	VPOS, VNEG
GAIN Voltage	VPOS, VNEG
Power Dissipation (Exposed Pad Soldered to PCB)	866 mW
Temperature	
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Thermal Data, 4-Layer JEDEC Board No Air Flow Exposed Pad Soldered to PCB	
θ_{JA}	75.4°C/W
θ_{JB}	47.5°C/W
θ_{JC}	17.9°C/W
Ψ_{JT}	2.2°C/W
Ψ_{JB}	46.2°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. FOR BEST THERMAL PERFORMANCE, EXPOSED PAD MUST BE SOLDERED TO PCB.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT	VGA Output.
2	VCOM	Common Ground When Using Plus and Minus Supply Voltages. For single-supply operation, provide half the positive supply voltage at the VPOS pin to VCOM pin.
3	INPP	Positive Input to Preamplifier.
4	INPN	Negative Input to Preamplifier.
5	PRAO	Preamplifier Output.
6	VNEG	Negative Supply (–VPOS for Dual-Supply; GND for Single-Supply).
7	GAIN	Gain Control Input Centered at VCOM.
8	VPOS	Positive Supply.
EP	Exposed Pad	For best thermal performance, exposed pad must be soldered to PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±2.5 V, T_A = 25°C, R_L = 500 Ω, including a 20 Ω snubbing resistor, f = 10 MHz, C_L = 2 pF, V_{IN} = 10 mV p-p, noninverting configuration, unless otherwise noted.

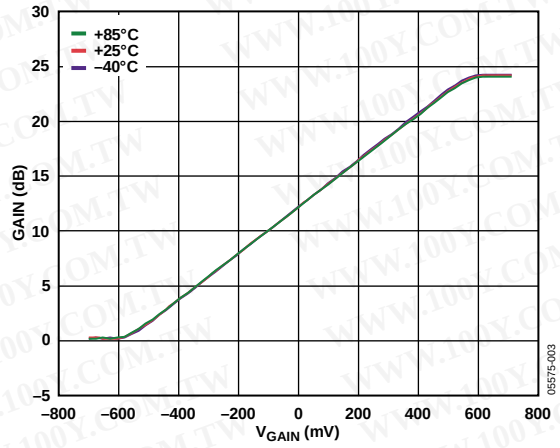


Figure 3. Gain vs. V_{GAIN} at Three Temperatures (See Figure 44)

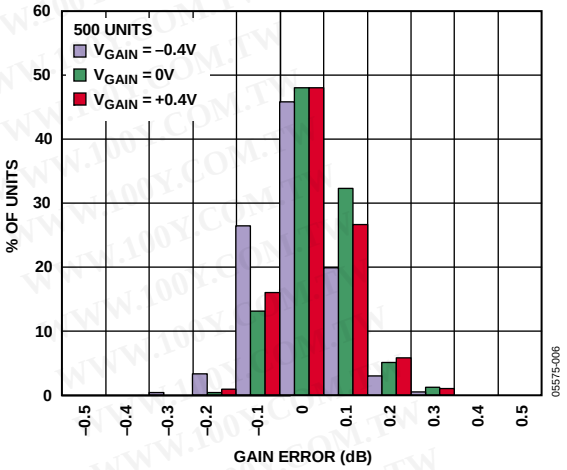


Figure 6. Gain Error Histogram for Three Values of V_{GAIN}

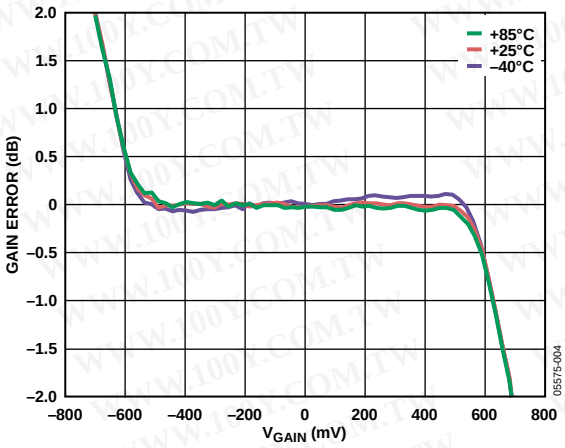


Figure 4. Gain Error vs. V_{GAIN} at Three Temperatures (See Figure 44)

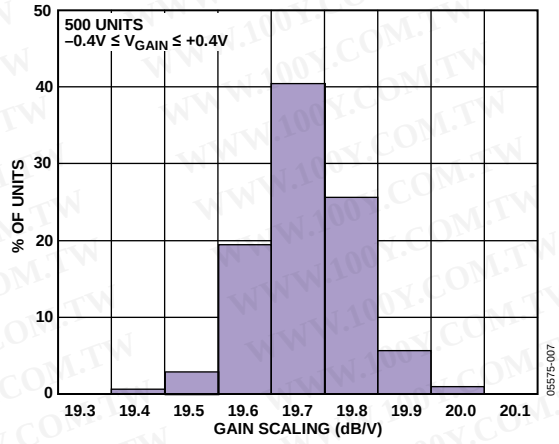


Figure 7. Gain Scaling Histogram

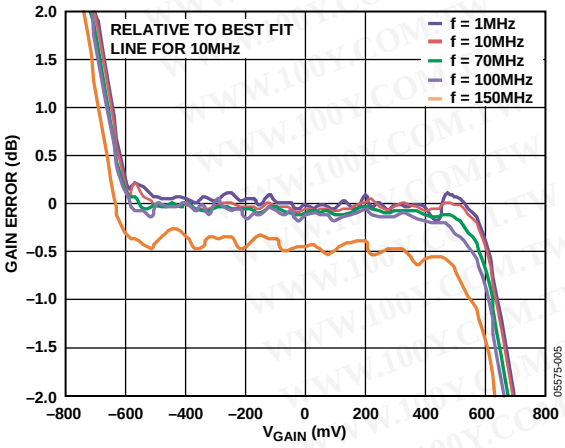


Figure 5. Gain Error vs. V_{GAIN} at Five Frequencies (See Figure 44)

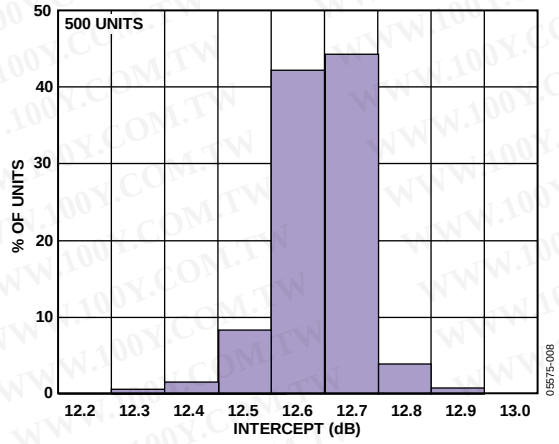


Figure 8. Intercept Histogram

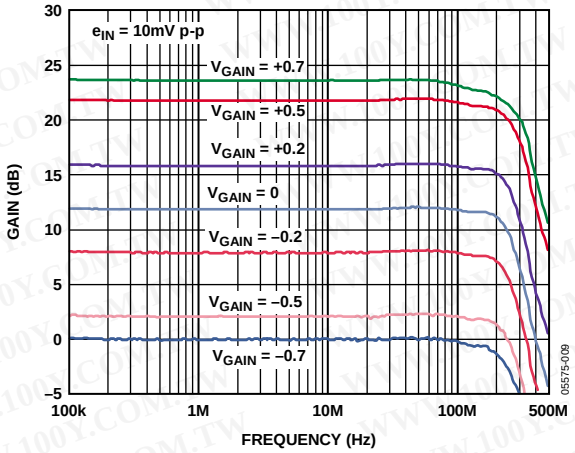


Figure 9. Frequency Response for Various Values of V_{GAIN} (See Figure 45)

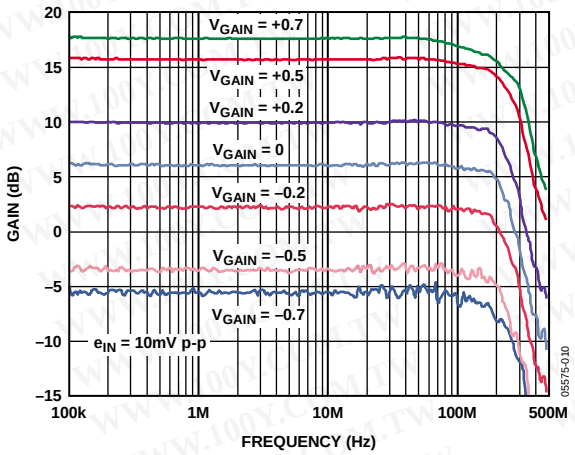


Figure 10. Frequency Response for Various Values of V_{GAIN}—Inverting Input (See Figure 58)

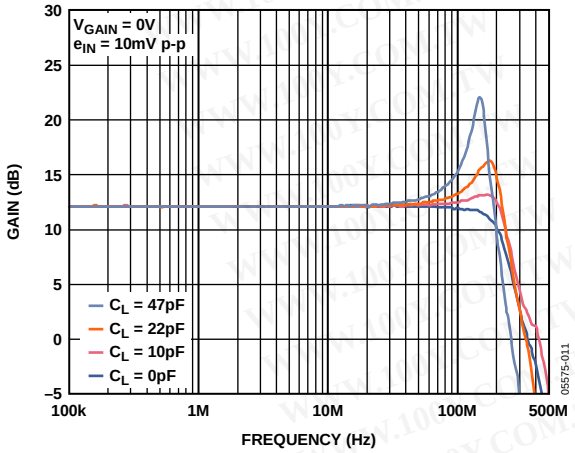


Figure 11. Frequency Response for Three Values of CL (See Figure 45)

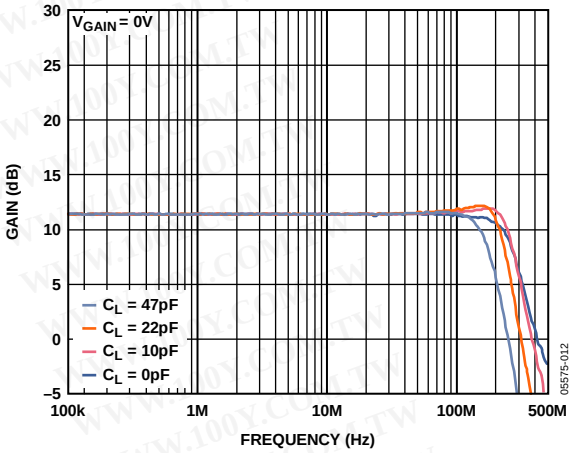


Figure 12. Frequency Response for Three Values of CL with a 20 Ω Snubbing Resistor (See Figure 45)

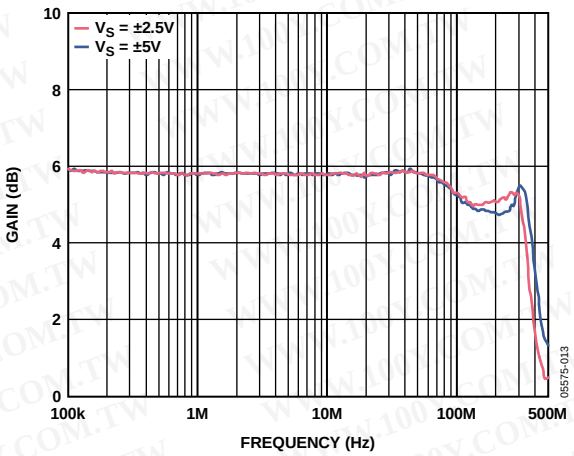


Figure 13. Frequency Response—Preamp (See Figure 46)

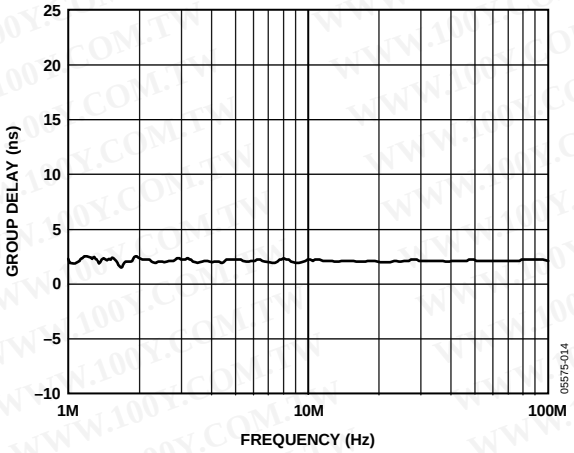


Figure 14. Group Delay vs. Frequency (See Figure 47)

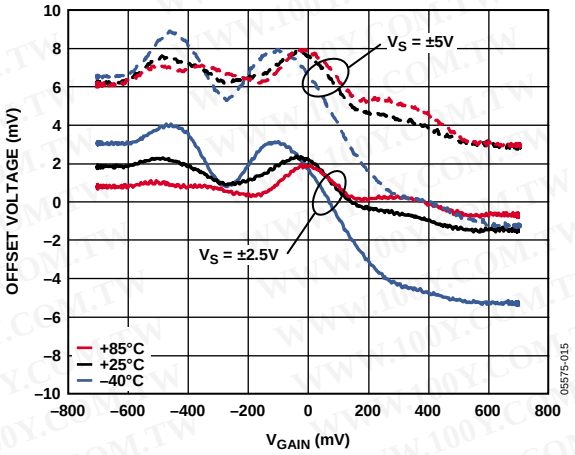


Figure 15. Offset Voltage vs. V_{GAIN} at Three Temperatures (See Figure 48)

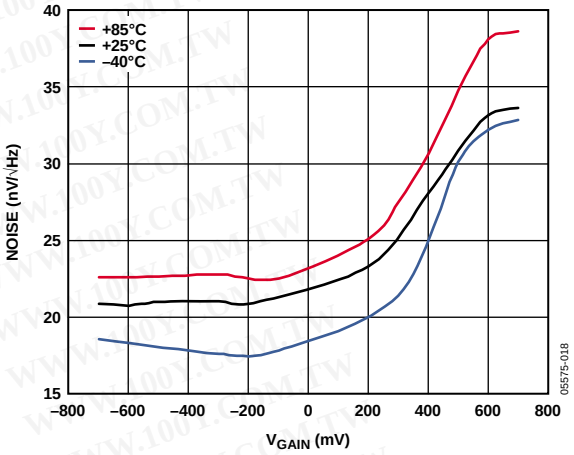


Figure 18. Output-Referred Noise vs. V_{GAIN} at Three Temperatures (See Figure 50)

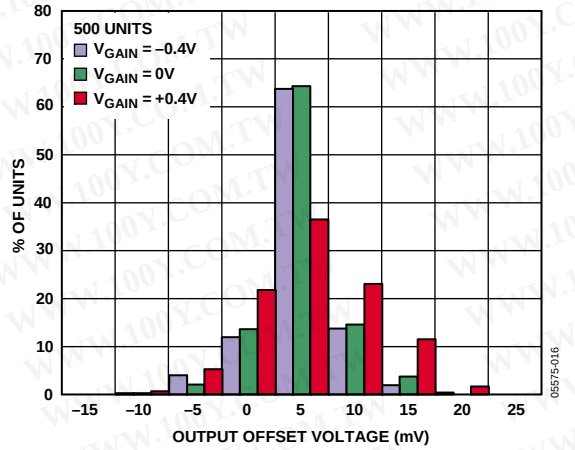


Figure 16. Output Offset Voltage Histogram for Three Values of V_{GAIN}

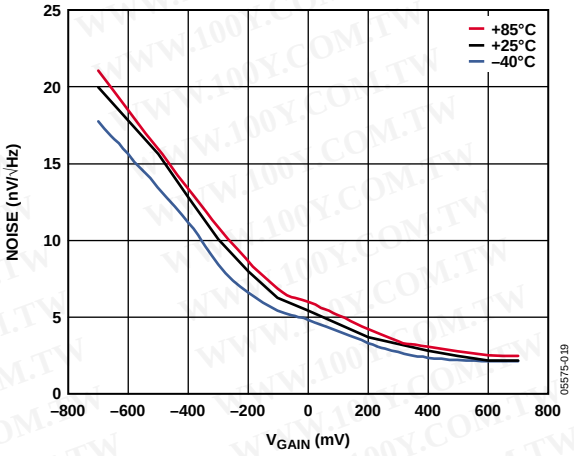


Figure 19. Short-Circuit, Input-Referred Noise at Three Temperatures (See Figure 50)

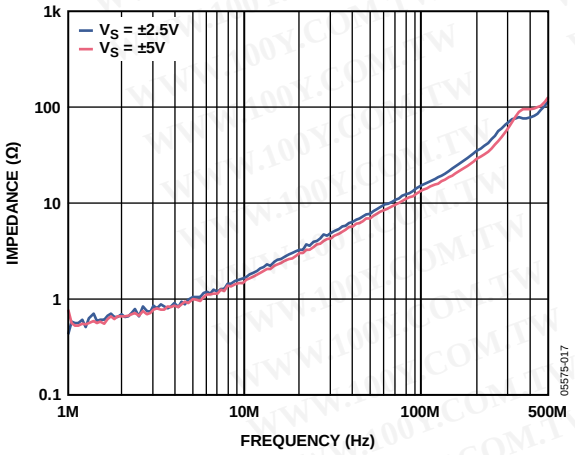


Figure 17. VGA Output Impedance vs. Frequency (See Figure 49)

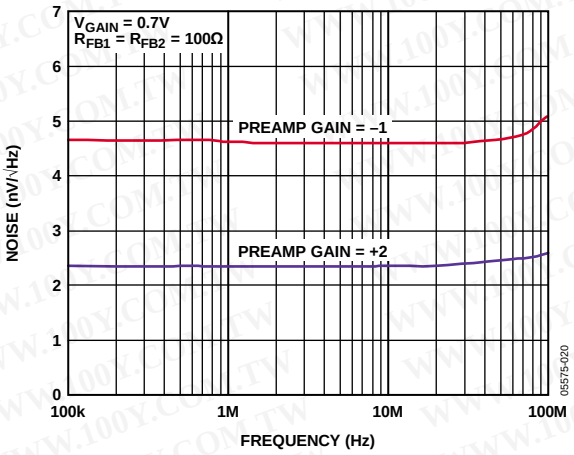


Figure 20. Short-Circuit, Input-Referred Noise vs. Frequency at Maximum Gain—Inverting and Noninverting Preamp Gain = –1 and +2 (See Figure 50)

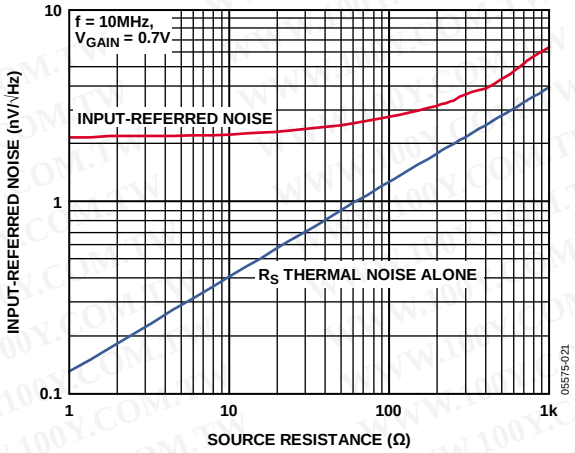


Figure 21. Input-Referred Noise vs. R_S
(See Figure 61)

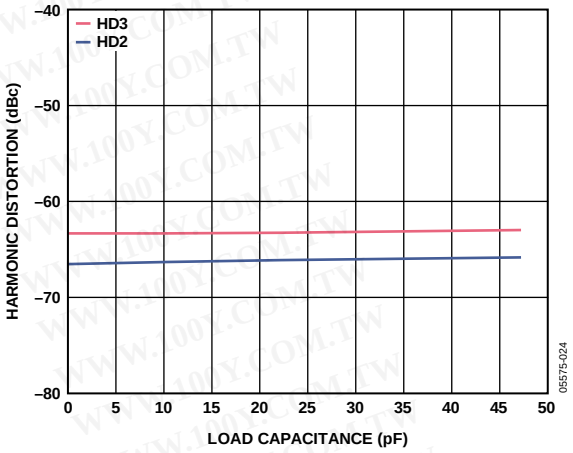


Figure 24. Harmonic Distortion vs. Load Capacitance
(See Figure 52)

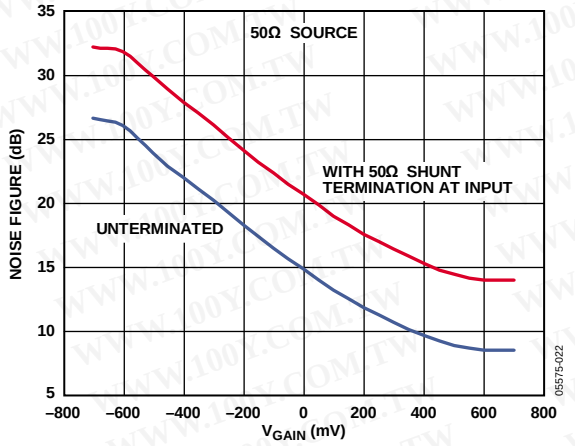


Figure 22. Noise Figure vs. V_{GAIN}
(See Figure 51)

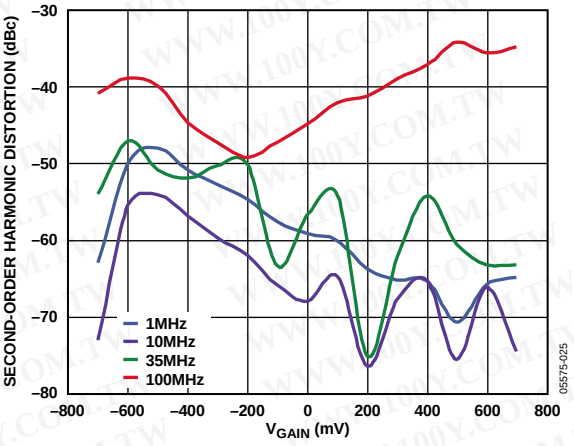


Figure 25. HD2 vs. V_{GAIN} at Four Frequencies
(See Figure 52)

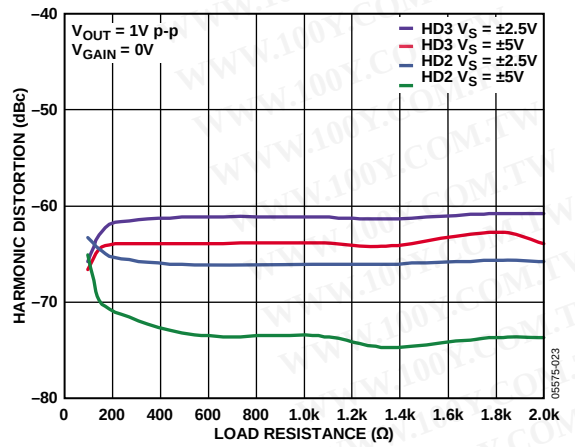


Figure 23. Harmonic Distortion vs. R_L and Supply Voltage
(See Figure 52)

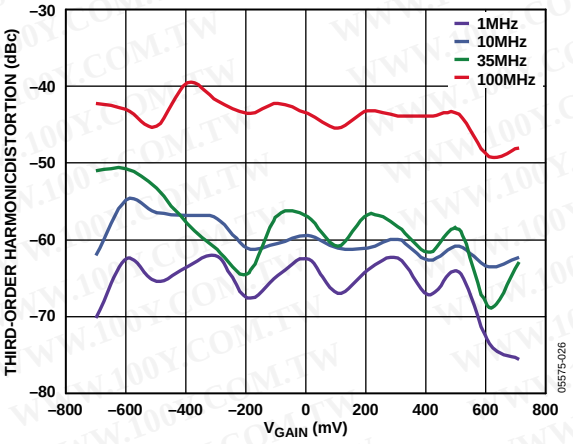


Figure 26. HD3 vs. V_{GAIN} at Four Frequencies
(See Figure 52)

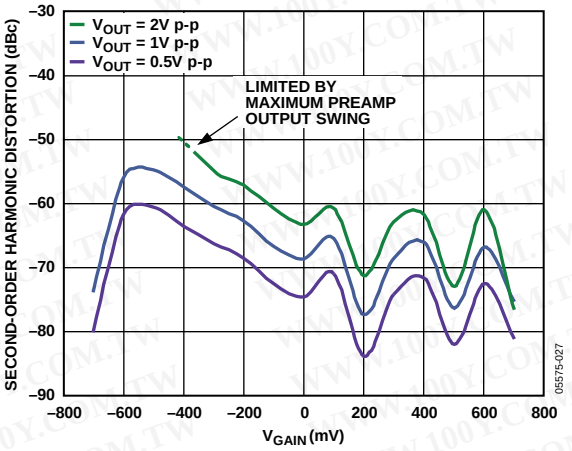


Figure 27. HD2 vs. V_{GAIN} for Three Levels of Output Voltage (See Figure 52)

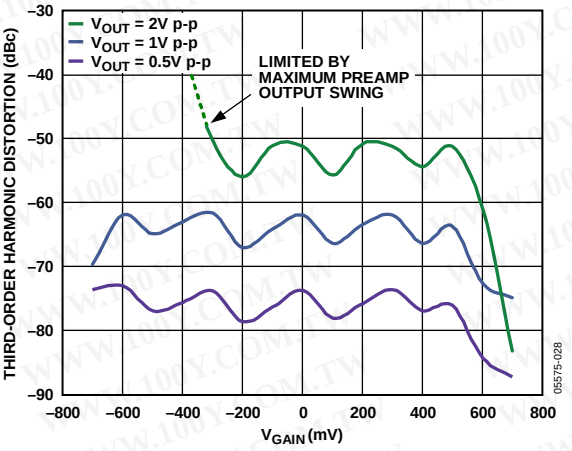


Figure 28. HD3 vs. V_{GAIN} for Three Levels of Output Voltage (See Figure 52)

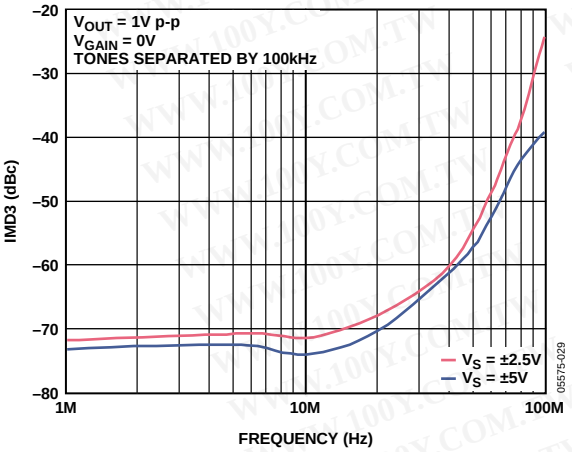


Figure 29. IMD3 vs. Frequency (See Figure 64)

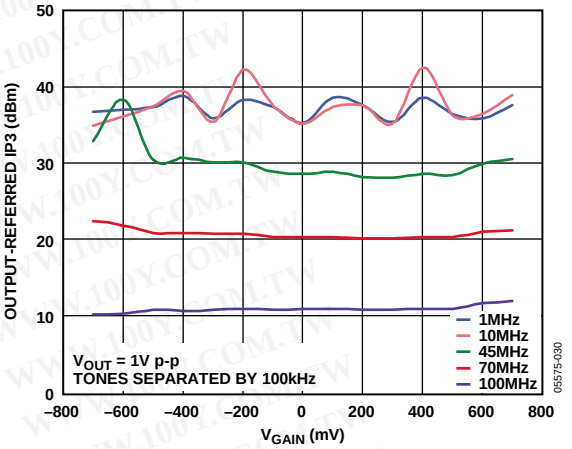


Figure 30. Output-Referred IP3 (OIP3) vs. V_{GAIN} at Five Frequencies (See Figure 64)

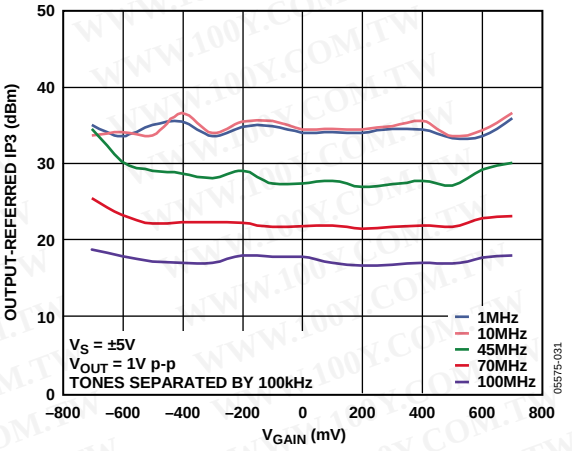


Figure 31. Output-Referred IP3 (OIP3) vs. V_{GAIN}, V_S = ±5 V at Five Frequencies (See Figure 64)

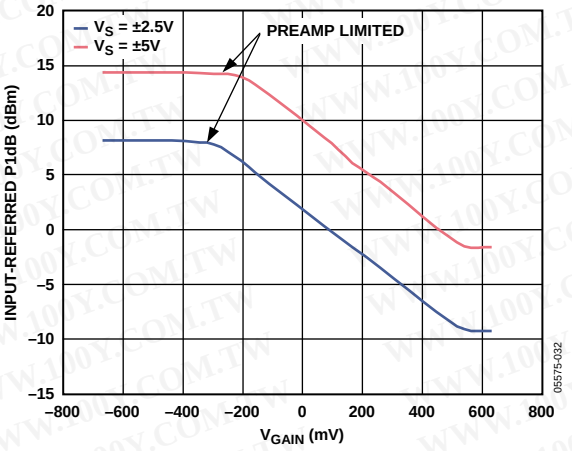


Figure 32. Input-Referred P1dB (IP1dB) vs. V_{GAIN} (See Figure 63)

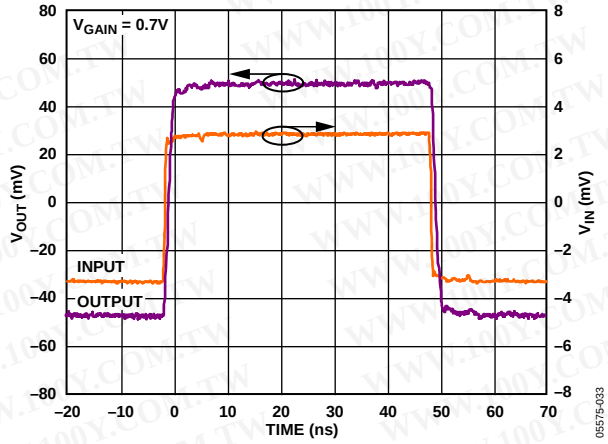


Figure 33. Small Signal Pulse Response
(See Figure 53)

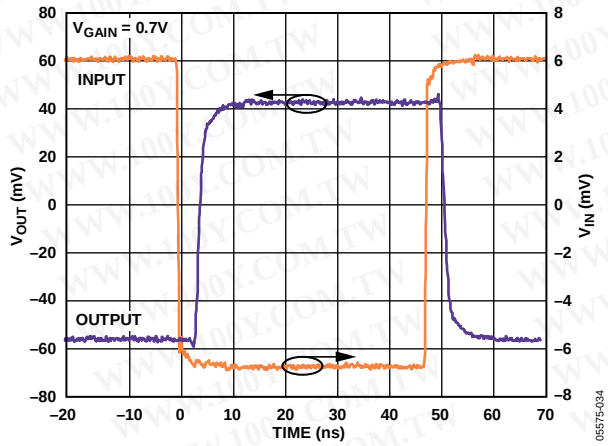


Figure 34. Small Signal Pulse Response—Inverting Feedback
(See Figure 59)

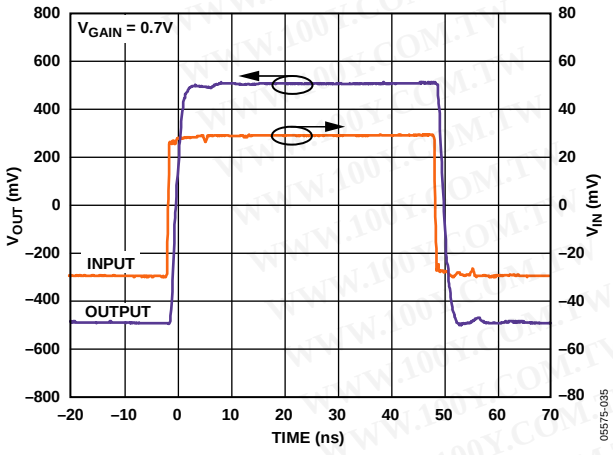


Figure 35. Large Signal Pulse Response
(See Figure 53)

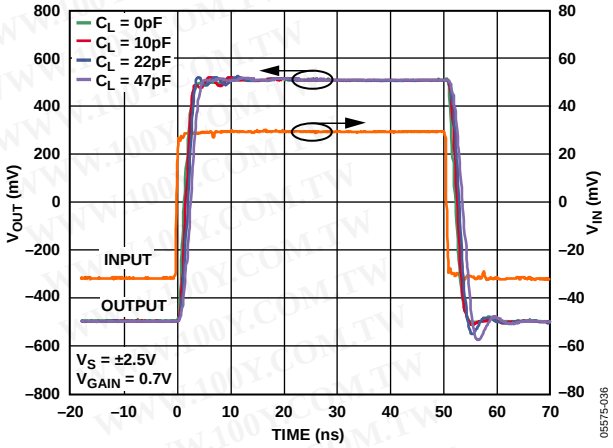


Figure 36. Large Signal Pulse Response for Three Capacitive Loads
(See Figure 53)

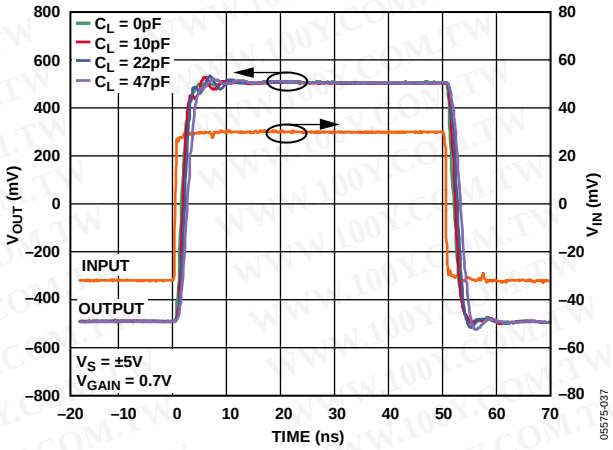


Figure 37. Large Signal Pulse Response for Three Capacitive Loads, V_S = ±5 V
(See Figure 53)

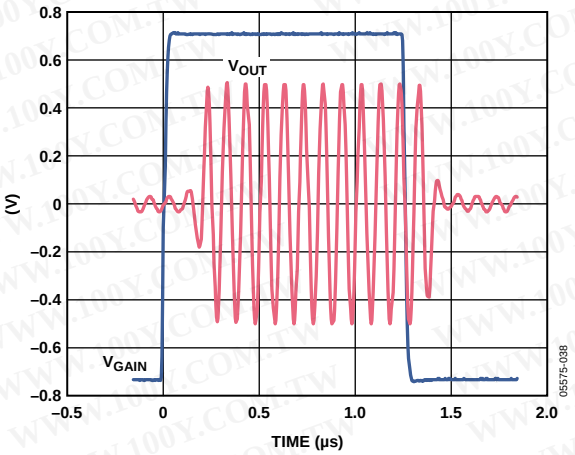


Figure 38. Gain Response
(See Figure 54)

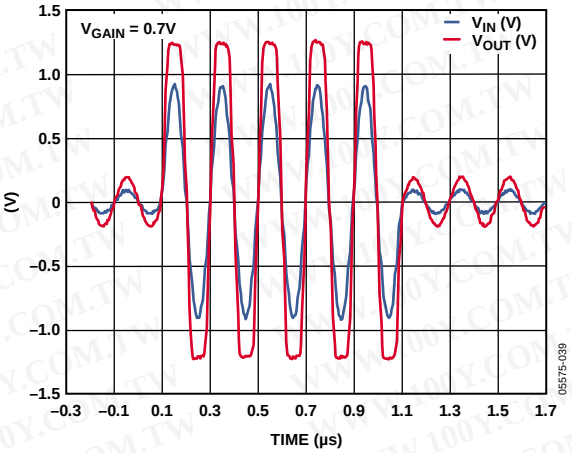


Figure 39. Preamp Overdrive Recovery
(See Figure 55)

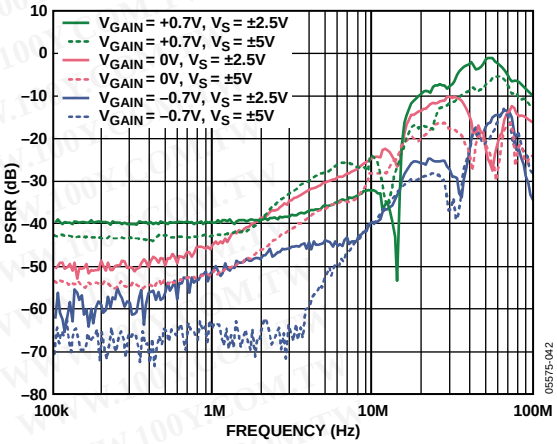


Figure 42. PSRR vs. Frequency of Negative Supply
(See Figure 60)

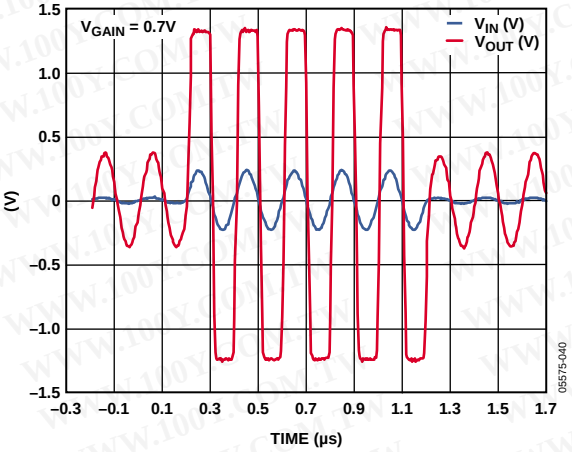


Figure 40. VGA Overdrive Recovery
(See Figure 56)

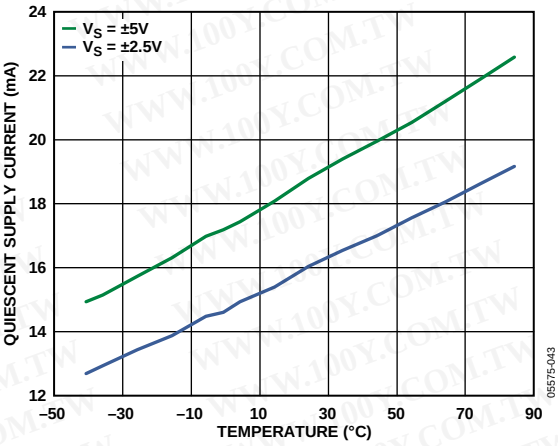


Figure 43. Quiescent Supply Current vs. Temperature
(See Figure 57)

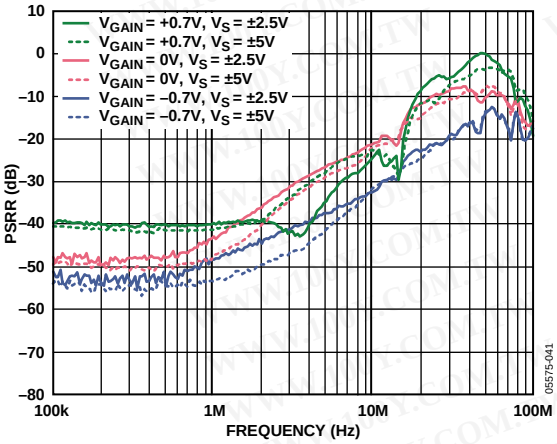


Figure 41. PSRR vs. Frequency of Positive Supply
(See Figure 60)

TEST CIRCUITS

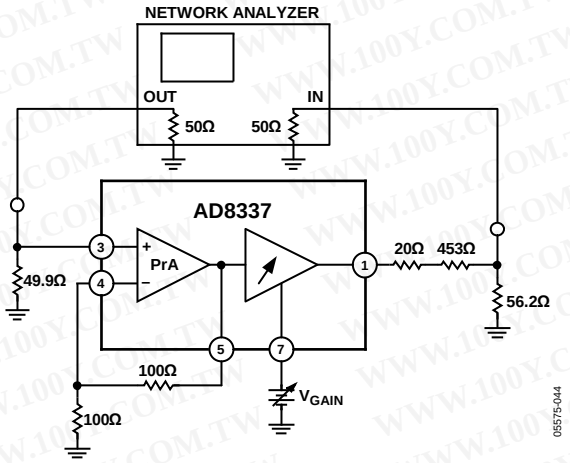


Figure 44. Gain and Gain Error vs. V_{GAIN}

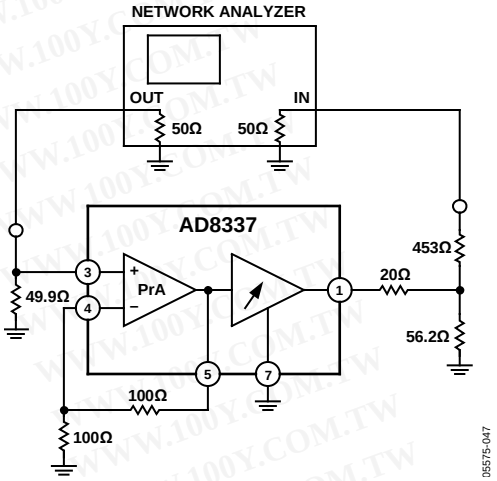


Figure 47. Group Delay

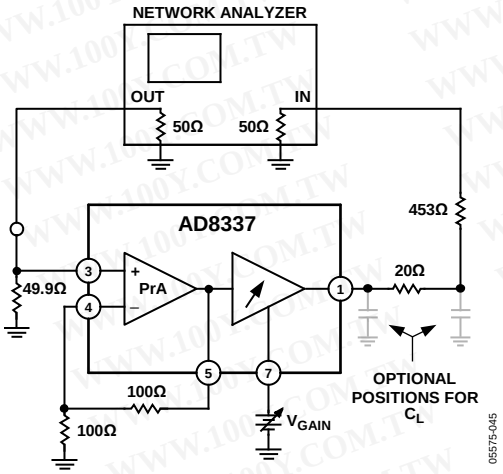


Figure 45. Frequency Response

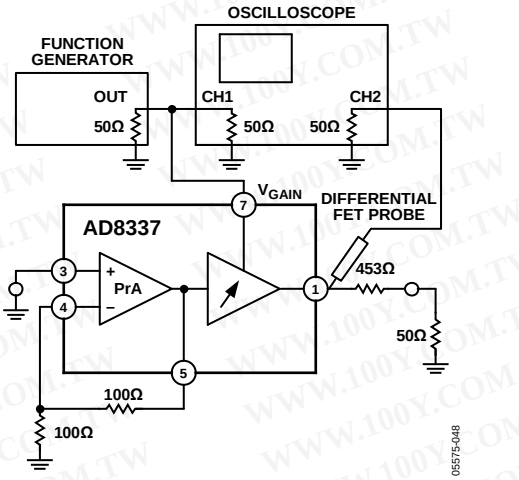


Figure 48. Offset Voltage

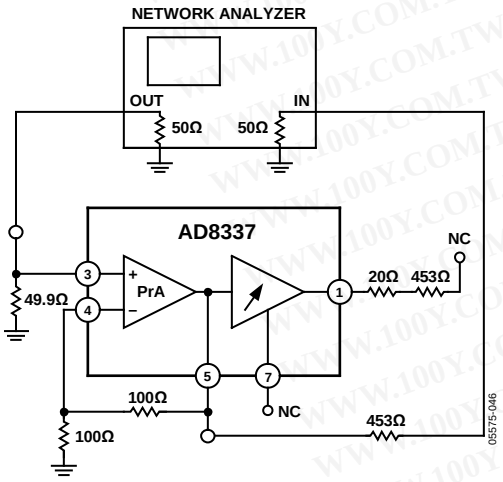


Figure 46. Frequency Response—Preamp

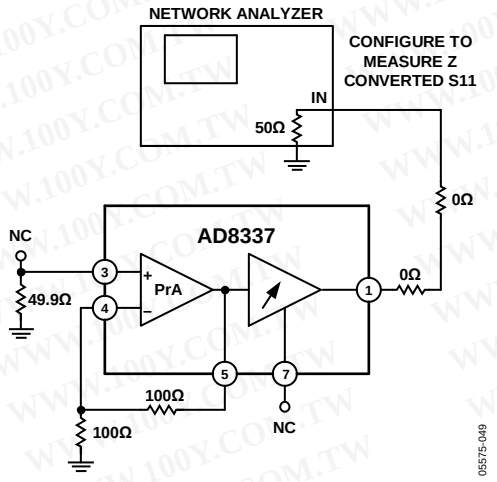


Figure 49. Output Impedance vs. Frequency

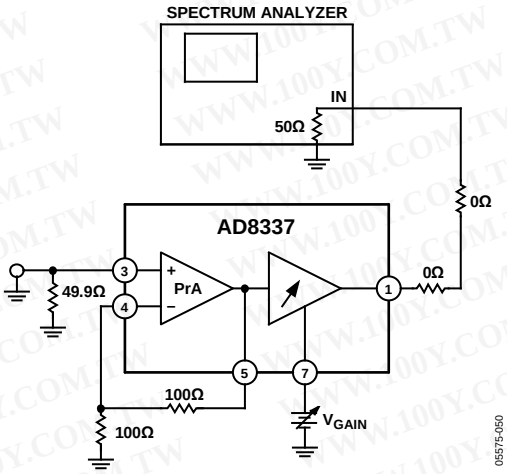


Figure 50. Input-Referred and Output-Referred Noise

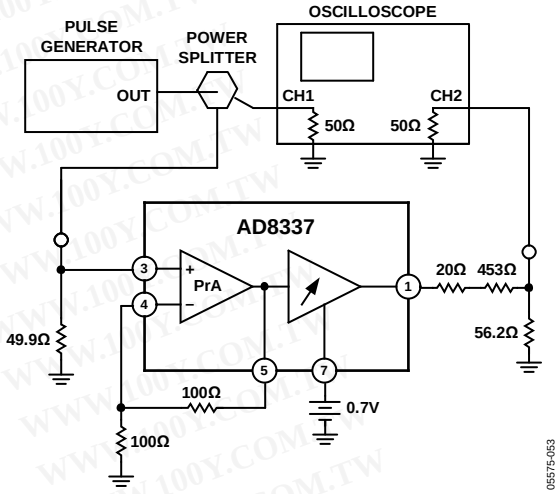


Figure 53. Pulse Response

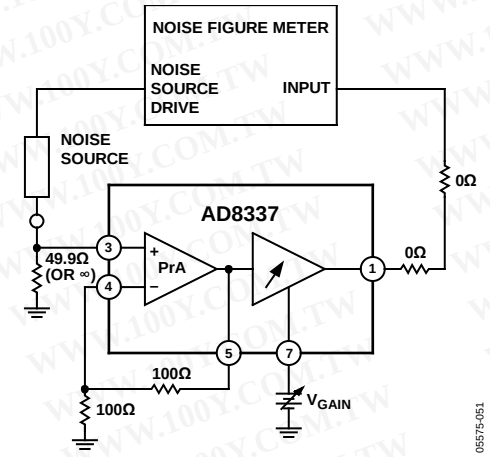


Figure 51. Noise Figure vs. V_{GAIN}

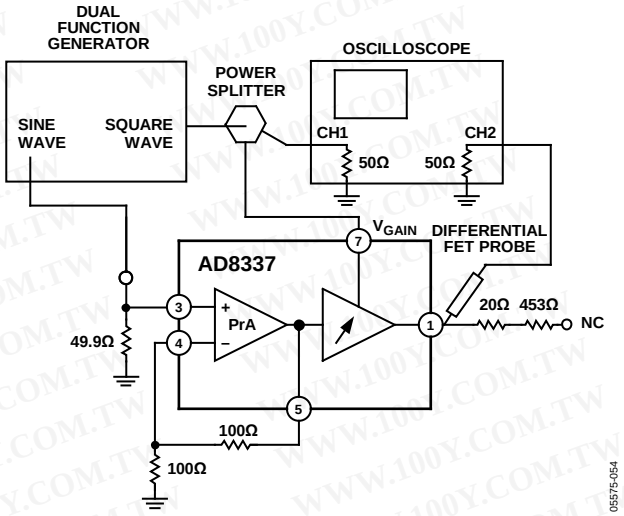


Figure 54. Gain Response

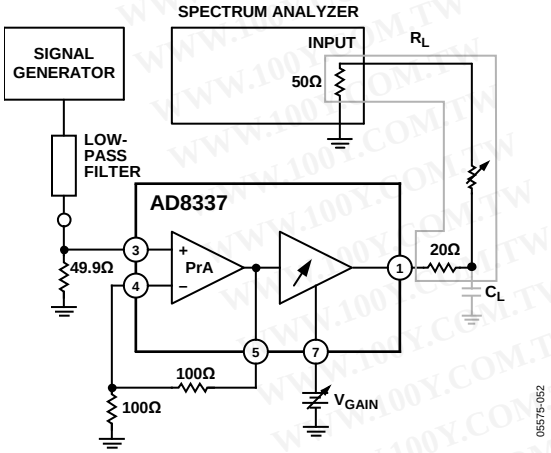


Figure 52. Harmonic Distortion

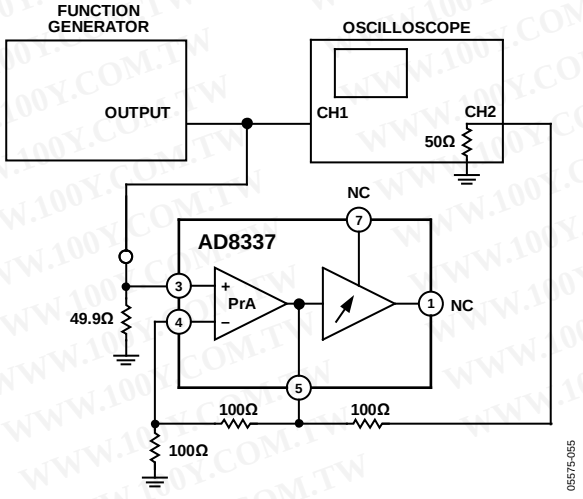


Figure 55. Preamp Overdrive Recovery

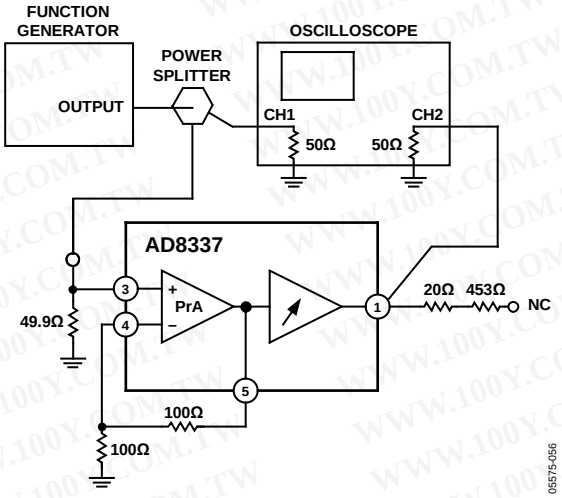


Figure 56. VGA Overdrive Recovery

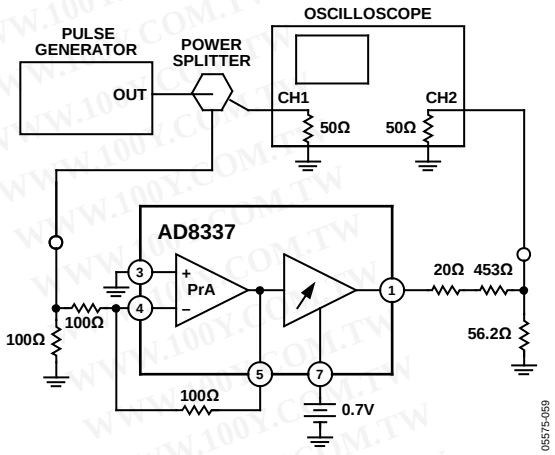


Figure 59. Pulse Response—Inverting Feedback

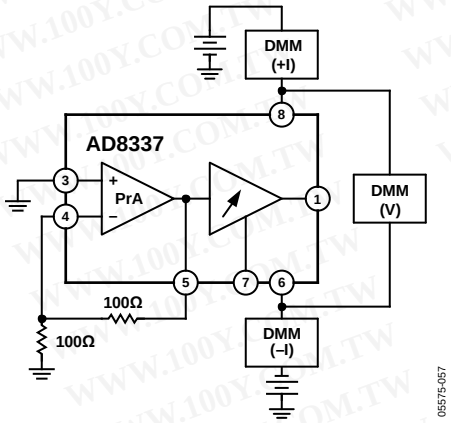


Figure 57. Supply Current

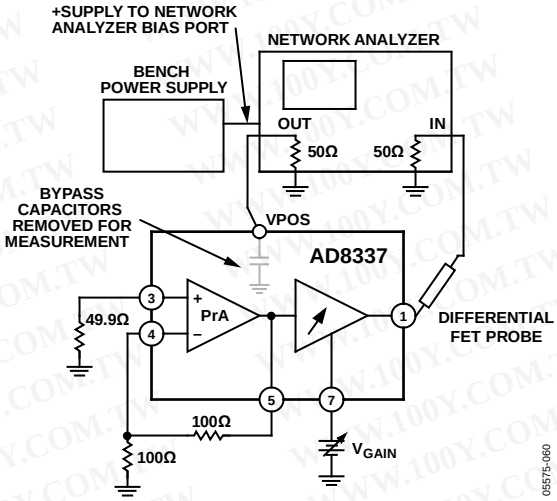


Figure 60. PSRR

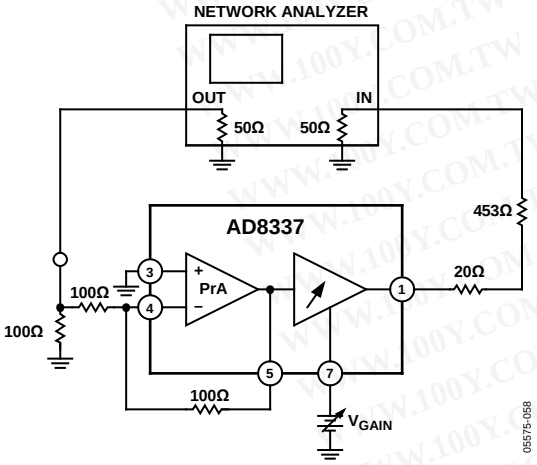


Figure 58. Frequency Response—Inverting Feedback

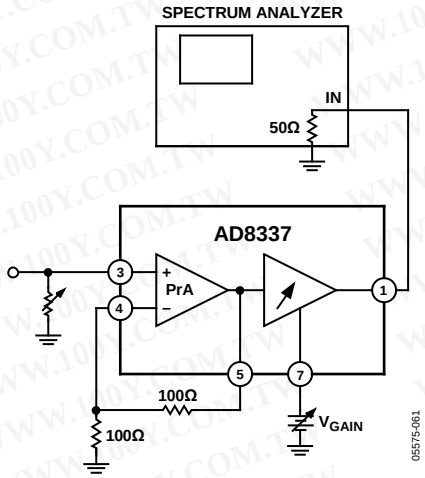


Figure 61. Input-Referred Noise vs. R_S

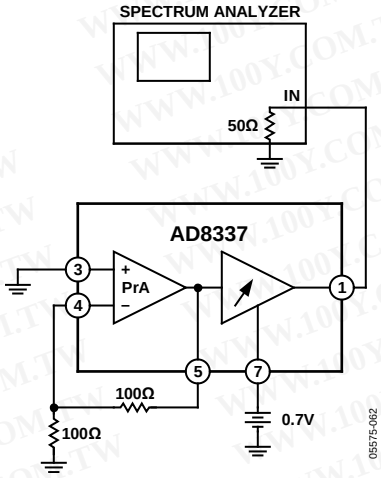


Figure 62. Short-Circuit Input Noise vs. Frequency

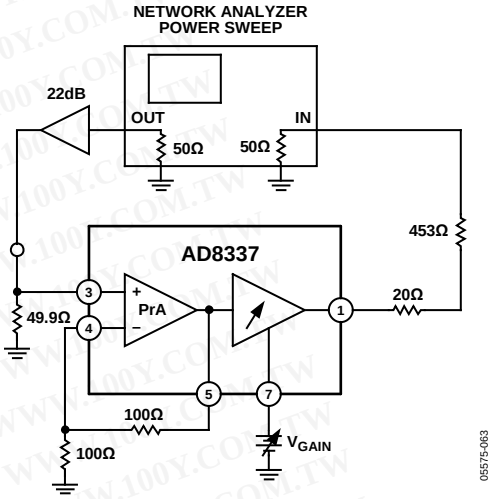


Figure 63. IP1dB vs. V_{GAIN}

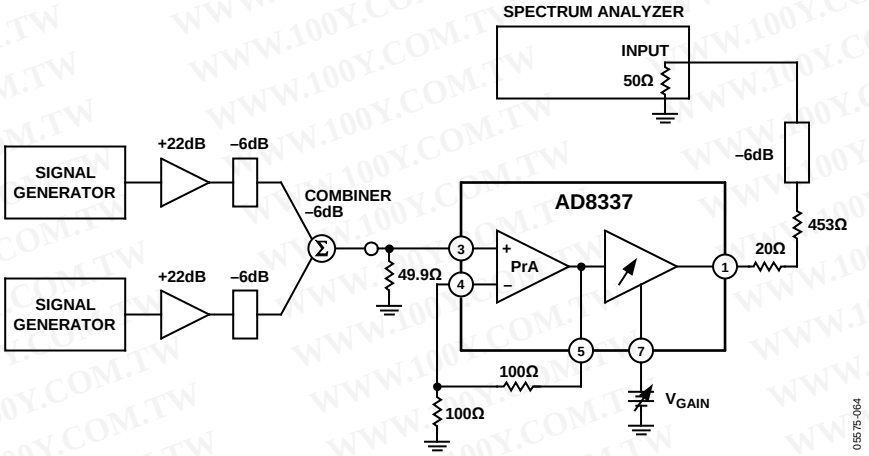


Figure 64. IMD and OIP3

THEORY OF OPERATION

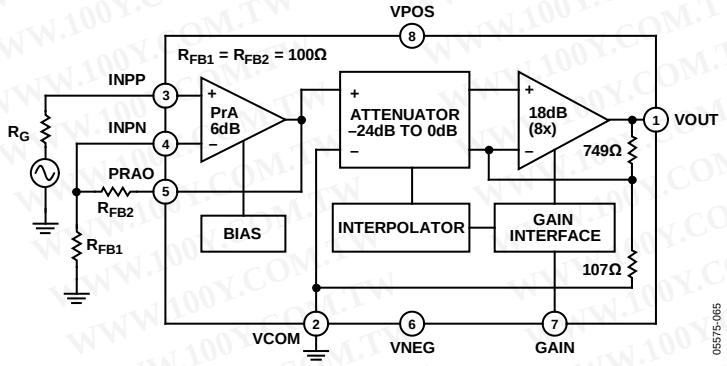


Figure 65. Circuit Block Diagram

OVERVIEW

The AD8337 is a low noise, single-ended, linear-in-dB, general-purpose variable gain amplifier (VGA) usable at frequencies up to 100 MHz. It is fabricated using a proprietary Analog Devices dielectrically isolated, complementary bipolar process. The bandwidth is dc to 280 MHz and features low dc offset voltage and an ideal nominal gain range of 0 dB to 24 dB. Requiring about 15.5 mA, the power consumption is only 78 mW from either a single +5 V or a dual ±2.5 V supply. Figure 65 is the circuit block diagram of the AD8337.

PREAMPLIFIER

An uncommitted current-feedback op amp included in the AD8337 can be used as a preamplifier to buffer the ladder network attenuator of the X-AMP. As with any op amp, the gain is established using external resistors, and the preamplifier is specified with a noninverting gain of 6 dB (2×) and gain resistor values of 100 Ω. The preamplifier gain can be increased using larger values of R_{FB2}, trading off bandwidth and offset voltage. The value of R_{FB2} is to be ≥100 Ω because the value and an internal compensation capacitor determine the 3 dB bandwidth, and smaller values can compromise preamplifier stability.

Because the AD8337 is dc-coupled, larger preamp gains increase the offset voltage. The offset voltage can be compensated by connecting a resistor between the INPN input and the supply voltage. If the offset is negative, the resistor value connects to the negative supply. For ease of adjustment, a trimmer network can be used.

For larger gains, the overall noise is reduced if a low value of R_{FB1} is selected. For values of R_{FB1} = 20 Ω and R_{FB2} = 301 Ω, the preamp gain is 16× (24.1 dB), and the input-referred noise is approximately 1.5 nV/√Hz. For this value of gain, the overall gain range increases by 18 dB; therefore, the gain range is 18 dB to 42 dB.

VGA

This X-AMP, with its linear-in-dB gain characteristic architecture, yields the optimum dynamic range for receiver applications. Referring to Figure 65, the signal path consists of a −24 dB variable attenuator followed by a fixed gain amplifier of 18 dB, for a total VGA gain range of −6 dB to +18 dB. With the preamplifier configured for a gain of 6 dB, the composite gain range is 0 dB to 24 dB.

The VGA plus preamp, with 6 dB of gain, implements the following exact gain law:

$$Gain(\text{dB}) = \left[19.7 \frac{\text{dB}}{\text{V}} \times V_{GAIN} \right] + ICPT(\text{dB})$$

where the nominal intercept (*ICPT*) = 12.65 dB.

The ICPT increases as the gain of the preamp is increased. For example, if the gain of the preamp is increased by 6 dB, ICPT increases to 18.65 dB. Although the previous equation shows the exact gain law as based on statistical data, a quick estimation of signal levels can be made using the default slope of 20 dB/V for a particular gain setting. For example, the change in gain for a V_{GAIN} change of 0.3 V is 6 dB using a slope of 20 dB/V and 5.91 dB using the exact slope of 19.6 dB/V. This is a difference of only 0.09 dB.

GAIN CONTROL

The gain control interface provides a high impedance input and is referenced to the VCOM pin (in a single-supply application to midsupply at [VPOS + VNEG]/2 for optimum swing). When dual supplies are used, VCOM is connected to ground. The voltage on the VCOM pin determines the midpoint of the gain range. For a ground referenced design, the VGAIN range is from −0.7 V to +0.7 V with the most linear-in-dB section of the gain control between −0.6 V and +0.6 V. In the center 80% of the VGAIN range, the gain error is typically less than ±0.2 dB. The gain control voltage can be increased or decreased to the positive or negative rails without gain foldover.

The gain scaling factor (gain slope) is designed for 20 dB/V. This relatively low slope ensures that noise on the GAIN input is not unduly amplified. Because a VGA functions as a multiplier, it is important that the GAIN input does not inadvertently modulate the output signal with unwanted noise. Because of its high input impedance, a simple low-pass filter can be added to the GAIN input to filter unwanted noise.

OUTPUT STAGE

The output stage is a Class AB, voltage-feedback, complementary emitter-follower with a fixed gain of 18 dB, similar to the preamplifier in speed and bandwidth. Because of the ac-beta roll-off of the output devices and the inherent reduction in feedback beyond the −3 dB bandwidth, the impedance looking into the output pin of the preamp and output stages appears to be inductive (increasing impedance with increasing frequency). The high speed output amplifier used in the AD8337 can drive large currents, but its stability is susceptible to capacitive loading. A small series resistor mitigates the effects of capacitive loading (see the Applications Information section).

ATTENUATOR

The input resistance of the VGA attenuator is nominally 265 Ω. For example, if the default preamplifier feedback network R_{FB1} + R_{FB2} is 200 Ω, the effective preamplifier load is approximately 114 Ω. The attenuator is composed of eight 3.01 dB sections for a total attenuation range of −24.08 dB. Following the attenuator is a fixed gain amplifier with 8× (18.06 dB) gain. Because of this relatively low gain, the output offset is kept well below 20 mV over temperature; the offset is largest at maximum gain when the preamplifier offset is amplified. The VCOM pin defines the common-mode reference for the output, as shown in Figure 65.

SINGLE-SUPPLY OPERATION AND AC COUPLING

If the AD8337 is to be operated from a single 5 V supply, the bias supply for VCOM must be a very low impedance 2.5 V reference, especially if dc coupling is used. If the device is dc-coupled, the VCOM source must be able to handle the preamplifier and VGA dynamic load currents in addition to the bias currents.

When ac coupling the preamplifier input, a bias network and bypass capacitor must be connected to the opposite polarity input pin. The bias generator for the VCOM pin must provide the dynamic current to the preamplifier feedback network and the VGA attenuator. For many single 5 V applications, a reference, such as the ADR391, and a good op amp provide an adequate VCOM source if a 2.5 V supply is unavailable.

NOISE

The total input-referred voltage and current noise of the positive input of the preamplifier are about 2.2 nV/√Hz and 4.8 pA/√Hz. The VGA output-referred noise is about 21 nV/√Hz at low gains. This result is divided by the VGA fixed gain amplifier gain of 8× and results in a voltage noise density of 2.6 nV/√Hz referred to the VGA input. This value includes the noise of the VGA gain setting resistors as well. If this voltage is again divided by the preamp gain of 2, the VGA noise referred all the way to the preamp input is about 1.3 nV/√Hz. From this, it is determined that the preamplifier, including the 100 Ω gain setting resistors, contributes about 1.8 nV/√Hz. The two 100 Ω resistors contribute 1.29 nV/√Hz each at the output of the preamp. With the gain resistor noise subtracted, the preamplifier noise is approximately 1.55 nV/√Hz.

Equation 2 shows the calculation that determines the output-referred noise at maximum gain (24 dB or 16×).

where:

A_t is the total gain from preamp input to VGA output.

R_S is the source resistance.

e_{n-PrA} is the input-referred voltage noise of the preamp.

i_{n-PrA} is the current noise of the preamp at the INPP pin.

$e_{n-R_{FB1}}$ is the voltage noise of R_{FB1}.

$e_{n-R_{FB2}}$ is the voltage noise of R_{FB2}.

e_{n-VGA} is the input-referred voltage noise of the VGA (low gain, output-referred noise divided by a fixed gain of 8×).

Assuming R_S = 0 Ω, R_{FB1} = R_{FB2} = 100 Ω, A_t = 16×, and A_{VGA} = 8×, the noise simplifies to

$$e_{n-out} = \sqrt{(1.75\times16)^2 + 2(1.29\times8)^2 + (1.9\times8)^2} = 35\ \text{nV}\sqrt{\text{Hz}} \quad (1)$$

Dividing the result by 16 gives the total input-referred noise with a short-circuited input as 2.2 nV/√Hz. When the preamplifier is used in the inverting configuration with the same R_{FB1} and R_{FB2} = 100 Ω as previously noted, e_{n-out} does not change. However, because the gain dropped by 6 dB, the input-referred noise increases by a factor of 2 to about 4.4 nV/√Hz. The reason for this increase is that the noise gain to the output of the noise generators stays the same, yet the preamp in the inverting configuration has a gain of −1 compared to the +2 in the noninverting configuration; this increases the input-referred noise by 2.

$$e_{n-out} = \sqrt{(e_n R_S \times A_t)^2 + (e_{n-PrA} \times A_t)^2 + (i_{n-PrA} \times R_S)^2 + (e_{n-R_{FB1}} \times \frac{R_{FB2}}{R_{FB1}} \times A_{VGA})^2 + (e_{n-R_{FB2}} \times A_{VGA})^2 + (e_{n-VGA} \times A_{VGA})^2} \quad (2)$$

APPLICATIONS INFORMATION

PREAMPLIFIER CONNECTIONS

Noninverting Gain Configuration

The AD8337 preamplifier is an uncommitted current-feedback op amp that is stable for values of $R_{FB2} \geq 100\ \Omega$. See Figure 66 for the noninverting feedback connections.

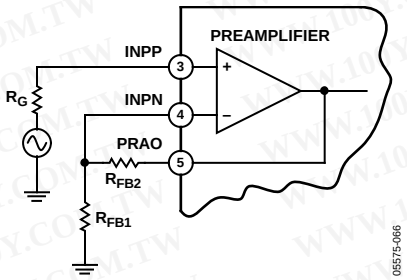


Figure 66. AD8337 Preamplifier Configured for Noninverting Gain

Two surface-mount resistors establish the preamplifier gain. Equal values of 100 Ω configure the preamplifier for a 6 dB gain and the device for a default gain range of 0 dB to 24 dB.

For preamplifier gains ≥2, select a value of $R_{FB2} \geq 100\ \Omega$ and $R_{FB1} \leq 100\ \Omega$. Higher values of R_{FB2} reduce the bandwidth and increase the offset voltage, but smaller values compromise stability. If $R_{FB1} \leq 100\ \Omega$, the gain increases and the input-referred noise decreases.

Inverting Gain Configuration

For applications requiring polarity inversion of negative pulses, or for waveforms that require current sinking, the preamplifier can be configured as an inverting gain amplifier. When configured with bipolar supplies, the preamplifier amplifies positive or negative input voltages with no level shifting of the common-mode input voltage required. Figure 67 shows the AD8337 configured for inverting gain operation.

Because the AD8337 is a very high frequency device, stability issues can occur unless the circuit board on which it is used is carefully laid out. The stability of the preamp is affected by parasitic capacitance around the INPN pin. To minimize stray capacitance position the preamp gain resistors, R_{FB1} and R_{FB2}, as close as possible to the INPN pin.

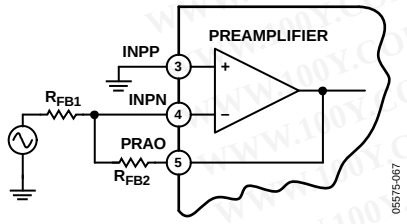


Figure 67. The AD8337 Preamplifier Configured for Inverting Gain

DRIVING CAPACITIVE LOADS

Because of the large bandwidth of the AD8337, stray capacitance at the output pin can induce peaking in the frequency response as the gain of the amplifier begins to roll off. Figure 68 shows peaking with two values of load capacitance using ±2.5 V supplies and $V_{GAIN} = 0$ V.

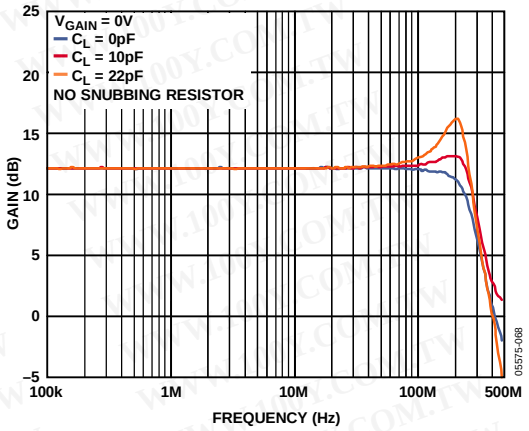


Figure 68. Peaking in the Frequency Response for Two Values of Output Capacitance with ±2.5 V Supplies and No Snubbing Resistor

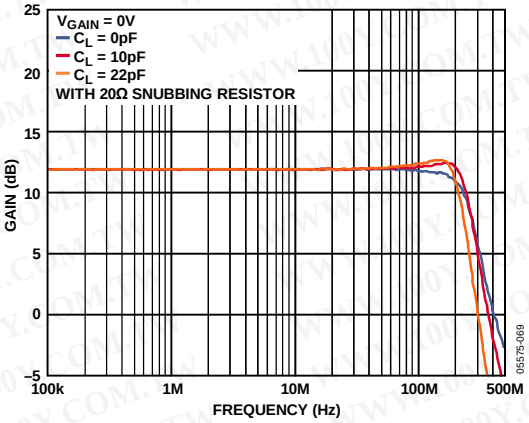


Figure 69. Frequency Response for Two Values of Output Capacitance with a 20 Ω Snubbing Resistor

In the time domain, stray capacitance at the output pin can induce overshoot on the edges of transient signals, as shown in Figure 70 and Figure 72. The amplitude of the overshoot is also a function of the slewing of the transient (not shown in Figure 70 and Figure 72). The transition time of the input pulses used for Figure 70 and Figure 72 is deliberately set high at 300 ps to demonstrate the fast response time of the amplifier. Signals with longer transition times generate less overshoot.

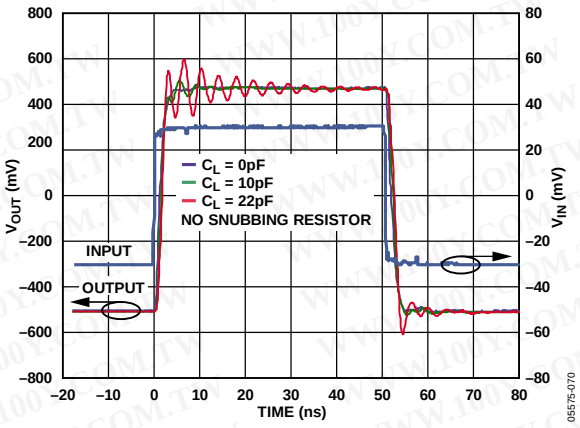


Figure 70. Pulse Response for Two Values of Output Capacitance with ±2.5 V Supplies and No Snubbing Resistor

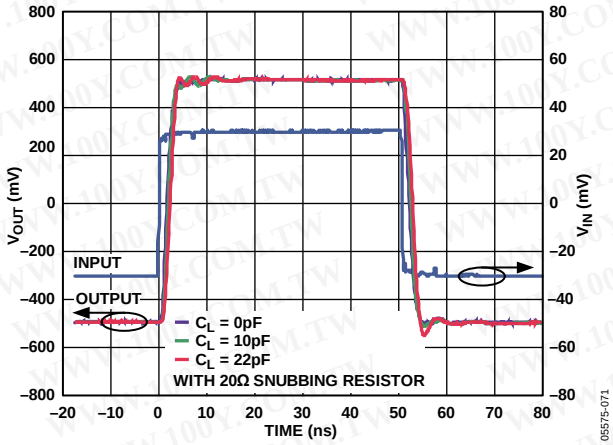


Figure 71. Pulse Response for Two Values of Output Capacitance with ±2.5 V Supplies and a 20 Ω Snubbing Resistor

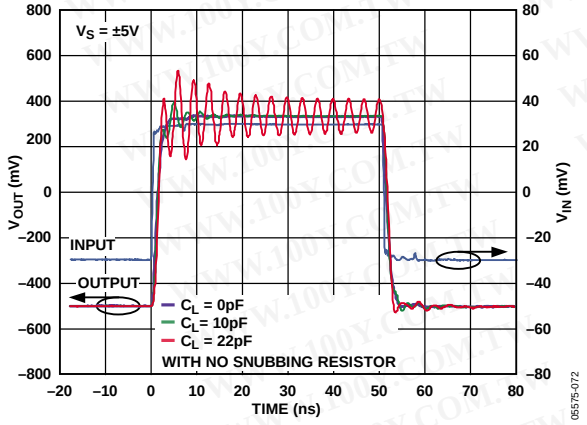


Figure 72. Large Signal Pulse Response for Two Values of Output Capacitance with ±5 V Supplies and No Snubbing Resistor

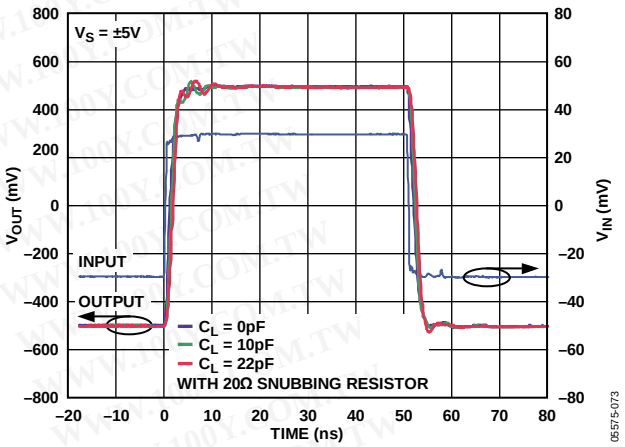


Figure 73. Pulse Response for Two Values of Output Capacitance with ±5 V Supplies and a 20 Ω Snubbing Resistor

The effects of stray output capacitance are mitigated with a small value snubbing resistor, R_{SNUB}, placed in series with, and as near as possible to, the VOUT pin. Figure 69, Figure 71, and Figure 73 show the improvement in dynamic performance with a 20 Ω snubbing resistor. R_{SNUB} reduces the gain slightly by the ratio of $R_L/(R_{SNUB} + R_L)$, a very small loss when used with high impedance loads, such as ADCs. For other loads, alternate values of R_{SNUB} can be determined empirically. The data for the curves in the Typical Performance Characteristics section are derived using a 20 Ω snubbing resistor.

The best way to avoid the effects of stray capacitance is to exercise care in the PCB layout. Locate the passive components or devices connected to the AD8337 output pins as close as possible to the package.

Although a nonissue, the preamplifier output is also sensitive to load capacitance. However, the series connection of R_{FB1} and R_{FB2} is typically the only load connected to the preamplifier. If overshoot appears, it can be mitigated by inserting a snubbing resistor, the same way as the VGA output.

GAIN CONTROL CONSIDERATIONS

In typical applications, voltages applied to the GAIN input are dc or relatively low frequency signals. The high input impedance of the AD8337 enables several devices to be connected in parallel. This is useful for arrays of VGAs, such as those used for calibration adjustments.

Under dc or slowly changing ramp conditions, the gain tracks the gain control voltage, as shown in Figure 3. However, it is often necessary to consider other effects influenced by the V_{GAIN} input.

The offset voltage effect of the AD8337, as with all VGAs, can appear as a complex waveform when observed across the range of V_{GAIN} voltage. Generated by multiple sources, each device has a unique offset voltage (V_{OS}) profile while the GAIN input is swept through its voltage range. The offset voltage profile seen in Figure 15 is a typical example. If the V_{GAIN} input voltage is modulated, the output is the product of the V_{GAIN} and the dc profile of the offset voltage. This is observed on a scope as a small ac signal, as shown in Figure 74. In Figure 74, the signal applied to the V_{GAIN} input is a 1 kHz ramp, and the output voltage signal is slightly less than 4 mV p-p.

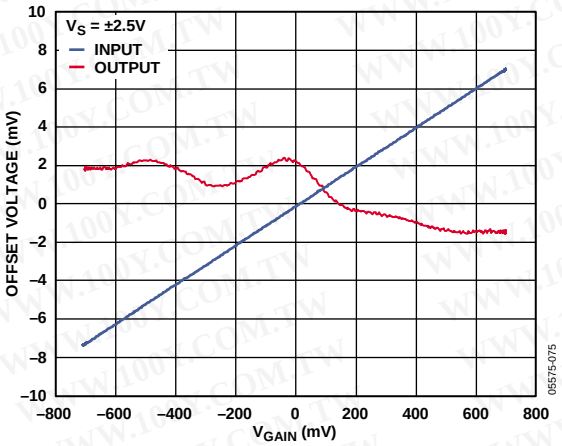


Figure 74. Offset Voltage vs. V_{GAIN} for a 1 kHz Ramp

The profile of the waveform shown in Figure 74 is consistent over a wide range of signals from dc to about 20 kHz. Above 20 kHz, secondary artifacts can be generated due to the effects of minor internal circuit tolerances, as shown in Figure 75. These artifacts are caused by settling and time constants of the interpolator circuit and appear at the output as the voltage spikes, as shown in Figure 75.

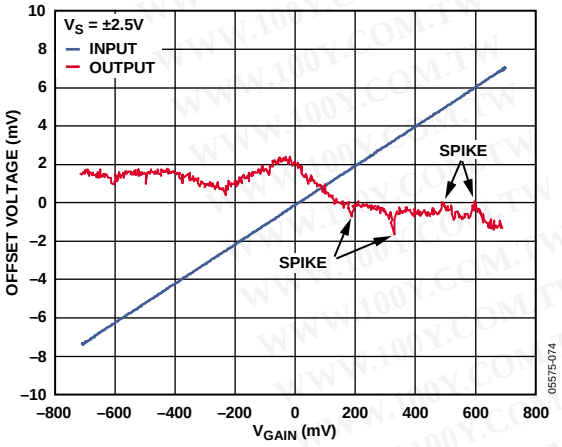


Figure 75. V_{OS} Profile for a 50 kHz Ramp

Under certain circumstances, the product of V_{GAIN} and the offset profile plus spikes is a coherent spurious signal within the signal band of interest and indistinguishable from desired signals. In general, the slower the ramp applied to the GAIN Pin, the smaller the spikes are. In most applications, these effects are benign and not an issue.

THERMAL CONSIDERATIONS

The thermal performance of LFCSPs, such as the AD8337, departs significantly from that of leaded devices such as the larger TSSOP or QFSP. In larger packages, heat is conducted away from the die by the path provided by the bond wires and the device leads. In LFCSPs, the heat transfer mechanisms are surface-to-air radiation from the top and side surfaces of the package and conduction through the metal solder pad on the mounting surface of the device.

θ_{JC} is the traditional thermal metric used for integrated circuits. Heat transfer away from the die is a three-dimensional dynamic, and the path is through the bond wires, leads, and the six surfaces of the package. Because of the small size of LFCSPs, the θ_{JC} is not measured conventionally. Instead, it is calculated using thermodynamic rules.

The θ_{JC} value of the AD8837 listed in Table 2 assumes that the tab is soldered to the board and that there are three additional ground layers beneath the device connected by at least four vias. For a device with an unsoldered pad, the θ_{JC} nearly doubles, becoming 138°C/W.

PSI (Ψ)

Table 2 lists a subset of the classic theta specification, Ψ_{JT} (Psi junction to top). θ_{JC} is the metric of heat transfer from the die to the case, involving the six outside surfaces of the package. $\Psi_{(XY)}$ is a subset of the theta value and the thermal gradient from the junction (die) to each of the six surfaces. Ψ can be different for each of the surfaces, but since the top of the package is a fraction of a millimeter from the die, the surface temperature of the package is very close to the die temperature. The die temperature is calculated as the product of the power dissipation and Ψ_{JT}. Since the top surface temperature and power dissipation are easily measured, it follows that the die temperature is easily calculated. For example, for a dissipation of 180 mW and a Ψ_{JT} of 5.3°C/W, the die temperature is slightly less than 1°C higher than the surface temperature.

BOARD LAYOUT

Because the AD8337 is a high frequency device, board layout is critical. It is very important to have a good ground plane connection to the VCOM pin. Coupling through the ground plane, from the output to the input, can cause peaking at higher frequencies.

EVALUATION BOARDS

The AD8337evaluation boards provide a family of platforms for testing and evaluating the AD8337 VGA. Three circuit configurations are available:

- AD8337-EVALZ, dc-coupled, with noninverting gain and dual power supplies
- AD8337-EVALZ-INV, dc-coupled, with inverting gain and dual power supplies
- AD8337-EVALZ-SS, ac-coupled, with noninverting gain configuration and a single supply

These fully assembled and tested boards are ready to use. Only the appropriate power supply and signal source connections need to be made. SMA connectors are provided for the preamplifier (PrA) and VGA outputs. Photos of fully assembled boards are shown in Figure 76 and Figure 77. The board component side layouts are shown in Figure 78 and Figure 79.

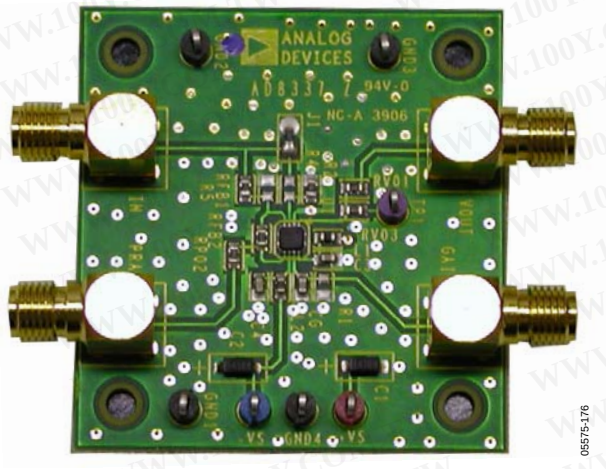


Figure 76. AD8337 Evaluation Board for dual Supplies

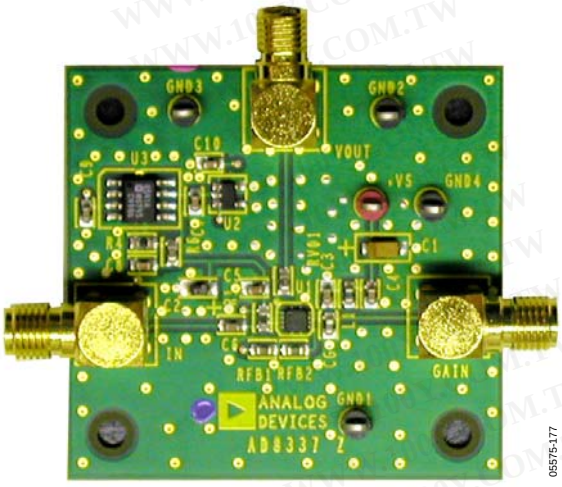


Figure 77. AD8337 Evaluation Board for Single Supply

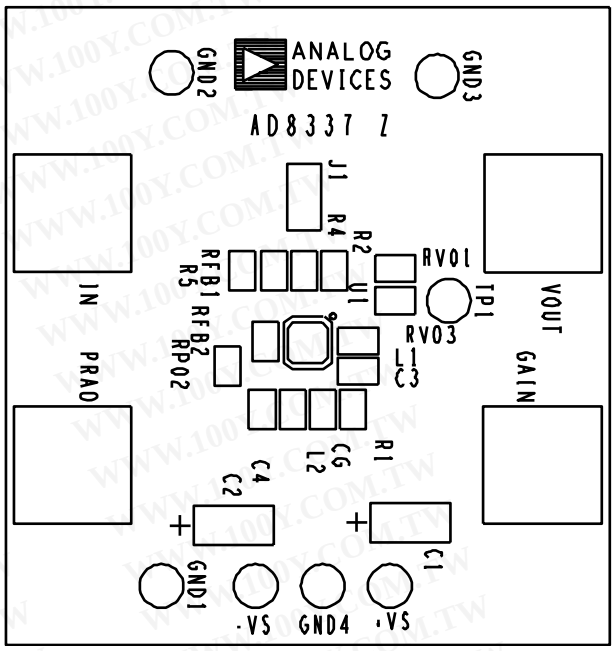


Figure 78. Assembly, Dual-Supply Evaluation Board

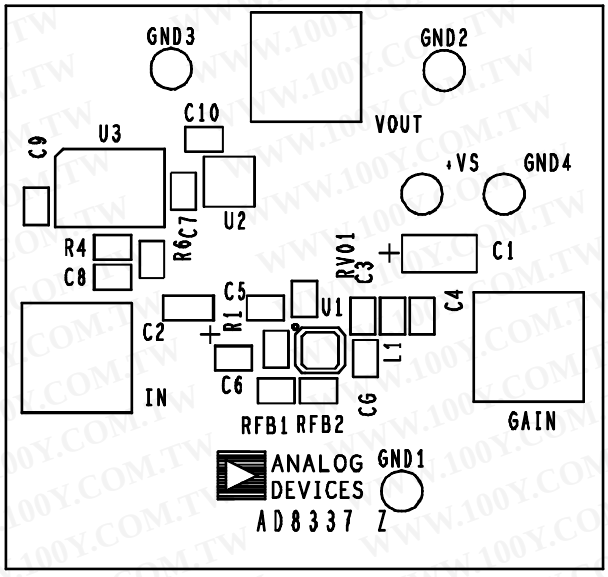


Figure 79. Assembly, Single-Supply Evaluation Board

Schematic diagrams of the dual-supply board for noninverting and inverting configurations are shown in Figure 80 and Figure 81. The dual-supply boards require ±2.5 V to ±5 V supplies capable of supplying 20 mA or greater. A schematic diagram of the single-supply board is shown in Figure 82. The single supply version accepts a +5 V to +10 V supply with 20 mA or greater capability.

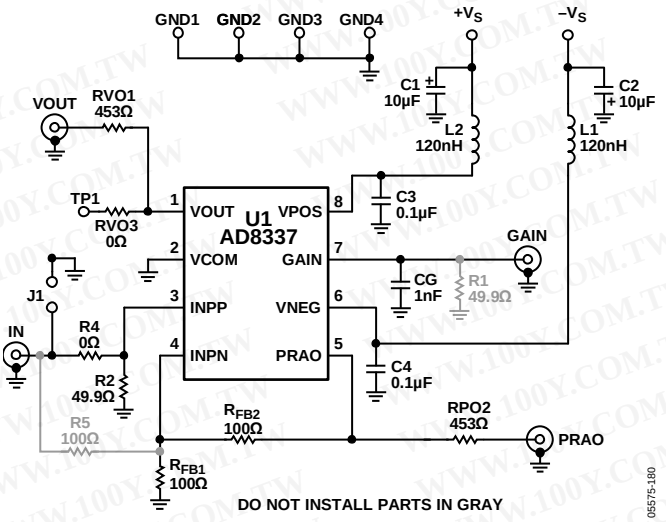


Figure 80. Schematic—AD8337-EVALZ - Noninverting Configuration

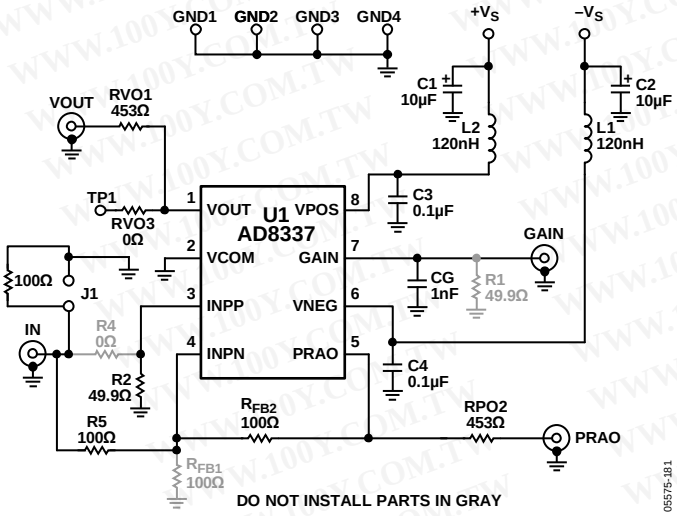


Figure 81. Schematic—AD8337-EVALZ-INV Inverting Configuration

CIRCUIT OPTIONS

Part numbers for fully assembled boards are listed in Table 4.

Table 4. AD8337 Evaluation Board Variations

Part Number	Configuration
AD8337-EVALZ	Dual-supply noninverting
AD8337-EVALZ-INV	Dual-supply inverting
AD8337-EVALZ-SS	Single-supply noninverting

Figure 80, Figure 81, and Figure 82 are schematics for the various circuit configurations. Within limits, the AD8337 preamplifier gain is controlled by Resistor R_{FB1} and Resistor R_{FB2}. For simple guidelines applying to the current-feedback preamplifier, see the Theory of Operation section.

OUTPUT PROTECTION

The AD8337 VGA output stage is specified for driving loads of 500 Ω or greater. To protect the stage from an accidental overload, a 453 Ω resistor is provided, which when connected to 50 Ω test equipment inputs, enables safe operation. In certain high load impedance situations, the value of this resistor can be reduced. However, if load capacitance values greater than approximately 20 pF are anticipated, such as a BNC cable, the minimum series resistor value is not to be less than 20 Ω.

An alternate test pin is also provided for direct access to the output of the AD8337 VGA. The pin is typically used for a probe, and a 0 Ω resistor is provided between the test loop and the output pin. If the test loop is connected to loads ≤500 Ω, then the 0 Ω resistor is to be changed to an appropriate value.

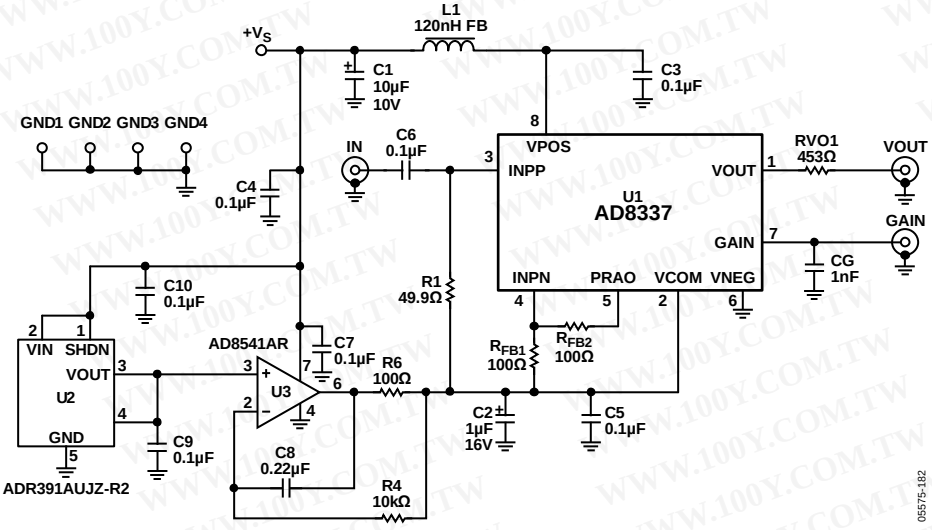


Figure 82. Evaluation Board Schematic—Single-Supply Version

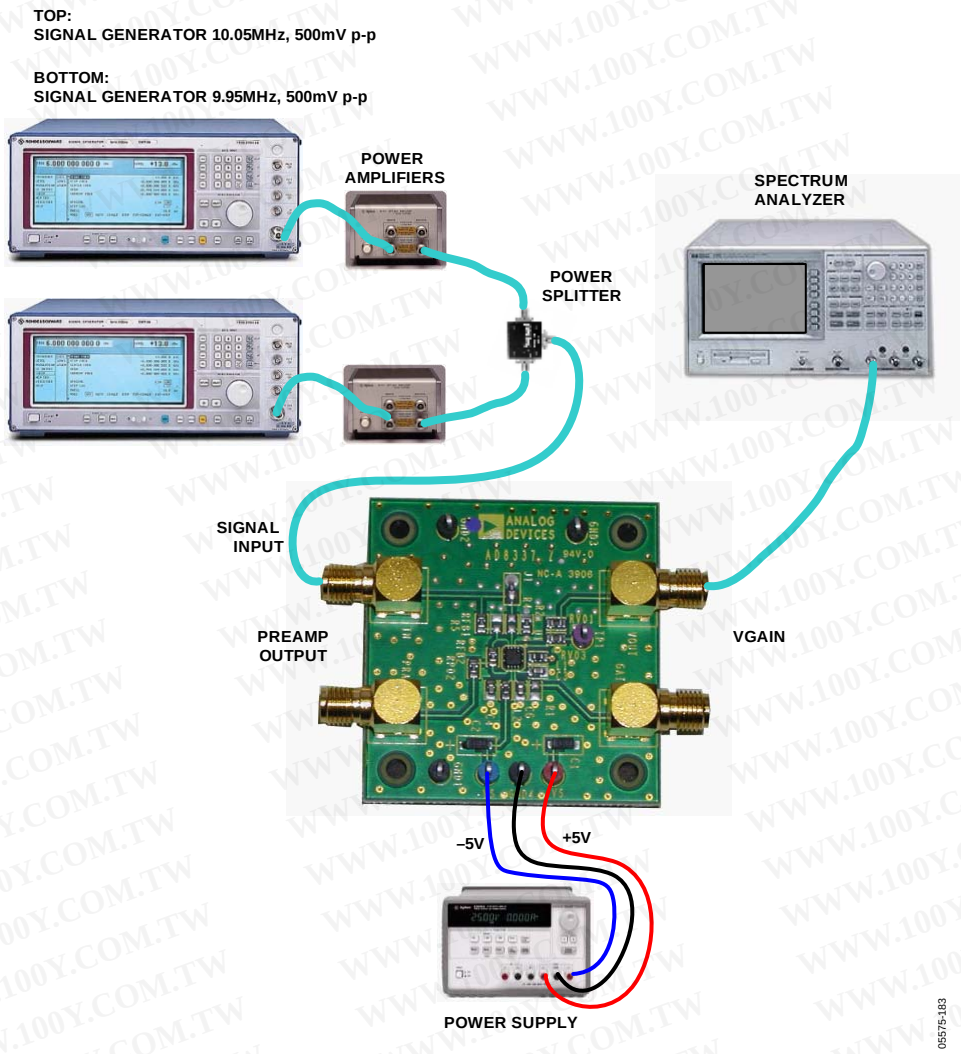


Figure 83. Typical Board Test Connections

MEASUREMENT SETUP

Figure 83 shows board connections for two generators. In this example, the experiment illustrates IMD measurements using standard off-the-shelf test equipment used by Analog Devices. However, any equivalent equipment can be used.

BOARD LAYOUT CONSIDERATIONS

The AD8337 evaluation board is designed using four layers. Interconnecting circuitry is located on the component and wiring sides, with the inner layers dedicated to power and ground planes. Figure 84 through Figure 88 show the copper layouts.

For ease of assembly, all board components are located on the primary side and are 0603 size surface mounts. Higher density applications may require components on both sides of the board and present no problem to the AD8337, as demonstrated in unreleased versions of the board that featured secondary-side components and vias. Not evident in the figures are thermal vias within the pad that solder to the mating pad of the AD8337 chip-scale package. These vias serve as a thermal path and are the primary means of removing heat from the device. The thermal specifications for the AD8337 are predicated on the use of multi-layer board construction with these thermal vias to enable heat conductivity from the die.

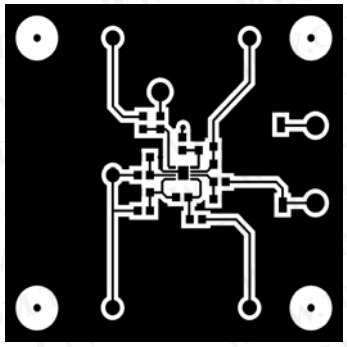


Figure 84. Dual-Supply Component Side Copper

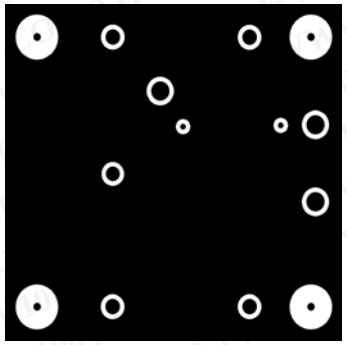


Figure 85. Dual-Supply Wiring Side Copper

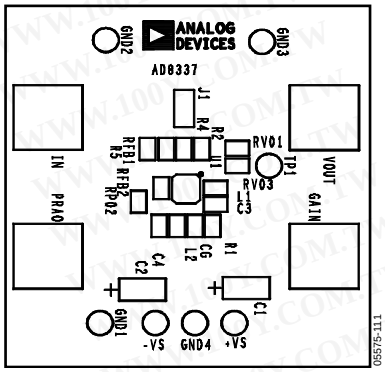


Figure 86. Dual-Supply Component Side Silk-Screen

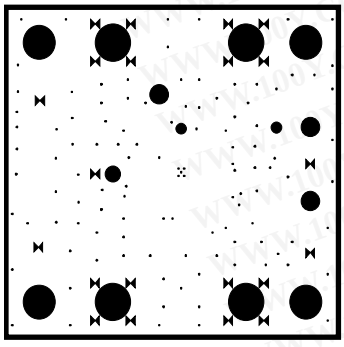


Figure 87. Dual-Supply Ground Plane

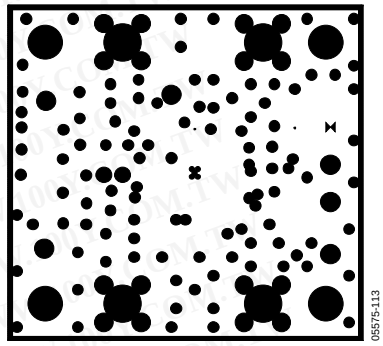


Figure 88. Dual-Supply Power Plane

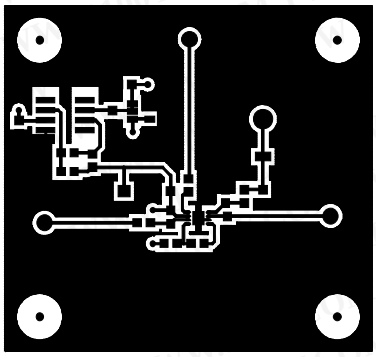


Figure 89. Single-Supply Component Side Copper

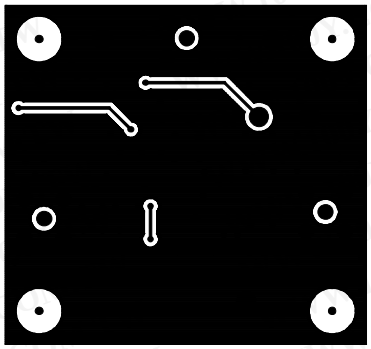


Figure 90. Single-Supply Wiring Side Copper

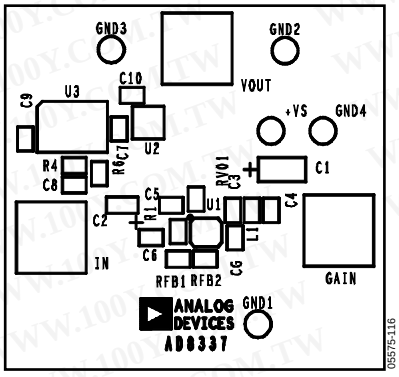


Figure 91. Single-Supply Component Side Silkscreen

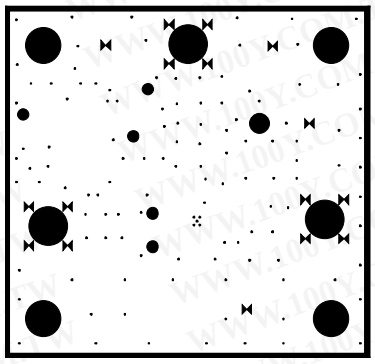


Figure 92. Single-Supply Ground Plane

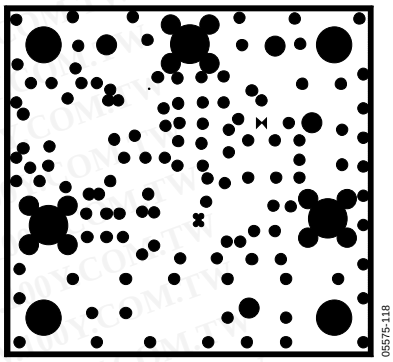


Figure 93. Single-Supply Power Plane

BILL OF MATERIALS

Table 5. Dual-Supply Noninverting Bill of Materials

Qty.	Reference Designator	Description	Manufacturer	Mfg. Part Number
1	$+V_S$	Red test loop, 0.125″ diameter	Bisco Industries	TP-104-01-02
4	GND1 to GND4	Black test loop, 0.125″ diameter	Bisco Industries	TP-104-01-00
1	$-V_S$	Blue test loop, 0.125″ diameter	Bisco Industries	TP-104-01-06
1	TP1	Purple test loop, 0.125″ diameter	Bisco Industries	TP-104-01-07
2	C3, C4	SM 0.1 µF, 16 V, 0603, X7R capacitors	KEMET	C0603C104K4RACTU
1	CG	SM 1 nF, 50 V, X7R, 10%, 0603 capacitor	Panasonic	ECJ-1VB2A102K
2	C1, C2	SM tantalum, 10 µF, 10 V, A size capacitors	Nichicon	T491A106M010AS
1	U1	Integrated circuit VGA	Analog Devices, Inc.	AD8337BCPZ-WP
4	GAIN, IN, PRAO, VOUT	SMA fem PC mount RA connectors	Amphenol	901-143-6RFX
2	L1, L2	120 nH, 0603 ferrite beads	Murata	BLM18BA750SN1D
1	R2	49.9 Ω, 1%, 1/16 W, 0603 resistor	Panasonic	ERJ-3EKF49R9V
2	R4, RVO3	0 Ω, 5%, 1/10 W, 0603 resistors	Panasonic	ERJ-2GE0R00X
2	R_{FB1}, R_{FB2}	100 Ω, 1%, 1/16 W, 0603 resistors	Panasonic	ERJ-3EKF1000V
2	RPO2, RVO1	453 Ω, 1/16 W, 1%, 0603 resistors	Panasonic	ERJ-3EKF4530V

Table 6. Dual-Supply Inverting Gain Bill of Materials

Qty.	Reference Designator	Description	Manufacturer	Mfg. Part Number
1	$+V_S$	Red test loop, 0.125″ diameter	Bisco Industries	TP-104-01-02
4	GND1 to GND4	Black test loop, 0.125″ diameter	Bisco Industries	TP-104-01-00
1	$-V_S$	Blue test loop, 0.125″ diameter	Bisco Industries	TP-104-01-06
1	TP1	Purple test loop, 0.125″ diameter	Bisco Industries	TP-104-01-07
2	C3, C4	SM 0.1 µF, 16 V, 0603, X7R capacitors	KEMET	C0603C104K4RACTU
1	CG	SM 1 nF, 50 V, X7R, 10%, 0603 capacitor	Panasonic	ECJ-1VB2A102K
2	C1, C2	SM tantalum, 10 µF, 10 V, A size capacitors	Nichicon	T491A106M010AS
1	U1	Integrated circuit VGA	Analog Devices, Inc.	AD8337BCPZ-WP
4	GAIN, IN, PRAO, VOUT	SMA fem PC mount RA connectors	Amphenol	901-143-6RFX
2	L1, L2	120 nH, 0603 ferrite beads	Murata	BLM18BA750SN1D
1	R2	49.9 Ω, 1%, 1/16 W, 0603 resistor	Panasonic	ERJ-3EKF49R9V
1	RVO3	0 Ω, 5%, 1/10 W, 0603 resistor	Panasonic	ERJ-2GE0R00X
3	R_{FB2}, R5, J1 (J1 POSITION)	100 Ω, 1%, 1/16 W, 0603 resistors	Panasonic	ERJ-3EKF1000V
2	RPO2, RVO1	453 Ω, 1/16 W, 1%, 0603 resistors	Panasonic	ERJ-3EKF4530V

Table 7. Single-Supply Bill of Materials

Qty.	Reference Designator	Description	Manufacturer	Mfg. Part Number
1	$+V_S$	Red test point, 0.125" diameter	Bisco Industries	TP-104-01-02
1	C1	Tantalum, 10 µF, 10 V, A size capacitor	Nichicon	T491A106M010AS
1	C2	Tantalum, 1 µF, P size capacitor	Nichicon	F921C105MPA
7	C3, C4, C5, C6, C7, C9, C10	0.1 µF, 16 V, 0603, X7R capacitors	KEMET	C0603C104K4RACTU
1	C8	0.22 µF, 10%, 0603, X7R capacitor	Panasonic	ECJ-1VB1H223K
1	CG	1 nF, 50 V, X7R, 10%, 0603 capacitor	Panasonic	ECJ-1VB2A102K
3	GAIN, IN, VOUT	SMA fem PC mount RA connectors	Amphenol	901-143-6RFX
4	GND1 to GND4	Loop, 0.125" diameter, black test points	Bisco Industries	TP-104-01-00
1	L1	120 nH, 0603 ferrite bead	Murata	BLM18BA750SN1D
1	R1	49.9 Ω, 1%, 1/16 W, 0603 resistor	Panasonic	ERJ-3EKF49R9V
1	R4	10 kΩ, 1%, 1/16 W, 0603 resistor	Panasonic	ERJ-3EKF1002V
3	R_{FB1}, R_{FB2}, R6	100 Ω, 1%, 1/16 W, 0603 resistors	Panasonic	ERJ-3EKF1000V
1	RVO1	453 Ω, 1%, 1/16 W, 0603 resistor	Panasonic	ERJ-3EKF4530V
1	U1	VGA integrated circuit	Analog Devices, Inc.	AD8337BCPZ-WP
1	U2	2.5 V regulator integrated circuit	Analog Devices, Inc.	ADR391AUJZ-R2
1	U3	SS rail-to-rail op amp integrated circuit	Analog Devices, Inc.	AD8541AR

OUTLINE DIMENSIONS

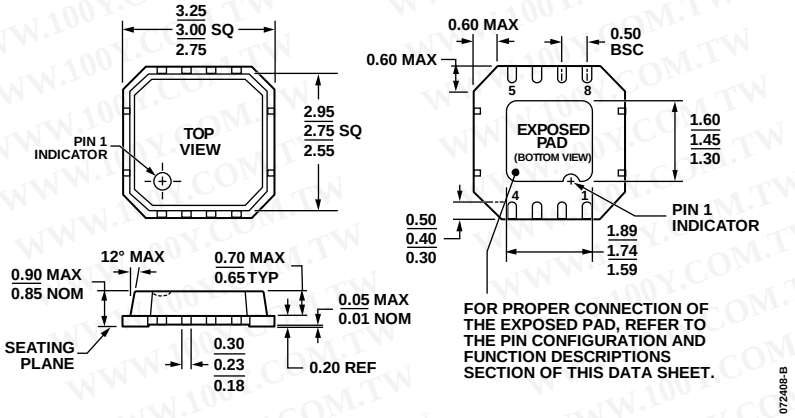


Figure 94. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8337BCPZ-R2[1]	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	HVB
AD8337BCPZ-REEL[1]	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	HVB
AD8337BCPZ-REEL7[1]	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	HVB
AD8337BCPZ-WP[1]	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-2	HVB
AD8337-EVALZ[1]		Evaluation Board with Noninverting Gain Configuration		
AD8337-EVALZ-INV[1]		Evaluation Board with Inverting Gain Configuration		
AD8337-EVALZ-SS[1]		Evaluation Board with Single-Supply Operation		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D05575-0-9/08(C)