ANALOG DEVICES

Precision, Dual-Channel Instrumentation Amplifier

AD8222

FEATURES

Two channels in small 4 mm × 4 mm LFCSP
Gain set with 1 resistor per amplifier (G = 1 to 10,000)
Low noise
- **8 nV/√Hz at 1 kHz**
- **0.25 μV p-p (0.1 Hz to 10 Hz)**

High accuracy dc performance (B grade)
- **60 μV maximum input offset voltage**
- **0.3 μV/°C maximum input offset drift**
- **1.0 nA maximum input bias current**
- **126 dB minimum CMRR (G = 100)**

Excellent ac performance
- **140 kHz bandwidth (G = 100)**
- **13 μs settling time to 0.001%**

Differential output option (single channel)
- **Fully specified**
- **Adjustable common-mode output**

Supply range: ±2.3 V to ±18 V

APPLICATIONS

Multichannel data acquisition for
- **ECG and medical instrumentation**
- **Industrial process controls**
- **Wheatstone bridge sensors**

Differential drives for
- **High resolution input ADCs**
- **Remote sensors**

FUNCTIONAL BLOCK DIAGRAM

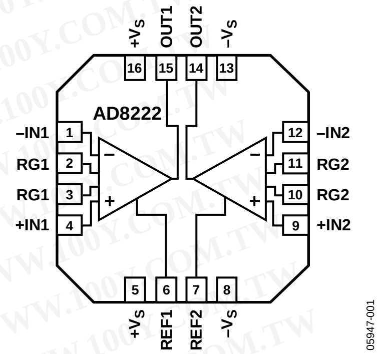

Figure 1. 4 mm × 4 mm LFCSP

Table 1. Instrumentation Amplifiers by Category[1]

General Purpose	Zero Drift	Military Grade	Low Power	High Speed PGA
AD8220	AD8231	AD620	AD8235	AD8250
AD8221	AD8290	AD621	AD8236	AD8251
AD8222	AD8293	AD524	AD627	AD8253
AD8224	AD8553	AD526	AD623	
AD8228	AD8556	AD624	AD8223	
AD8295	AD8557		AD8226	
			AD8227	

[1] See www.analog.com for the latest selection of instrumentation amplifiers.

GENERAL DESCRIPTION

The AD8222 is a dual-channel, high performance instrumentation amplifier that requires only one external resistor per amplifier to set gains of 1 to 10,000.

The AD8222 is the first dual-instrumentation amplifier in the small 4 mm × 4mm LFCSP. It requires the same board area as a typical single instrumentation amplifier. The smaller package allows a 2× increase in channel density and a lower cost per channel, all with no compromise in performance.

The AD8222 can also be configured as a single-channel, differential output instrumentation amplifier. Differential outputs provide high noise immunity, which can be useful when the output signal must travel through a noisy environment, such as with remote sensors. The configuration can also be used to drive differential input ADCs.

The AD8222 maintains a minimum CMRR of 80 dB to 4 kHz for all grades at G = 1. High CMRR over frequency allows the AD8222 to reject wideband interference and line harmonics, greatly simplifying filter requirements. The AD8222 also has a typical CMRR drift over temperature of just 0.07 μV/V/°C at G = 1.

The AD8222 operates on both single and dual supplies and only requires 2.2 mA maximum supply current for both amplifiers. It is specified over the industrial temperature range of −40°C to +85°C and is fully RoHS compliant.

For a single-channel version, see the AD8221.

Rev. A

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REVISION HISTORY

2/10—Rev. 0 to Rev. A

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Change to Reference Input Parameter, Table 2 ... 4
Changed Output Short-Circuit Current to Output Short-Circuit Duration, Table 5 ... 6
Changes to Thermal Resistance Section and Table 6 ... 6
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7/06—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm15$ V, $V_{REF} = 0$ V, $T_A = 25°C$, G = 1, $R_L = 2$ kΩ, unless otherwise noted.

Table 2. Single-Ended and Differential[1] Output Configuration

Parameter	Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	$V_{CM} = -10$ V to +10 V							
CMRR DC to 60 Hz	1 kΩ source imbalance							
G = 1		80			86			dB
G = 10		100			106			dB
G = 100		120			126			dB
G = 1000		130			140			dB
CMRR at 4 kHz								
G = 1		80			80			dB
G = 10		90			100			dB
G = 100		100			110			dB
G = 1000		100			110			dB
CMRR Drift	$T_A = -40°C$ to +85°C, G = 1		0.07			0.07		μV/V/°C
NOISE								
Voltage Noise, 1 kHz	RTI noise = $\sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$							
Input Voltage Noise, e_{NI}	V_{+IN}, V_{-IN}, $V_{REF} = 0$ V			8			8	nV/√Hz
Output Voltage Noise, e_{NO}	V_{+IN}, V_{-IN}, $V_{REF} = 0$ V			75			75	nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 1			2			2		μV p-p
G = 10			0.5			0.5		μV p-p
G = 100 to 1000			0.25			0.25		μV p-p
Current Noise	f = 1 kHz		40			40		fA/√Hz
	f = 0.1 Hz to 10 Hz		6			6		pA p-p
VOLTAGE OFFSET	RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$							
Input Offset, V_{OSI}	$V_S = \pm5$ V to ±15 V			120			60	μV
Over Temperature	$T_A = -40°C$ to +85°C			150			80	μV
Average TC				0.4			0.3	μV/°C
Output Offset, V_{OSO}	$V_S = \pm5$ V to ±15 V			500			350	μV
Over Temperature	$T_A = -40°C$ to +85°C			0.8			0.5	mV
Average TC				9			5	μV/°C
Offset RTI vs. Supply (PSR)	$V_S = \pm2.3$ V to ±18 V							
G = 1		90	110		94	110		dB
G = 10		110	120		114	130		dB
G = 100		124	130		130	140		dB
G = 1000		130	140		140	150		dB
INPUT CURRENT (PER CHANNEL)								
Input Bias Current, I_{BIAS}			0.5	2.0		0.2	1.0	nA
Over Temperature	$T_A = -40°C$ to +85°C			3.0			1.5	nA
Average TC			1			1		pA/°C
Input Offset Current, I_{OFFSET}			0.2	1		0.1	0.5	nA
Over Temperature	$T_A = -40°C$ to +85°C			1.5			0.6	nA
Average TC			1			0.5	2	pA/°C

Parameter	Conditions	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE INPUT								
R_{IN}			20			20		kΩ
I_{IN}	V_{+IN}, V_{-IN}, $V_{REF} = 0$ V		50	60		50	60	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%
GAIN	$G = 1 + (49.4\ k\Omega/R_G)$							
Gain Range		1		10000	1		10000	V/V
Gain Error	$V_{OUT} \pm 10$ V							
G = 1				0.05			0.02	%
G = 10				0.3			0.15	%
G = 100				0.3			0.15	%
G = 1000				0.3			0.15	%
Gain Nonlinearity	$V_{OUT} = -10$ V to $+10$ V							
G = 1			3	10		1	5	ppm
G = 10			7	20		7	20	ppm
G = 100			7	20		7	20	ppm
Gain vs. Temperature								
G = 1			3	10		2	5	ppm/°C
G > 1[2]				−50			−50	ppm/°C
INPUT								
Input Impedance								
Differential			100‖2			100‖2		GΩ‖pF
Common Mode			100‖2			100‖2		GΩ‖pF
Input Operating Voltage Range[3]	$V_S = \pm 2.3$ V to ± 5 V	$-V_S + 1.9$		$+V_S - 1.1$	$-V_S + 1.9$		$+V_S - 1.1$	V
Over Temperature	$T_A = -40°C$ to $+85°C$	$-V_S + 2.0$		$+V_S - 1.2$	$-V_S + 2.0$		$+V_S - 1.2$	V
Input Operating Voltage Range[3]	$V_S = \pm 5$ V to ± 18 V	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	V
Over Temperature	$T_A = -40°C$ to $+85°C$	$-V_S + 2.0$		$+V_S - 1.2$	$-V_S + 2.0$		$+V_S - 1.2$	V
OUTPUT	$R_L = 10$ kΩ							
Output Swing	$V_S = \pm 2.3$ V to ± 5 V	$-V_S + 1.1$		$+V_S - 1.2$	$-V_S + 1.1$		$+V_S - 1.2$	V
Over Temperature	$T_A = -40°C$ to $+85°C$	$-V_S + 1.4$		$+V_S - 1.3$	$-V_S + 1.4$		$+V_S - 1.3$	V
Output Swing	$V_S = \pm 5$ V to ± 18 V	$-V_S + 1.2$		$+V_S - 1.4$	$-V_S + 1.2$		$+V_S - 1.4$	V
Over Temperature	$T_A = -40°C$ to $+85°C$	$-V_S + 1.6$		$+V_S - 1.5$	$-V_S + 1.6$		$+V_S - 1.5$	V
Short-Circuit Current			18			18		mA
POWER SUPPLY								
Operating Range	$V_S = \pm 2.3$ V to ± 18 V	±2.3		±18	±2.3		±18	V
Quiescent Current (per Amplifier)			0.9	1.1		0.9	1.1	mA
Over Temperature	$T_A = -40°C$ to $+85°C$		1	1.2		1	1.2	mA
TEMPERATURE RANGE								
Specified Performance		−40		+85	−40		+85	°C
Operational[4]		−40		+125	−40		+125	°C

[1] Refers to differential configuration shown in Figure 49.
[2] Does not include the effects of external resistor, R_G.
[3] One input grounded. G = 1.
[4] See the Typical Performance Characteristics section for expected operation between 85°C and 125°C.

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, R_L = 2 kΩ, unless otherwise noted.

Table 3. Single-Ended Output Configuration—Dynamic Performance (Both Amplifiers)

		A Grade			B Grade			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			1200			1200		kHz
G = 10			750			750		kHz
G = 100			140			140		kHz
G = 1000			15			15		kHz
Settling Time 0.01%	10 V step							
G = 1 to 100			10			10		µs
G = 1000			80			80		µs
Settling Time 0.001%	10 V step							
G = 1 to 100			13			13		µs
G = 1000			110			110		µs
Slew Rate	G = 1	1.5	2		1.5	2		V/µs
	G = 5 to 1000	2	2.5		2	2.5		V/µs

Table 4. Differential Output Configuration[1]—Dynamic Performance

		A Grade			B Grade			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			1000			1000		kHz
G = 10			650			650		kHz
G = 100			140			140		kHz
G =1000			15			15		kHz
Settling Time 0.01%	10 V step							
G = 1 to 100			15			15		µs
G = 1000			80			80		µs
Settling Time 0.001%	10 V step							
G = 1 to 100			18			18		µs
G = 1000			110			110		µs
Slew Rate	G = 1	1.5	2		1.5	2		V/µs
	G = 5 to 1000	2	2.5		2	2.5		V/µs

[1] Refers to differential configuration shown in Figure 49.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +130°C
Operational Temperature Range	−40°C to +125°C
Package Glass Transition Temperature (T_G)	130°C
ESD	
Human Body Model	1 kV
Charge Device Model	1 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package	θ_{JA}	Unit
CP-16-19: LFCSP Without Thermal Pad	86	°C/W
CP-16-13: LFCSP with Thermal Pad	48	°C/W

The θ_{JA} values in Table 6 assume a 4-layer JEDEC standard board. For the LFCSP with thermal pad, it is assumed that the thermal pad is soldered to a landing on the PCB board, with the landing thermally connected to a heat dissipating power plane. θ_{JC} at the exposed pad is 4.4°C/W.

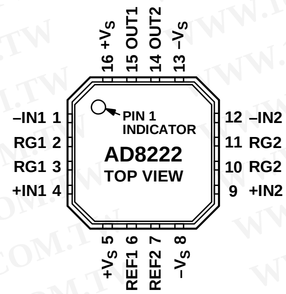
Maximum Power Dissipation

The maximum safe power dissipation for the AD8222 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 130°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 130°C for an extended period can result in a loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE AD8222 COMES IN TWO PACKAGE TYPES—EACH A 16 LEAD 4mm × 4mm LFCSP. ONE PACKAGE TYPE HAS AN EXPOSED THERMAL PAD, WHICH IS CONNECTED TO $-V_S$. THE OTHER PACKAGE TYPE DOES NOT EXPOSE THE THERMAL PAD. SEE THE PACKAGE CONSIDERATIONS SECTION FOR MORE INFORMATION.

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Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No	Mnemonic	Description
1	−IN1	Negative Input In-Amp 1
2	RG1	Gain Resistor In-Amp 1
3	RG1	Gain Resistor In-Amp 1
4	+IN1	Positive Input In-Amp 1
5	$+V_S$	Positive Supply
6	REF1	Reference Adjust In-Amp 1
7	REF2	Reference Adjust In-Amp 2
8	$-V_S$	Negative Supply
9	+IN2	Positive Input In-Amp 2
10	RG2	Gain Resistor In-Amp 2
11	RG2	Gain Resistor In-Amp 2
12	−IN2	Negative Input In-Amp 2
13	$-V_S$	Negative Supply
14	OUT2	Output In-Amp 2
15	OUT1	Output In-Amp 1
16	$+V_S$	Positive Supply

TYPICAL PERFORMANCE CHARACTERISTICS

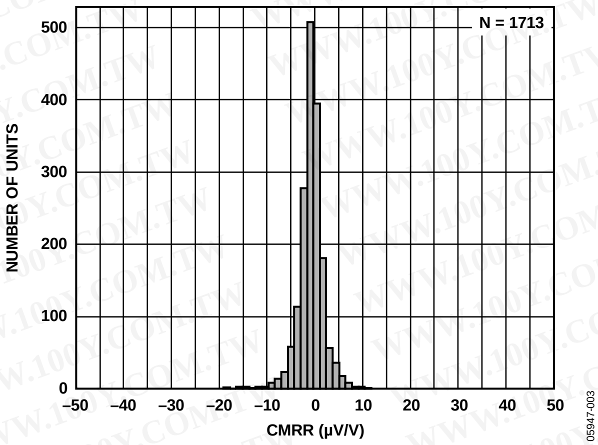


Figure 3. Typical Distribution for CMRR (G = 1)

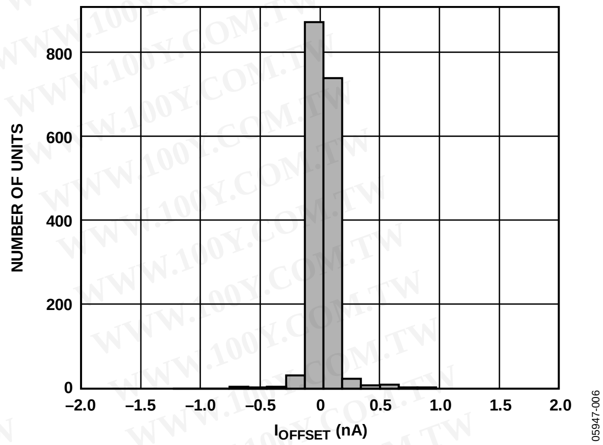


Figure 6. Typical Distribution of Input Offset Current

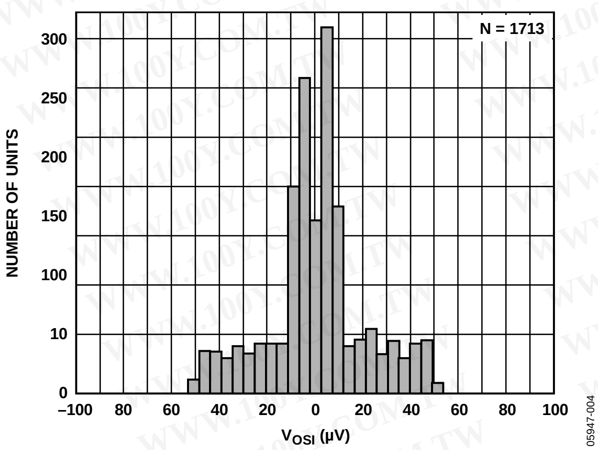


Figure 4. Typical Distribution of Input Offset Voltage

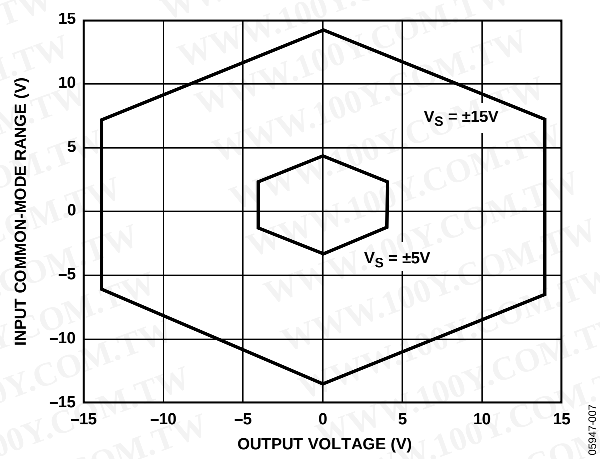


Figure 7. Input Common-Mode Range vs. Output Voltage, G = 1

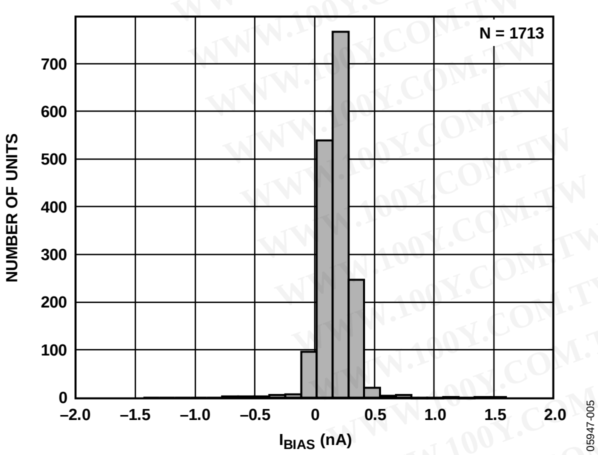


Figure 5. Typical Distribution of Input Bias Current

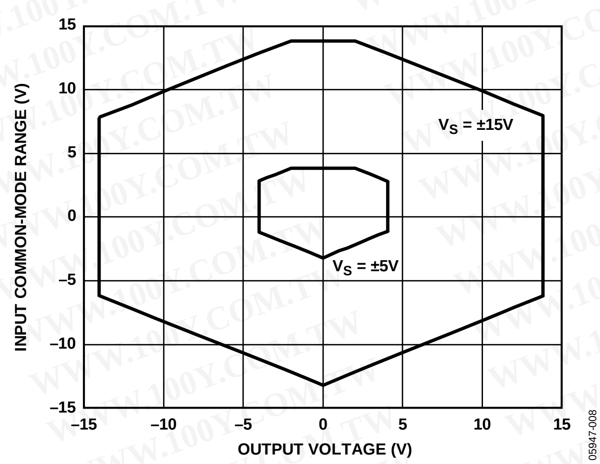


Figure 8. Input Common-Mode Range vs. Output Voltage, G = 100

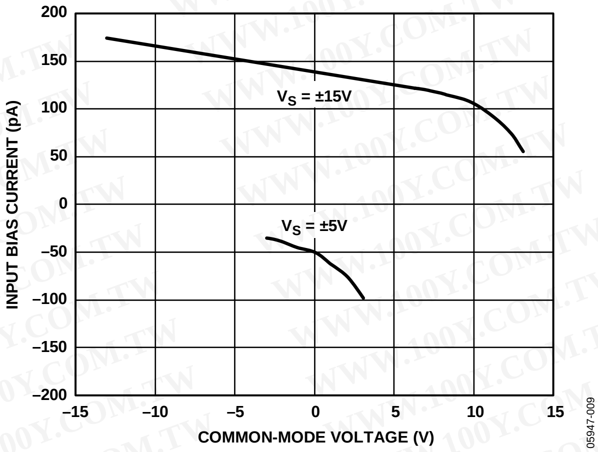


Figure 9. I_{BIAS} vs. Common-Mode Voltage

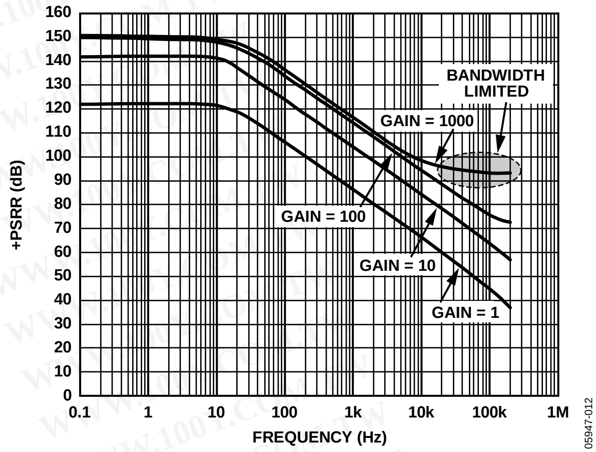


Figure 12. Positive PSRR vs. Frequency, RTI (G = 1 to 1000)

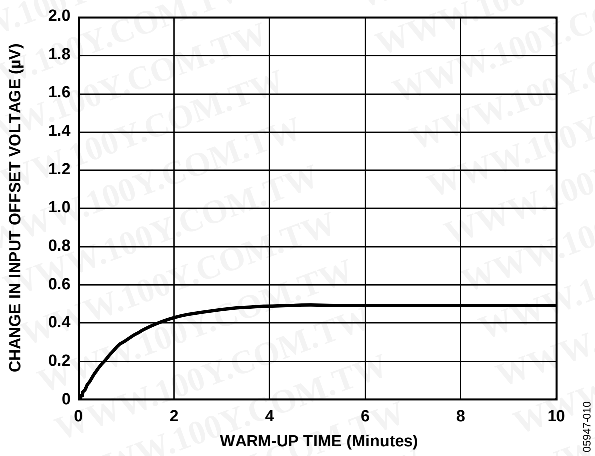


Figure 10. Change in Input Offset Voltage vs. Warm-Up Time

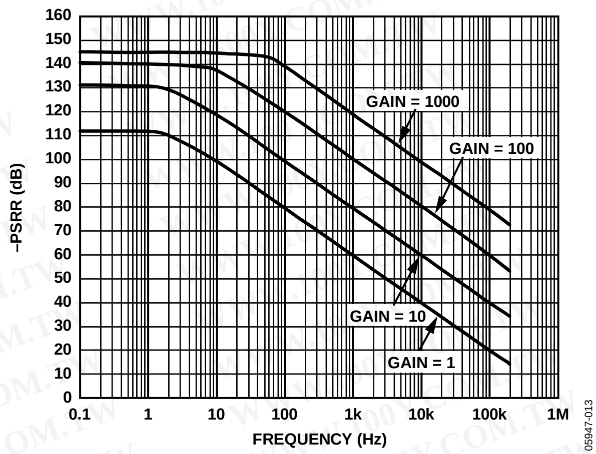


Figure 13. Negative PSRR vs. Frequency, RTI (G = 1 to 1000)

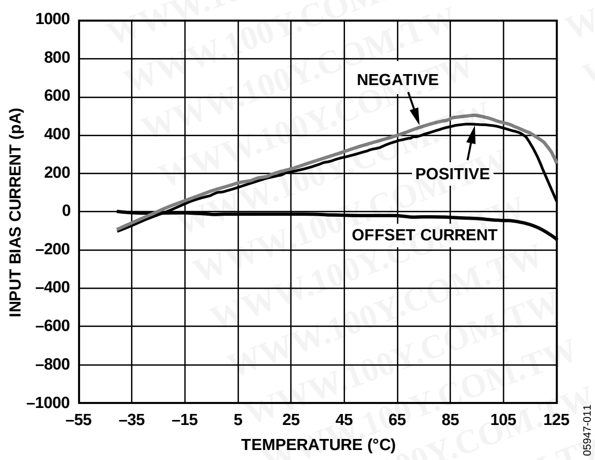


Figure 11. Input Bias Current and Offset Current vs. Temperature

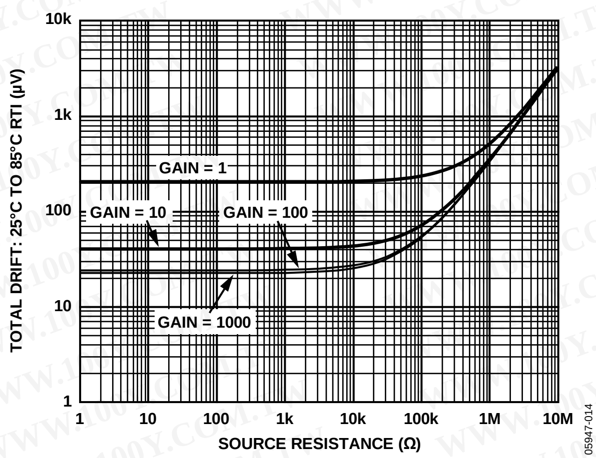


Figure 14. Total Drift vs. Source Resistance

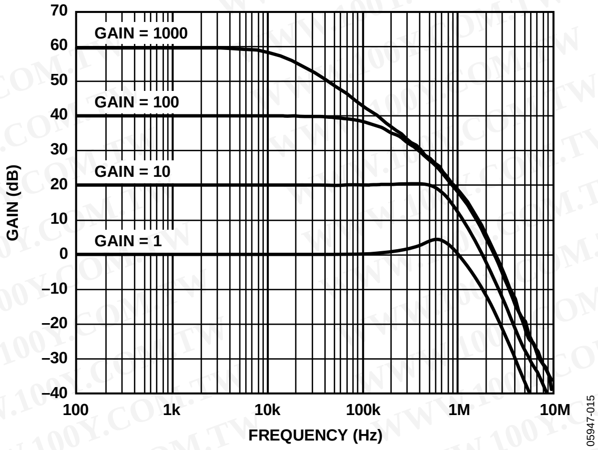


Figure 15. Gain vs. Frequency

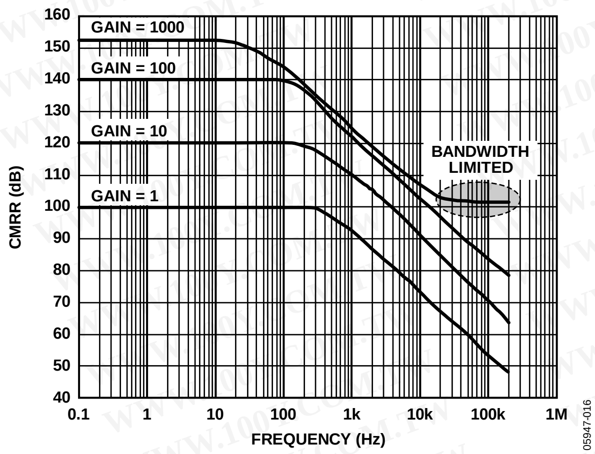


Figure 16. CMRR vs. Frequency, RTI

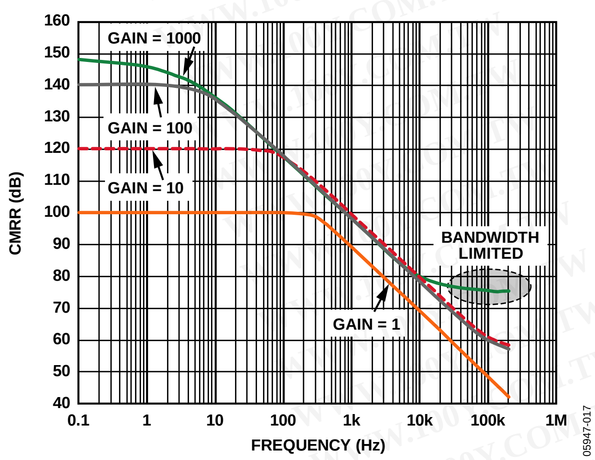


Figure 17. CMRR vs. Frequency, RTI, 1 kΩ Source Imbalance

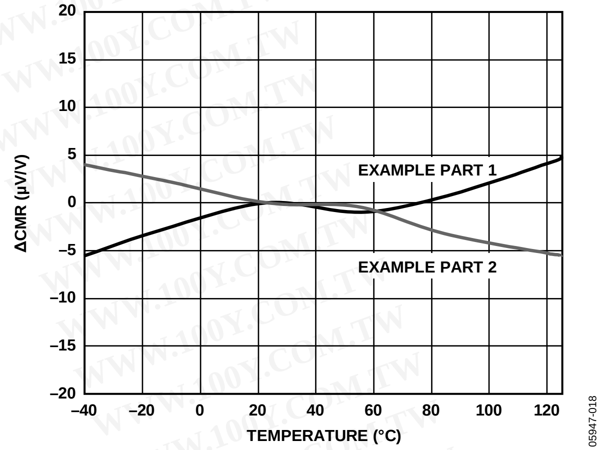


Figure 18. ΔCMR vs. Temperature, G = 1

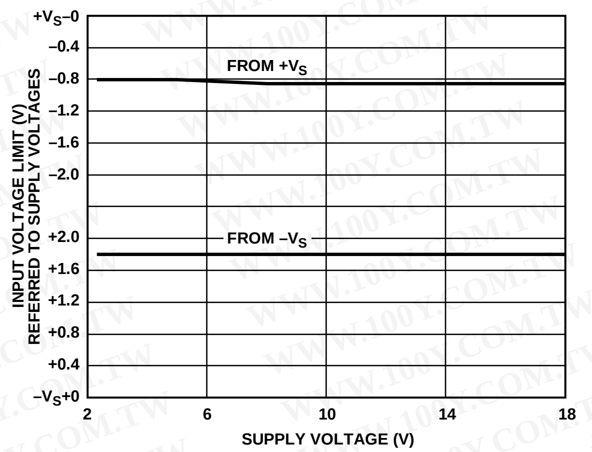


Figure 19. Input Voltage Limit vs. Supply Voltage, G = 1

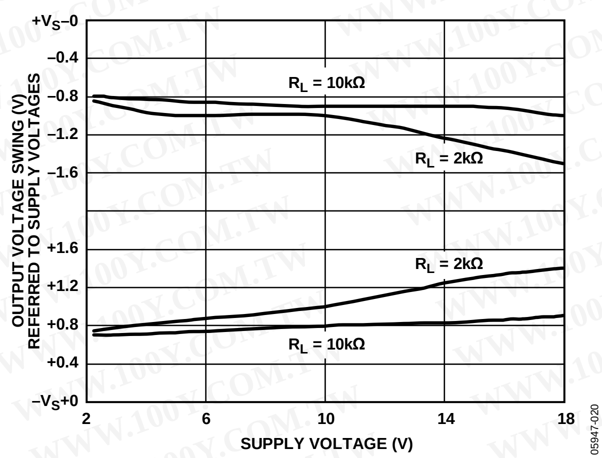


Figure 20. Output Voltage Swing vs. Supply Voltage, G = 1

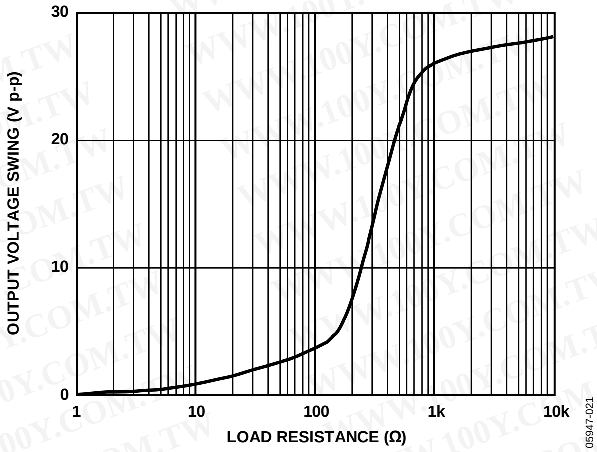


Figure 21. Output Voltage Swing vs. Load Resistance

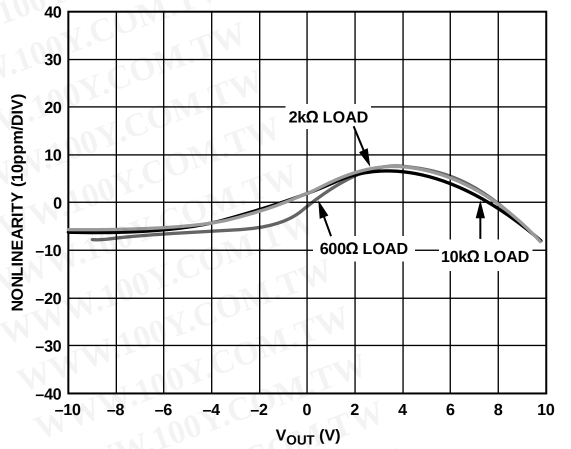


Figure 24. Gain Nonlinearity, G = 100

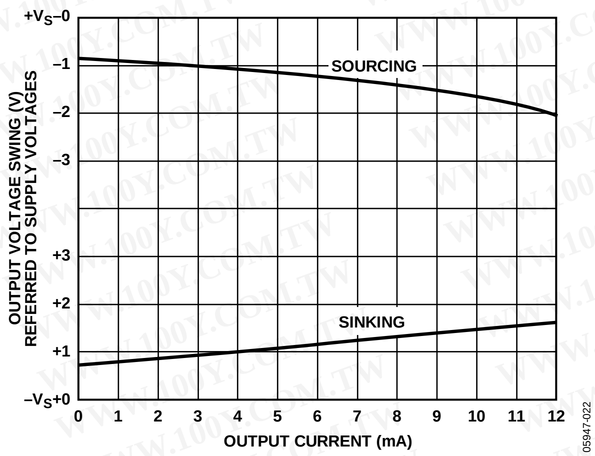


Figure 22. Output Voltage Swing vs. Output Current, G = 1

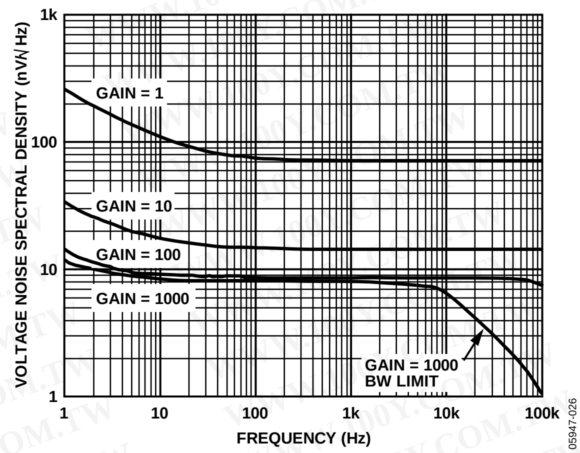


Figure 25. Voltage Noise Spectral Density vs. Frequency (G = 1 to 1000)

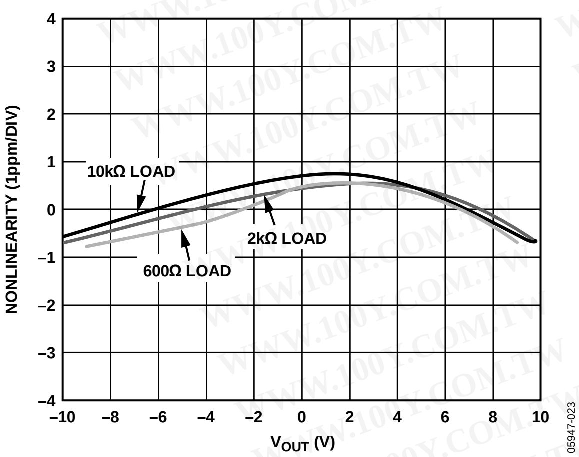


Figure 23. Gain Nonlinearity, G = 1

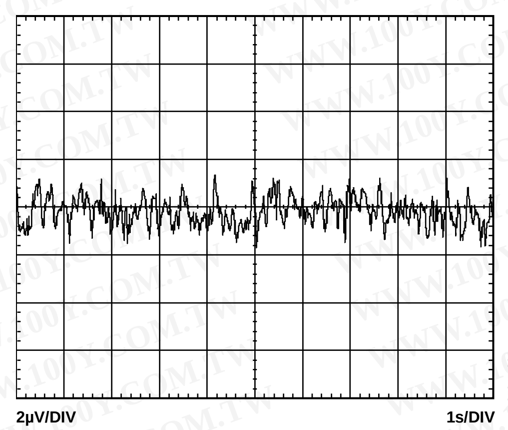


Figure 26. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

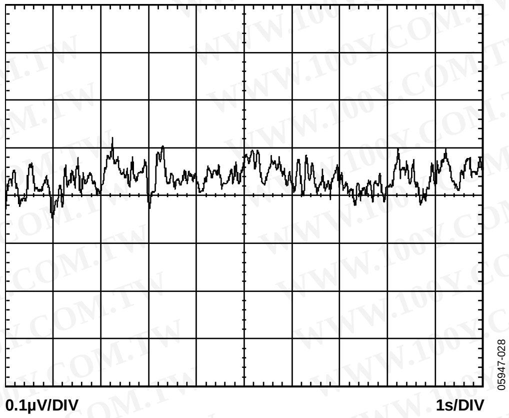


Figure 27. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

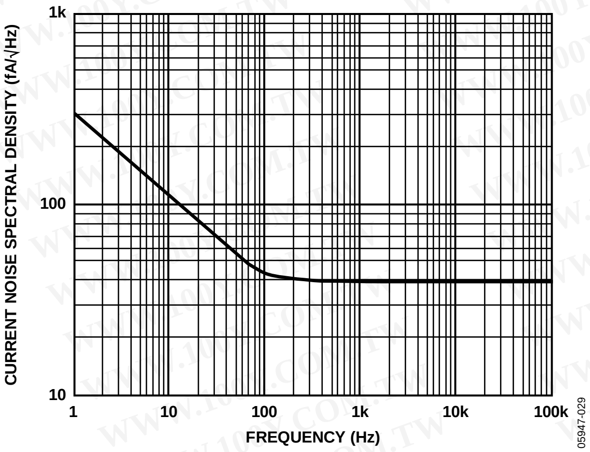


Figure 28. Current Noise Spectral Density vs. Frequency

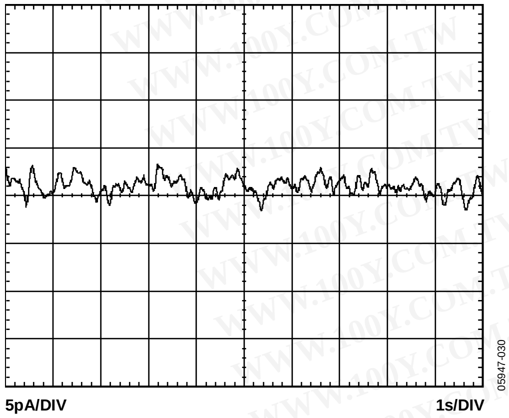


Figure 29. 0.1 Hz to 10 Hz Current Noise

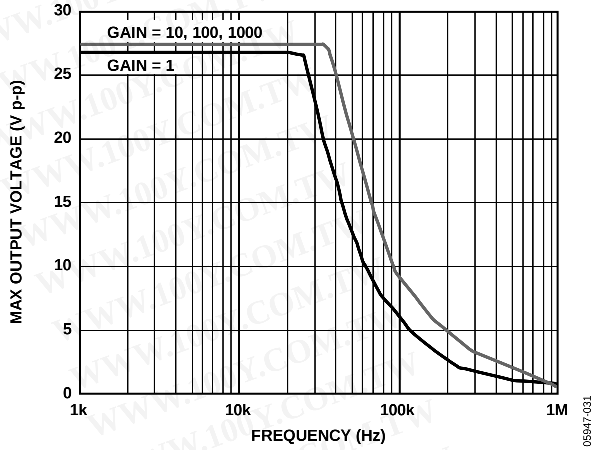


Figure 30. Large Signal Frequency Response

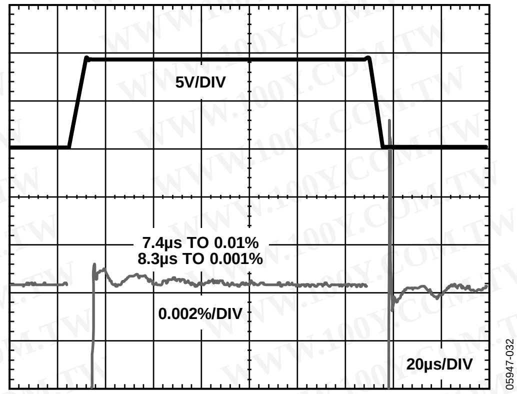


Figure 31. Large Signal Pulse Response and Settling Time (G = 1)

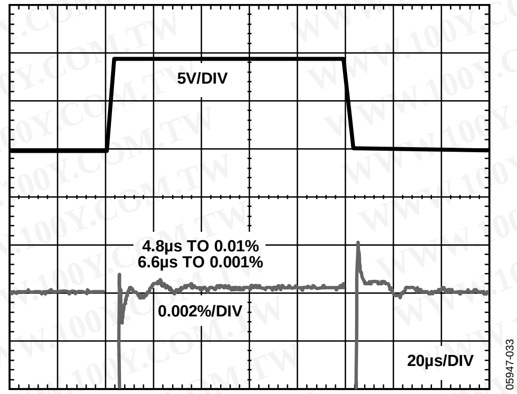


Figure 32. Large Signal Pulse Response and Settling (G = 10)

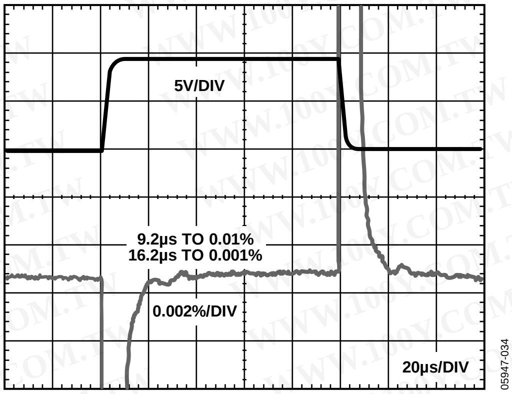


Figure 33. Large Signal Pulse Response and Settling Time (G = 100)

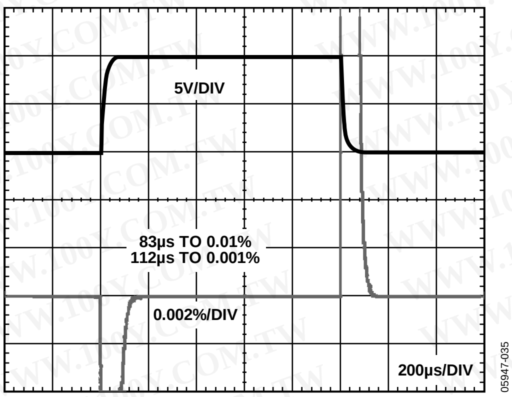


Figure 34. Large Signal Pulse Response and Settling Time (G = 1000)

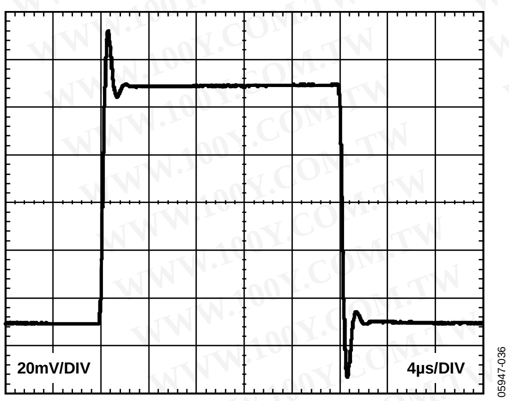


Figure 35. Small Signal Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

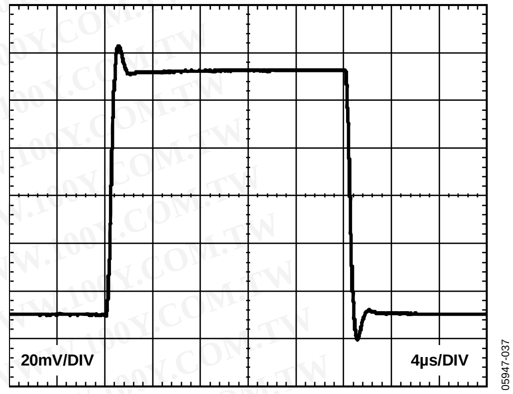


Figure 36. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

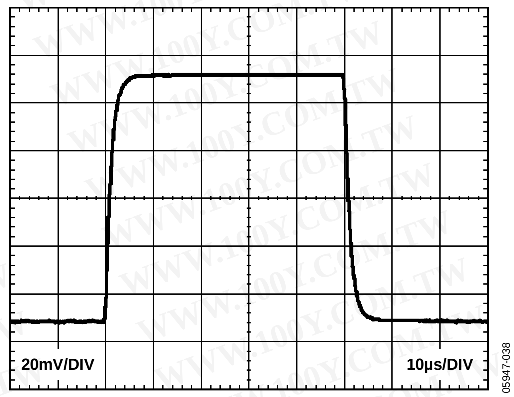


Figure 37. Small Signal Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

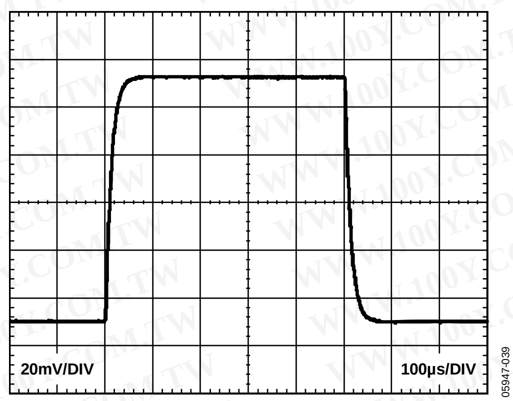


Figure 38. Small Signal Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

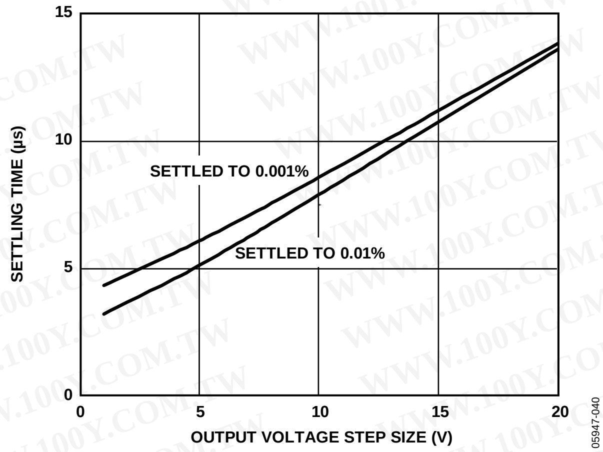


Figure 39. Settling Time vs. Step Size (G = 1)

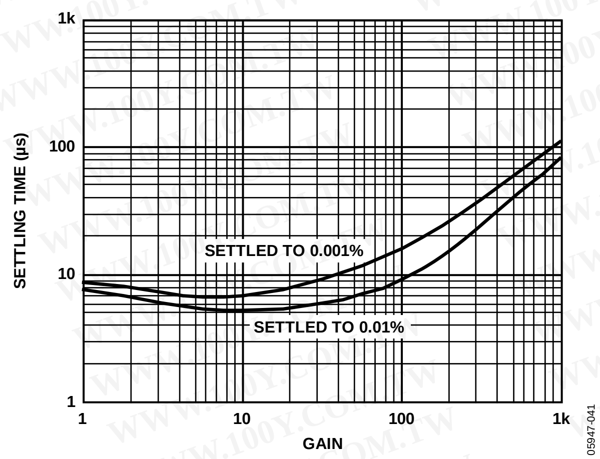


Figure 40. Settling Time vs. Gain for a 10 V Step

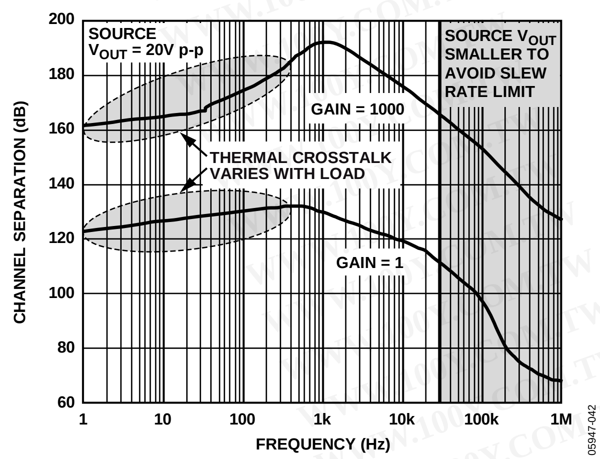


Figure 41. Channel Separation vs. Frequency, $R_L = 2\ k\Omega$, Source Channel at G = 1

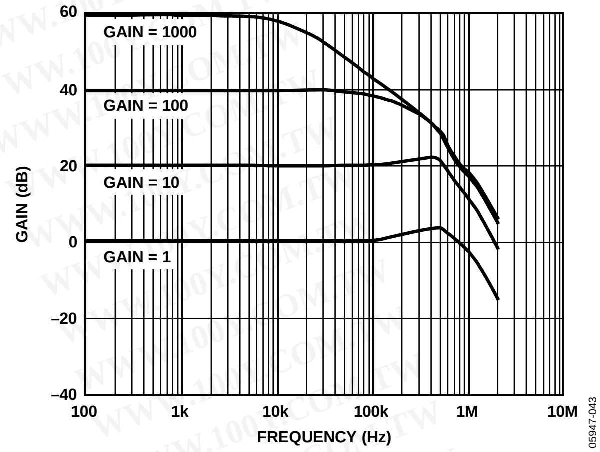


Figure 42. Differential Output Configuration: Gain vs. Frequency

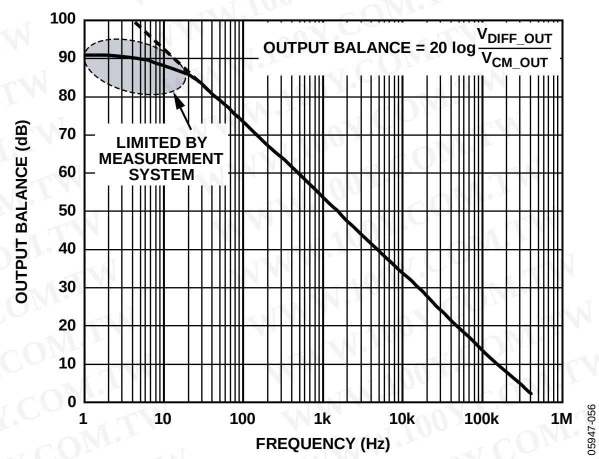


Figure 43. Differential Output Configuration: Output Balance vs. Frequency

THEORY OF OPERATION

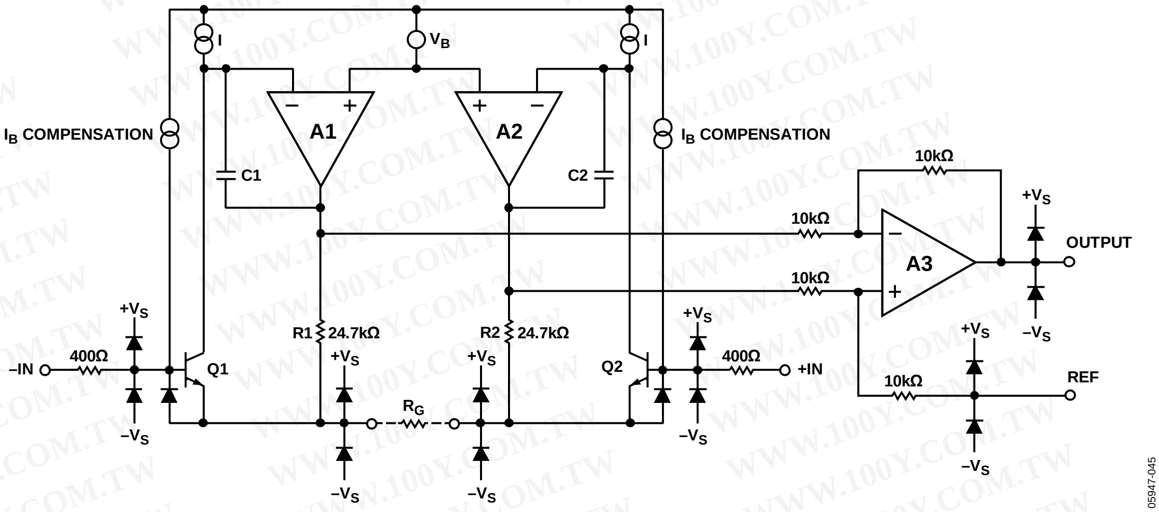


Figure 44. Simplified Schematic

AMPLIFIER ARCHITECTURE

The two instrumentation amplifiers of the AD8222 are based on the classic 3-op-amp topology. Figure 44 shows a simplified schematic of one of the amplifiers. The input transistors, Q1 and Q2, are biased at a fixed current. Any differential input signal forces the output voltages of A1 and A2 to change so that the differential voltage also appears across R_G. The current that flows through R_G must also flow through R1 and R2, resulting in a precisely amplified version of the differential input signal between the outputs of A1 and A2. Topologically, Q1 + A1 + R1 and Q2 + A2 + R2 can be viewed as precision current feedback amplifiers. The common-mode signal and the amplified differential signal are applied to a difference amplifier that rejects the common-mode voltage. The difference amplifier employs innovations that result in low output offset voltage as well as low output offset voltage drift.

Because the input amplifiers employ a current feedback architecture, the gain-bandwidth product of the AD8222 increases with gain, resulting in a system that does not suffer from the expected bandwidth loss of voltage feedback architectures at higher gains.

The transfer function of the AD8222 is

$$V_{OUT} = G(V_{+IN} - V_{-IN}) + V_{REF}$$

where:

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8222, which can be calculated by referring to Table 8 or by using the following gain equation:

$$R_G = \frac{49.4\ \text{k}\Omega}{G - 1}$$

Table 8. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

The AD8222 defaults to G = 1 when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the AD8222's specifications to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are kept to a minimum.

REFERENCE TERMINAL

The output voltage of an AD8222 channel is developed with respect to the potential on the corresponding reference terminal. Typically the reference terminal is connected to ground, but it can also be driven with a voltage to offset the output signal. For example, connect a voltage to the reference terminal to level-shift the output so that the AD8222 can drive a single-supply ADC. Both REF1 and REF2 are protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to a reference terminal should be kept below 1 Ω. As shown in Figure 44, the reference terminal is at one end of a 10 kΩ resistor. Additional impedance at the reference terminal adds to this 10 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be computed by

$$\frac{2\left(10\text{ k}\Omega + R_{REF}\right)}{20\text{ k}\Omega + R_{REF}}$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades the amplifier's CMRR.

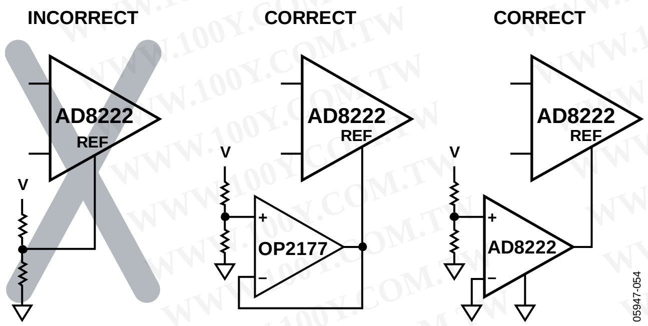


Figure 45. Driving the Reference Pin

PACKAGE CONSIDERATIONS

The AD8222 comes in a 4 mm × 4 mm LFCSP. Beware of blindly copying the footprint from another 4 mm × 4 mm LFCSP part; the landing pattern may be different. Refer to the Outline Dimensions section to verify that the PCB symbol has the correct dimensions.

The AD8222 comes in two package varieties, both with and without a thermal pad.

Package Without Thermal Pad

The AD8222 ships with a package that does not include a thermal pad; it is the preferred package for the AD8222. Unlike chip scale packages where the pad limits routing capability, the AD8222 package allows routes and vias directly underneath the chip, so that the full space savings of the small LFCSP can be realized.

Although the package has no metal in the center of the part, the manufacturing process does leave a very small section of exposed metal at each of the package corners, shown in Figure 55 in the Outline Dimensions section. This metal is connected to $-V_S$ through the part. Because of a possibility of a short, vias should not be placed underneath this exposed metal.

Package with Thermal Pad

This package is included primarily for legacy reasons. Because the AD8222 dissipates so little power, there is little need for the thermal pad.

The thermal pad is connected internally to $-V_S$. The pad can either be left unsoldered, soldered to an otherwise unconnected PCB landing, or soldered to a landing connected to the negative supply rail ($-V_S$). If pin compatibility with the AD8224 is desired, the pad should not be electrically connected to any net, including $-V_S$.

The solder process can leave flux and other contaminants on the board. When these contaminants are between the AD8222 leads and thermal pad, they can create leakage paths that are larger than the AD8222's bias currents. A thorough washing process removes these contaminants and restores the AD8222's excellent bias current performance.

LAYOUT

The AD8222 is a high precision device. To ensure optimum performance at the PC board level, care must be taken in the design of the board layout. The AD8222 pinout is arranged in a logical manner to aid in this task.

Common-Mode Rejection Over Frequency

The AD8222 has a higher CMRR over frequency than typical in-amps, which gives it greater immunity to disturbances, such as line noise and its associated harmonics. A well-implemented layout is required to maintain this high performance. Input source impedances should be matched closely. Source resistance should be placed close to the inputs so that it interacts with as little parasitic capacitance as possible.

Parasitics at the RGx pins can also affect CMRR over frequency. The PCB should be laid out so that the parasitic capacitances at each pin match. Traces from the gain setting resistor to the RGx pins should be kept short to minimize parasitic inductance.

Reference

Errors introduced at the reference terminal feed directly to the output. Care should be taken to tie REF to the appropriate local ground.

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance.

The AD8222 has two positive supply pins (Pin 5 and Pin 16) and two negative supply pins (Pin 8 and Pin 13). Although the part functions with only one pin from each supply pair connected, both pins should be connected for specified performance and optimum reliability.

The AD8222 should be decoupled with 0.1 μF bypass capacitors, one for each supply. The positive supply decoupling capacitor should be placed near Pin 16, and the negative supply decoupling capacitor should be placed near Pin 8. Each supply should also be decoupled with a 10 μF tantalum capacitor. The tantalum capacitor can be placed further away from the AD8222 and can generally be shared by other precision integrated circuits. Figure 46 shows an example layout.

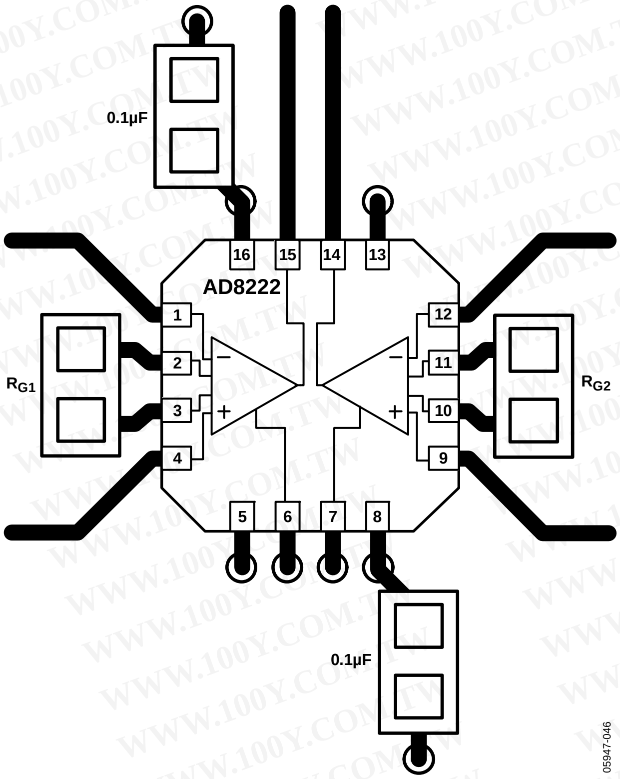


Figure 46. Example Layout

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8222 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 47.

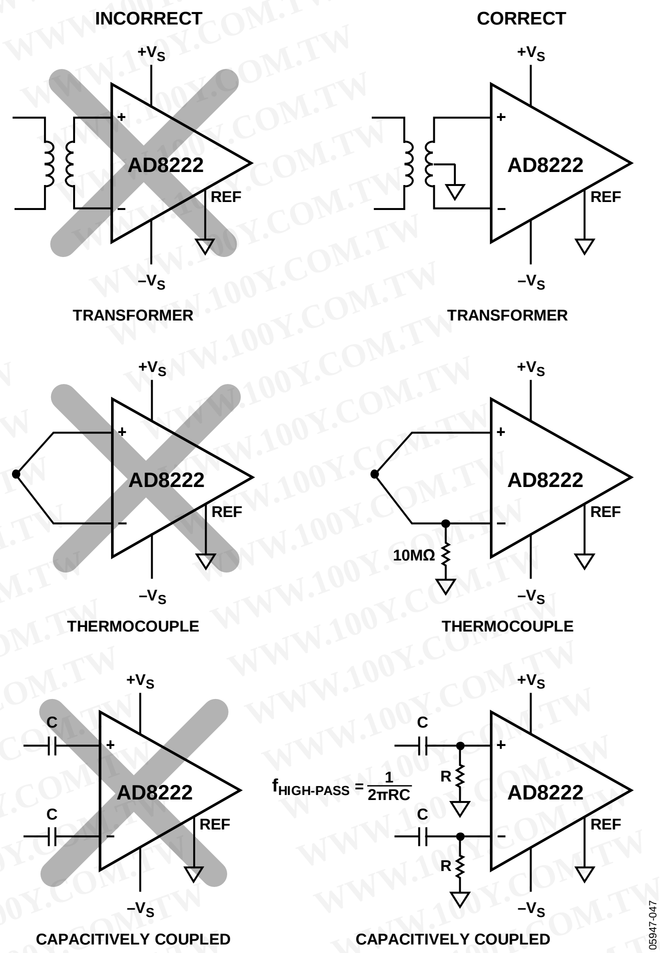


Figure 47. Creating an I_{BIAS} Path

INPUT PROTECTION

All terminals of the AD8222 are protected against ESD (1 kV, human body model). In addition, the input structure allows for dc overload conditions of about 2.5 V beyond the supplies.

Input Voltages Beyond the Rails

For larger input voltages, an external resistor should be used in series with each input to limit current during overload conditions. The AD8222 can safely handle a continuous 6 mA current. The limiting resistor can be computed from

$$R_{LIMIT} \geq \frac{V_{IN} - V_{SUPPLY}}{6\ \text{mA}} - 400\ \Omega$$

For applications in which the AD8222 encounters extreme overload voltages, such as cardiac defibrillators, external series resistors and low leakage diode clamps, such as the BAV199L, the FJH1100, or the SP720, should be used.

Differential Input Voltages at High Gains

When operating at high gain, large differential input voltages can cause more than 6 mA of current to flow into the inputs. This condition occurs when the differential voltage exceeds the following critical voltage:

$$V_{CRITICAL} = (400 + R_G) \times (6\ \text{mA})$$

This is true for differential voltages of either polarity.

The maximum allowed differential voltage can be increased by adding an input protection resistor in series with each input. The value of each protection resistor should be

$$R_{PROTECT} = (V_{DIFF\_MAX} - V_{CRITICAL})/6\ \text{mA}$$

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass, RC network placed at the input of the instrumentation amplifier, as shown in Figure 48. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{Diff} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi R \times C_C}$$

where $C_D \geq 10C_C$.

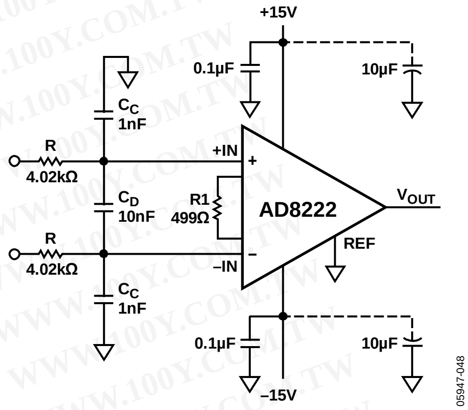


Figure 48. RFI Suppression

Figure 48 shows an example where the differential filter frequency is approximately 2 kHz, and the common-mode filter frequency is approximately 40 kHz.

Values of R and C_C should be chosen to minimize RFI. Mismatch between the R × C_C at the positive input and the R × C_C at negative input degrades the CMRR of the AD8222. By using a value of C_D 10× larger than the value of C_C, the effect of the mismatch is reduced and performance is improved.

COMMON-MODE INPUT VOLTAGE RANGE

The 3-op-amp architecture of the AD8222 applies gain and then removes the common-mode voltage. Therefore, internal nodes in the AD8222 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. Figure 7 and Figure 8 show the allowable common-mode input voltage ranges for various output voltages, supply voltages, and gains.

APPLICATIONS INFORMATION

DIFFERENTIAL OUTPUT

The differential configuration of the AD8222 has the same excellent dc precision specifications as the single-ended output configuration and is recommended for applications in the frequency range of dc to 100 kHz.

The circuit configuration is shown in Figure 49. The differential output specifications in Table 2 and Table 4 refer to this configuration only. The circuit includes an RC filter that maintains the stability of the loop.

The transfer function for the differential output is:

$$V_{DIFF\_OUT} = V_{+OUT} - V_{-OUT} = (V_{+IN} - V_{-IN}) \times G$$

where $G = 1 + \frac{49.4\ k\Omega}{R_G}$

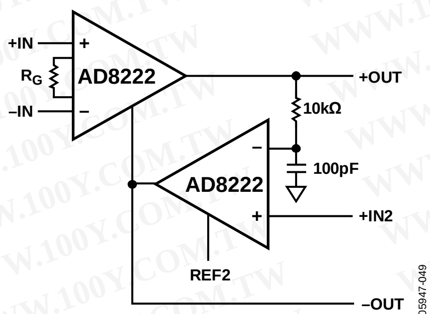


Figure 49. Differential Circuit Schematic

Setting the Common-Mode Voltage

The output common-mode voltage is set by the average of +IN2 and REF2. The transfer function is

$$V_{CM\_OUT} = (V_{+OUT} + V_{-OUT})/2 = (V_{+IN2} + V_{REF2})/2$$

+IN2 and REF2 have different properties that allow the reference voltage to be easily set for a wide variety of applications. +IN2 has high impedance but cannot swing to the supply rails of the part. REF2 must be driven with a low impedance but can go 300 mV beyond the supply rails.

A common application sets the common-mode output voltage to the midscale of a differential ADC. In this case, the ADC reference voltage is sent to the +IN2 terminal, and ground is connected to the REF2 terminal. This produces a common-mode output voltage of half the ADC reference voltage.

2-Channel Differential Output Using a Dual Op Amp

Another differential output topology is shown in Figure 50. Instead of a second in-amp, ½ of a dual OP2177 op amp creates the inverted output. Because the OP2177 is packaged in an MSOP, this configuration allows the creation of a dual channel, precision differential output in-amp with little board area.

Errors from the op amp are common to both outputs and are thus common mode. Errors from mismatched resistors also create a common-mode dc offset. Because these errors are common mode, they will likely be rejected by the next device in the signal chain.

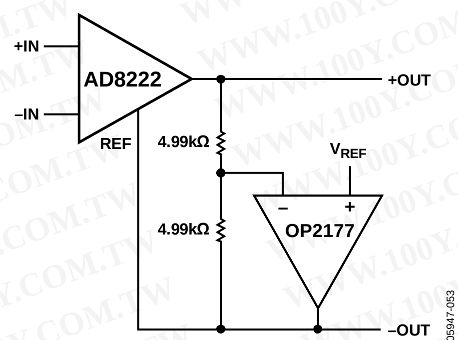


Figure 50. Differential Output Using Op Amp

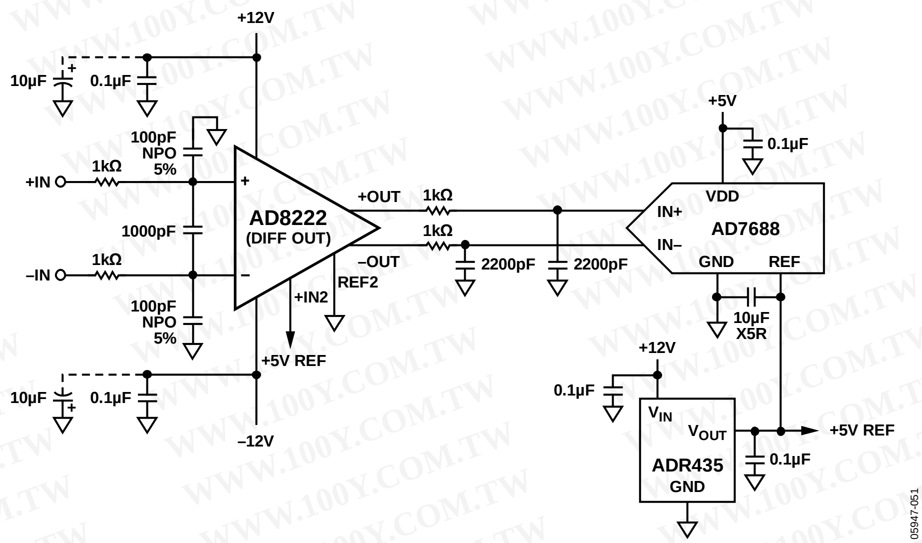


Figure 51. Driving a Differential ADC

DRIVING A DIFFERENTIAL INPUT ADC

The AD8222 can be configured in differential output mode to drive a differential analog-to-digital converter. Figure 51 illustrates several of the concepts.

RFI and Antialiasing Filter

The 1 kΩ resistors, 1000 pF capacitor, and 100 pF capacitors in front of the in-amp form filter circuitry that performs many functions. The 1 kΩ and 100 pF capacitors form common-mode filters that protect the amplifier from incoming radio frequency signals. Without the filtering, these RFI signals can be rectified in the in-amp. The 1 kΩ resistors provide some overvoltage protection. The 1 kΩ resistors and 1000 pF capacitor form a 76 kHz antialiasing filter for the ADC.

Note that the 100 pF capacitors are 5% COG/NPO types. These capacitors match well over time and temperature, which keeps the system CMRR high over frequency.

Second Antialiasing Filter

A 1 kΩ resistor and 2200 pF capacitor are placed between each AD8222 output and ADC input. They create a 72 kHz low-pass filter for another stage of antialiasing protection.

These four elements also improve distortion performance. The 2200 pF capacitor provides charge to the switched capacitor front end of the ADC, and the 1 kΩ resistor shields the AD8222 from driving any sharp current changes. If the application requires a lower frequency antialiasing filter and is distortion sensitive, increase the value of the capacitor rather than the resistor.

The 1 kΩ resistors can also protect an ADC from overvoltages. Because the AD8222 runs on wider supply voltages than a typical ADC, there is a possibility of overdriving the ADC. This is not an issue with a PulSAR® converter, such as the AD7688. Its input can handle a 130 mA overdrive, which is much higher than the short-circuit limit of the AD8222. However, other converters have less robust inputs and may need the added protection.

Reference

The ADR435 supplies a reference voltage to both the ADC and the AD8222. Because REF2 on the AD8222 is grounded, the common-mode output voltage is precisely half the reference voltage, exactly where it needs to be for the ADC.

PRECISION STRAIN GAGE

The low offset and high CMRR over frequency of the AD8222 make it an excellent candidate for both ac and dc bridge measurements. As shown in Figure 52, the bridge can be connected to the inputs of the amplifier directly.

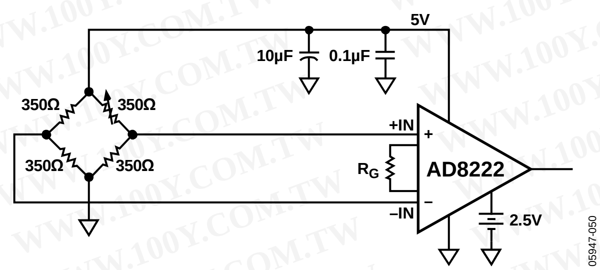


Figure 52. Precision Strain Gauge

DRIVING CABLING

All cables have a certain capacitance per unit length, which varies widely with cable type. The capacitive load from the cable may cause peaking in the AD8222's output response. To reduce the peaking, use a resistor between the AD8222 and the cable. Because cable capacitance and desired output response vary widely, this resistor is best determined empirically. A good starting point is 50 Ω.

The AD8222 operates at a low enough frequency that transmission line effects are rarely an issue; therefore, the resistor need not match the characteristic impedance of the cable.

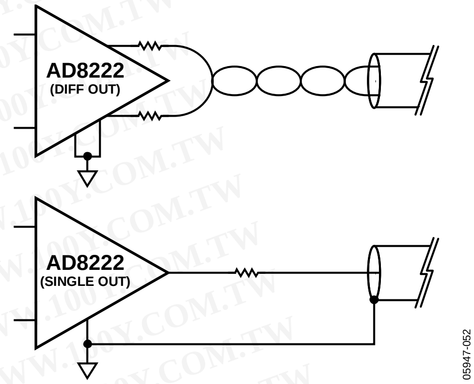
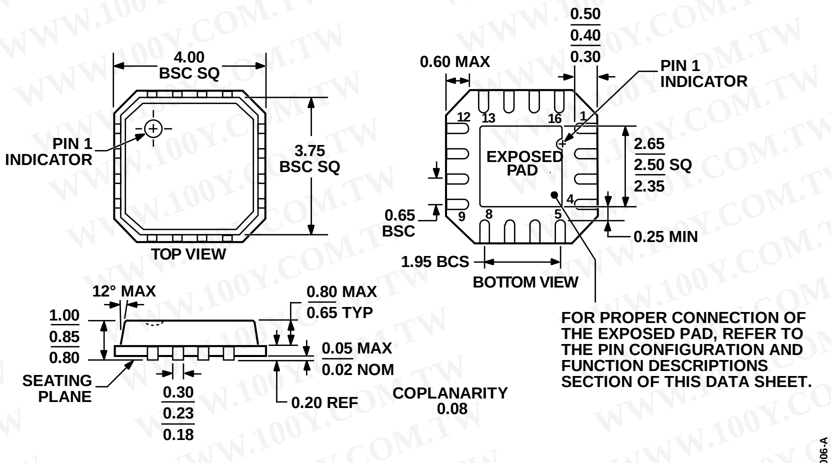


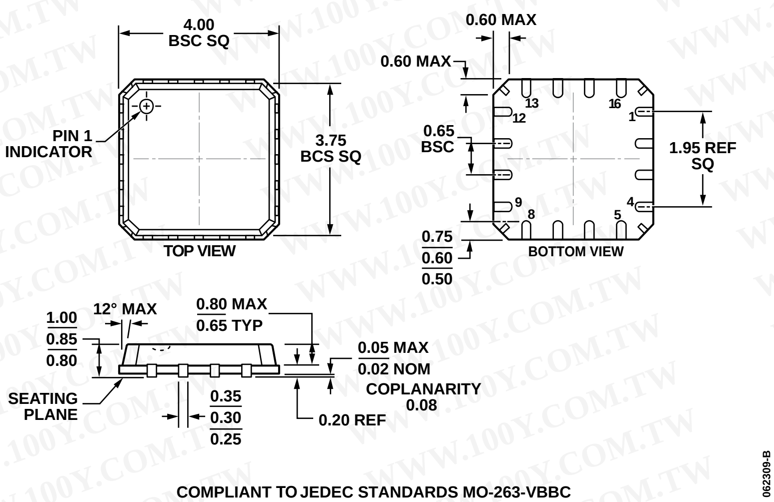
Figure 53. Driving a Cable

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC.

Figure 54. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-13)
Dimensions are shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-263-VBBC

Figure 55. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad, with Hidden Paddle
CP-16-19
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Product Description	Package Description	Package Option
AD8222ACPZ-R7	−40°C to +85°C	Standard Grade with Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Tape and Reel	CP-16-13
AD8222ACPZ-RL	−40°C to +85°C	Standard Grade with Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13"Tape and Reel	CP-16-13
AD8222ACPZ-WP	−40°C to +85°C	Standard Grade with Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Waffle Pack	CP-16-13
AD8222BCPZ-R7	−40°C to +85°C	High Performance Grade with Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Tape and Reel	CP-16-13
AD8222BCPZ-RL	−40°C to +85°C	High Performance Grade with Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13" Tape and Reel	CP-16-13
AD8222BCPZ-WP	−40°C to +85°C	High Performance Grade with Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Waffle Pack	CP-16-13
AD8222HACPZ-R7	−40°C to +85°C	Standard Grade Without Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Tape and Reel	CP-16-19
AD8222HACPZ-RL	−40°C to +85°C	Standard Grade Without Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13" Tape and Reel	CP-16-19
AD8222HACPZ-WP	−40°C to +85°C	Standard Grade Without Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Waffle Pack	CP-16-19
AD8222HBCPZ-R7	−40°C to +85°C	High Performance Grade Without Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Tape and Reel	CP-16-19
AD8222HBCPZ-RL	−40°C to +85°C	High Performance Grade Without Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13" Tape and Reel	CP-16-19
AD8222HBCPZ-WP	−40°C to +85°C	High Performance Grade Without Thermal Pad	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Waffle Pack	CP-16-19
AD8222-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

ANALOG DEVICES

www.analog.com