

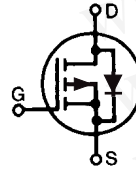
Standard Power MOSFET

IXTH 24P20

$V_{DSS} = -200 \text{ V}$
 $I_{D25} = -24 \text{ A}$
 $R_{DS(on)} \leq 0.11 \Omega$

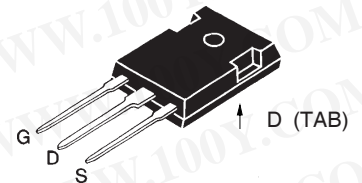
P-Channel Enhancement Mode
Avalanche Rated

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-34970699
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Symbol	Test Conditions	Maximum Ratings	TO-247 AD
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	-200 V	
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	-200 V	
V_{GS}	Continuous	± 20 V	
V_{GSM}	Transient	± 30 V	
I_{D25}	$T_C = 25^\circ\text{C}$	-24 A	
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_J	-96 A	
I_{AR}	$T_C = 25^\circ\text{C}$	-24 A	
E_{AR}	$T_C = 25^\circ\text{C}$	30 mJ	
P_D	$T_C = 25^\circ\text{C}$	300 W	
T_J		-55 ... +150 $^\circ\text{C}$	
T_{JM}		150 $^\circ\text{C}$	
T_{stg}		-55 ... +150 $^\circ\text{C}$	
T_L	Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s	400 $^\circ\text{C}$	
M_d	Mounting torque	1.13/10 Nm/lb.in.	
Weight		6 g	

TO-247 AD



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- International standard package JEDEC TO-247 AD
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance (<5 nH)
- easy to drive and to protect

Applications

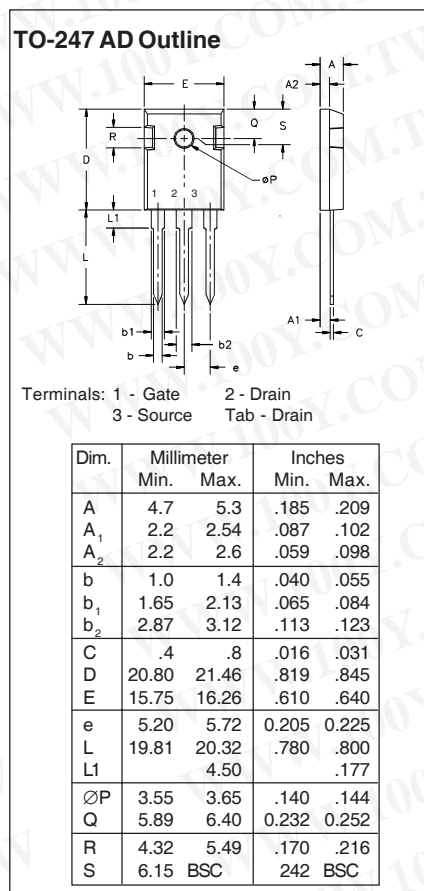
- High side switching
- Push-pull amplifiers
- DC choppers
- Automatic test equipment

Advantages

- Easy to mount with 1 screw (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$	-200		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	-3.0		V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100 \text{ nA}$
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$		-25 μA
		$T_J = 125^\circ\text{C}$		-1 mA
$R_{DS(on)}$	$V_{GS} = -10 \text{ V}$, $I_D = 0.5 \cdot I_{D25}$			0.11 Ω

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$V_{DS} = -10\text{ V}; I_D = I_{D25}$, pulse test	10	15	S
C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1\text{ MHz}$		4200	pF
C_{oss}			830	pF
C_{rss}			350	pF
$t_{d(on)}$	$V_{GS} = -10\text{ V}, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}$ $R_G = 4.7\ \Omega$ (External)		36	ns
t_r			29	ns
$t_{d(off)}$			68	ns
t_f			28	ns
$Q_{g(on)}$	$V_{GS} = -10\text{ V}, V_{DS} = 0.5 V_{DSS}, I_D = 0.5 I_{D25}$		150	nC
Q_{gs}			40	nC
Q_{gd}			70	nC
R_{thJC}			0.42	K/W
R_{thCS}			0.25	K/W



Source-Drain Diode

($T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Test Conditions	Characteristic Values		
		min.	typ.	max.
I_S	$V_{GS} = 0$			-24 A
I_{SM}	Repetitive; pulse width limited by T_{JM}			-96 A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			-3 V
t_{rr}	$I_F = I_S, di/dt = 100\text{ A}/\mu\text{s}, V_R = -50\text{ V}$	250		ns

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IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065B1	6,683,344	6,727,585
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123B1	6,534,343	6,710,405B2	6,759,692
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	

Fig. 1. Output Characteristics @ 25°C

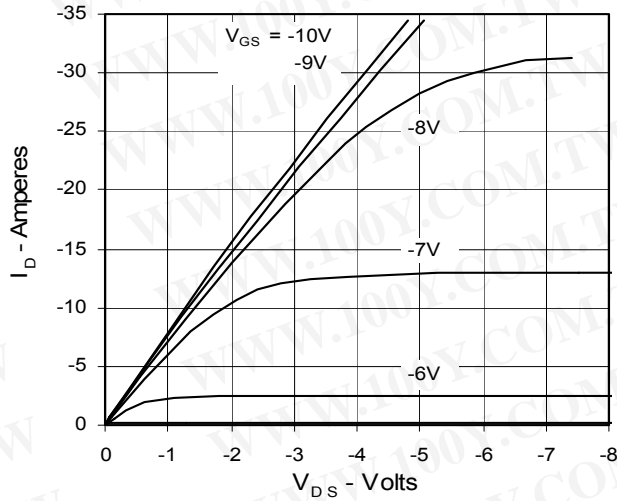


Fig. 2. Output Characteristics @ 125°C

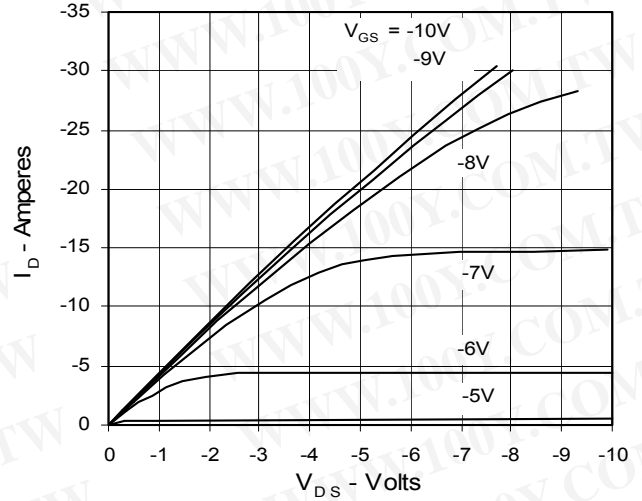


Fig. 3. $R_{DS(on)}$ Normalized to I_{D25} Value vs. Junction Temperature

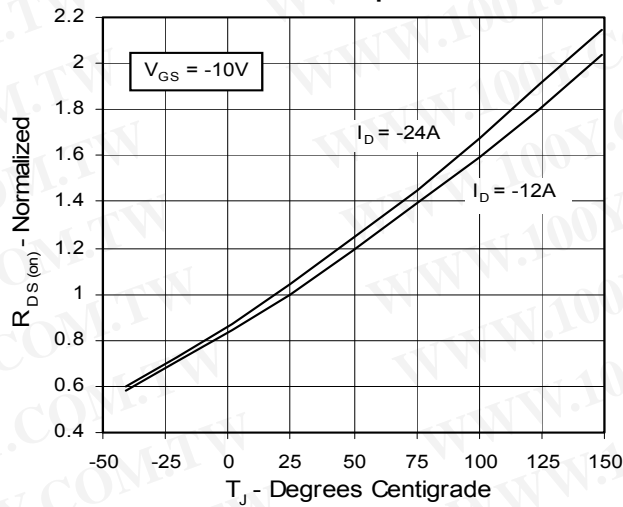


Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D

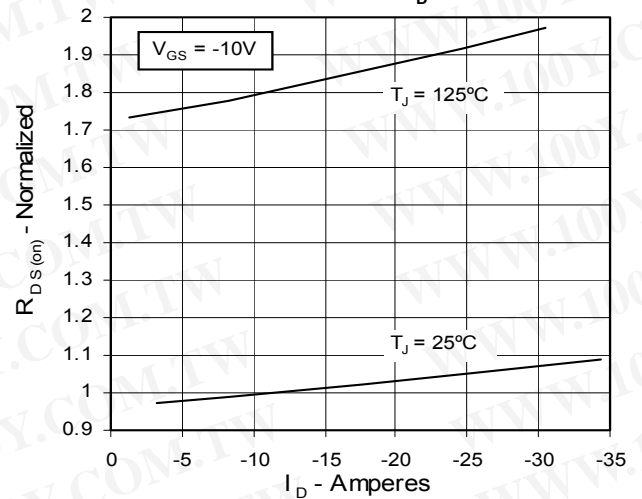


Fig. 5. Drain Current vs. Case Temperature

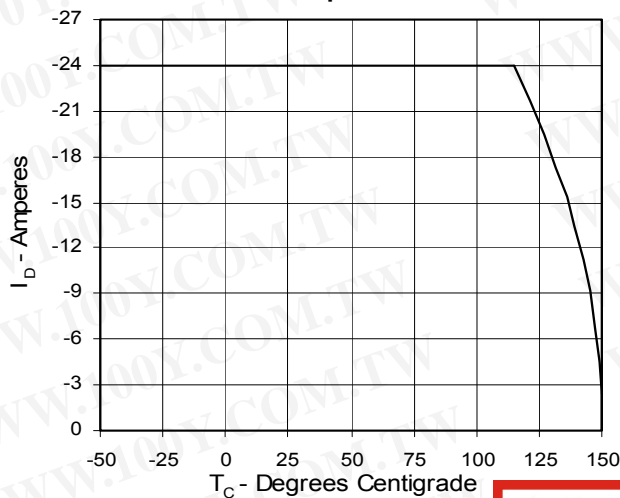


Fig. 6. Input Admittance

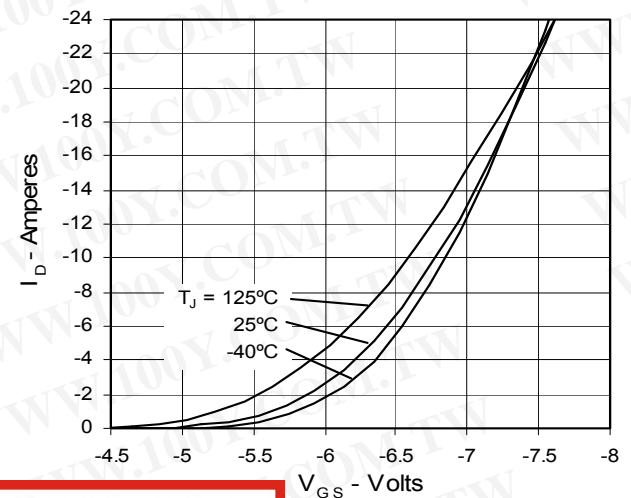


Fig. 7. Transconductance

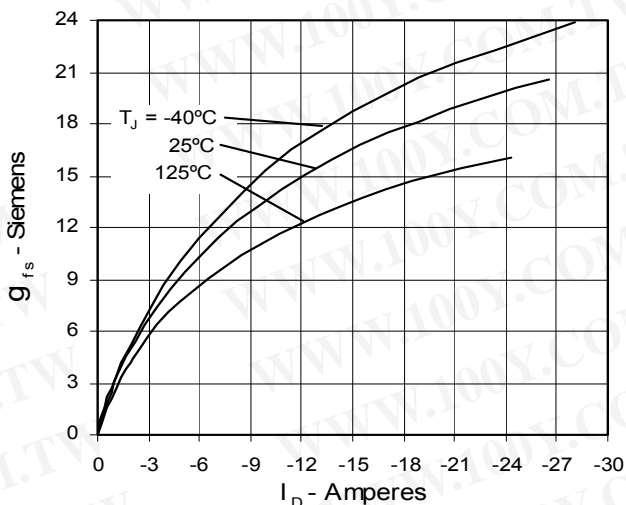


Fig. 8. Source Current vs. Source-To-Drain Voltage

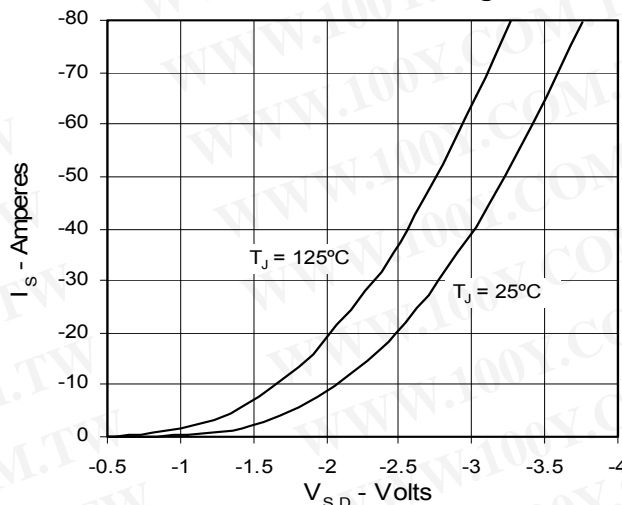


Fig. 9. Gate Charge

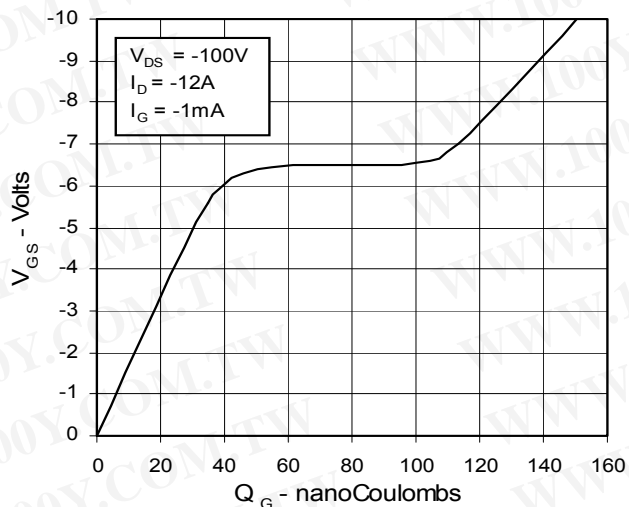


Fig. 10. Temperature dependence of Breakdown and Threshold Voltage

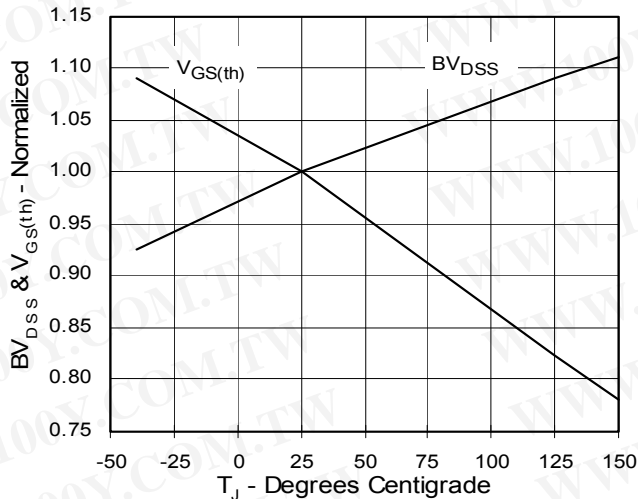


Fig. 11. Capacitance

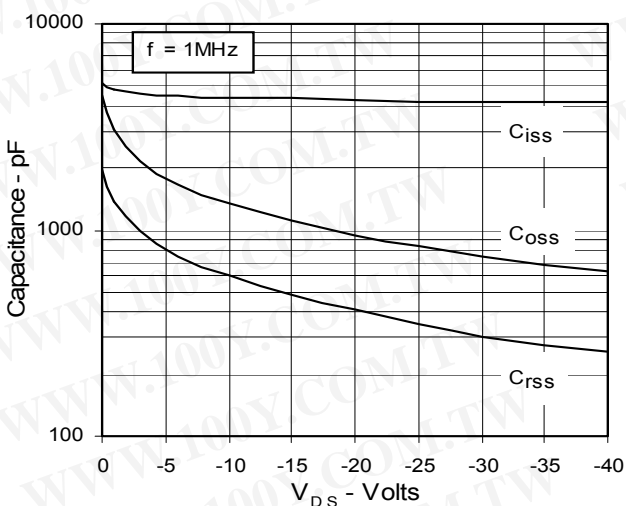
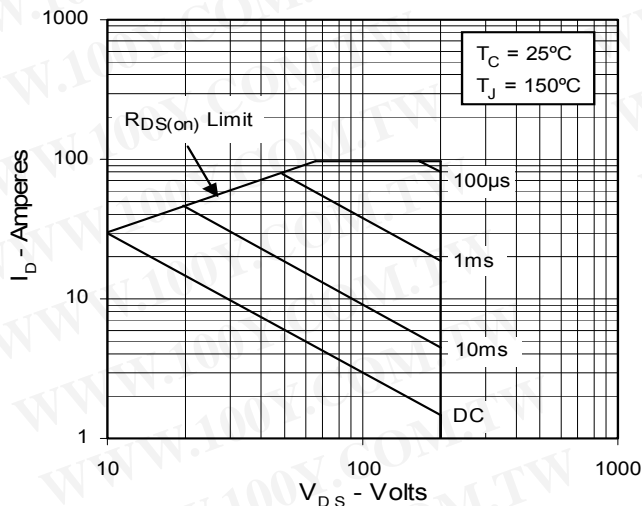


Fig. 12. Forward-Bias Safe Operating Area



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Fig. 13. Maximum Transient Thermal Resistance

