



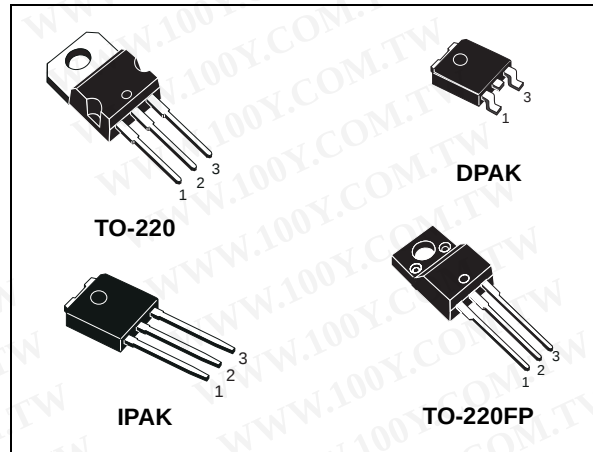
STD4NK50ZD - STD4NK50ZD-1 STF4NK50ZD - STP4NK50ZD

N-channel 500V - 2.4Ω - 3A - TO-220 - TO-220FP- DPAK - IPAK
 Fast diode SuperMESH™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _W
STD4NK50ZD-1	500V	<2.7Ω	3A	45W
STD4NK50ZD	500V	<2.7Ω	3A	45W
STF4NK50ZD	500V	<2.7Ω	3A	20W
STP4NK50ZD	500V	<2.7Ω	3A	45W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeability



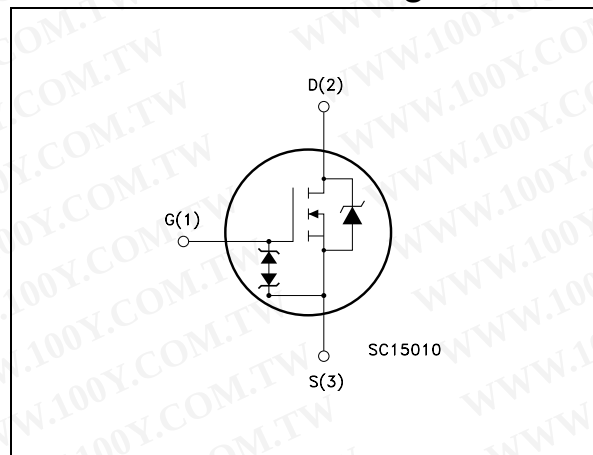
Description

The fast SuperMESH™ series associates all advantages of reduced on-resistance, zener gate protection and outstanding dc/dt capability with a Fast body-drain recovery diode. Such series complements the FDmesh™ advanced technology.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD4NK50ZD-1	D4NK50ZD-1	IPAK	Tube
STD4NK50ZD	D4NK50ZD	DPAK	Tape & reel
STF4NK50ZD	F4NK50ZD	TO-220FP	Tube
STP4NK50ZD	P4NK50ZD	TO-220	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220	IPAK/DPAK	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500			V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	500			V
V_{GS}	Gate-source voltage	± 30			V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	3	3 ⁽¹⁾	3 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100^\circ C$	1.9	1.9 ⁽¹⁾	1.9 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	12	12 ⁽¹⁾	12 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	45			W
	Derating factor	0.36			W/ $^\circ C$
$V_{ESD(G-D)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	2800			V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15			V/ns
V_{ISO}	Insulation withstand voltage (DC)	--	--	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150			$^\circ C$

1. Limited only by maximum temperature allowed

2. Pulse width limited by safe operating area

3. $I_{SD} \leq 3A$, $di/dt \leq 200A/\mu s$, $V_{DD} = 80\%V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value			Unit
		TO-220	IPAK/DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case Max	2.78			$^\circ C/W$
R_{thj-a}	Thermal resistance junction-ambient Max	62.5	100	62.5	$^\circ C/W$
T_I	Maximum lead temperature for soldering purpose	300			$^\circ C$

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J Max)	3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ C$, $I_d = I_{AR}$, $V_{dd} = 50V$)	120	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @}125^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$		2.3	2.7	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 1.5\text{A}$		1.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		310 49 10		pF pF pF
$C_{oss\text{ eq}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{V to } 400\text{V}$		33		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{V}$, $I_D = 3\text{A}$ $V_{GS} = 10\text{V}$ (see Figure 11)		12 3 7		nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{V}$, $I_D = 1.5\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (see Figure 18)		9.5		ns
t_r	Rise time			15.5		ns
$t_{d(off)}$	Turn-off delay time			23		ns
t_f	Fall time			22		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3A, V_{GS}=0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 3A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 34V, T_j = 25^\circ C$		73		ns
Q_{rr}	Reverse recovery charge			140		nC
I_{RRM}	Reverse recovery current			3.82		A
t_{rr}	Reverse recovery time	$I_{SD} = 3A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 34V, T_j = 150^\circ C$		118		ns
Q_{rr}	Reverse Recovery Charge			260		nC
I_{RRM}	Reverse recovery current			4.4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source braekdown voltage	$I_{GS} = \pm 1mA$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

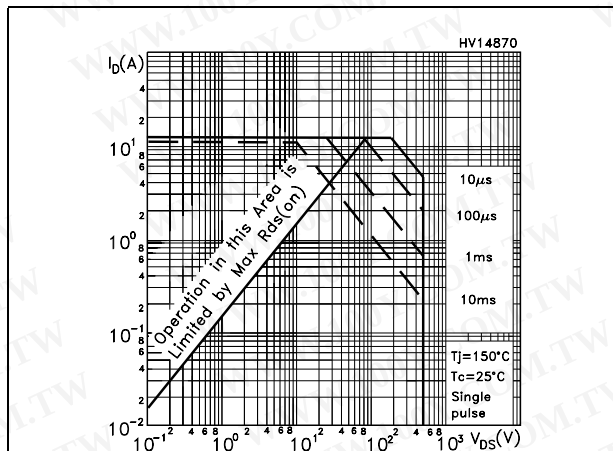


Figure 2. Thermal impedance for TO-220

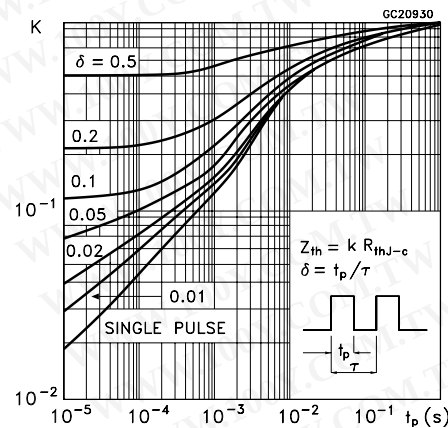


Figure 3. Safe operating area for TO-220FP

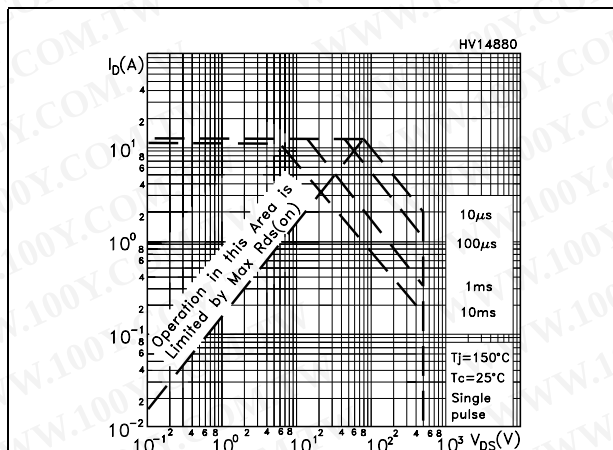


Figure 4. Thermal impedance for TO-220FP

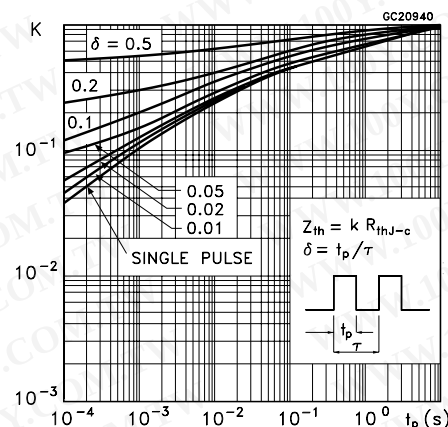


Figure 5. Safe operating area for DPAK/IPAK

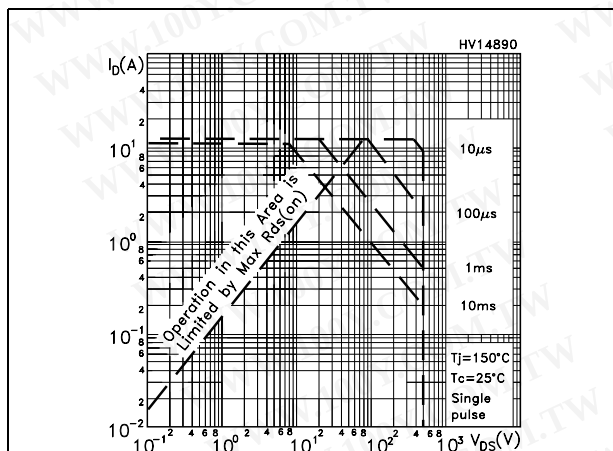


Figure 6. Thermal impedance for DPAK/IPAK

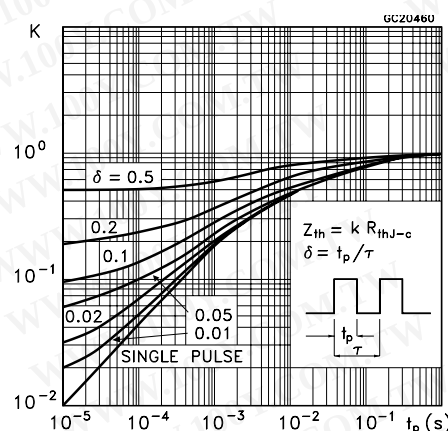


Figure 7. Output characteristics

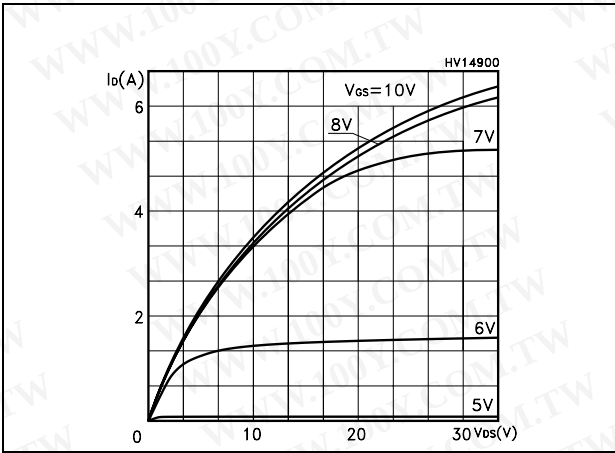


Figure 8. Transfer characteristics

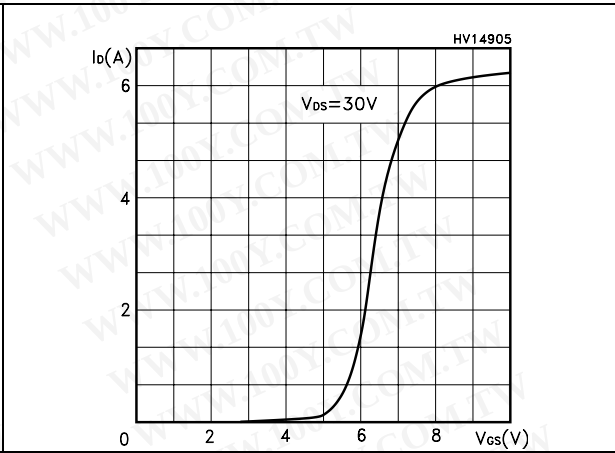


Figure 9. Transconductance

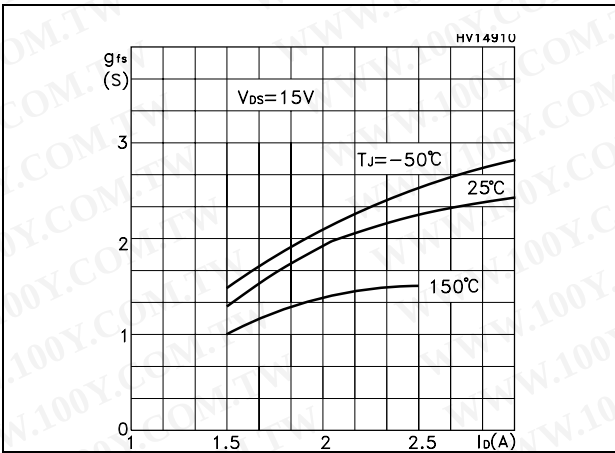


Figure 10. Static drain-source on resistance

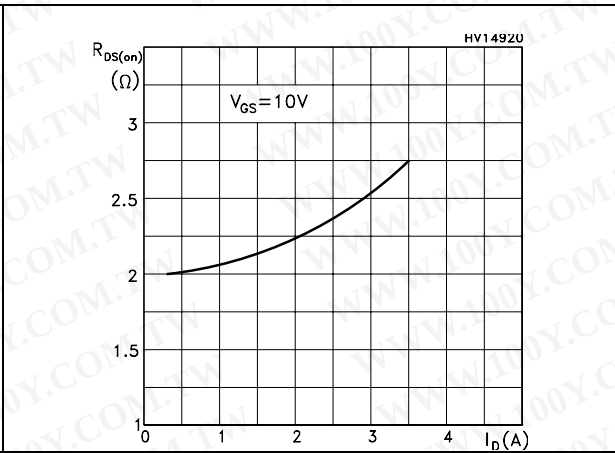


Figure 11. Gate charge vs gate-source voltage

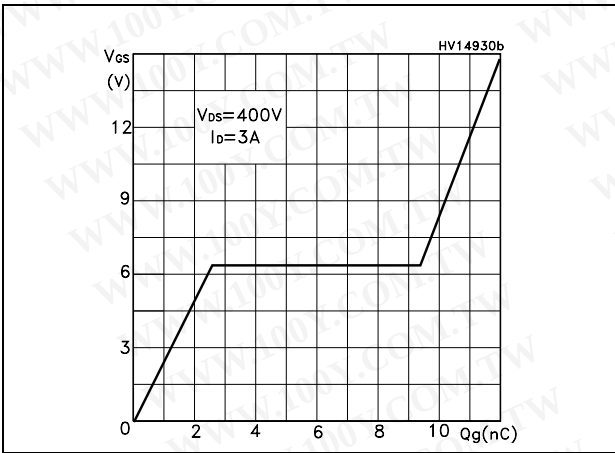


Figure 12. Capacitance variations

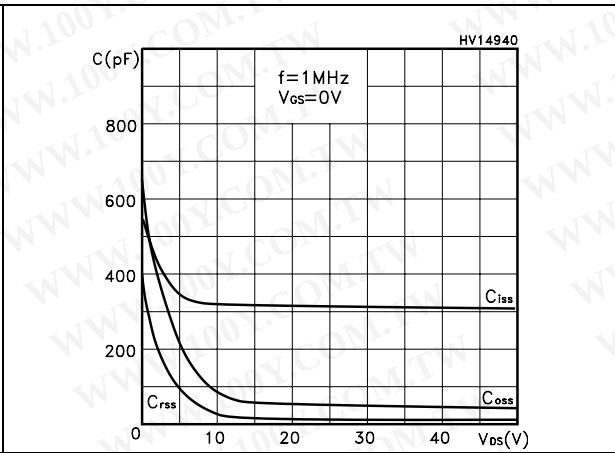


Figure 13. Normalized gate threshold voltage vs temperature

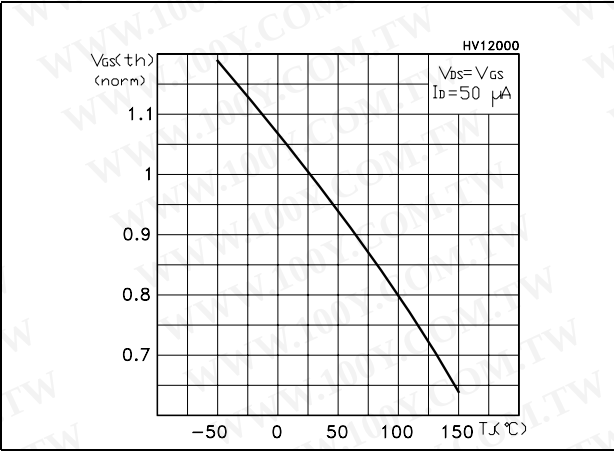


Figure 14. Normalized on resistance vs temperature

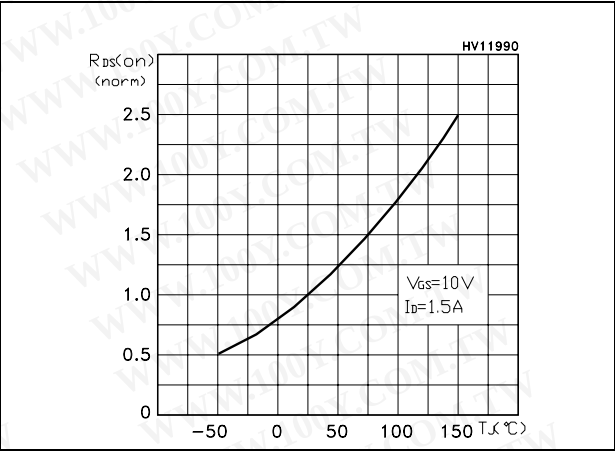


Figure 15. Source-drain diode forward characteristics

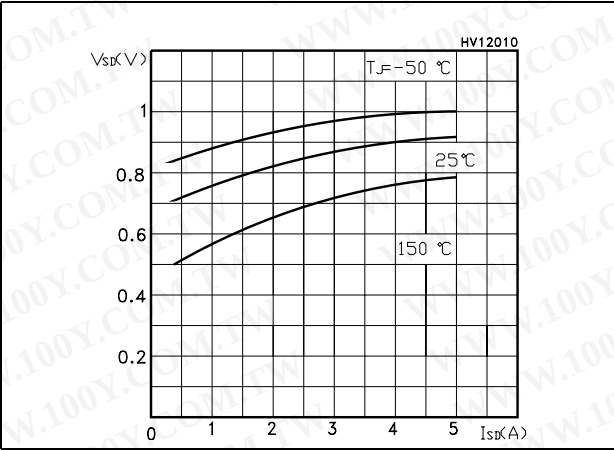


Figure 16. Normalized $B_{V_{DS}}$ vs temperature

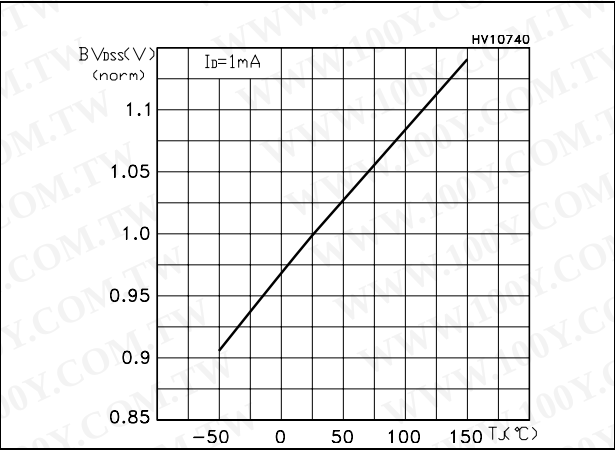
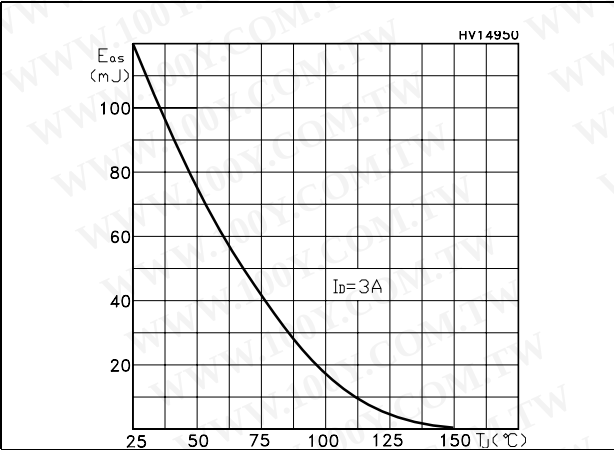


Figure 17. Maximum avalanche energy vs temperature



3 Test circuit

Figure 18. Switching times test circuit for resistive load

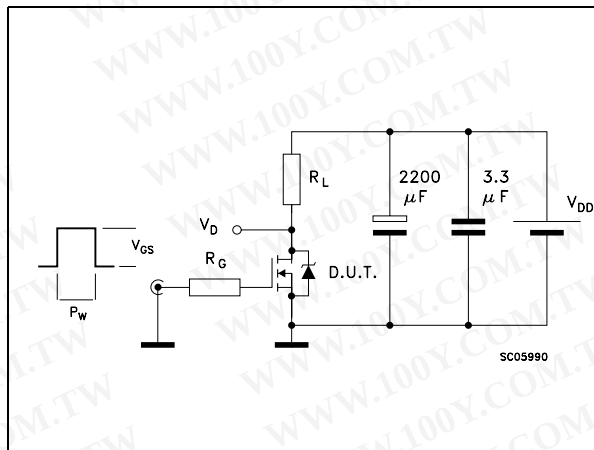


Figure 19. Gate charge test circuit

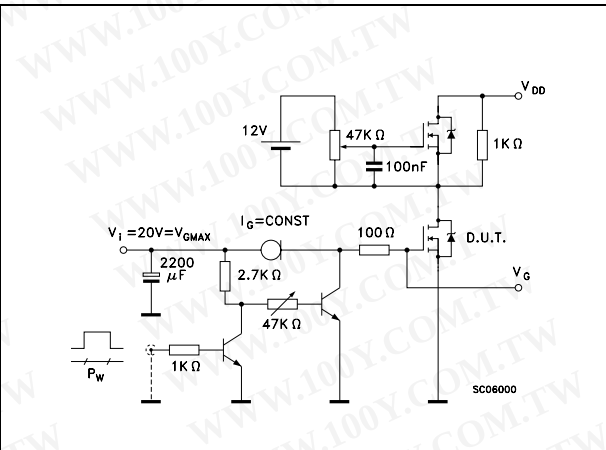


Figure 20. Test circuit for inductive load switching and diode recovery times

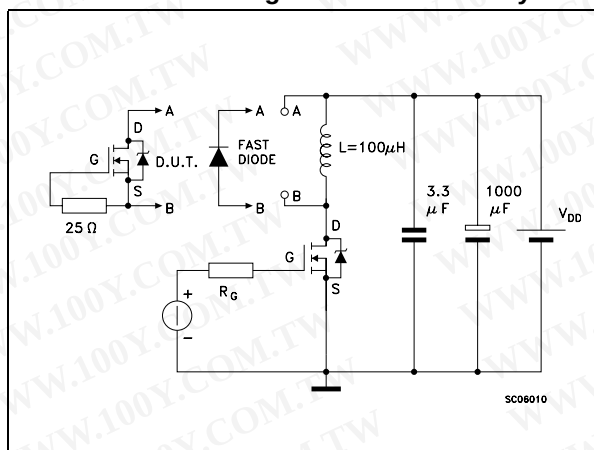


Figure 21. Unclamped inductive load test circuit

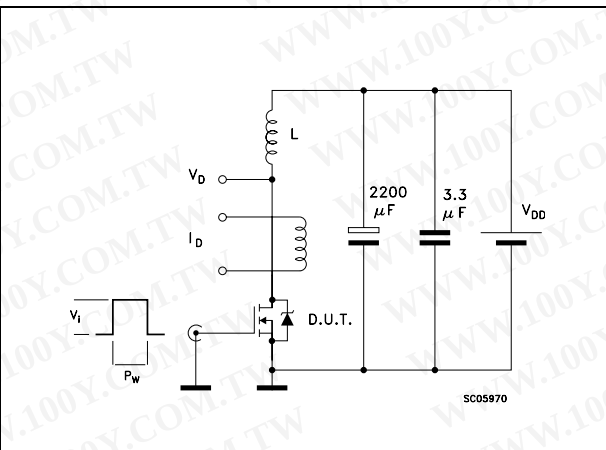


Figure 22. Unclamped inductive waveform

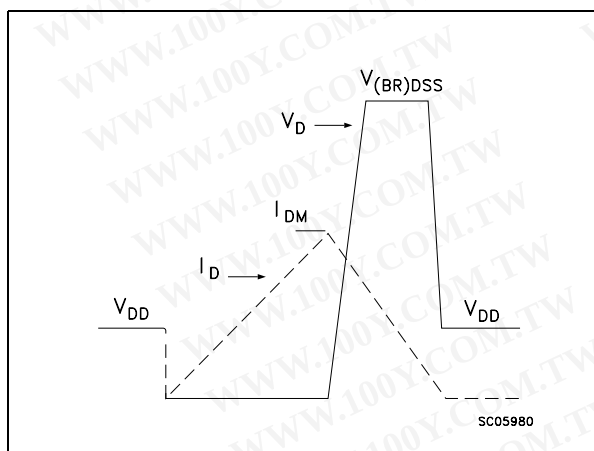
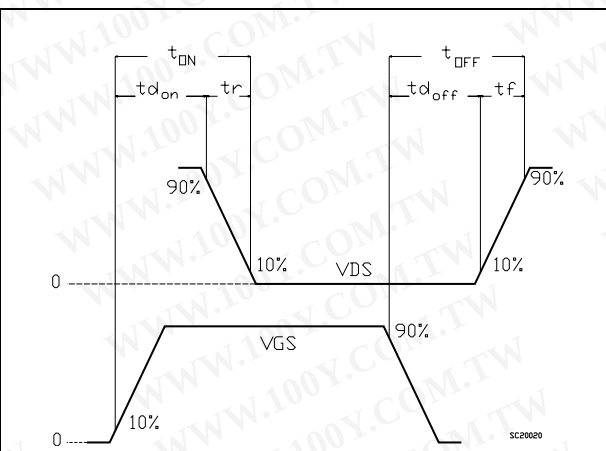


Figure 23. Switching time waveform

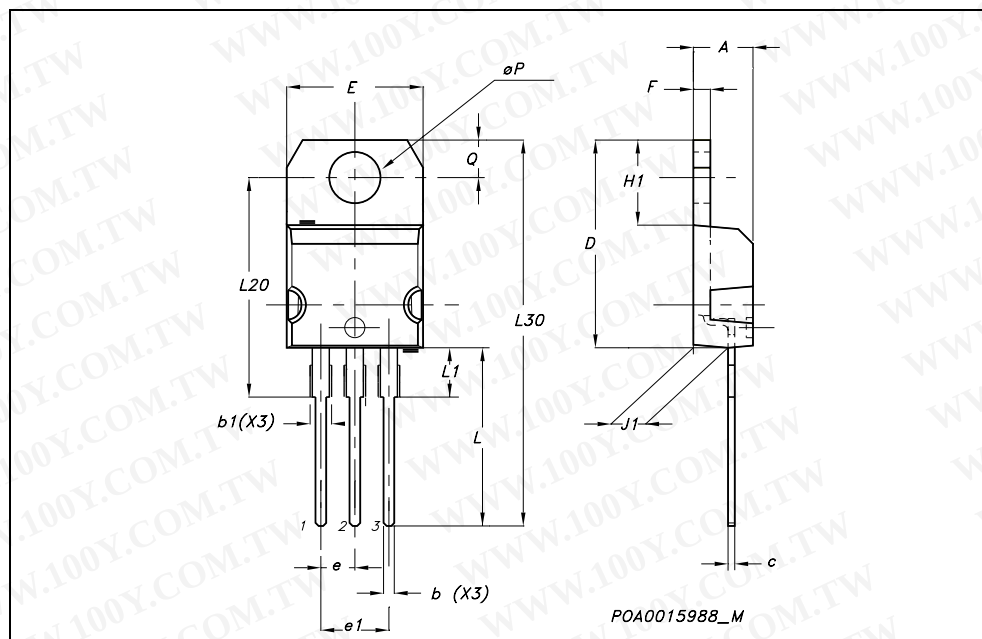


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

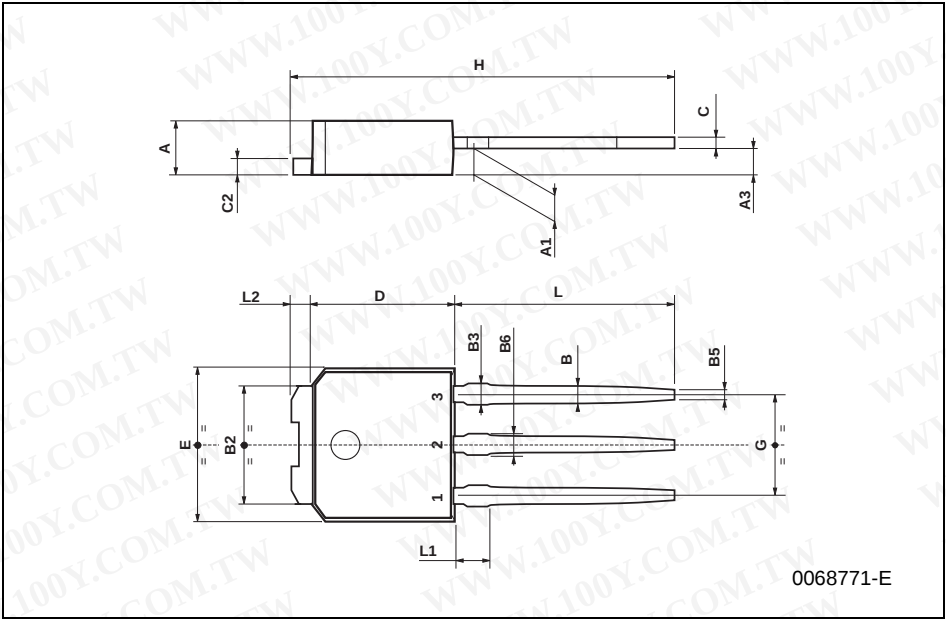
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



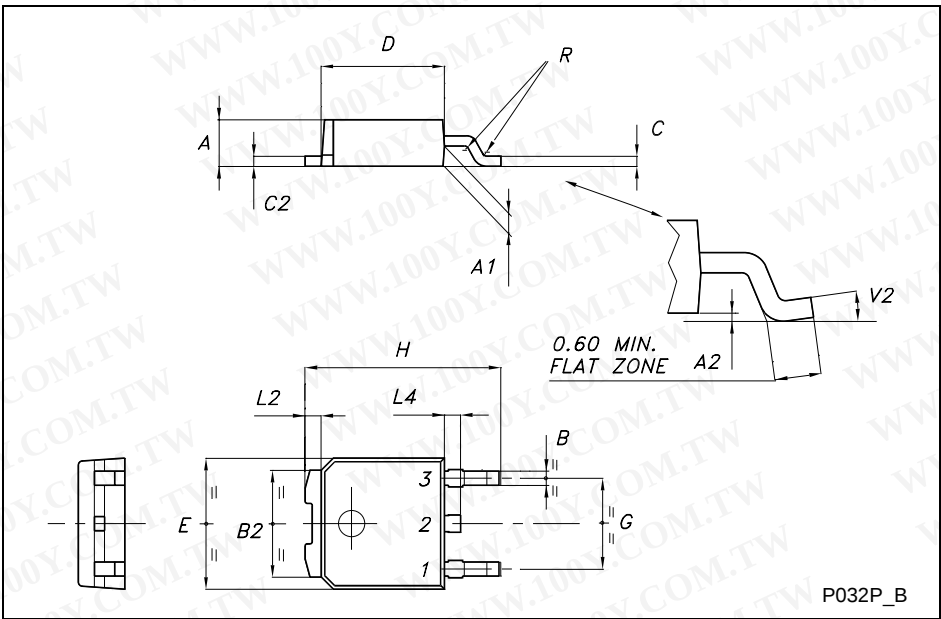
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



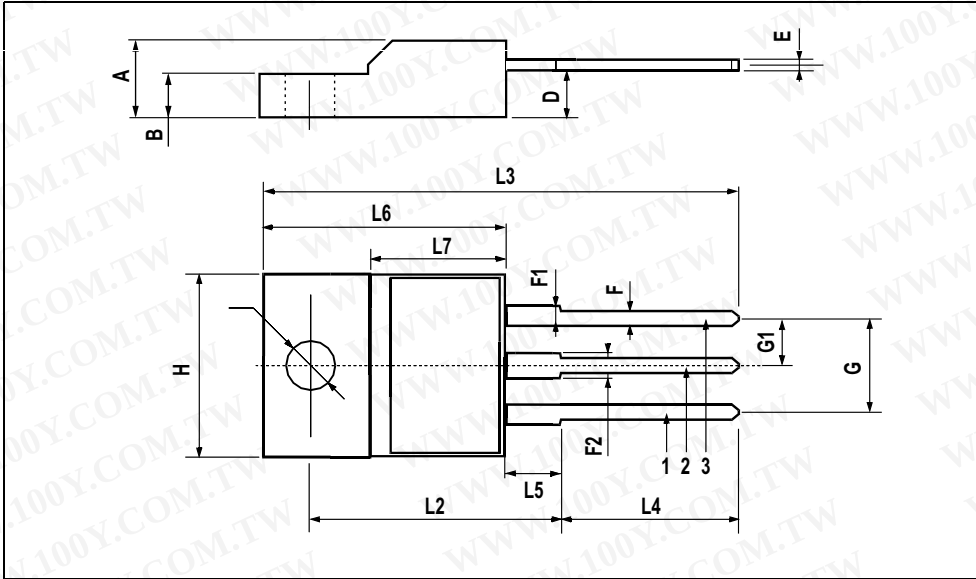
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



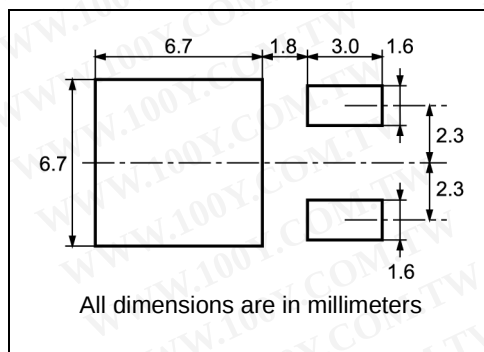
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

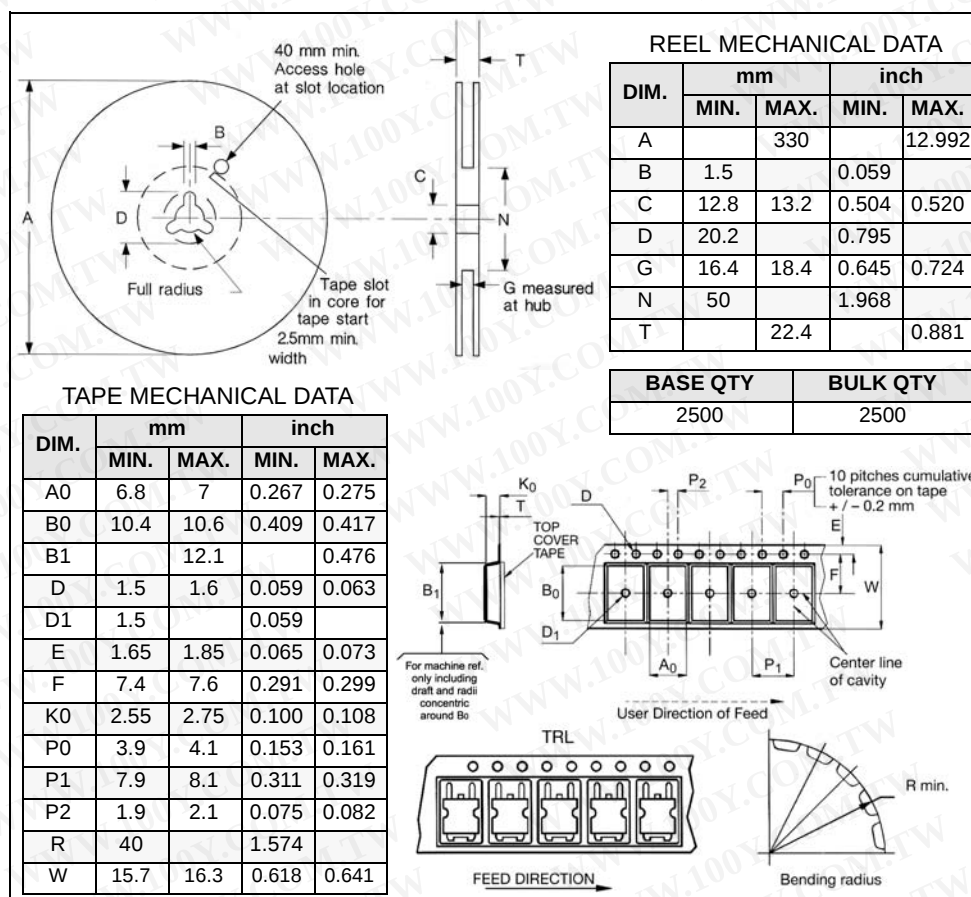


5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 9. Revision history

Date	Revision	Changes
09-Feb-2006	1	First Release
20-Feb-2006	2	Corrected Part Number
27-Apr-2006	3	Modified curves on page 6

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-34970699
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

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