



STGW30NC120HD

N-channel 1200V - 30A - TO-247
 very fast PowerMESH™ IGBT

Features

Type	V _{CES}	V _{CE(sat)} @25°C	I _C @100°C
STGW30NC120HD	1200V	< 2.75V	30A

- Low on-losses
- Low on-voltage drop (V_{cesat})
- High current capability
- High input impedance (voltage driven)
- Low gate charge
- Ideal for soft switching application

Application

- Induction heating

Description

Using the latest high voltage technology based on its patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, with outstanding performances. The suffix "H" identifies a family optimized for high frequency application in order to achieve very high switching performances (reduced t_{fall}) maintaining a low voltage drop.

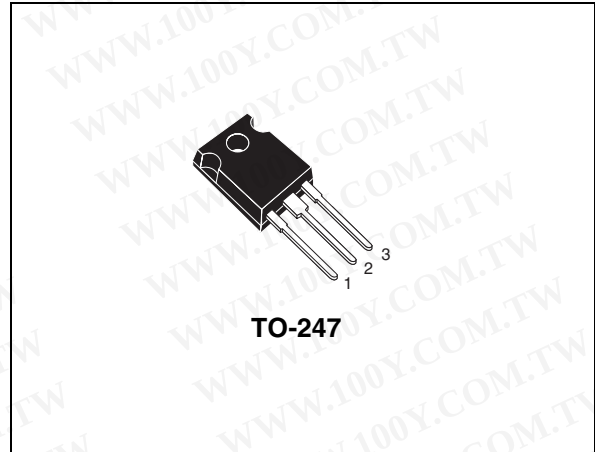


Figure 1. Internal schematic diagram

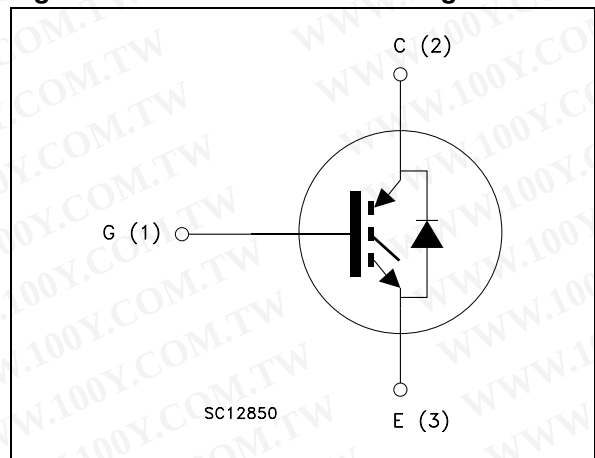


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW30NC120HD	GW30NC120HD	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	1200	V
$I_C^{(1)}$	Collector current (continuous) at 25°C	60	A
$I_C^{(1)}$	Collector current (continuous) at 100°C	30	A
$I_{CL}^{(2)}$	Collector current (pulsed)	135	A
V_{GE}	Gate-emitter voltage	± 25	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	220	W
I_f	Diode RMS forward current at $T_C = 25^\circ\text{C}$	30	A
T_j	Operating junction temperature	-55 to 150	$^\circ\text{C}$

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. $V_{clamp} = 80\%$ of BV_{ces} , $T_j = 150^\circ\text{C}$, $R_G = 10\Omega$, $V_{GE} = 15V$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.57	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (diode)	1.6	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient (IGBT)	30	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$, $V_{GE} = 0$	1200			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}$, $I_C = 20\text{A}$, $T_j = 25^{\circ}\text{C}$ $V_{GE} = 15\text{V}$, $I_C = 20\text{A}$, $T_j = 125^{\circ}\text{C}$		2.2 2.0	2.75	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 250\mu\text{A}$	3.75		5.75	V
I_{CES}	Collector-emitter leakage current ($V_{GE} = 0$)	$V_{CE} = \text{Max rating}$, $T_c = 25^{\circ}\text{C}$ $V_{CE} = \text{Max rating}$, $T_c = 125^{\circ}\text{C}$			500 10	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}$, $V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 25\text{V}$, $I_C = 20\text{A}$		14		S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GE} = 0$		2510		pF
C_{oes}	Output capacitance			175		pF
C_{res}	Reverse transfer capacitance			30		pF
Q_g	Total gate charge	$V_{CE} = 960\text{V}$, $I_C = 20\text{A}$, $V_{GE} = 15\text{V}$		110		nC
Q_{ge}	Gate-emitter charge			16		nC
Q_{gc}	Gate-collector charge			49		nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 960V, I_C = 20A$		29		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V,$		11		ns
$(di/dt)_{on}$	Turn-on current slope	$T_j = 25^\circ C$ (see Figure 17)		1820		A/ μs
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 960V, I_C = 20A$		27		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V,$		14		ns
$(di/dt)_{on}$	Turn-on current slope	$T_j = 125^\circ C$ (see Figure 17)		1580		A/ μs
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 960V, I_C = 20A$		90		ns
$t_{d(off)}$	Turn-off delay time	$R_G = 10\Omega, V_{GE} = 15V,$		275		ns
t_f	Current fall time	$T_j = 25^\circ C$ (see Figure 17)		312		ns
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 960V, I_C = 20A$		150		ns
$t_{d(off)}$	Turn-off delay time	$R_G = 10\Omega, V_{GE} = 15V,$		336		ns
t_f	Current fall time	$T_j = 125^\circ C$ (see Figure 17)		592		ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 960V, I_C = 20A$		1660		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V,$		4438		μJ
E_{ts}	Total switching losses	$T_j = 25^\circ C$ (see Figure 17)		6098		μJ
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 960V, I_C = 20A$		3015		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V,$		6900		μJ
E_{ts}	Total switching losses	$T_j = 125^\circ C$ (see Figure 17)		9915		μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pack diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature ($25^\circ C$ and $125^\circ C$)

2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	$I_f = 20A, T_j = 25^\circ C$ $I_f = 20A, T_j = 125^\circ C$		1.9 1.7	2.5	V V
t_{rr}	Reverse recovery time	$I_f = 20A, V_R = 27V,$		152		ns
Q_{rr}	Reverse recovery charge	$T_j = 125^\circ C, di/dt = 100A/\mu s$		722		nC
I_{rrm}	Reverse recovery current	(see Figure 20)		9		A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

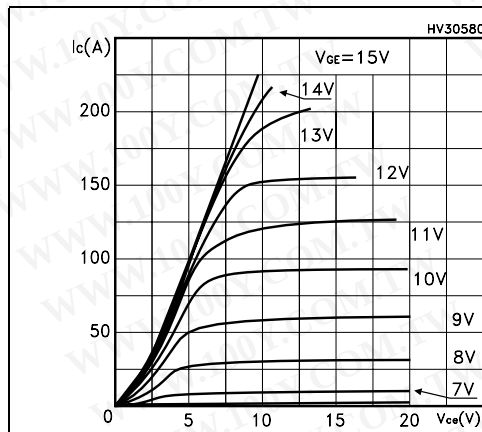


Figure 3. Transfer characteristics

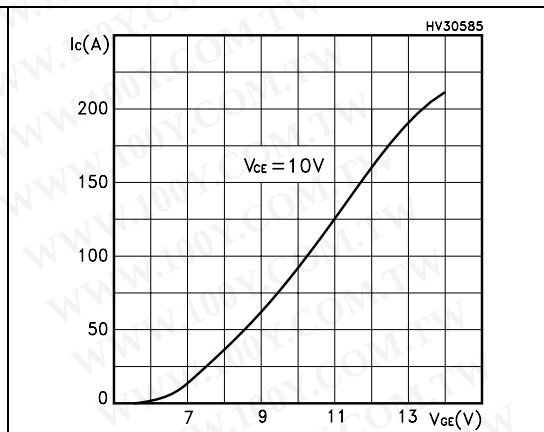


Figure 4. Transconductance

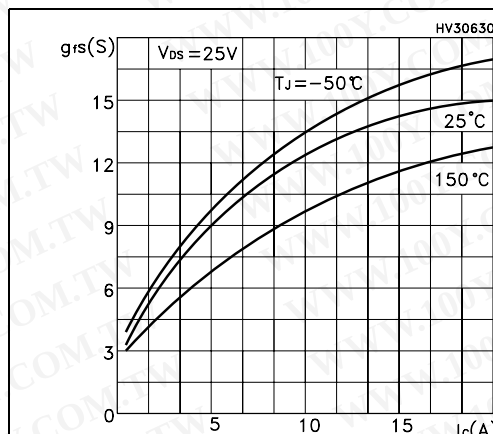


Figure 5. Collector-emitter on voltage vs. temperature

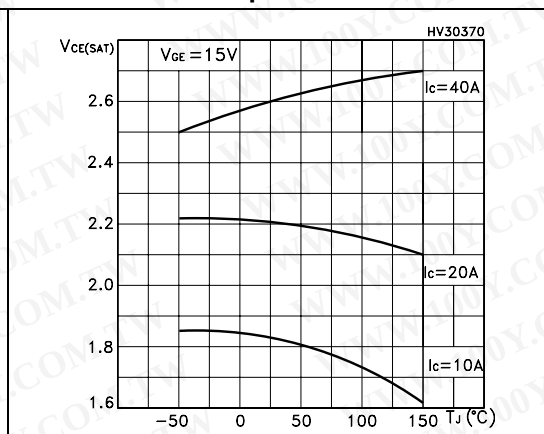


Figure 6. Gate charge vs. gate-source voltage

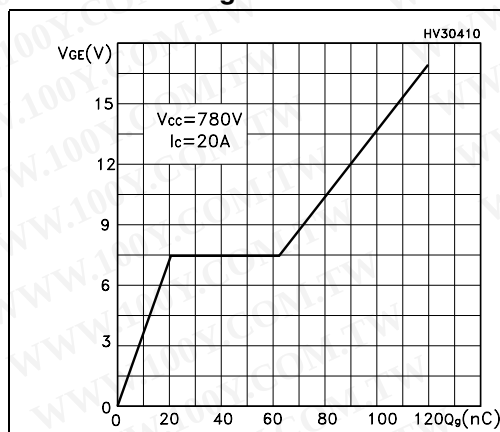


Figure 7. Capacitance variations

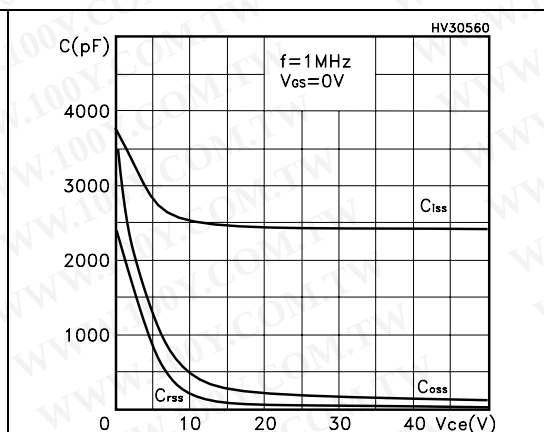


Figure 8. Normalized gate threshold voltage vs. temperature

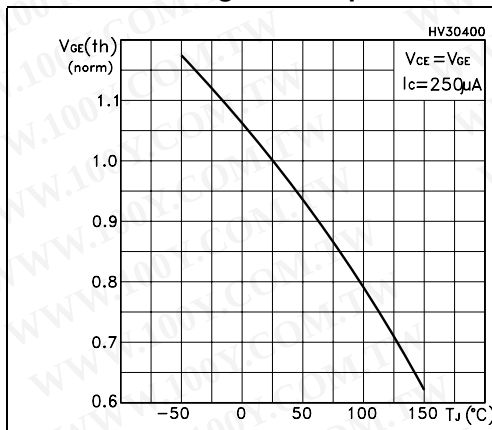


Figure 9. Collector-emitter on voltage vs. collector current

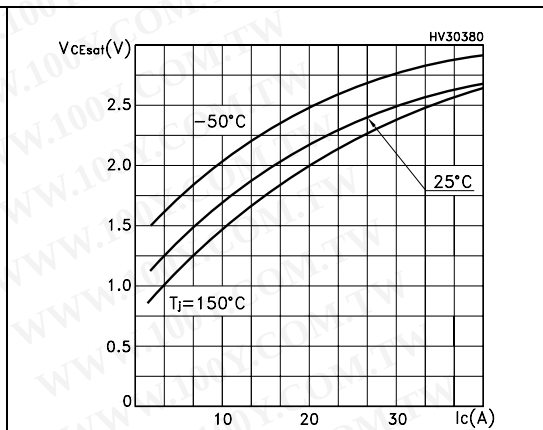


Figure 10. Normalized breakdown voltage vs. temperature

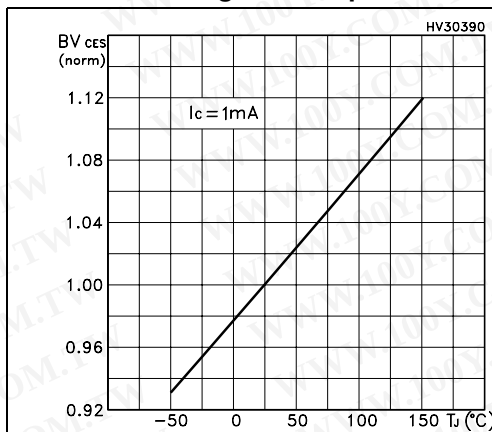


Figure 11. Switching losses vs. temperature

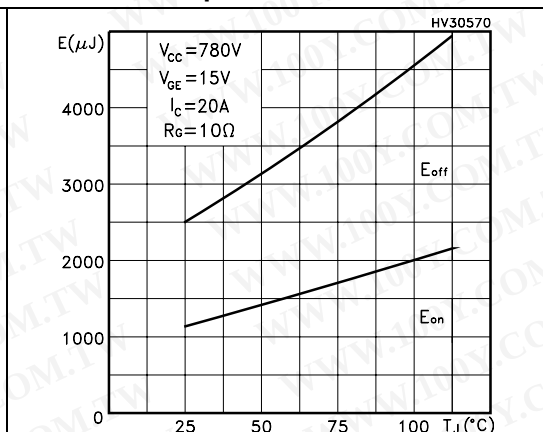


Figure 12. Switching losses vs. gate resistance

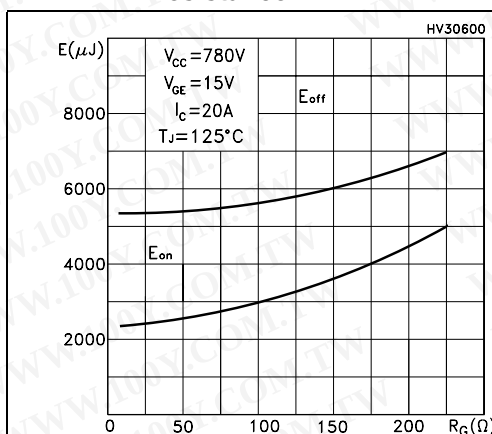


Figure 13. Switching losses vs. collector current

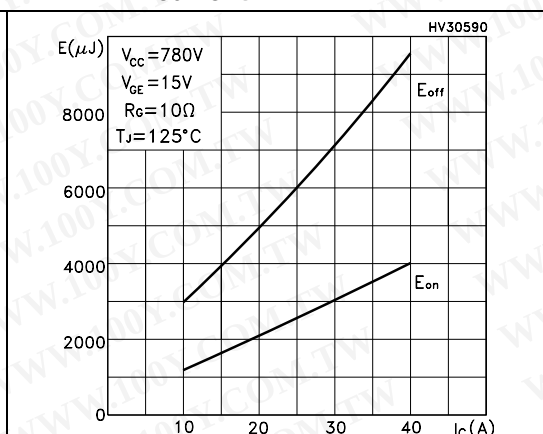


Figure 14. Thermal Impedance

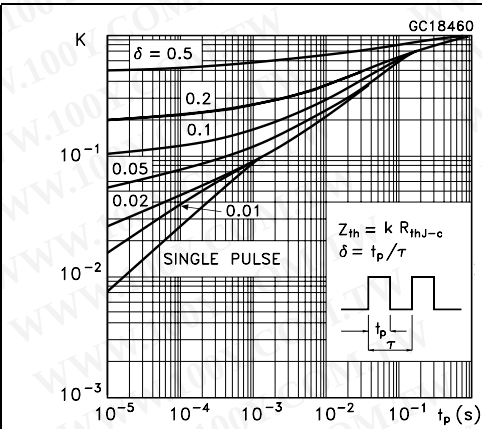


Figure 15. Turn-off SOA

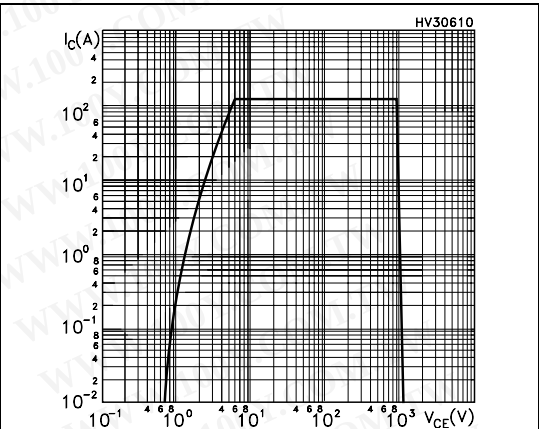


Figure 16. Emitter-collector diode characteristics

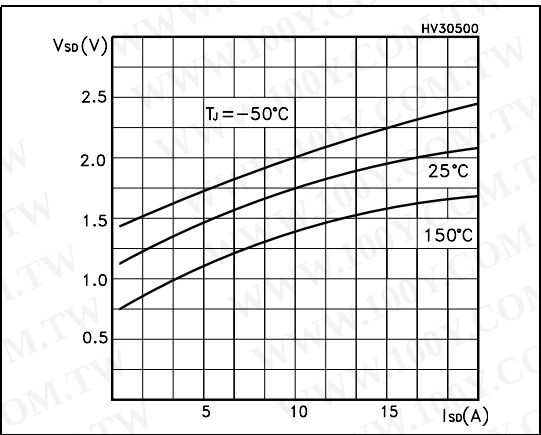


Figure 17. Test circuit for inductive load switching

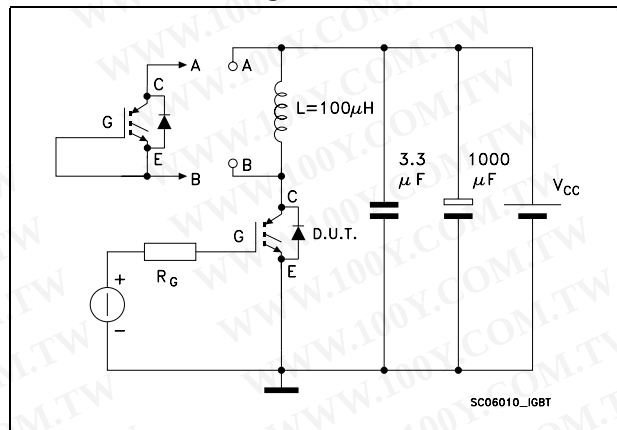


Figure 19. Switching waveform

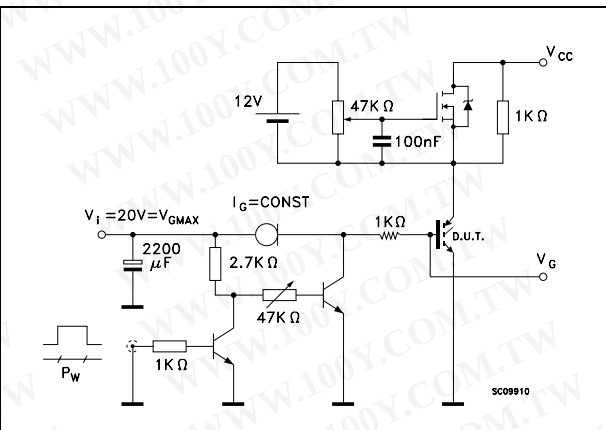
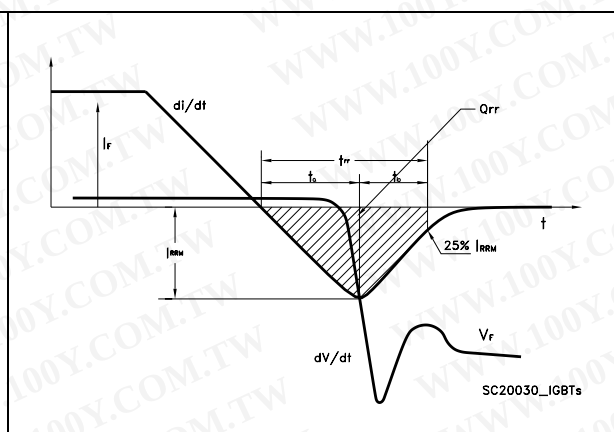
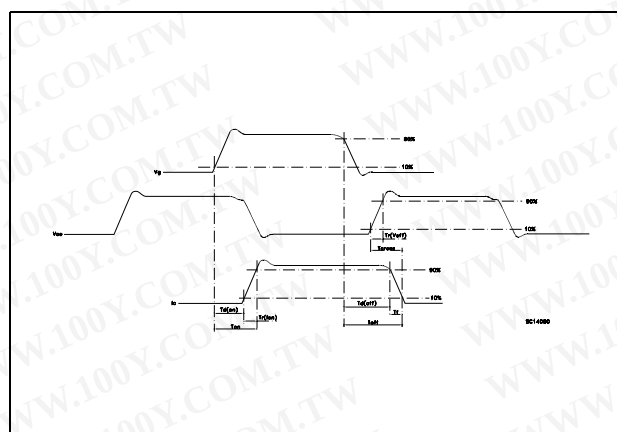


Figure 20. Diode recovery time waveform

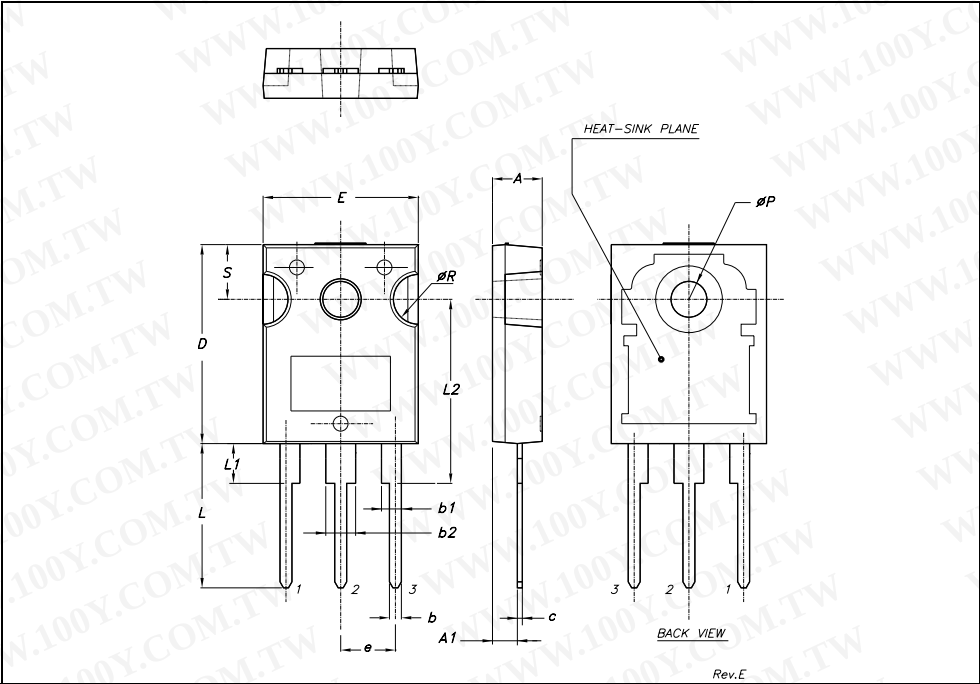


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
23-Nov-2005	1	First issue.
17-Mar-2006	2	Complete version
05-May-2006	3	Modified value on Table 2.: Absolute maximum ratings
30-May-2006	4	New values on Table 3: Thermal resistance
23-Jun-2006	5	Modified value on Table 4.: Static
07-Sep-2006	6	Modified T _J temperature range to 150°C in Table 2.: Absolute maximum ratings
14-Nov-2006	7	Modified Figure 5. and Figure 9.
26-Jan-2007	8	Typing error on first page.
04-Oct-2007	9	Modified test conditions in Table 4.: Static

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